# Single-Chip 5-Port SerDes Gigabit Switch

## GENERAL DESCRIPTION

The BCM5387 is a 5-port gigabit switch integrated with five 1.25 Gbps SerDes/SGMII port interfaces for connecting to external gigabit PHYs or fiber modules. The BCM5387 provides the lowest-cost Gigabit Ethernet-to-the-desktop switching solution or WebSmart™ application.

The BCM5387 is a highly integrated solution, combining all the functions of a high-speed switch system, including packet buffer, media access controllers (MACs), address management, and a non-blocking switch controller into a single monolithic 0.13-µm CMOS device. The BCM5387 complies with the IEEE 802.3, IEEE 802.3u, IEEE 802.3ab, and IEEE 802.3x specifications, including the MAC control PAUSE frame and auto-negotiation subsections, providing compatibility with all industry-standard Ethernet, Fast Ethernet, and Gigabit Ethernet devices.

The BCM5387 provides integrated 1.25 Gbps SerDes, reducing board footprint requirements. The five ports have SGMII interfaces for connecting with external Gigabit transceivers.

## FEATURES

- 5-port 10/100/1000 Mbps integrated switch controller via 1.25 Gbps SerDes/SGMII/Fiber
- Embedded 128 KB on-chip packet buffer
- One 1000/100/10 Mbps inband management port (IMP) with a GMII/RGMII/RvMII interface for PHY-less connection to a CPU/management entity
- Integrated address management
- Supports up to 4000 unicast addresses
- Supports jumbo frame up to 9728 bytes
- Supports EEPROM for low-cost chip configuration
- Integrated Motorola® SPI-compatible interface
- Port-mirroring support
- Port-based VLAN and 4K IEEE 802.1Q tag VLAN
- Port, DiffServ, weighted/strict priority, and IEEE 802.1p-based QoS for four queues
- Spanning tree support
- MAC-based trunking with link failover
- Low-power (1.0W [total], 1.2V [core], and 2.5V [RGMII], or 3.3V [GMII/MII]) with 3.3V I/O tolerance
- 256-FBGA



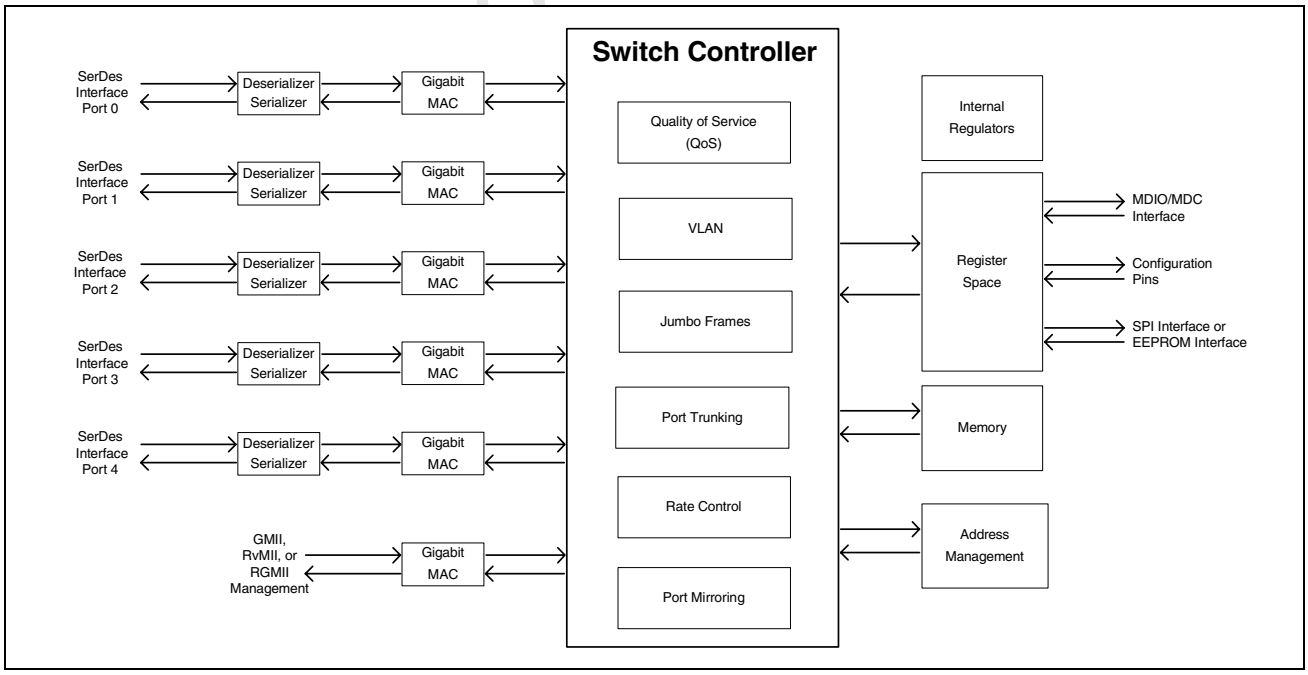


**Figure 1: Functional Block Diagram**

# Revision History

| *Revision* | *Date* | *Change Description* |
|---|---|---|
| 5387-DS10-R | 06/09/10 | **Added:**<br>• "Serial Interface Input Timing" on page 191<br>**Updated:**<br>• Table 143: "MAC Trunk Control Register (Page 032h, Address 01h)," on page 167 |
| 5387-DS09-R | 01/12/09 | **Updated:**<br>• "Ordering Information" on page 168 |
| 5387-DS07-R | 7/16/07 | **Updated:**<br>• "Port Trunking/Aggregation" on page 7<br>• Table 141, "Trunk Group Register (Page 032h, Address 090h–091h)," on page 132 |
| 5387-DS06-R | 2/28/07 | • "Programming the VLAN Table" on page 6<br>• Table 13 on page 24<br>• Table 124 on page 124 |
| 5387-DS05-R | 10/18/06 | **Updated:**<br>• Low-power voltage value in cover page Features bullet. |
| 5387-DS04-R | 10/09/06 | **Updated:**<br>• "Transmit Output Port Queues" on page 37<br>• Table 101, "MII Status Register (Page 010h-017h: Address 02h-03h)," on page 117<br>• Table 106, "SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h-021h)," on page 121<br>• Table 107, "Analog Transmit Register (Page 010h-017h: Address 020h-021h, Block 1)," on page 123<br>• Table 108, "SerDes/SGMII Control 2 Register (Page 010h-017h: Address 022h-023h)," on page 123<br>• Table 167, "Electrical Characteristics," on page 165 |
| 5387-DS03-R | 03/23/06 | **Updated:**<br>• Table 99, "Internal Serial Port Registers (Page 010h–017h)," on page 115.<br>• Table 160, "External PHY Registers (Serial Ports) (Page 080h–087h)," on page 162<br>**Added:**<br>• "Master Mode" on page 50.<br>• "Slave Mode" on page 51.<br>• Table 107, "Analog Transmit Register (Page 010h-017h: Address 020h-021h, Block 1)," on page 123.<br>• "Serial Interface Timing" on page 167. |
| 5387-DS02-R | 09/15/05 | **Updated:**<br>• Table 167, "Electrical Characteristics," on page 165.<br>• Table 172, "RGMII Output Timing (Normal Mode)," on page 170. |

| *Revision* | *Date* | *Change Description* |
|---|---|---|
| 5387-DS01-R | 05/27/05 | • Minor updates.<br>• Modified GMII and MDS/MDIO timing.<br>• Updated internal SerDes registers. |
| 5387-DS00-R | 03/09/05 | Initial release. |



Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

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# Section 1: Introduction

## Overview

The BCM5387 is a single-chip, 5-port switch device. The device provides:

- 6-port non-blocking 10/100/1000 Mbps switch controller
- Five ports with SerDes/SGMII interface for connection to external 10/100/1000-Mbps Ethernet transceiver or SerDes interface connection to 1000 Mbps full-duplex fiber module
- Five integrated gigabit MACs (GMACs)
- One GMII/RGMII/RvMII port for PHY-less connection to the management agent
- An integrated Motorola SPI-compatible interface
- High-performance integrated packet buffer memory
- An address-resolution engine

The GMACs support full-duplex and half-duplex modes for 10 Mbps and 100 Mbps and full-duplex for 1000 Mbps. Flow control is supported in the half-duplex mode with backpressure. In full-duplex mode, IEEE 802.3x frame-based flow control is supported. The GMACs are IEEE 802.3-compliant and support maximum frame sizes of 9.6 KB.

An integrated address-management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for learning up to 4K unicast addresses. Addresses are added to the table after receiving an error-free packet.

**Note:** The RvMII/GMII/RGMII port is used as a IMP (Management) Port only. It is not available for a PHY or network port connection.

## Audience

This document is for designers interested in integrating the BCM5387 switch into their hardware designs and for others who need specific data about the physical characteristics and operation of the BCM5387 switch.

## Data Sheet Information

The following notational conventions are used in this document:

- Signal names are shown in uppercase letters (such as DATA).
- A bar over a signal name indicates that it is active low (such as $\overline{CE}$).
- In register and signal descriptions, [n:m] indicates a range from bit n to bit m (such as [7:0] indicates bits 7 through 0, inclusive).

- The use of R or Reserved indicates that a bit or a field is reserved by Broadcom for future use. Typically, R is used for individual bits and Reserved is used for fields.
- Numerical modifiers such as K or M follow traditional usage (for example, 1 KB means 1,024 bytes, 100 Mbps [referring to fast Ethernet speed] means 100,000,000 bps, and 133 MHz means 133,000,000 Hz).

# Section 2: Features and Operation

## Overview

The BCM5387 includes the following features:

- "Quality of Service" on page 22
- "Port-Based VLAN" on page 25
- "IEEE 802.1Q VLAN" on page 26
- "Jumbo Frame Support" on page 28
- "Port Trunking/Aggregation" on page 28
- "Rate Control" on page 29
- "Protected Ports" on page 31
- "Port Mirroring" on page 31
- "IGMP Snooping" on page 33
- "Address Management" on page 33

The following sections discuss each feature in more detail.



## Quality of Service

The Quality of Service (QoS) feature provides up to four internal queues per port to support four different traffic priorities. These priorities can be programmed in such a way that high-priority traffic experiences less delay in the switch under congested conditions than that of lower-priority traffic. This can be important in minimizing latency for delay-sensitive traffic. The BCM5387 can assign the packet to one of the four egress transmit queues according to information in:

- "Port-Based QoS" on page 23 (ingress port ID)
- "IEEE 802.1p QoS" on page 24
- "MAC-Based QoS" on page 24
- "DiffServ QoS" on page 25

The "Frame Priority Decision Tree" on page 25 decides which priority system is used based on three programmable register bits detailed in Table 1 on page 25. The corresponding Priority ID is then assigned to one of the four priority queues on a port-by-port basis.

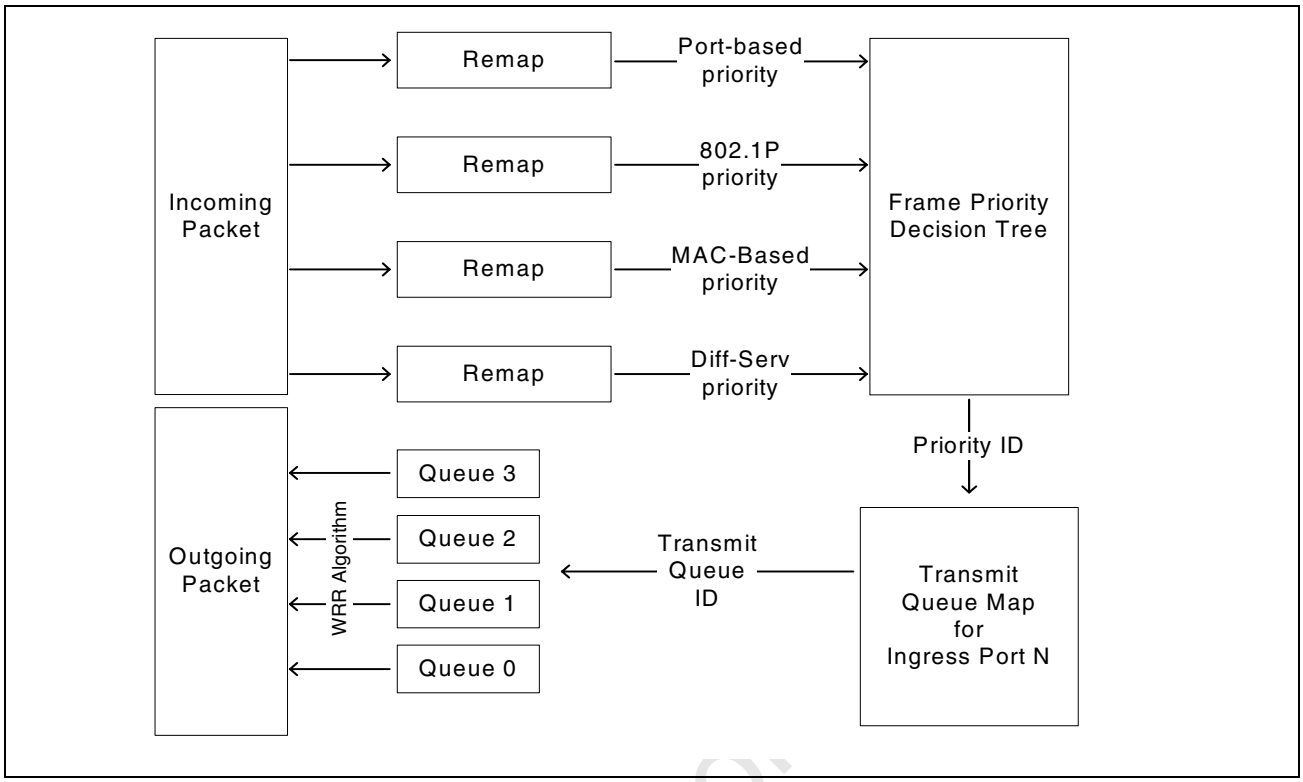


**Figure 2: QoS Block Diagram**

## Egress Transmit Queues

Each egress port has the ability to support up to four transmit queues as programmed in the "TX Queue Control Register (Page 030h: Address 080h)" on page 164. Each incoming frame is assigned to an egress transmit queue depending on its assigned priority. Each egress transmit queue is a list specifying an order for packet transmission. The corresponding egress port transmits packets from each of the queues according to a programmable algorithm, with the higher-priority queues being given greater access than the lower-priority queues, with Queue 0 being the lowest-priority queue.

The BCM5387 uses a Weighted Round Robin (WRR) algorithm to schedule each transmit queue. The weights for each queue can be programmed via the "TX Queue Weight Register (Page 030h: Address 081h)" on page 165. The weights are programmable to a maximum decimal value of 49. The BCM5387 also supports a High Queue Preempt (HQP) feature, enabled via the "TX Queue Control Register (Page 030h: Address 080h)" on page 164, which works in conjunction with the WRR. When enabled, the highest priority queue is emptied first, then the lower priority queues use WRR to schedule their transmission.

## Port-Based QoS

Port-based QoS can be activated by either asserting the QoS_EN strap pin or by programming the "QoS Global Control Register (Page 030h: Address 00h)" on page 159.

The priority of the ingress port is determined by the PORT_QOS_PRI, bits[15:13] of the "Default IEEE 802.1Q Tag Register (Page 034h, Address 010h)" on page 174. The port-based priority is assigned to the Priority ID bits depending upon the result shown in Table 1 on page 25. Each priority ID is mapped to one of the egress transmit queues based on the ingress port via the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163.

If the QoS_EN strap pin is pulled high during power-on/reset, ports [3:0] are assigned the highest queue by default, whereas all others are assigned the lowest.

If port-based QoS is disabled, the port-based priority for all traffic for the given ingress port defaults to 0. For more information about the egress transmit queues, see "Egress Transmit Queues" on page 23.

## IEEE 802.1p QoS

IEEE 802.1p QoS is enabled on a port-by-port basis via the 802_1P_EN bit in the "QoS IEEE 802.1p Enable Register (Page 030h: Address 04h)" on page 159.

When using the IEEE 802.1p priority mechanism, the packet is examined for the presence of a valid IEEE 802.1p priority tag. If the tag is present, the packet is assigned a remapped IEEE 802.1p priority based on the mapping in "IEEE 802.1p Priority Map Register (Page 030h: Address 010h–013h)" on page 160. The IEEE 802.1p priority is assigned to the Priority ID bits depending upon the result shown in Table 1 on page 25. The priority ID is mapped to one of the egress transmit queues based on the ingress port via the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163. For more information about the egress transmit queues, see "Egress Transmit Queues" on page 23.

## MAC-Based QoS

MAC-based QoS is enabled when the IEEE 802.1p QoS is disabled via the 802_1P_EN bit in the "QoS IEEE 802.1p Enable Register (Page 030h: Address 04h)" on page 159.

When using MAC-based QoS, the destination address and VLAN ID is used to index the ARL table as described in "Address Management" on page 33. The matching ARL entry contains a 3-bit PRI field as shown in Table 1. These bits set the MAC-based priority for the frame. The MAC-based priority is assigned to the Priority ID bits depending upon the result shown in Table 1. The priority ID for the frame is mapped to one of the egress transmit queues based on the ingress port via the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163. The PRI bits for a learned ARL entry default to priority 0. To change the default, an ARL entry is written to the ARL table as described in the "Writing an ARL Entry" on page 40. For more information about the egress transmit queues, see "Egress Transmit Queues" on page 23.

## DiffServ QoS

DiffServ QoS is enabled on a port-by-port basis via the "QoS DiffServ Enable Register (Page 030h: Address 06h)" on page 160. When using the DiffServ priority mechanism, the packet is classified based on the DSCP field in the IP header. If the tag is present, the packet is assigned a remapped DiffServ priority based on "DiffServ Priority Map 0 Register (Page 030h: Address 030h)" on page 161 through "DiffServ Priority Map 3 Register (Page 030h: Address 042h)" on page 163. The DiffServ priority is assigned to the Priority ID bits depending upon the result shown in Table 1. Each Priority ID is mapped to one of the egress transmit queues based on the ingress port via the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163. For more information, see "Egress Transmit Queues" on page 23.

## Frame Priority Decision Tree

The Frame Priority Decisions Tree determines which priority system is assigned to the Priority ID bits for the given frame. As summarized above, the Priority ID bits for the frame can be determined according to the ingress port-based priority, IEEE 802.1p priority, MAC-based priority, or DiffServ priority information. The decision as to which priority system to use is based on the Port_QoS_En bit and the QoS_Layer_Sel bits of the "QoS Global Control Register (Page 030h: Address 00h)" on page 159. Table 1 summarizes how these programmable bits affect the derived priority. The DiffServ and IEEE 802.1p QoS priorities are only available if the respective QoS is enabled, and the received packet has the appropriate tagging.

***Table 1: Frame Priority Decision Tree Summary***

| *Port_QoS_En* | *QoS_Layer_Sel* | *Value of Priority ID Bits* |
|---|---|---|
| 0 | 00 | Remapped IEEE 802.1p QoS if available; otherwise, MAC-based QoS |
| 0 | 01 | Remapped DiffServ QoS if available; otherwise, Priority ID = 000 |
| 0 | 10 | Remapped DiffServ QoS if available, else (remapped IEEE 802.1p QoS if available, else MAC-based QoS) |
| 0 | 11 | The highest available priority of the following: remapped IEEE 802.1p QoS, remapped DiffServ QoS, or MAC-based QoS |
| 1 | 00 | Port-based QoS |
| 1 | 01 | Port-based QoS |
| 1 | 10 | Port-based QoS |
| 1 | 11 | The highest available priority of the following: port-based QoS, remapped IEEE 802.1p QoS, remapped DiffServ QoS, or MAC-based QoS |



# Port-Based VLAN

The port-based virtual LAN (VLAN) feature partitions the switching ports into virtual private domains designated on a per port basis. Data switching outside of the port's private domain is not allowed. The BCM5387 provides flexible VLAN configuration for each ingress (receiving) port.

The port-based VLAN feature works as a filter, filtering out traffic destined to non-private domain ports. The private domain ports are selected for each ingress port via the "Port-Based VLAN Control Register (Page 031h, Address 00h)" on page 165. For each received packet, the ARL resolves the DA and obtains a forwarding vector (list of ports to which the frame shall be forwarded). The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the non-private domain ports. The frame is only forwarded to those ports that meet the ARL table criteria, as well as the port-based VLAN criteria.

# IEEE 802.1Q VLAN

The BCM5387 supports IEEE 802.1Q VLAN and up to approximately 4000 VLAN table entries that reside in the internal embedded memory. Once the VLAN table is programmed and maintained by the microcontroller, the BCM5387 autonomously handles all operations of the protocol. These actions include the stripping or adding of the IEEE 802.1Q tag, depending on the requirements of the individual transmitting port. It also performs all the necessary VLAN lookups in addition to MAC L2 lookups.

## IEEE 802.1Q VLAN Table Organization

Each VLAN table entry, also referred to as a VID or VLAN ID, consists of a Valid bit, Untag map, and Forward map.

- The Valid bit designates whether the VID is valid.
- The Untag map controls whether the egress packet is tagged or untagged.
- The Forward map defines the membership within a VLAN domain.

The Untag map and Forward map include bit-wise representation of all the ports.

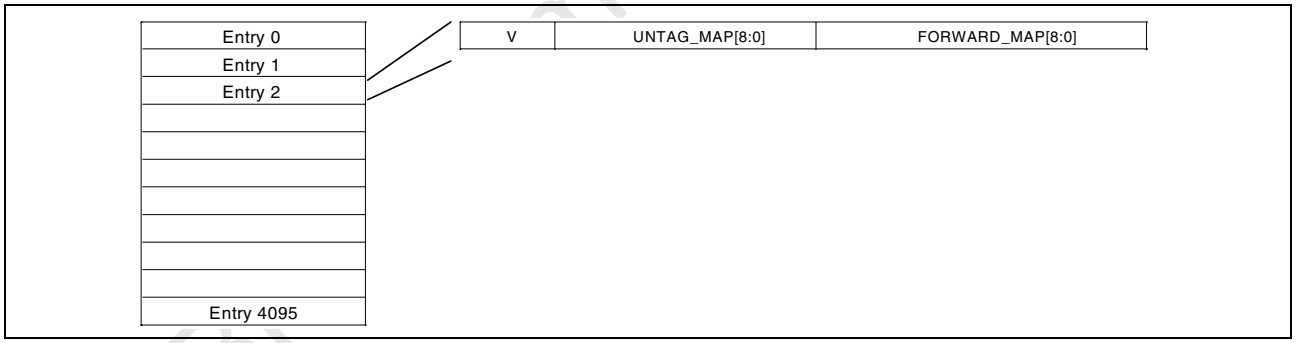


**Figure 3: VLAN Table Organization**

**Note:** When the IEEE 802.1Q feature is enabled, frames sent via the CPU shall be tagged.

## Programming the VLAN Table

The IEEE 802.1Q VLAN feature can be enabled by writing to the Enable IEEE 802.1Q bit in the "Global IEEE 802.1Q Register (Pages 034h, Address 00h)" on page 169. The default priority and VID can be assigned to each port in the "Default IEEE 802.1Q Tag Register (Page 034h, Address 010h)" on page 174. These are necessary when tagging a previously untagged frame. The Hashing algorithm uses either [VID, MAC] or [MAC] for the ARL index key, depending on the VLAN Learning Mode bits in the "Global IEEE 802.1Q Register (Pages 034h, Address 00h)" on page 169. If both the VID and MAC address are used, a single MAC address is able to be a member of multiple VLANs simultaneously.

The VLAN table can be written using the following steps:

1. Use the "VLAN Table Entry Register (Page 05h: Address 063h)" on page 134 to define the ports that are part of the VLAN group and the ports that should be untagged. The Valid bit should be set to 1.
2. Use the "VLAN Table Address Index Register (Page 05h: Address 061h)" on page 134 to define the VLAN ID of the VLAN group.

**Note:** For Rev A0 silicon, 000h and FFFh are not valid VID numbers. But FFFh is a valid VID number for Rev A1 silicon.

3. Set bit 0 of the "VLAN Table Read/Write Control Register (Page 05h: Address 060h)" on page 133 to 0, indicating a write operation.
4. Set bit 7 of the "VLAN Table Read/Write Control Register (Page 05h: Address 060h)" on page 133 to 1, starting the write operation. This bit returns to 0 when the write is complete.

The VLAN table can be read using the following steps:

1. Use the "VLAN Table Address Index Register (Page 05h: Address 061h)" on page 134 to define from which VLAN group to read the data.
2. Set bit 0 of the "VLAN Table Read/Write Control Register (Page 05h: Address 060h)" on page 133 to 1 to indicate a read operation.
3. Set bit 7 of the "VLAN Table Read/Write Control Register (Page 05h: Address 060h)" on page 133 to 1 start the read operation. This bit returns to 0 when the read is complete.
4. Read the "VLAN Table Entry Register (Page 05h: Address 063h)" on page 134 to obtain the VLAN table entry information.

# Jumbo Frame Support

The BCM5387 can receive and transmit frames of extended length on ports linked at gigabit speed. Referred to as jumbo frames, these packets are longer than 1518 bytes (when untagged), but shorter than 9728 bytes. This feature can be enabled on individual ports by writing to the "Jumbo Frame Port Mask Register (Page 040h, Address 01h)" on page 176. Jumbo packets can only be received or forwarded to 1000BASE-T linked ports that are jumbo-frame enabled. Jumbo packets consume larger blocks of buffer memory. Up to 38 buffer memory pages are required for storing the longest allowed jumbo frame. While there is no physical limitation to the number of ports that can be jumbo enabled, it is recommended that no more than two are enabled simultaneously to ensure system performance. There is no performance penalty for enabling additional jumbo ports beyond the potential strain on memory resources that can occur due to accumulated jumbo packets at multiple ports.

# Port Trunking/Aggregation

The BCM5387 supports MAC-based trunking. The trunking feature allows two ports to be grouped together as a single-link connection between two switch devices. This increases the effective bandwidth through a link and provides redundancy. The BCM5387 allows up to two trunk groups. Trunks are composed of predetermined port pairs and can be enabled via "Trunking Group Register (Page 032h, Address 090h)" on page 167. Ports within a trunk group must be of the same linked speed. By performing a dynamic hashing algorithm on the MAC address, each packet destined for the trunk is forwarded to one of the valid ports within the trunk group. This method has several key advantages. By dynamically performing this function, the traffic patterns can be more balanced across the ports within a trunk. In addition, the MAC-based algorithm provides dynamic failover. If a port within a trunking group fails, the other port within the trunk automatically assumes all traffic designated for the trunk. It allows for a seamless, automatic redundancy scheme. This hashing function can be performed on either the DA, SA, or DA/SA, depending on the Trunk Hash Selector bit of the "MAC Trunking Control Register (Page 032h, Address 01h)" on page 167.

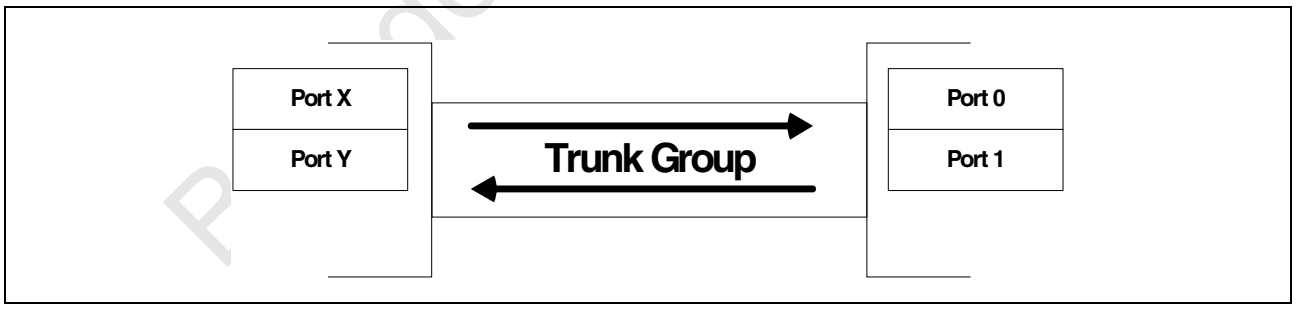


**Figure 4: Trunking**

# Rate Control

Forwarding broadcast traffic consumes switch resources, which can negatively impact the forwarding of other traffic. The rate-based broadcast storm suppression mechanism is used to protect regular traffic from an overabundance of broadcast or multicast traffic. This feature monitors the rate of ingressed traffic of programmable packet types. If the rates of these packet types exceed the programmable maximum rate, the packets are dropped or flow control is activated. To enable the Broadcast Storm Suppression, pull the BC_SUPP_EN high during power-on/reset. Alternatively, the feature can be activated in the "Port Rate Control Register (Page 041h, Address 010h)" on page 180.

The broadcast storm mechanism works on a credit-based rate system that figuratively uses a bucket to track the bandwidth of each port (see Figure 5). Credit is continually added to the bucket at a programmable bucket bit rate. Credit is decremented from the bucket whenever one of the programmable packet types is ingressed at the port. If no packets are ingressed for a considerable length of time, the bucket credit continues to increase up to a programmable-maximum bucket size. If a heavy burst of traffic is suddenly ingressed at the port, the bucket credit becomes drained. When the bucket is emptied, incoming traffic is constrained to the bucket bit rate (the rate at which credit is added to the bucket). At this point, excess packets are either dropped or deterred via flow control, depending upon the Suppression Drop mode in the "Global Rate Control Register (Page 041h, Address 00h)" on page 178.

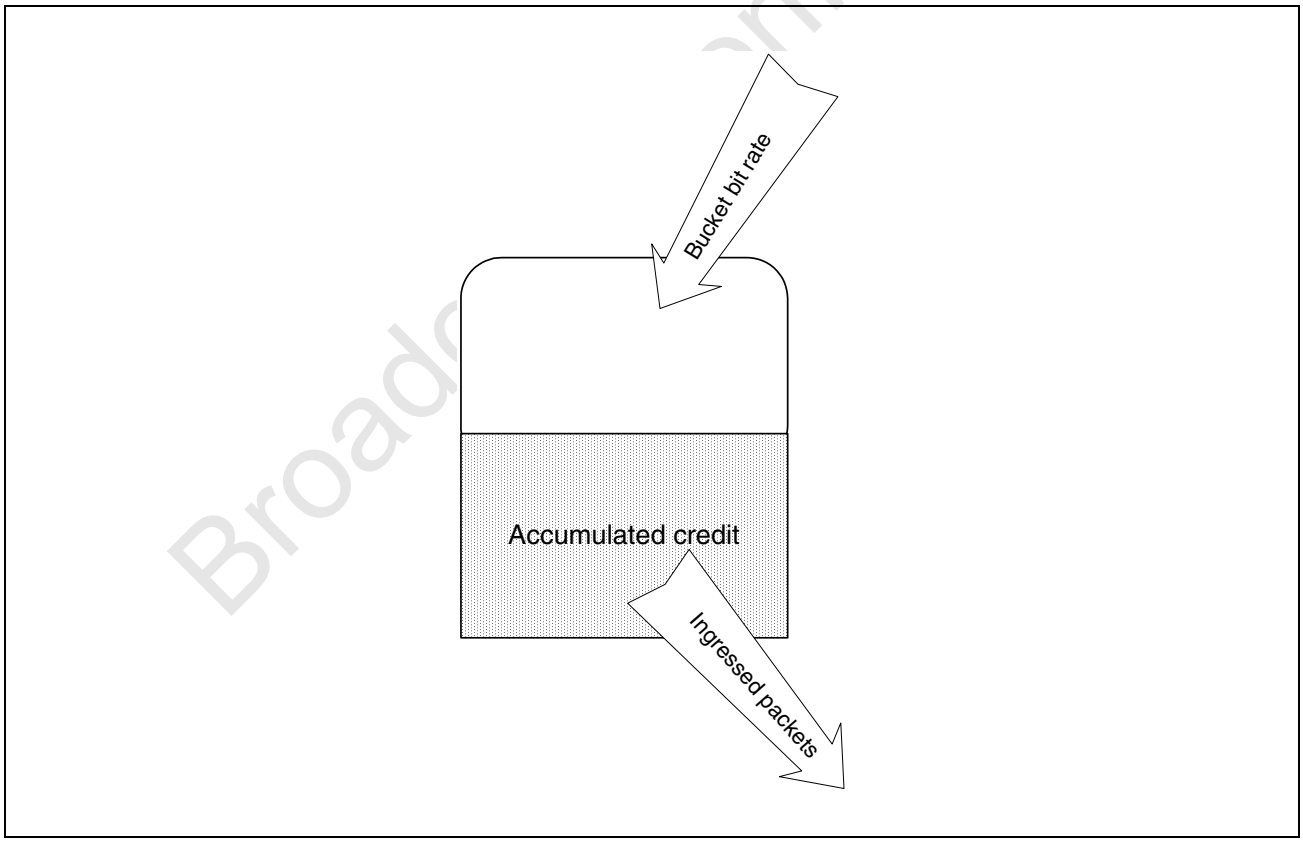


**Figure 5: Bucket Flow**

## The Two-Bucket System

For added flexibility, the BCM5387 employs two buckets to track the rate of ingressed packets. Each of the two buckets (Bucket 0 and Bucket 1) can be programmed to monitor different packet types via the Suppressed Packet Type Mask of the "Global Rate Control Register (Page 041h, Address 00h)" on page 178. For example, Bucket 0 could monitor broadcast packets, while Bucket 1 monitors multicast packets. Multiple packet types can be monitored by each bucket, and a packet type can be monitored by both buckets.

The rates of each bucket can be individually programmed (see "The Bucket Bit Rate" on page 30). For example, the broadcast packets of Bucket 0 could have a maximum rate of 3 Mbps, whereas the multicast packets of Bucket 1 could be allowed up to 80 Mbps. The size of each bucket can be programmed via the "Port Rate Control Register (Page 041h, Address 010h)" on page 180. This determines the maximum credit than can accumulate in each bucket. The Rate Count and Bucket Size can be individually programmed for each port, providing another level of flexibility. Suppression control can be enabled or disabled on a per-port basis via the "Port Rate Control Register (Page 041h, Address 010h)" on page 180. This system allows the user to control dual packet-type rates on a per-port basis.

## The Bucket Bit Rate

The relative ingress rates of each bucket can be programmed via the Rate Count value of the "Port Rate Control Register (Page 041h, Address 010h)" on page 180 on a per port basis. Each port has a programmable Rate Count value for Bucket 0 and Bucket 1. Additionally, the bit rate mode is programmed via the "Global Rate Control Register (Page 041h, Address 00h)" on page 178 on a chip basis. If this bit is 1, the packet rate is automatically scaled according to the port link speed. Ports operating at 1000 Mbps would be allotted a 100 times higher ingress rate than ports linked at 10 Mbps. Together, the Rate Count value and the bit rate mode determine the bucket bit rate, which is a reflection of how quickly data can be ingressed (Kbps) at the given port for a given bucket. The Rate Count values are specified in Table 2. Values outside these ranges are not valid entries.

***Table 2: Bucket Bit Rate***

| *Rate Count (RC)* | *Bit Rate Mode* | *Link Speed* | *Bucket Bit Rate Equation* | *Approximate Computed Bucket Bit Rate Values (as a function of RC)* |
|---|---|---|---|---|
| 1–28 | 0 | Any | = (RC x 8 x 1M) / 125 | 64 KB, 128 KB, 192 KB,..., 1.792 MB |
| 29–127 | 0 | Any | = (RC - 27) x 1M | 2 MB, 3 MB, 4 MB,..., 100 MB |
| 128–240 | 0 | Any | = (RC - 115) x 1M x 8 | 104 MB, 112 MB, 120 MB,..., 1000 MB |
| 1–125 | 1 | 10 Mbps | = (RC x 8 x 1M) / 100 | 0.08 MB, 0.16 MB, 0.24 MB,... 10 MB |
| 1–125 | 1 | 100 Mbps | = (RC x 8 x 1M) / 10 | 0.8 MB, 1.6 MB, 2.4 MB,..., 100 MB |
| 1–125 | 1 | 1000 Mbps | = RC x 8 x 1M | 8 MB, 16 MB, 24 MB,... 1000 MB |

***Note:*** 1M represents 1 x $10^6$.

# Protected Ports

The Protected Ports feature allows certain ports to be designated as protected. The protected ports are selected via the “Protected Port Selection Register (Page 00h: Address 24h)” on page 100. All other ports are non-protected. Traffic between protected port group members is blocked. However, protected ports are able to send traffic to unprotected ports. Unprotected port can send traffic to any port. Several applications that can benefit from protected ports:

- Aggregator: For example, all of the available ports are designated as protected ports except a single aggregator port. All traffic incoming to the protected ports will not be sent within the protected ports group. Any flooded traffic is forwarded only to the aggregator port.
- To prevent non-secured ports from monitoring important information on a server port, the server port and non-secured ports are designated as protected. The non-secured ports will not be able to receive traffic from the server port.

# Port Mirroring

The BCM5387 supports port mirroring, allowing ingress and/or egress traffic to be monitored by a single port defined as the mirror capture port. The BCM5387 can be configured to mirror the ingress traffic and/or egress traffic of any other port(s). Mirroring multiple ports is possible, but can create congestion at the mirror capture port. Several filters are used to decrease congestion.

## Enabling Port Mirroring

Port Mirroring is enabled by setting the Mirror Enable bit in the “Mirror Capture Control Register (Page 02h: Address 010h)” on page 115.

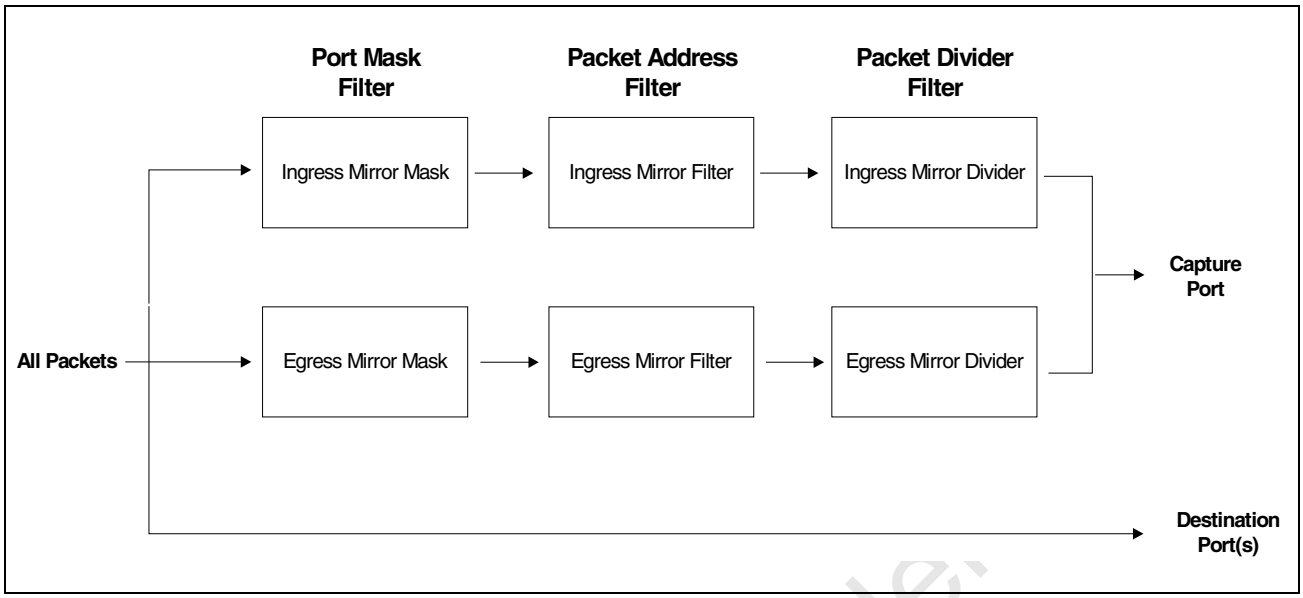


**Figure 6: Mirror Filter Flow**

## Capture Port

The Capture port is capable of monitoring other specified ports. Frames transmitted and received at the other ports are forwarded to the Capture port according to the "Mirror Filtering Rules"as discussed below. The capture port is specified by the Capture Port bits of the "Mirror Capture Control Register (Page 02h: Address 010h)" on page 115.

## Mirror Filtering Rules

Mirror filtering rules consist of a set of three filter operations (Port Mask, Packet Address, and Packet Divider) that are applied to traffic ingressed and/or egressed at a switch port.

### Port Mask Filter

The IN_MIRROR_MASK bits in the "Ingress Mirror Control Register (Page 02h: Address 012h)" on page 116 define the receive ports that are monitored. The OUT_MIRROR_MASK bits in the "Egress Mirror Control Register (Page 02h: Address 01Ch)" on page 118 define the transmit ports that are monitored.

Any number of ingress/egress ports can be programmed to be mirrored, but bandwidth restrictions on the one-mirror capture port should be taken under advisement so as not to cause congestion or packet loss.

### Packet Address Filter

The "Ingress Mirror Control Register (Page 02h: Address 012h)" on page 116 is used to set the type of filtering that is applied to frames received on the mirrored ports. The IN_MIRROR_FILTER bits select among the following:

- Mirror all received frames
- Mirror received frames with DA = x
- Mirror received frames with SA = x

Where x is the 48-bit MAC address programmed into the "Ingress Mirror MAC Address Register (Page 02h: Address 016h)" on page 117.

Likewise, the "Egress Mirror Control Register (Page 02h: Address 01Ch)" on page 118 is used to set the type of filtering that is applied to frames transmitted on the egressed mirrored ports. The filtering MAC address is specified in the "Egress Mirror MAC Address Register (Page 02h: Address 020h)" on page 119.

### Packet Divider Filter

The IN_DIV_EN bit in the "Ingress Mirror Control Register (Page 02h: Address 012h)" on page 116 allows further statistical sampling to be performed. When IN_DIV_EN = 1, the receive frames passing the initial filter are divided by the value IN_MIRROR_DIV, which is a 10-bit value stored in the "Ingress Mirror Divider Register (Page 02h: Address 014h)" on page 117. Only one out of every n frames is forwarded to the mirror capture port, where n = IN_MIRROR_DIV +1. This allows the following additional capabilities:

- Mirror every $n^{th}$ received frame
- Mirror every $n^{th}$ received frame with DA = x
- Mirror every $n^{th}$ received frame with SA = x

Similarly, the Egress Mirror Divide function is controlled by the "Egress Mirror Control Register (Page 02h: Address 01Ch)" on page 118 and the "Egress Mirror Divider Register (Page 02h: Address 01Eh)" on page 119.

**Note:** When multiple ingress ports have been enabled in the IN_MIRROR_MASK, the cumulative total packet count received from all ingress ports is divided by the value of IN_MIRROR_DIV to deliver the $n^{th}$ receive frame to the mirror capture port. Egressed frames are governed by the OUT_MIRROR_MASK bit and the OUT_MIRROR_DIV bit.

## IGMP Snooping

IGMP is a commonly used protocol to transmit video and multimedia streams over IP. When Enable IGMP IP Layer Snooping is set in the "Global Management Configuration Register (Page 02h: Address 00h)" on page 114, the BCM5387 forwards IGMP control packets to the IMP port based on the values contained in the protocol field of the IP header. The external management entity can then determine from the received IGMP control packets which ports should belong within which multicast address group. The management entity applies this by writing to the corresponding multicast address entry. See "Multicast Addresses" on page 37 for more information.

### Address Management

The BCM5387 Address Resolution Logic contains the following features:

- The two-bins-per-bucket address table configuration

- Hashing of the MAC/VID address to generate the address table pointer

The address management unit of the BCM5387 provides wire-speed learning and recognition functions. The address table supports approximately 4000 unicast/multicast addresses using on-chip memory.

## Address Table Organization

The MAC addresses are stored in embedded SRAM. Each bucket contains two entries (or bins). The address table has approximately 2000 buckets, with two entries in each bucket. This allows up to two different MAC addresses with the same hashed index bits to be simultaneously mapped into the address table.

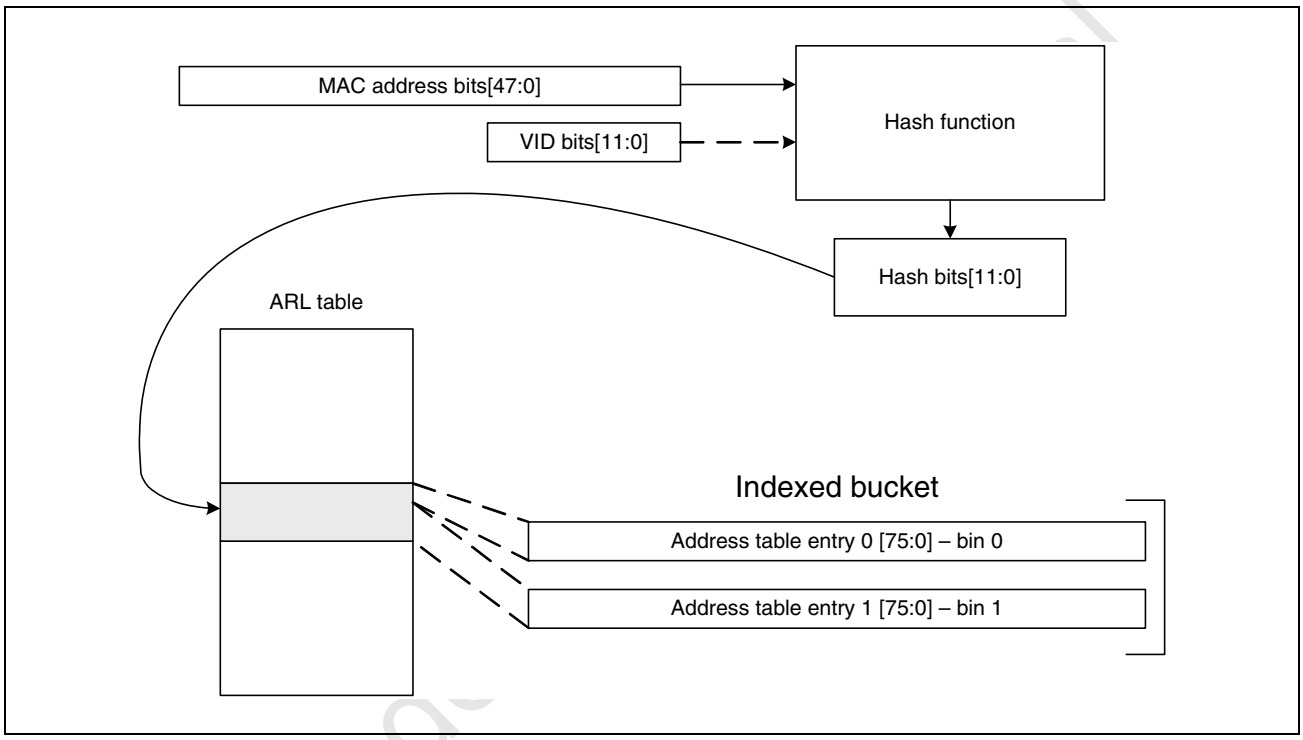


**Figure 7: Address Table Organization**

The index to the address table is computed using a hash algorithm based on the MAC address.

**Note:** If the Enable IEEE 802.1Q bit = 1 and VLAN Learning Mode bits = 11 in the "Global IEEE 802.1Q Register (Pages 034h, Address 00h)" on page 169, both the MAC address and the VLAN ID (VID) are used to compute the hashed index. See "IEEE 802.1Q VLAN" on page 26 for more information.

The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16-bit CRC hash value. Bits[11:0] of the hash are used as an index to the approximately 2000 buckets of the address table.

The CRC-CCITT polynomial is:

$x^{16}+x^{12}+x^5+1$

Hashing can be disabled by setting Hash Disable bit = 1 in the "Global ARL Configuration Register (Page 04h: Address 00h)" on page 120. When hashing is disabled, the BCM5387 device uses a direct-addressing method via the MAC address.

## Address Learning

Information is gathered from received unicast packets and learned or stored for the future purpose of forwarding frames addressed to the receiving port. During the receive process, the frame information (such as the Source Address [SA] and VID) is saved until completion of the packet. An entry is created in the ARL table memory if the following conditions are met:

- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast SA.
- If using IEEE 802.1Q VLAN, the packet is from an SA that belongs to the indicated VLAN domain.
- The packet does not have a reserved multicast destination address. The Multicast Learning bit of the "Reserved Multicast Control Register (Page 00h: Address 02Fh)" on page 101 can disable this condition.
- There is free space available in memory to which the hashed index points.

When unicast packets are dynamically learned, the VALID bit is set, the AGE bit is set, and the STATIC bit is cleared in the entry. See Table 4 on page 36 for a description of a unicast ARL entry.

Multicast addresses are not learned into the ARL table, but must be written via one of the "Programming Interfaces" on page 61. See "Writing an ARL Entry" on page 40 and Table 6 on page 37 for more information.

## Address Resolution and Frame Forwarding

Received packets are forwarded based on the information learned or written into the ARL table. Address resolution is the process of locating this information and assigning a forwarding destination to the packet. The Destination Address (DA) and VID of the received packet is used to calculate a hashed index to the ARL table. The hashed index key is used by the address resolution function to locate a matching ARL entry. The frame is assigned a destination based on the forward field (PORTID or IPMC0) of the ARL entry. If the address resolution function fails to return a matching ARL entry, the packet is flooded to all appropriate ports. The following two sections describe the specifics of address resolution and frame forwarding for "Unicast Addresses" on page 35 and "Multicast Addresses" on page 37.

### Unicast Addresses

Frames containing a unicast destination address are assigned a forwarding field corresponding to a single port. Listed below is the unicast address-resolution algorithm:

- If the Multiport Addressing feature is enabled and the DA matches one of the programmed multiport addresses, then it is forwarded accordingly. See "Using the Multiport Addresses" on page 42.
- The lower 12 bits of the hashed index key are used as a pointer into the address table memory, and both entries in the bucket are retrieved. The address resolution logic processes the two entries in parallel.
  - If the valid indicator is set and the address stored at one of the locations matches the index key of the packet received, the forwarding field port ID is assigned to the destination port of the packet.

  – If the destination port matches the source port, the packet is not forwarded.
- If the address resolution function fails to return a matching valid ARL entry and the Unicast DFL Forward bit of the "Port Forward Control Register (Page 00h: Address 021h)" on page 100 is set, the frame is forwarded according to the port map in the "Unicast Lookup Failed Forward Map Register (Page 00h: Address 032h)" on page 102.
- Otherwise, the packet is flooded to all appropriate ports.

See Table 3 for definitions of the unicast index key and the assigned forwarding field. The forwarding field for a unicast packet is the port ID contained in the matching ARL entry. See Table 4 on page 36 for a description of a unicast ARL entry.

***Table 3: Unicast Forward Field Definitions***

| *EN_1QVLAN* | *Index Key* | *Forwarding Field* |
|---|---|---|
| 1 | DA and VID | Port ID |
| 0 | DA | Port ID |

***Table 4: Address Table Entry for Unicast Address***

| *Field* | *Description* |
|---|---|
| VID | VLAN ID associated with the MAC address. |
| VALID | 1 = Entry is valid.<br>0 = Entry is empty. |
| STATIC | 1 = Entry is static—is not to be aged out and is written and updated by software.<br>0 = Entry is dynamically learned and aged. |
| AGE | 1 = Entry has been accessed or learned since last aging process.<br>0 = Entry has not been accessed since last aging process. |
| PRI | MAC-based priority (only valid for static entries) See "Quality of Service" on page 22 for more information. |
| Reserved | – |
| Reserved | Only 00 is valid. |
| PORTID | Port identifier. The port associated with the MAC address. |
| MAC ADDRESS | 48-bit MAC address. |

**Note:** The fields described in Table 4 can be written via the "ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h)" on page 126, "ARL Table Data Entry 0 Register (Page 05h: Address 018h)" on page 127, and the corresponding registers for entry 1.

Multicast ARL table entries are described in Table 6 on page 37.

## Multicast Addresses

Frames containing a multicast destination address are assigned a forwarding field corresponding to multiple ports specified in a port map. If the IP_MULTICAST bit is set in the "Port Forward Control Register (Page 00h: Address 021h)" on page 100, multicast frames are assigned a forwarding field corresponding to a multicast port map from the matching ARL entry. If no matching ARL entry is found, the packet is flooded to all appropriate ports.

Listed below is the multicast address resolution algorithm:

- If the DA matches one of the globally assigned reserved addresses between 01-80-C2-00-00-00 and 01-80-C2-00-00-2F, the packet is handled as described in Table 7 on page 38.
- If the Multiport Addressing feature is enabled and the DA matches one of the programmed Multiport Addresses, then it is forwarded accordingly. See "Using the Multiport Addresses" on page 42.
- Otherwise, the lower 12 bits of the hashed index key are used as a pointer into the ARL table memory, and both entries in the bucket are retrieved. The address resolution logic processes the two entries in parallel. If the valid indicator is set, and the address stored at one of the entry locations matches the index key of the packet received, the forwarding field port map is assigned to the destination port of the packet.
- If the address resolution function fails to return a matching valid ARL entry and the Multicast DFL Forward bit of the "Port Forward Control Register (Page 00h: Address 021h)" on page 100 is set, the frame is forwarded according to the port map in the "Multicast Lookup Failed Forward Map Register (Page 00h: Address 034h)" on page 103.
- Otherwise, all other multicast and broadcast packets are flooded to all appropriate ports.

See Table 5 on page 37 for definitions of the multicast index key and the assigned forwarding field. The forwarding field for a multicast packet is the port map contained in the matching ARL entry. See Table 6 on page 37 for a description of a multicast ARL entry. See "Accessing the ARL Table Entries" on page 39 for more information.

***Table 5: Multicast Forward Field Definitions***

| *EN_1QVLAN* | *IP_MULTICAST* | *Index Key* | *Forwarding Field* |
|---|---|---|---|
| 1 | 0 | DA and VID | Port ID |
| 0 | 0 | DA | Port ID |
| 1 | 1 | DA and VID | IPMC0 |
| 0 | 1 | DA | IPMC0 |

***Table 6: Address Table Entry for Multicast Address***

| *Field* | *Description* |
|---|---|
| VID | VLAN ID associated with the MAC address. |
| VALID | 1 = Entry is valid.<br>0 = Entry is empty. |
| STATIC | 1 = Entry is static—is not aged out and is written and updated by software.<br>0 = Not defined. |
| AGE | The AGE bit is ignored for static ARL table entries. |

*Table 6: Address Table Entry for Multicast Address (Cont.)*

| Field | Description |
|---|---|
| PRI | MAC-based priority (only valid for static entries) See "Quality of Service" on page 22 for more information. |
| Reserved | – |
| IPMC0 [8:0] | Multicast forwarding mask. The field is a per port vector. Bits[4:0] correspond to ports [4:0]and bit 8 corresponds to IMP port, respectively.<br>1 = Forwarding enable.<br>0 = Forwarding disable. |
| MAC ADDRESS | 48-bit MAC address. |

**Note:** The fields described in Table 6 can be written via the "ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h)" on page 126, "ARL Table Data Entry 0 Register (Page 05h: Address 018h)" on page 127, and the corresponding registers for entry 1.

Unicast ARL table entries are described in Table 4 on page 36.

## Reserved Multicast Addresses

Table 7 summarizes the actions taken for specific reserved multicast addresses. Packets identified with these destination addresses are handled uniquely since they are designed for special functions. Bits[4:0] of the "Reserved Multicast Control Register (Page 00h: Address 02Fh)" on page 101 program groups of these addresses to be dropped or forwarded. Writing to these bits can change the default action of Unmanaged mode summarized in Table 7.

*Table 7: Behavior for Reserved Multicast Addresses*

| MAC Address | Function | IEEE 802.1 Specified Action | Unmanaged Mode Action | Managed Mode Action |
|---|---|---|---|---|
| 01-80-C2-00-00-00 | Bridge group address | Drop frame | Flood frame | Forward frame to IMP only |
| 01-80-C2-00-00-01 | IEEE 802.3x MAC control frame | Drop frame | Receive MAC determines if it is a valid pause frame and then acts accordingly | Receive MAC determines if valid pause frame and acts accordingly |
| 01-80-C2-00-00-02 | Reserved | Drop frame | Drop frame | Forward to frame management port only |
| 01-80-C2-00-00-03 | IEEE 802.1x port-based network access control | Drop frame | Drop frame | Forward frame to management port only |
| 01-80-C2-00-00-04~ 01-80-C2-00-00-0F | Reserved | Drop frame | Drop frame | Forward frame to management port only |

*Table 7: Behavior for Reserved Multicast Addresses (Cont.)*

| *MAC Address* | *Function* | *IEEE 802.1 Specified Action* | *Unmanaged Mode Action* | *Managed Mode Action* |
|---|---|---|---|---|
| 01-80-C2-00-00-10 | All LANs bridge management group address | Forward frame | Flood frame | Forward frame to all ports including management port |
| 01-80-C2-00-00-11 ~ 01-80-C2-00-00-1F | Reserved | Forward frame | Flood frame | Forward frame to all ports excluding management port |
| 01-80-C2-00-00-20 | GMRP address | Forward frame | Flood frame | Forward frame to all ports excluding management port, or forward frame to management port only (by setting bit 4 of page 34, offset 04h register) |
| 01-80-C2-00-00-21 | GVRP address | Forward frame | Flood frame | Forward frame to all ports excluding management port, or forward frame to management port only (by setting bit 5 of page 34, offset 04h register) |
| 01-80-C2-00-00-22~ 01-80-C2-00-00-2F | Reserved | Forward frame | Flood frame[a] | Forward frame to all ports excluding management port |

a. Frames flood to all ports. Certain exclusions apply, such as VLAN restrictions.

## Static Address Entries

The BCM5387 supports static ARL table entries that are created and updated via one of the "Programming Interfaces" on page 61. These entries can contain either unicast or multicast destinations. The entries are created by writing the entry location via "Page 05h: ARL/VTBL Access Registers" on page 124 and setting the STATIC bit. The AGE bit is ignored. Static entries do not automatically learn MAC addresses or port associations and are not aged out by the automatic internal aging process. See "Writing an ARL Entry" on page 40 for details.

## Accessing the ARL Table Entries

ARL table entries are accessed by one of two mechanisms. The first mechanism uses the ARL read/write control, which allows an address-entry location to be read, modified, or written based on the value of a known MAC address. The second mechanism searches the ARL table sequentially, returning all valid entries.

## Reading an ARL Entry

To read an ARL entry:

1. Set the MAC address in the "MAC Address Index Register (Page 05h: Address 02h)" on page 125.
2. Set the VLAN ID in the "VLAN ID Index Register (Page 05h: Address 08h)" on page 126. This is necessary only if the VID is used in the index key.
3. Set the ARL_R/W bit to 1 in the "ARL Table Read/Write Control Register (Page 05h: Address 00h)" on page 125.
4. Set the START/DONE bit to 1 in the "ARL Table Read/Write Control Register (Page 05h: Address 00h)" on page 125. This initiates the read operation.

The MAC address and VID are used to calculate the hashed index to the ARL table. The matching ARL bucket is read. The contents of entry 0 are stored in the "ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h)" on page 126 and the "ARL Table Data Entry 0 Register (Page 05h: Address 018h)" on page 127. The contents of entry 1 are stored in the "ARL Table MAC/VID Entry 1 Register (Page 05h: Address 20h)" on page 128 and the "ARL Table Data Entry 1 Register (Page 05h: Address 028h)" on page 129.

Entries that do not have the VALID bit set should be ignored. The contents of the MAC/VID registers must be compared against the known MAC address and VID. Entries that do not match may be a valid entry, but are not a valid match for the index key. All other read entries are considered valid ARL entries.

## Writing an ARL Entry

To write an ARL entry:

1. Follow the steps in "Reading an ARL Entry"to read the ARL entry matching the MAC address and VID that are written to the table.
2. Keep the values that remain from the previous read operation:
   - "MAC Address Index Register (Page 05h: Address 02h)" on page 125
   - "VLAN ID Index Register (Page 05h: Address 08h)" on page 126
   - "ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h)" on page 126
   - "ARL Table Data Entry 0 Register (Page 05h: Address 018h)" on page 127
   - "ARL Table MAC/VID Entry 1 Register (Page 05h: Address 20h)" on page 128
   - "ARL Table Data Entry 1 Register (Page 05h: Address 028h)" on page 129
3. Determine which ARL entry (0 or 1) is to be written based on the existing values of the VALID bit and MAC/VID bits.
4. Modify the correct entry as necessary. Set the STATIC bit so that the entry is not aged out.
5. Set the ARL_R/W bit to 0 in the "ARL Table Read/Write Control Register (Page 05h: Address 00h)" on page 125.
6. Set the START/DONE bit to 1 in the "ARL Table Read/Write Control Register (Page 05h: Address 00h)" on page 125. This initiates the write operation.

The MAC address and VID are used to calculate the hashed index to the ARL table. Both entry 0 and entry 1 are written to the matching ARL bucket.

### Searching the ARL Table

The second method to access the ARL table is through the ARL search control. The entire ARL table is searched sequentially, revealing each valid ARL entry. Setting the Start/Done bit in the "ARL Table Search Control Register (Page 05h: Address 030h)" on page 130 begins the search from the top of the ARL table. This bit is cleared when the search is complete. During the ARL search, the Search Valid bit indicates when a found valid 76-bit entry is available in the "ARL Table Search MAC/VID Result Register (Page 05h: Address 033h)" on page 131 and the "ARL Table Search Data Result Register (Page 05h: Address 03Bh)" on page 132. When the host reads the contents of the "ARL Table Search Data Result Register (Page 05h: Address 03Bh)" on page 132, the search process automatically continues to seek the next valid entry in the address table. Invalid address entries are skipped, providing the host with an efficient way of searching the entire address table.

The ARL search and ARL read/write operations execute in parallel with other register accesses. This allows the host processor to start a read, write, or search process and then read/write other registers, returning periodically to see if the operation has completed.

## Address Aging

The aging process periodically removes dynamically learned addresses from the ARL table. When an ARL entry is learned or referenced, the AGE bit is set to 1. The aging process scans the ARL table at regular intervals, aging out entries not accessed during the previous one to two aging intervals. The aging interval is programmable via the Aging Enable and AGE Time bits in the "Aging Time Control Register (Page 02h: Address 06h)" on page 115.

Entries that are written and updated via one of the "Programming Interfaces" on page 61, should have the STATIC bit set. Thus, they are not affected by the aging process.

For each entry in the ARL table, the aging process performs the following:

- If the VALID bit is not set, then do nothing.
- If the VALID bit is set and the STATIC is set, then do nothing.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is set, then clear the AGE bit. This keeps the entry in the table, but marks it so that it is removed if it is not accessed before the subsequent aging scan.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is reset, then reset the VALID bit. This effectively deletes the entry from the ARL table. The entry has been aged out.

## Fast Aging

The fast aging function can be enabled per port or VLAN ID:

- The port fast aging can be enabled by setting the Start/Done of the "Fast-Aging Control Register (Page 00h: Address 088h)" on page 108, the Fast Age All Ports bit of the "Fast-Aging Port Control Register (Page 00h: Address 089h)" on page 108, and the appropriate port bits in the "Fast-Aging Port Control Register (Page 00h: Address 089h)" on page 108.
- The VLAN ID fast aging can be enabled by setting the Start/Done of the "Fast-Aging Control Register (Page 00h: Address 088h)" on page 108, the Fast Age All VID bit of the "Fast-Aging VID Control Register (Page 00h: Address 08Ah)" on page 108, and the appropriate VLAN ID bits of the "Fast-Aging VID Control Register (Page 00h: Address 08Ah)" on page 108.

When fast aging is enabled, the switch continuously searches the ARL table and ages out the ARL entry for that port or for VLAN ID.

## Using the Multiport Addresses

The “Multiport Address 1 Register (Page 04h: Address 010h)” on page 121 and the “Multiport Address 2 Register (Page 04h: Address 020h)” on page 122 can be used to forward a given MAC address to multiple ports. Packets with a corresponding DA are forwarded to the port map contained in the “Multiport Vector 1 Register (Page 04h: Address 016h)” on page 122 or the “Multiport Vector 2 Register (Page 04h: Address 026h)” on page 123. These registers must be enabled via the Multiport Address Enable bit in the “Global ARL Configuration Register (Page 04h: Address 00h)” on page 120.

# Section 3: System Functional Blocks

## Overview

The BCM5387 includes the following blocks:

- “Media Access Controller” on page 43
- “Frame Management Block” on page 45
- “MIB Engine” on page 48
- “Integrated High-Performance Memory” on page 55
- “Switch Controller” on page 56

Each of these is discussed in more detail in the following sections.

## Media Access Controller

The BCM5387 contains five 10/100/1000 GMACs.

The MAC automatically selects the appropriate speed (CSMA/CD or full-duplex) based on the PHY auto-negotiation result. In full-duplex mode, IEEE 802.3x PAUSE frame-based flow control is also determined through auto-negotiation. The MAC is IEEE 802.3, IEEE 802.3u, and IEEE 802.3x compliant.

### Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than 1518 bytes (when untagged) or 9728 bytes for jumbo-enabled ports

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded. Receive functions can be disabled by writing to “Port Traffic Control Register (Page 00h: Address 00h)” on page 96.

### Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and inter-packet gap enforcement.

In 10/100 Mbps half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the IEEE 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the 16th consecutive collision, the backoff algorithm starts over at the initial state, and the collision counter is reset and attempts to transmit the current frame continue. Following a late collision, the frame is aborted, and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame, and the 96 bit-times of IPG have been observed. Transmit functions can be disabled by writing to "Port Traffic Control Register (Page 00h: Address 00h)" on page 96.

# Flow Control

The BCM5387 implements an intelligent flow-control algorithm to minimize the system impact resulting from traffic congestion. Buffer memory allocation is adaptive to the status of each port's speed and duplex mode, providing an optimal balance between flow management and per-port memory depth. The BCM5387 initiates flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in both full-and half-duplex modes.

## 10/100 Mbps Half-Duplex

In 10/100 half-duplex mode, the MAC backpressures a receiving port by transmitting a 96-bit time jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow-control state.

## 10/100/1000 Mbps Full-Duplex

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow-control frames are recognized and, when properly received, set the flow-control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control, the transmit controller transmits a MAC control PAUSE frame with the pause time set to maximum. When the condition that caused the flow-control state is no longer present, a second MAC control PAUSE frame is sent with the pause time field set to 0.

The flow control capabilities of the BCM5387 are enabled based on the results of auto-negotiation and the state of the ENFDXFLOW and ENHDXFLOW control signals loaded during reset. Flow control in half-duplex mode is independent of the state of the link partner flow control (IEEE 802.3x) capability. See Table 8 for detailed information.

*Table 8: Flow Control Modes*

| *Link Partner Flow Control (IEEE 802.3x)* | *Control Input ENFDXFLOW* | *Control Input ENHDXFLOW* | *Auto-Negotiated Link Speed* | *Flow Control Mode* |
|---|---|---|---|---|
| X | X | 0 | Half-duplex | Disabled |
| X | X | 1 | Half-duplex | Jam pattern |
| 0 | 0 | X | Full-duplex | Disabled |
| 0 | 1 | X | Full-duplex | Disabled |
| 1 | 0 | X | Full-duplex | Disabled |
| 1 | 1 | X | Full-duplex | IEEE 802.3x flow control |

# Frame Management Block

The RvMII/GMII/RGMII port configured as a frame management port is referred to as the Independent Management Port (IMP). The IMP can be used as a full-duplex 1000/100/10 Mbps port and can be configured to operate in RGMII, GMII, or RvMII modes. This port can be used to forward extensive management information to the external management agent, such as BPDUs, mirrored frames, or frames addressed to other static address entries that have been identified as a special interest to the management system.

## Frame Forwarding

Frame forwarding to the Frame Management port is given special consideration:

- Unicast, Multicast, and Broadcast Packets—forwarded to the Frame Management port based on the state of bits[4:2] of the "IMP Traffic Control Register (Page 00h: Address 08h)" on page 97. If these bits are cleared, no frame data is forwarded to the Frame Management port with the exception of frames meeting the criteria in "Port Mirroring" on page 31.
- Reserved Multicast Packets—frames with IEEE 802.1 administered reserved multicast addresses (DA between
  01-80-C2-00-00-00 and 01-80-C2-00-00-2F) are forwarded to the IMP with a header that includes the ingress port ID. See "Reserved Multicast Addresses" on page 38.
- Directed Frame Management Agent Packets—packets with the DA equal to one of the MAC addresses associated with the management port. These addresses are generally entered as static addresses by the management entity itself.

## Broadcom Management Tag

The BCM5387 device intrusively tags frames destined to the management entity to allow the identity of the originating ingress port to be retained. Additional header information is inserted into the original frame between the original SA field and Type/Length fields. The tag includes the BRCM Type (8874h) field and the BRCM Tag field. A recalculated FCS is appended to the resultant frame before the frame is forwarded. The management frame format is defined in Table 9.

***Table 9: Transmit/Receive Frame Format Over Management Port***

| Destination Address | Source Address | BRCM Type | BRCM Tag (32 bits) | Original Type/Length | Frame Data | Original FCS | Recalculated FCS |
|---|---|---|---|---|---|---|---|

Similarly, the external frame management entity must insert the BRCM Type/Length and Tag fields into frames it wishes to send into the management port to be routed to specific egress ports. The OPCODE within the Tag field determines how the frame is handled and allows frames to be forwarded using the normal address lookup or via a port ID designation within the tag.

The BRCM Tag and BRCM Type/Length fields are transmitted with the convention of highest significant octet first, followed by the lowest significant octet, etc., and with the least significant bit of each octet transmitted out from the MAC first. So, for the BRCM Type/Length field in Table 10, the most significant octet would be transmitted first (bits[24:31]), with bit 24 being the first bit transmitted.

Item 10 on page 46 shows the format of the BRCM Tag field for frames egressed at the IMP port. The OPCODE field slightly modifies the use and validity of some fields in the tag (see Table 12 on page 46). Table 11 on page 46 shows the format of the BRCM Tag field for frames ingressed at the IMP port. Table 13 on page 47 identifies each of the other fields in the BRCM Tag in detail.

***Table 10: Egress BRCM Tag Format***

| ***Tag [31:29]*** | ***Tag [28:15]*** | ***Tag [14:4]*** | ***Tag [3:0]*** |
|---|---|---|---|
| Opcode = 000 | FrameByteCount [13:0] | NA | SrcPortID [3:0] |

***Table 11: Ingress BRCM Tag Format***

| ***Tag [31:29]*** | ***Tag [28:9]*** | ***Tag [8:4]*** | ***Tag [3:0]*** |
|---|---|---|---|
| Opcode = 000 | NA | NA | NA |
| Opcode = 010 | NA | NA | DSTPortID [3:0] |
| Opcode = 011 | NA | | FowardMap [8:0] = Tag [8:0] |

***Table 12: OPCODE Field in Ingress BRCM Tag***

| ***OpCodes*** | ***Name*** | ***Description*** |
|---|---|---|
| 0 0 0 | Unicast/Multicast | Frame treated like a normal network port. If egress frame is unicast/ multicast, it is checked by ARL. If frame is broadcast, it follows broadcast rules. |
| 0 0 1 | Reserved | – |
| 0 1 0 | Egress Directed | Frame is forwarded to a single destination port based on Tag [3:0]. IMP loopback can be configured by setting Tag bits to the IMP Port ID. |
| 0 1 1 | Multiple Egress Directed | Frame forward map is copied from TAG[8:0]. IMP loopback can be configured by setting the IMP Port bit. |
| 1 x x | Reserved | Reserved. |

*Table 13: Fields in BRCM Tag for Management Port Frame*

| *Field* | *Name* | *Description* |
|---|---|---|
| DSTPortID | Destination Port ID | Indicates the destination Port ID for egress-directed frames.<br>DSTPortID[0100] to DSTPortID[0000] corresponds to ports [4:0].<br>DSTPortID[1000] corresponds to the IMP port. |
| ForwardMap | Forward Map | Port map signifying the ports to which the frame is to be sent.<br>Bits[7:0] correspond to Port [7:0].<br>Bit 8 corresponds to the IMP port. |
| SRCPortID | Source Port ID | Indicates the source Port ID for ingress directed frames.<br>SRCPortID[0100] to SRCPortID[0000] corresponds to ports [4:0].<br>SRCPortID[1000] corresponds to the IMP port. |
| FrameByte Count [13:0] | Frame Byte Count | This 14-bit field incorporates the byte count of the entire Ethernet frame octet count starting at the DA field and inclusive of CRC, but not including the BRCM Type, BRCM Tag, and recalculated FCS. |

## Additional Frame Management Port Configuration

The Frame Management port is given special consideration when configuring some of the management-related features. Refer to "Quality of Service" on page 22, "Port Mirroring" on page 31, and "IEEE 802.1Q VLAN" on page 26 for more information.

# MIB Engine

The MIB Engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM5387 implements 70-plus MIB counters on a per-port basis. MIB counters can be categorized into three groups: receive-only counters, transmit-only counters, and receive or transmit counters. This latter group can, as a group, be selectively steered to the receive or transmit process on a per-port basis. The section below describes each individual counter.

## MIB Counters Per Port

***Table 14: Receive Only Counters (18)***

| *Name* | *Description* |
|---|---|
| **RxDropPkts (32-bit)** | The number of good packets received by a port that were dropped due to a lack of resources (e.g., lack of input buffers) or were dropped due to a lack of resources before a determination of the validity of the packet was able to be made (e.g., receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxExcessSizeDisc, the RxAlignmentErrors, or the RxFCSErrors counters. |
| **RxOctets (64-bit)** | The number of data bytes received by a port (excluding preamble, but including FCS), including bad packets. |
| **RxBroadcastPkts (32-bit)** | The number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets. The maximum packet size can be programmed via "Jumbo MIB Good Frame Max Size Register (Page 040h, Address 05h)" on page 176. |
| **RxMulticastPkts (32-bit)** | The number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. The maximum packet size can be programmed via "Jumbo MIB Good Frame Max Size Register (Page 040h, Address 05h)" on page 176. |
| **RxSAChanges (32-bit)** | The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network. The maximum packet size can be programmed via "Jumbo MIB Good Frame Max Size Register (Page 040h, Address 05h)" on page 176. |
| **RxUndersizePkts (32-bit)** | The number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS). |
| **RxOversizePkts (32-bit)** | The number of good packets received by a port that are greater than 1522 bytes (tagged) and 1518 bytes (untagged). Note that this counter alone is incremented for packets in the range 1523–1536 bytes inclusive, whereas both this counter and the RxExcessSizeDisc counter are incremented for packets of 1537 bytes and higher. The maximum packet size can be programmed via "Jumbo MIB Good Frame Max Size Register (Page 040h, Address 05h)" on page 176. |
| **RxFragments (32-bit)** | The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error. |

*Table 14: Receive Only Counters (18) (Cont.)*

| *Name* | *Description* |
|---|---|
| **RxJabbers (32-bit)** | The number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error. |
| **RxUnicastPkts (32-bit)** | The number of good packets received by a port that are addressed to a unicast address. The maximum packet size can be programmed via "Jumbo MIB Good Frame Max Size Register (Page 040h, Address 05h)" on page 176. |
| **RxAlignmentErrors (32-bit)** | The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and 1522 bytes, inclusive, and have a bad FCS with a non-integral number of bytes. |
| **RxFCSErrors (32-bit)** | The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and 1522 bytes inclusive, and have a bad FCS with an integral number of bytes. |
| **RxGoodOctets (64-bit)** | The total number of bytes in all good packets received by a port (excluding framing bits, but including FCS). The maximum packet size can be programmed via "Jumbo MIB Good Frame Max Size Register (Page 040h, Address 05h)" on page 176. |
| **RxExcessSizeDisc (32-bit)** | The number of good packets received by a port that are greater than 1536 bytes (excluding framing bits but including the FCS) and were discarded due to excessive length. Note that the RxOversizePkts counter alone is incremented for packets in the range 1523–1536 bytes inclusive, whereas both this counter and the RxOversizePkts counter are incremented for packets of 1537 bytes and higher |
| **RxPausePkts (32-bit)** | The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88-08h), have a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE opcode (00-01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3 compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a non-compliant transmitting device on the network. |
| **RxSymbolErrors (32-bit)** | The total number of times a valid-length packet was received at a port and at least one invalid data symbol was detected. The counter only increments once per carrier event and does not increment on detection of a collision during the carrier event. |
| **RxQoSQPkt (32-bit)** | The total number of good packets received in any priority, which is specified in the MIB Queue Select register when QoS is enabled. |
| **RxQoSQOctet (64-bit)** | The total number of good bytes received in any priority, which is specified in the MIB Queue Select register when QoS is enabled. |

*Table 15: Transmit Counters Only (15)*

| *Name* | *Description* |
|---|---|
| **TxDropPkts (32-bit)** | This counter is incremented every time a transmit packet is dropped due to lack of resources (e.g., transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters. |
| **TxOctets (64-bit)** | The total number of good bytes of data transmitted by a port (excluding preamble but including FCS). |
| **TxBroadcastPkts (32-bit)** | The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets. |
| **TxMulticastPkts (32-bit)** | The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. |
| **TxCollisions (32-bit)** | The number of collisions experienced by a port during packet transmissions. |
| **TxUnicastPkts (32-bit)** | The number of good packets transmitted by a port that are addressed to a unicast address. |
| **TxSingleCollision (32-bit)** | The number of packets successfully transmitted by a port that have experienced exactly one collision. |
| **TxMultipleCollision (32-bit)** | The number of packets successfully transmitted by a port that have experienced more than one collision. |
| **TxDeferredTransmit (32-bit)** | The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy. |
| **TxLateCollision (32-bit)** | The number of times that a collision is detected later than 512 bit-times into the transmission of a packet. |
| **TxExcessiveCollision (32-bit)** | The number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts. |
| **TxPausePkts (32-bit)** | The number of PAUSE events at each port. |
| **TxFrameInDisc (32-bit)** | The number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue (not maintained or reported in the MIB counters). Located in the Congestion Management registers (Page 0Ah). This attribute only increments if a network device is not acting in compliance with a flow control request, or the BCM5387 internal flow-control/buffering scheme has been misconfigured. |
| **TxQoSQPkt (32-bit)** | The total number of good packets transmitted on any queue, which is specified in MIB Queue Select register when QoS is enabled. |
| **TxQoSQOctet (64-bit)** | The total number of good bytes transmitted on any queue, which is specified in MIB Queue Select register when QoS is enabled. |

***Table 16: Transmit or Receive Counters (10) Description of Counter***

| ***Name*** | ***Description*** |
|---|---|
| Pkts64Octets (32-bit) | The number of packets (including error packets) that are 64 bytes long. |
| Pkts65to127Octets (32-bit) | The number of packets (including error packets) that are between 65 and 127 bytes long. |
| Pkts128to255Octets (32-bit) | The number of packets (including error packets) that are between 128 and 255 bytes long. |
| Pkts256to511Octets (32-bit) | The number of packets (including error packets) that are between 256 and 511 bytes long. |
| Pkts512to1023Octets (32-bit) | The number of packets (including error packets) that are between 512 and 1023 bytes long. |
| Pkts1024to1522Octets (32-bit) | The number of packets (including error packets) that are between 1024 and 1522 bytes long. |
| Pkts1523to2047Octets (32-bit) | The number of packets (including error packets) that are between 1523 and 2047 bytes long. |
| Pkts2048to4095Octets (32-bit) | The number of packets (including error packets) that are between 2048 and 4095 bytes long. |
| Pkts4096to8191Octets (32-bit) | The number of packets (including error packets) that are between 4096 and 8191 bytes long. |
| Pkts8192to9728Octets (32-bit) | The number of packets (including error packets) that are between 8192 and 9728 bytes long. |
| ***Total number of counters per port: 43*** | |

Table 17 identifies the mapping of the BCM5387 MIB counters and their generic mnemonics to the specific counters and mnemonics for each of the key IETF MIBs that are supported. Note that direct mappings are defined. However, there are several additional statistics counters, which are indirectly supported that make up the full complement of the counters required to fully support each MIB. These are shown in Table 18 on page 54. Finally, Table 19 on page 55 identifies the additional counters supported by the BCM5387 and references the specific standard or reason for the inclusion of the counter.

***Table 17: Directly Supported MIB Counters***

| *BCM5387 MIB* | *Ethernet-Like MIB RFC 1643* | *Bridge MIB RFC 1493* | *MIB II Interface RFC 1213/1573* | *RMON MIB RFC 1757* |
|---|---|---|---|---|
| RxDropPkts | dot3StatsInternalMACReceiveErrors | dot1dTpPortInDiscards | ifInDiscards | – |
| RxOctets | – | – | ifInOctets | etherStatsOctets |
| RxBroadcastPkts | – | – | ifInBroadcastPkts | etherStatsBroadcastPkts |
| RxMulticastPkts | – | – | ifInMulticastPkts | etherStatsMulticastPkts |
| RxSAChanges | Note 2 | Note 2 | Note 2 | Note 2 |
| RxUndersizePkts | – | – | – | etherStatsUndersizePkts |
| RxOversizePkts | dot3StatsFrameTooLongs | – | – | etherStatsOverrsizePkts |
| RxFragments | – | – | – | eytherStatsFragments |
| RxJabbers | – | – | – | etherStatsJabbers |
| RxUnicastPkts | – | – | ifInUcastPkts | – |
| RxAlignmentErrors | dot3StatsAlignmentErrors | – | – | – |
| RxFCSErrors | dot3StatsFCSErrors | – | – | – |
| RxGoodOctets | – | – | – | – |
| RxExcessSizeDisc | Note 2 | Note 2 | Note 2 | Note 2 |
| RxPausePkts | Note 2 | Note 2 | Note 2 | Note 2 |
| RxSymbolErrors | Note 2 | Note 2 | Note 2 | Note 2 |
| Note 1 | – | – | ifInErrors | – |
| Note 1 | – | – | ifInUnknownProtos | – |
| Note 1 | — | dot1dTpPortInFrames | – | – |
| TxDropPkts | dot3StatsInternalMACTransmitErrors | – | ifOutDiscards | – |
| TxOctets | – | – | ifOutOctets Note 3 | – |
| Note 1 | – | dot1dTpPortOutFrames | – | – |
| TxBroadcastPkts | – | – | ifOutBroadcastPkts | – |

*Table 17: Directly Supported MIB Counters (Cont.)*

| *BCM5387 MIB* | *Ethernet-Like MIB RFC 1643* | *Bridge MIB RFC 1493* | *MIB II Interface RFC 1213/1573* | *RMON MIB RFC 1757* |
|---|---|---|---|---|
| TxMulticastPkts | – | – | ifOutMulticastPkts | – |
| TxCollisions | – | – | – | etherStatsCollisions |
| TxUnicastPkts | – | – | ifOutUcastPkts | – |
| TxSingleCollision | dot3StatsSingle CollisionFrames | – | – | – |
| TxMultipleCollision | dot3StatsMultiple CollisionFrames | – | – | – |
| TxDeferredTransmit | dot3StatsDeferred Transmissions | – | – | – |
| TxLateCollision | dot3StatsLate Collision | – | – | – |
| TxExcessiveCollision | dot3StatsExcessive Collision | – | – | – |
| TxFrameInDisc | Note 2 | Note 2 | Note 2 | Note 2 |
| TxPausePkts | Note 2 | Note 2 | Note 2 | Note 2 |
| Note 4 | dot3StatsCarrier SenseErrors | – | – | – |
| Note 1 | – | – | ifOutErrors | – |
| Pkts64Octets | – | – | – | etherStatsPkt64 Octets |
| Pkts65to127Octets | – | – | – | etherStatsPkt65to 127Octets |
| Pkts128to255Octets | – | – | – | etherStatsPkt128to 255Octets |
| Pkts256to511Octets | – | – | – | etherStatsPkt256to 511Octets |
| Pkts512to1023Octets | – | – | – | etherStatsPkt512to 1023Octets |
| Pkts1024to1522Octet s | – | – | – | etherStatsPkt1024to 1522Octets |
| Note 1 | – | – | – | etherStatsDrop Events |
| Note 1 | – | – | – | etherStatsPkts |
| Note 1 | – | – | – | etherStatsCRCAlign Errors |
| Note 4 | dot3StatsSQETest Errors | – | – | – |

*Table 17: Directly Supported MIB Counters (Cont.)*

| BCM5387 MIB | Ethernet-Like MIB RFC 1643 | Bridge MIB RFC 1493 | MIB II Interface RFC 1213/1573 | RMON MIB RFC 1757 |
|---|---|---|---|---|

Note 1: Derived by summing two or more of the supported counters. See Table 18 on page 54 for specific details.
Note 2: Extensions required by recent Standards developments or BCM5387 operation specifics.
Note 3: The MIB II interfaces specification for ifOutOctets includes preamble/SFD and errored bytes. Because IEEE 802.3 compliant MACs have no requirement to keep track of the number of transmit bytes in an errored frame, this count is impossible to maintain. The TxOctets counter maintained by the BCM5387 is consistent with good bytes transmitted, excluding preamble, but including FCS. The count can be adjusted to more closely match the ifOutOctets definition by adding the preamble for TxGoodPkts and possibly an estimate of the octets involved in TxCollisions and TxLateCollision.
Note 4: The attributes TxCarrierSenseErrors and TxSQETestErrors are not supported in the BCM5387. These attributes were originally defined to support coax-based AUI transceivers. The BCM5387 integrated transceiver design means these error conditions are eliminated. MIBs intending to support such counters should return a value of 0 or not supported.

*Table 18: Indirectly Supported MIB Counters*

| BCM5387 MIB | Ethernet-Like MIB RFC 1643 | Bridge MIB RFC 1493 | MIB II Interface RFC 1213/1573 | RMON MIB RFC 1757 |
|---|---|---|---|---|
| RxErrorPkts = RxAlignmentErrors + RxFCSErrors + RxFragments + RxOversizePkts + RxJabbers | – | – | ifInErrors | – |
| | – | – | ifInUnknownProtos | – |
| RxGoodPkts = RxUnicastPkts + RxMulticastPkts + RxBroadcastPkts | – | dot1dTpPortIn Frames | – | — |
| DropEvents = RxDropPkts + TxDropPkts | – | – | – | etherStatsDrop Events |
| RxTotalPkts = RxGoodPkts + RxErrorPkts | – | – | – | etherStatsPkts |
| RxCRCAlignErrors = RxCRCErrors + RxAlignmentErrors | – | – | – | etherStatsCRCAlign Errors |
| | dot3StatsSQETest Errors | – | – | – |
| RxFramesTooLong = RxOversizePkts + RxJabber | dot3StatsFrameToo Longs | – | – | – |

*Table 18: Indirectly Supported MIB Counters (Cont.)*

| *BCM5387 MIB* | *Ethernet-Like MIB RFC 1643* | *Bridge MIB RFC 1493* | *MIB II Interface RFC 1213/1573* | *RMON MIB RFC 1757* |
|---|---|---|---|---|
| TxGoodPkts = TxUnicastPkts + TxMulticastPkts + TxBroadcastPkts | – | dot1dTpPortOut Frames | – | – |
| TxErrorPkts = TxExcessiveCollision + TxLateCollision Note 1 | – | – | ifOutErrors | – |

Note 1: The number of packets transmitted from a port that experienced a late collision or excessive collisions. Though some media types operate in half-duplex mode, frames that experience carrier sense errors are also summed in this counter. The BCM5387 integrated design eliminates this error condition.

*Table 19: BCM5387 Supported MIB Extensions*

| *BCM5387 MIB* | *Appropriate Standards Reference* |
|---|---|
| RxSAChanges | IEEE 802.3u Clause 30—Repeater Port Managed Object Class a SourceAddressChanges. |
| RxExcessSizeDisc | The BCM5387 cannot store packets in excess of 1536 bytes (excluding preamble/SFD, but inclusive of FCS). This counter indicates packets that were discarded by the BCM5387 due to excessive length. |
| RxPausePkts | IEEE 802.3x Clause 30—PAUSE Entity Managed Object Class aPAUSEMACCtrlFramesReceived. |
| RxSymbolErrors | IEEE 802.3u Clause 30—Repeater Port Managed Object Class aSymbolErrorDuringPacket. |
| TxFrameInDisc | Internal diagnostic use for optimization of flow control and buffer allocation algorithm. |
| TxPausePkts | The number of PAUSE events at a given port. |

# Integrated High-Performance Memory

The BCM5387 embeds a 128 KB high-performance SRAM for storing packet data, the ARL table, the VLAN table, the TX queues, and descriptors. This eliminates the need for external memory and allows for the implementation of extremely low-cost systems. The internal RAM controller efficiently executes memory transfers and achieves non-blocking performance for stand-alone 8-port applications.

# Switch Controller

The core of the BCM5387 device is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration, and transmit descriptor queueing.

## Buffer Management

The frame buffer memory is divided into pages (units of data consisting of 256 bytes each). Each received packet may be allocated more than one page. For example, six pages are required to store a 1522-byte frame. Frame data is stored in the buffer memory as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. This list tracks the transmission of the packet. After successful packet transmission, the buffer memory is released to the free buffer pool.

## Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, the VLAN lookup, learning and aging functions, egress descriptor update, and output-port queue managers. These processes are arbitrated to provide fair access to the memory and minimize the latency of critical processes to provide a fully non-blocking solution.

## Transmit Output Port Queues

Frames are maintained in the egress port using a linked list. Two levels of linked lists are used to maintain one output queue (see Figure 8). The first level is the TXQ linked list, and the second level is the Buffer Tag linked list. The TXQ linked list is used to maintain frame-priority order for each port. For each frame, the Buffer Tag linked list is used to maintain the order of the buffer pages corresponding to each frame.

Each egress port supports up to four transmit queues for servicing Quality of Service (QoS). All four transmit queues share the 512 entries of the TXQ table. The TXQ table is maintained as a linked list, and each node in the TXQ uses one entry in the TXQ table. The TXQ size for each priority can be programmed to up to 512 entries.

When the QoS function has been turned off, the switch controller maintains one output queue for each egress port. The TXQ table is maintained in a per-port individual internal memory. Each node in the queue represents a pointer that points to a frame-buffer tag. Each buffer tag includes frame information and a pointer to the next buffer tag. Each buffer tag has an associated page allocated in the frame buffer. For a packet with a frame size larger than 256 bytes, multiple buffer tags are required. For instance, a 9728-byte jumbo frame requires 38 buffer tags for handling the frame.

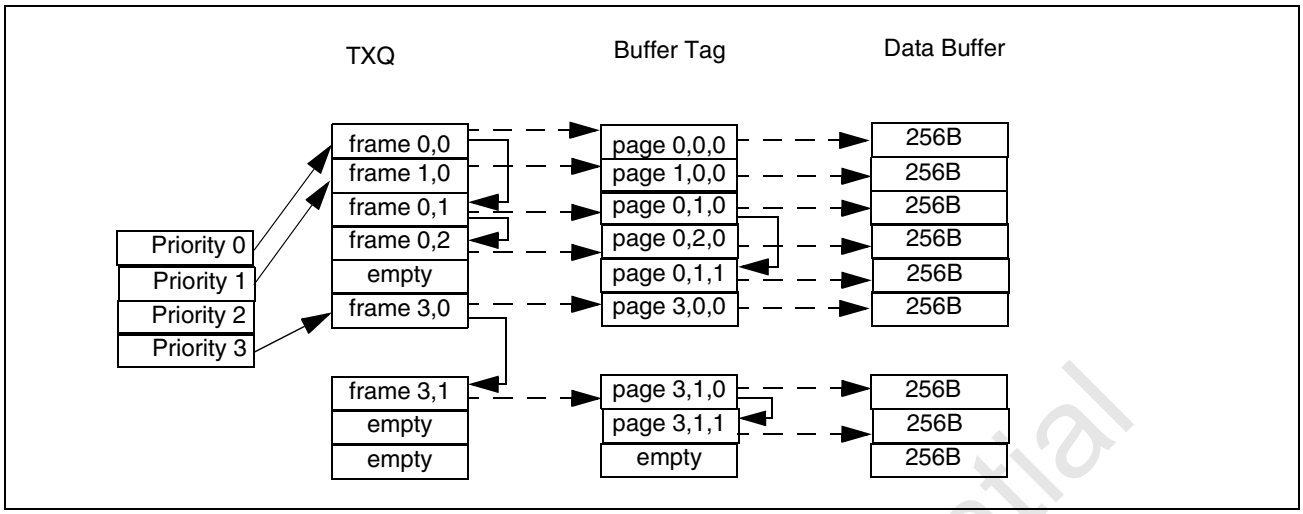


**Figure 8: TXQ and Buffer Tag Structure**

# Section 4: System Interfaces

## Overview

The BCM5387 includes the following interfaces:



Each interface is discussed in detail in the following sections.

## Serial Interface

Each LVDS-compatible serial port can be configured in SGMII or SerDes mode.

### SGMII Mode

The SGMII interface transmits serial data differentially at 1.25 gigabaud via the SGTX± pins and receives serial data differentially via the SGRX± pins. Transmit data timing is recovered from the incoming data signal, and the attached link partner does so, likewise. The SGMII interface pins are shared with the SerDes interface pins.

The data signals operate at 1.25 gigabaud. Each of these signals is realized as a differential pair because of the speed of operation, providing signal integrity while minimizing system noise. The SGMII signals use LVDS voltage levels. Both the data and clock signals are DC-balanced; therefore, implementations that meet the AC parameters, but fail to meet the DC parameters, can be AC-coupled.

The 1.25-gigabaud transfer rate of the SGMII is greater than required for the BCM5387 transceiver operating at 10 Mbps or 100 Mbps. When these situations occur, the BCM5387 elongates the frame by replicating each frame byte 10 times for 100 Mbps and 100 times for 10 Mbps. This frame elongation takes place above the IEEE 802.3z PCS layer, making the start-frame delimiter appear only once per frame.

When the device operates at 10 Mbps or 100 Mbps, the SGMII differential pair replicates the data 100 and 10 times, respectively.

## SerDes Mode

The SerDes interface operates via 1000BASE-X and complies with IEEE 802.3, Clauses 36 and 37. The interface shares differential data pins with the SGMII interface. The BCM5387 SerDes can be used in various applications as listed below.

- The SerDes interface can be connected to SerDes fiber modules creating switched fiber ports.
- The SerDes interface can be connected to a SerDes-to-copper PHY creating switched copper ports.
- The SerDes interface can be connected to a SerDes MAC or switch for a SerDes switch-to-switch application.

The SerDes auto-negotiation is similar to the SGMII, except for the link timer. Table 17 summarizes the differences between the two interfaces.The differential pair runs at 1.25 Gbps. The data is 8b/10b encoded, and the decoded data throughput is 1 Gbps.

## SerDes/SGMII Auto-Negotiation

It is necessary to pass control information to the link partner when establishing link. The link partner receives and decodes the sent control information and also begins auto-negotiation. The link partner acknowledges the update of the link status and visa versa. Upon receiving proper acknowledgement, the BCM5387 completes auto-negotiation and returns to normal data mode. The included control information for SerDes and SGMII is compared in Table 20.

***Table 20: SGMII and SerDes Auto-Negotiation***

| *Mode* | *Link Timer* | *Remote Fault* | *PAUSE Frame* | *Speed Bit* | *Link Status* | *Duplex Bit* |
|---|---|---|---|---|---|---|
| SGMII | 1.6 ms | Not supported | Not supported | Supported | Supported | Supported |
| SerDes | 10 ms | Supported | Supported | Not supported (always 1000BASE-X) | Not supported | Supported |

# Frame Management Port Interface

The dedicated frame management port provides high-speed connection to transfer management packets to an external management agent. For more information about frame management, see “Frame Management Block” on page 45. The port is configurable to Reverse MII (RvMII), GMII, or RGMII via strap pins or software configuration.

**Note:** The RvMII/GMII/RGMII port is used as a IMP (Management) Port only. It is not available for a PHY or network port connection.

## Reverse MII Port (RvMII)

The media independent interface (MII) serves as a digital data interface between the BCM5387 and an external 10/100 Mbps management entity. Reverse MII notation reflects the MII port interfacing to a MAC-based external agent. The RvMII contains all the signals required to transmit and receive data at 100 Mbps and 10 Mbps for both full-duplex and half-duplex operation. See Figure 9 on page 60 for connection information.

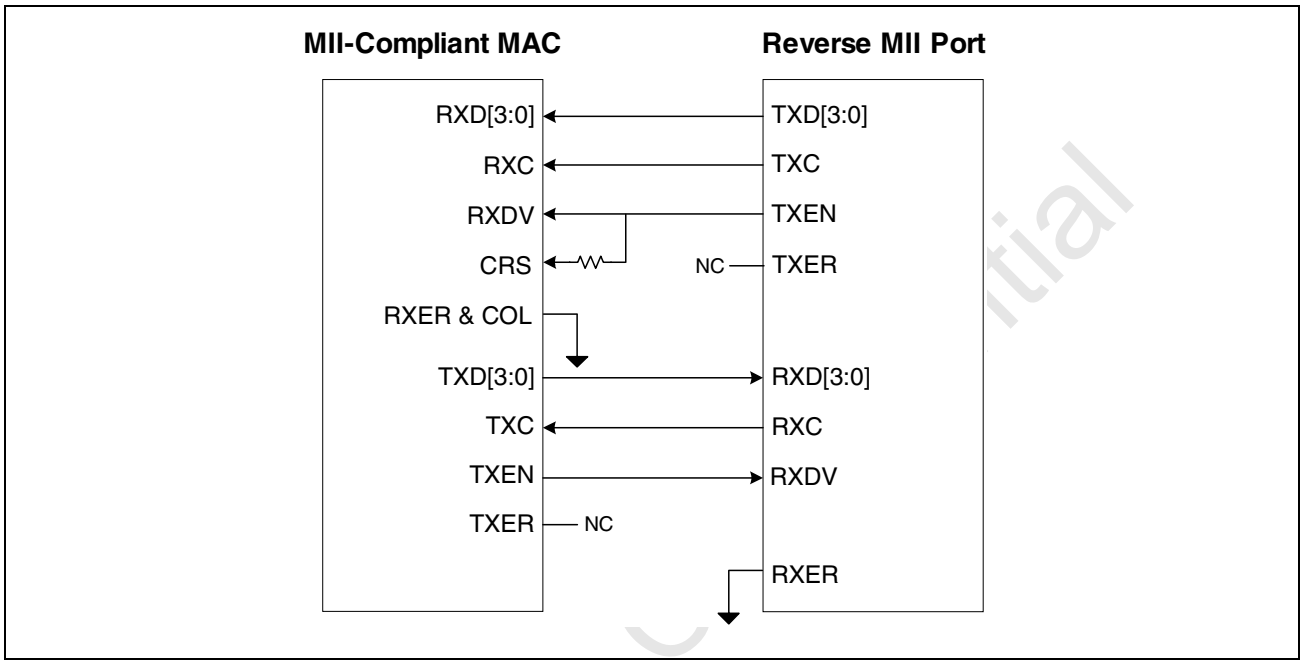


**Figure 9: RvMII Port Connection**

## GMII Port

The Gigabit Media Independent Interface (GMII) serves as a digital data interface between the BCM5387 and an external gigabit management entity. Transmit and receive data is clocked on the rising edge of the clocks. The GMII transmits data synchronously via the TXD[3:0] and RXD[3:0] data signals. The GMII port operates in 1000 Mbps mode only.

## RGMII Port

The Reduced Gigabit Media Independent Interface (RGMII) serves as a digital data interface between the BCM5387 and an external gigabit management entity. Transmit and receive data is clocked on the rising and falling edge of the clocks. This reduces the number of data signals crossing the MAC interface without affecting the data-transmission rate. The RGMII transmits data synchronously via the TXD[3:0] and RXD[3:0] data signals.

# Configuration Pins

Initial configuration of the BCM5387 takes place during power-on/reset by loading internal control values from hardware strap pins. The value of the pin is loaded when the reset sequence completes, and the pin transitions to normal operation. Pull-up or pulldown resistors can be added to these pins to control the device configuration. If the pins are left floating, the default value is determined based on the internal pull-up or pulldown configuration. See "Signal Descriptions" on page 84 for more information.

# Programming Interfaces

The BCM5387 can be programmed via the SPI interface or the EEPROM interface. The interfaces share a common pin set that is configured via the CPU_EPROM_SEL strap pin. The "SPI Interface" on page 61 provides access for a general-purpose microcontroller, allowing read and write access to the internal BCM5387 register space. It is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol. Alternatively, the "EEPROM Interface" on page 67 can be connected to an external EEPROM for writing register values upon power-up initialization.

The internal address space of the BCM5387 device is broken into a number of pages. Each page groups a logical set of registers associated with a specific function (for example, "Page 00h: Control Registers" on page 95, "Page 01h: Status Registers" on page 109, "Page 04h: ARL Control Register" on page 120, etc.). Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is utilized.

All pages have reserved registers from addresses F0h–FFh, and all pages behave identically over this space, as shown in the "Global Registers" on page 185. Address FFh is the "Page Register (Global, Address 0FFh)" on page 186 and is accessible from any page. Writing a new binary value to these bits changes the currently accessible page. Address FEh is the "SPI Status Register (Global, Address 0FEh)" on page 185, and addresses F0h–F7h are the "SPI Data I/O Register (Global, Address 0F0h)" on page 185. These registers are used for writing and reading data to the register space.

An explanation follows for using the serial interface with an SPI-compatible CPU ("SPI Interface" on page 61) or an EEPROM ("EEPROM Interface" on page 67). Either mode can be selected with the strap pin, CPU_EPROM_SEL. Either mode has access to the same register space.

## SPI Interface

The BCM5387 can be controlled over a serial interface that is compatible with a subset of the Motorola Synchronous Serial Peripheral Interconnect (SPI) bus. The microcontroller interface consists of four signals: serial clock (SCK), slave select (SS/CS), master-in/slave-out (MISO/DO), and master-out/slave-in (MOSI/DI). The BCM5387 always operates as an SPI slave device, in that it never initiates a transfer on the SPI and only responds to the read and write requests issued from a master device.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM5387. This protocol establishes the definition of the first 2 bytes issued by the master to the BCM5387 slave during an SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

The SPI mode supports two different access mechanisms: normal SPI and fast SPI: The SPI mode is determined by the content of the command byte. Figure 10 shows the normal SPI command byte, and Figure 11 shows the fast SPI command byte. These two mechanisms should not be mixed in an implementation; the CPU should always initiate transfers consistently with only one of the two mechanisms.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | MODE = 0 | CHIP ID 2 (MSB) | CHIP ID 1 | CHIP ID 0 (LSB) | Read/Write (0/1) |

**Figure 10: Normal SPI Command Byte**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Byte Offset (MSB) | Byte Offset | Byte Offset (LSB) | MODE = 1 | CHIP ID 2 (MSB) | CHIP ID 1 | CHIP ID 0 (LSB) | Read/Write (0/1) |

**Figure 11: Fast SPI Command Byte**

The MODE bit (bit 4) of the command byte determines the meaning of bits[7:5]. If bit 4 is a 0, it is a normal SPI command byte, and bits[7:5] should be defined as 011b. If bit 4 is a 1, bits[7:5] indicate a fast SPI command byte, and bits[7:5] indicate the byte offset into the register that the BCM5387 starts to read from (byte offsets are not supported for write operations).

In both command bytes, bits[3:1] indicate the chip ID to be accessed. Because the BCM5387 operates as a single-chip system, the CHIP ID is 000. Note that the $\overline{SS}$ signal must also be active for any BCM5387 device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = read, 1 = write) and determines the transmission direction of the data.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page, which is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/received, allowing a contiguous block of data from a register to be stored/read in a single transmission. When the fast SPI command byte mode is used, the actual start location of a read operation can be modified by the offset contained in bits[7:5] of the command byte. Reading/writing data from/to separate registers, even if those registers are contiguous in the current page, must be performed by supplying a new command byte and register address for each register, with the address as defined in the appropriate page register map.

Non-contiguous blocks are also stored/read through the use of multiple transmissions, which allow a new command byte and register base address to be specified. The $\overline{SS}$ signal must remain low for the entire read or write transaction, as shown in Figure 12 and Figure 13, with the transaction terminated by the deassertion of the $\overline{SS}$ line by the master.

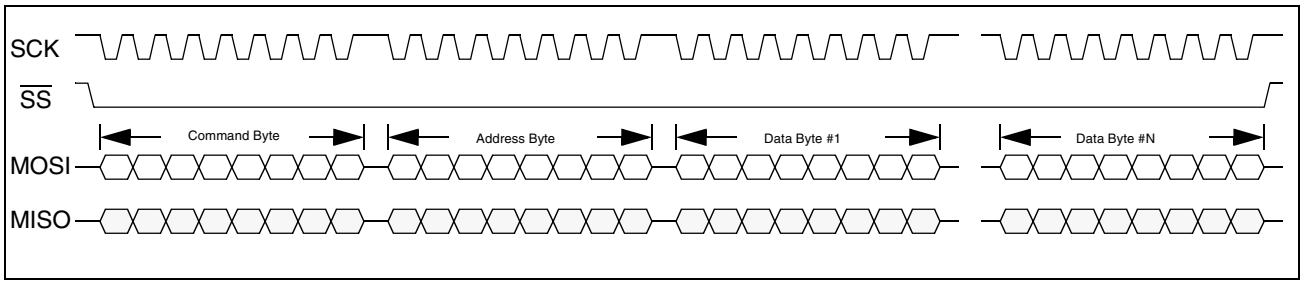


**Figure 12: SPI Serial Interface Write Operation**

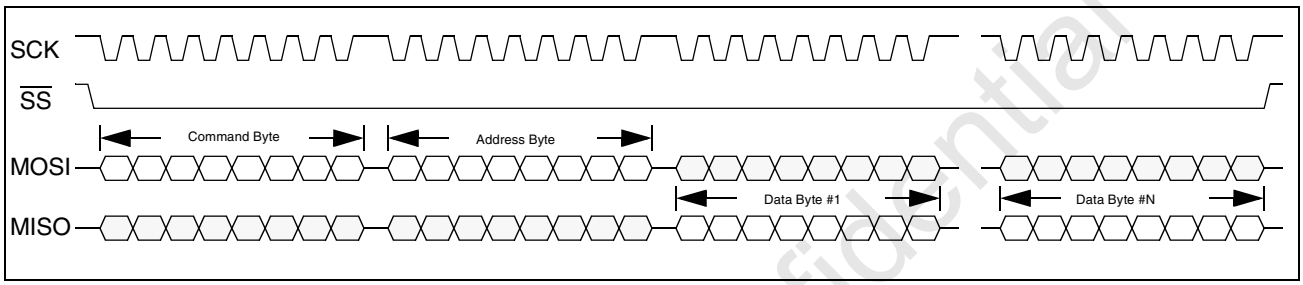


**Figure 13: SPI Serial Interface Read Operation**

The serial interface supports operation up to 2 MHz in SPI mode. A maximum of four devices can be cascaded/addressed.

## Normal SPI Mode

Normal SPI mode allows single-byte read and multibyte string write operations, with the CPU polling to monitor progress. Read operations are performed using the"SPI Status Register (Global, Address 0FEh)" on page 185 and "SPI Data I/O Register (Global, Address 0F0h)" on page 185. All read operations take the form:

<CMD, CHIP ID, R><REG ADDR>

The first byte is the command byte with the appropriate CHIP ID and Read bits set, and the second byte is the register address.

All write operations are of the form:
<CMD, CHIP ID, W><REG ADDR><DATA0>...<DATAn>

The first byte is the command byte with the appropriate CHIP ID and Write bits set, the second byte is the register address, and the remaining bytes are the exact number of data bytes appropriate for the selected register. Failure to provide the correct number of data bytes means the register write operation does not occur.

A simple flow chart for the read process is shown in Figure 14 on page 65.

To read a register, first the "Page Register (Global, Address 0FFh)" on page 186 is written (<CMD, CHIP ID, W><REG ADDR = FFh><DATA = NEW PAGE>). It is only necessary to write the page register when moving to a new page. Once in the correct page, a read operation is performed on the appropriate register (<CMD, CHIP ID, R><REG ADDR>). Once the "SPI Status Register (Global, Address 0FEh)" on page 185 indicates that the data is available (RACK = 1), the data can be read. Data is read from the "SPI Data I/O Register (Global, Address 0F0h)" on page 185, located at F0h–F7h on every page (so no page swap is necessary to read the data on any page). A read operation can access any or all of the bytes on a specific register, including the ability to start at any offset.

> ***Example:*** Reading [0] from "SPI Data I/O Register (Global, Address 0F0h)" on page 185 reads the least significant byte of the register, and successive reads to [0] "SPI Data I/O Register (Global, Address 0F0h)" on page 185 read the remaining bytes. However, reading the first byte from [2] "SPI Data I/O Register (Global, Address 0F0h)" on page 185 reads the third byte of the register, and successive reads to [2] "SPI Data I/O Register (Global, Address 0F0h)" on page 185 read the remaining bytes of the register up to the most significant byte of the register. It is not necessary to read all bytes of a registers, only the bytes of interest. The SPI master can then move on to perform another read or write operation.

A flow chart for the write process is shown in Figure 15 on page 66. To write a register, the "Page Register (Global, Address 0FFh)" on page 186 is written, if necessary (<CMD, CHIP ID, W><REG ADDR = FFh><DATA = NEW PAGE>), then data is written to the selected register (<CMD, CHIP ID, W><REG ADDR><DATA0>...<DATAn>), where DATA0 is the least significant byte of the register, and DATAn is the most significant byte of the register, and the exact number of bytes is present as defined by the register width. No byte offset is provided for write operations, and all bytes must be present to activate the write process internal to the BCM5387.

The following simple rules apply to the normal SPI mode:

- A write to the page register at any time causes the SPI state machine to reset.
- A read operation can access any number of bytes at any offset using "SPI Data I/O Register (Global, Address 0F0h)" on page 185.
- A write operation must write the exact number of bytes to the register being accessed.
- The RXRDY/TXRDY flags in "SPI Status Register (Global, Address 0FEh)" on page 185 must be checked after each 8-byte string has been read/written to ensure the next string is ready and can be accepted (since the largest internal register is 8 bytes, this restriction only applies to reading and writing frames via the SPI).

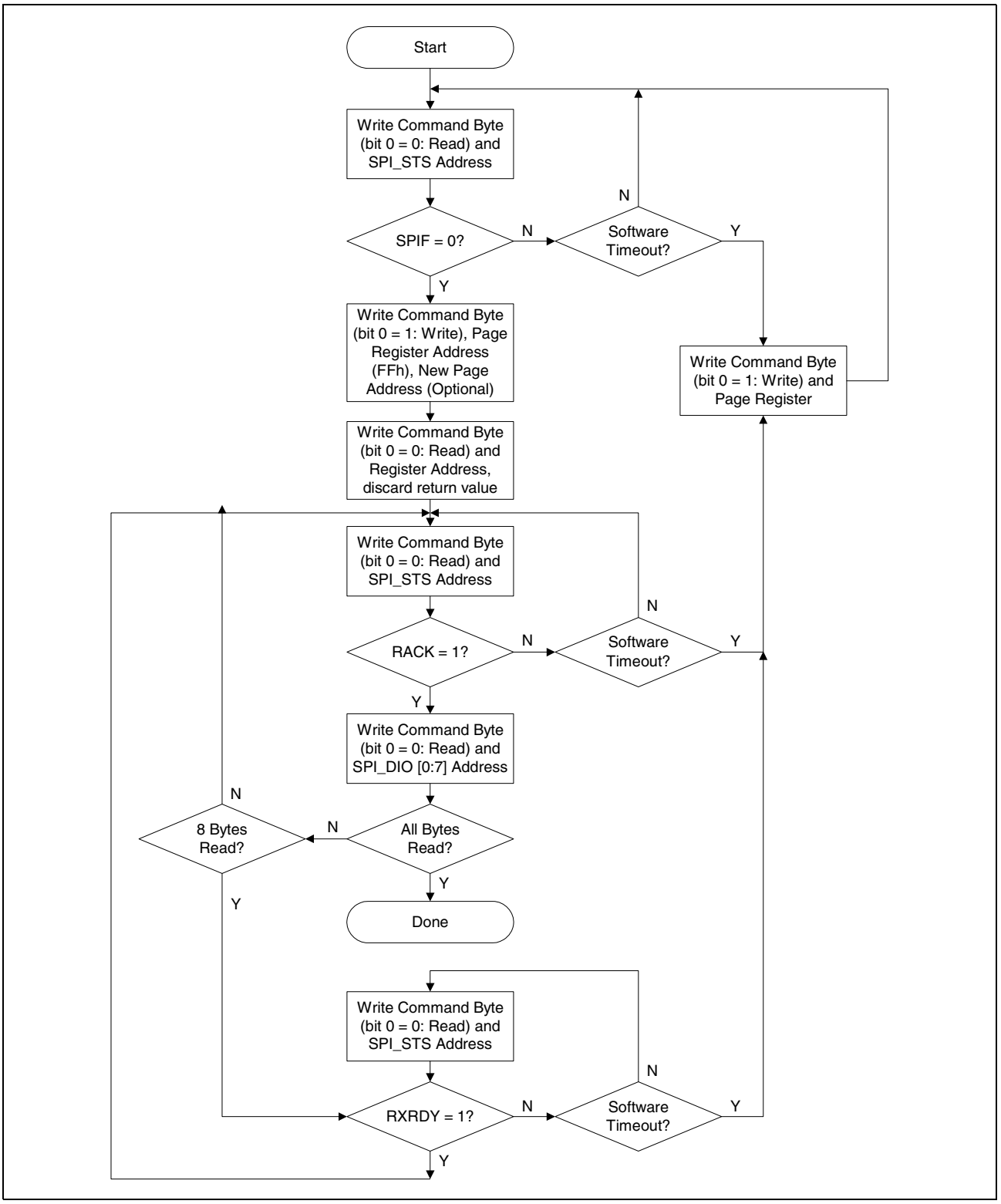


**Figure 14: Normal SPI Mode Read Flow Chart**

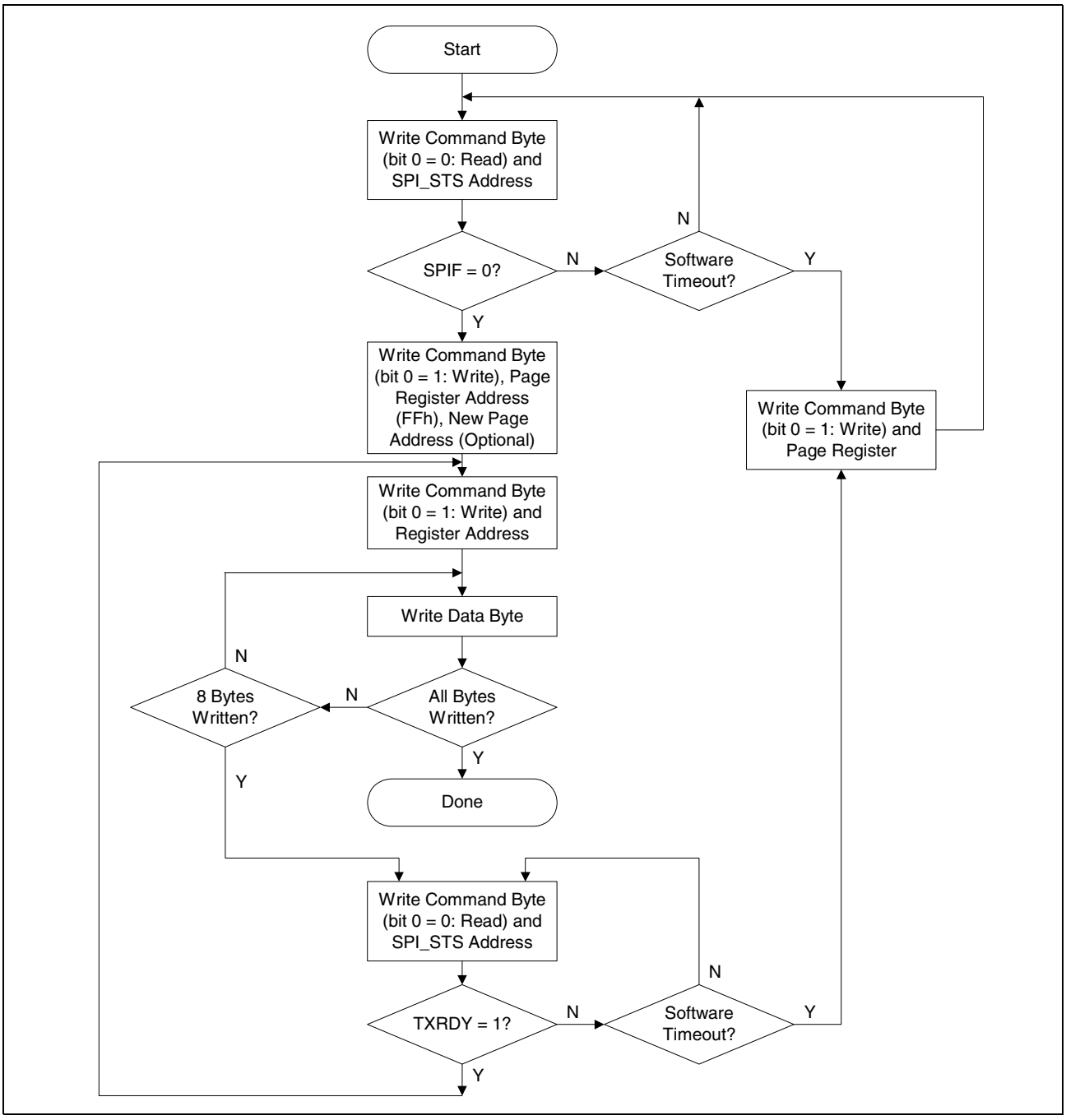


**Figure 15: Normal SPI Mode Write Flow Chart**

## Fast SPI Mode

Fast SPI mode makes use of the fact that the SPI port is inherently full-duplex and provides an explicit acknowledge on read cycles to eliminate the polling of the SPI_STS register for RACK polling. Fast SPI mode requires the MODE bit in the command byte to be set as indicated in Figure 11 on page 62. Like normal SPI mode, fast SPI mode also supports byte offsets for read operations.

Read operations do not access the "SPI Data I/O Register (Global, Address 0F0h)" on page 185 registers. Instead, status and data are output on the MISO line by the BCM5387. Once the page register and the register within that page have been set, the master reads the MISO line state. The BCM5387 immediately puts out a byte string that indicates the state of the RACK bit in bit 0. Once bit 0 is sampled high, the next byte is the least significant byte of the read data, and successive bytes follow. Byte offset of the register is provided by using bits[7:5] of the command byte to index from byte 0 (000) to byte 7 (111) as the first byte to be presented on MISO.

For example, if command byte [7:0] = 011_1_001_0, that indicates a read offset of 3 (4th byte) in the register to be accessed (register 6 in this example). The RACK status bit is provided on the MISO line (00000001) when the read data (dddddddd) is to follow on the MISO line. An example of the timing is shown below.

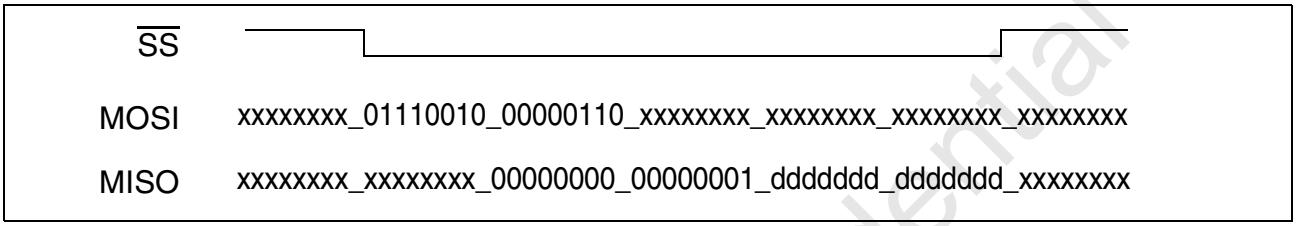


**Figure 16: Timing Example**

Write operations are identical in both fast and normal SPI modes.

## EEPROM Interface

The BCM5387 can be connected via the serial interface to a low-cost external serial EEPROM, enabling it to download register-programming instructions during power-on initialization. For each programming instruction fetched from the EEPROM, the instruction executes immediately and affects the register file.

During the chip-initialization phase, the data is sequentially read-in from the EEPROM after the internal memory has been cleared. The first data read-in is the HEADER and it matches a predefined magic code. In the case where the HEADER data does not match the instruction fetch, the process stops, and the EEPROM controller treats it as if no EEPROM exists. If the magic code matches, the fetch instruction process continues until it reaches the instruction length defined in the HEADER.

Due to the different access cycles of different capacity EEPROMs, the strap pins "EEPROM_TYPE[1:0]" are used to support the various EEPROM devices according to Table 21.

***Table 21: EEPROM_TYPE[1:0] Settings***

| *EEPROM_TYPE[1:0]* | *EEPROM* |
|---|---|
| 00 | 93C46 |
| 01 | 93C56 |
| 10 | 93C66 |
| 11 | 93C86 |

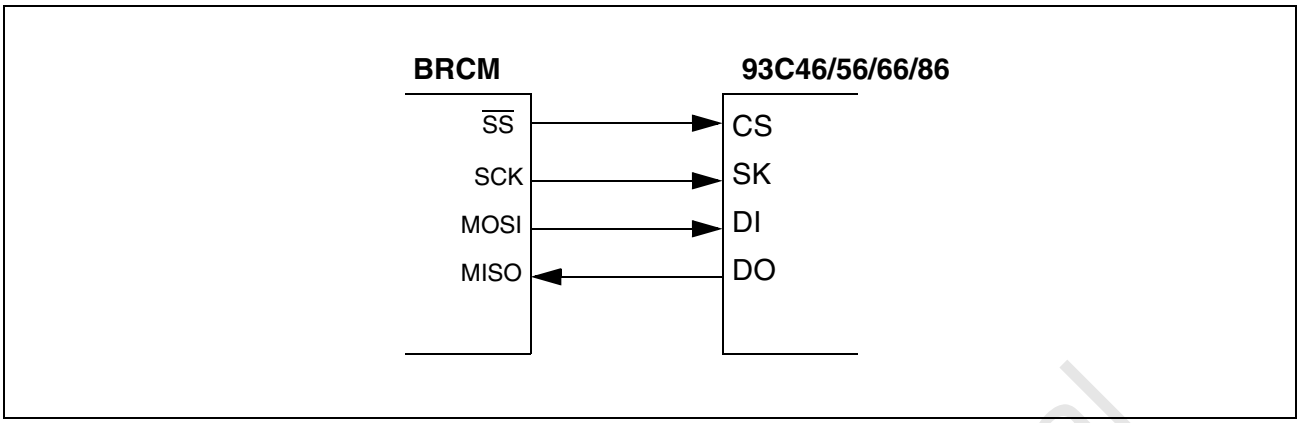


**Figure 17: Serial EEPROM Connection**

## EEPROM Format

The EEPROM should be configured to x16 word format. The first entry is the header. The header contains the magic code key and length information as shown in Table 22. The actual data stored in the EEPROM is byte-swapped as shown in Table 23.

- Upper 5 bits are magic code (10101), which indicates that valid data follows.
- Bit 10 is for speed indication. This bit shall always be 0.
- Lower 10 bits indicate the total number of entries. For example:
  - 93C46 up to 64 words
  - 93C56 up to 128 words
  - 93C66 up to 256 words
  - 93C86 up to 1024 words

***Table 22: EEPROM Header Format***

| *Bits[15:11}* | *Bit 10* | *Bits[9:0]* |
|---|---|---|
| Magic code: 10101 | Speed:0 | Total entry number<br>93C46: 0 ~ 63<br>93C56: 0 ~ 127<br>93C66: 0 ~ 255<br>93C86: 0 ~ 1023 |

**Note:** Data is stored in the EEPROM in byte-swapped format. Bits[7:0] are followed by Bits[15:8].

After chip initialization, the header is read from the EEPROM and is used to compare to the predefined magic code. When the fetched data does not match the predefined magic code, the EEPROM-instruction fetch process is stopped. If the magic code is matched, fetching instructions continue for the number of cycles defined in the header.

The 16-bit entries following the header are constructed in commands as shown in Table 23. The first entry of the command specifies an address and data entry number. The address specifies the address offset location within the page. The data entry number indicates the length of data that is to be written. Specifically, it is the number of proceeding EEPROM entries that are to be written. In the example in Table 23, the first command changes the current register page to Page 02h. The second EEPROM command, writes to Address Offset 06h to increase the ageing timer. The second command writes 4-bytes, so the first entry of the command is followed by two data entries (16-bits each).

***Table 23: Example EEPROM Contents***

| ***Bits[15:8]*** | ***Bits[7:0]*** |
|---|---|
| EEPROM Header Entry | |
| Address (FFh) | Data Entry Number (01h) |
| Data (00h) | Data (02h) |
| Address (06h) | Data Entry Number (02h) |
| Data (00h) | Data (10h) |
| Data (0Fh) | Data (FFh) |

The EEPROM port shares pins with the SPI port. Either the SPI port or the EEPROM can be selected by using the strap pin, CPU_EEPROM_SEL. The register space for the EEPROM port is the same as for the SPI port.

# MDC/MDIO Interface

The BCM5387 has an MDC/MDIO interface to read/write register information. The interface operates in two modes: Master or Pseudo-PHY

## MDC/MDIO Interface Register Programming

The BCM5387 is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MDC pin of the BCM5387 sources a 2.5-MHz clock. Serial bidirectional data transmitted via the MDIO pin is synchronized with the MDC clock. Each MII read or write instruction is initiated by the BCM5387 and contains the following:

- **Preamble (PRE)**. To signal the beginning of an MII instruction after reset, at least 32 consecutive 1-bits must be written to the MDIO pin. A preamble of 32 1-bits is required only for the first read or write following reset. A preamble of fewer than 32 1-bits causes the remainder of the instruction to be ignored.
- **Start of Frame (ST).** A 01 pattern indicates that the start of the instruction follows.
- **Operation Code (OP)**. A read instruction is indicated by 10, while a write instruction is indicated by 01.
- **PHY Address (PHYAD)**. A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
- **Register Address (REGAD)**. A 5-bit register address follows, with the MSB transmitted first.
- **Turnaround (TA).** The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent by the BCM5387 chip during

these two bit times. When a read operation is being performed, the MDIO pin of the BCM5387 must be put in a high-impedance state during these bit times. The external PHY drives the MDIO pin to 0 during the second bit time.

- **Data.** The last 16 bits of the Instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first by the BCM5387. During a read operation, the data bits are driven by the external PHY with the MSB transmitted first.

# Master Mode

External PHYs can be connected to the MDC and MDIO pins of the BCM5387. The BCM5387 can automatically poll the register set of the external PHY if the AUTO_POLL pin is pulled low during power-on/reset. These values automatically update to"Page 080-087h: External PHY Registers (Serial Ports)" on page 183. Register values of the external PHY can be written to "Page 080-087h: External PHY Registers (Serial Ports)" on page 183 via the "Programming Interfaces" on page 61. They in turn, are updated to the external PHY via MDC/MDIO during the following auto-poll read/write.

Each serial port of the BCM5387 is assigned a unique PHY address. Each port has a default PHY address matching the port number. The default can be modified via the "MDIO/MDC Port Address Register (Page 00h: Address 070h)" on page 107. Each external PHY checks that the PHY address of the initiated command matches that of its own before executing the command.

# Slave Mode

An external entity such as a CPU or Microprocessor can read and write to the internal registers of the BCM5387 via the MDC/MDIO. Internal registers corresponding to an imbedded Serdes transceiver are addressed individually by the corresponding PHY address. Serdes ports have a PHY Address corresponding to the port number. When using the MDC/MDIO bus in slave mode, use caution that external PHYs connected to the same MDIO/MDC bus are not configured to the internally assigned PHY addresses. This will cause contention across the MDC/MDIO bus, when two devices seek to respond to the same command.

All other register accesses internal to the switch, proceed via Pseudo-PHY access.

## Pseudo-PHY

The MDC/MDIO can be used by an external management entity to read/write register values internal to the BCM5387. This mode offers an alternative programming interface to the chip. The BCM5387 operates in MDC/MDIO slave mode with a PHY address of 30d. The AUTO_POLL pin shall be set high to disable PHY polling. The CPU_EPROM_SEL pin shall be latched high to activate the SPI interface of the device. EEPROM mode is incompatible with the Pseudo-PHY mode. The figures below show the register setup flow chart for accessing the registers via the MDC/MDIO interface.

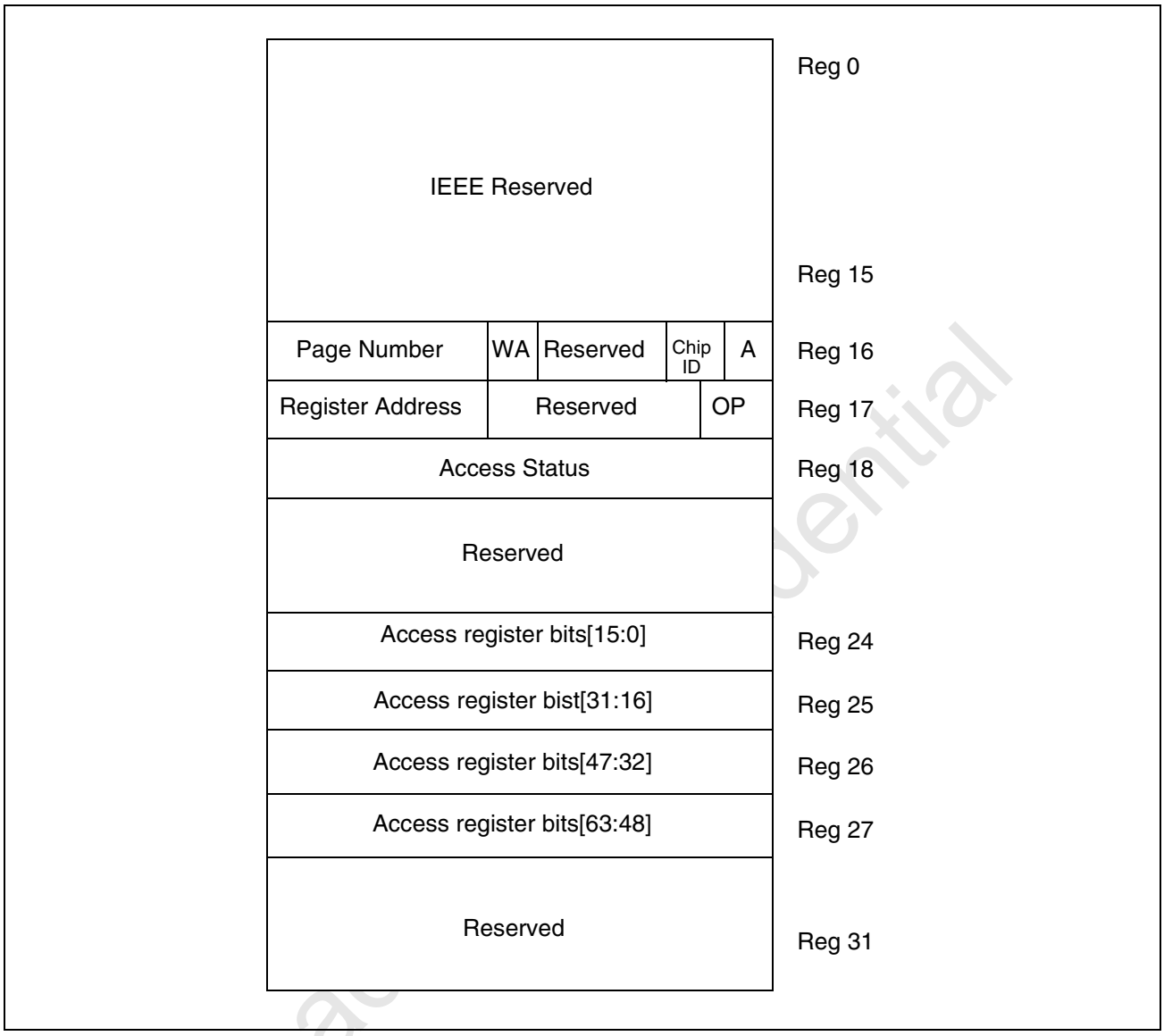


**Figure 18: Pseudo-PHY MII Register Definitions**

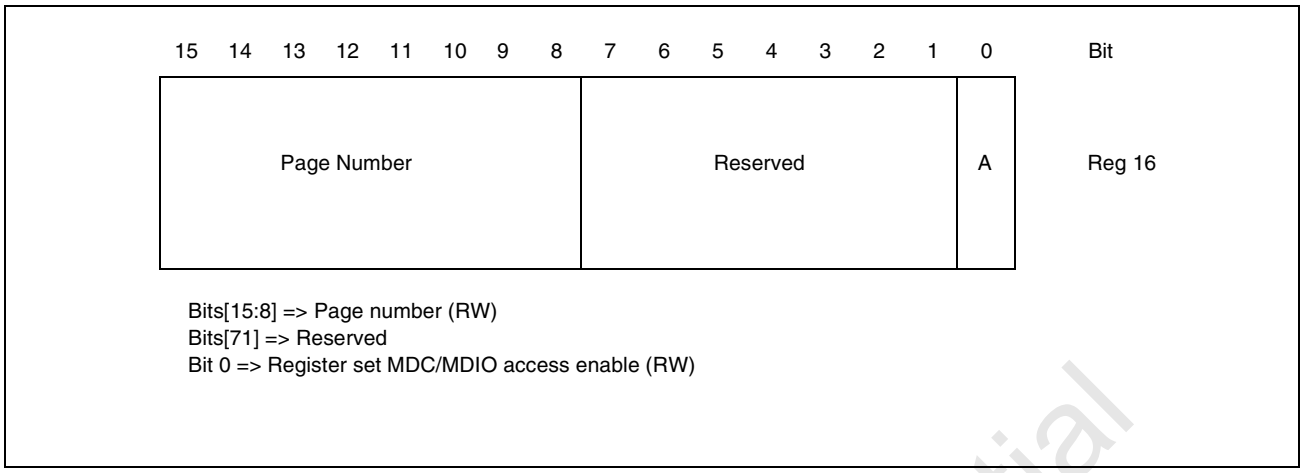


**Figure 19: Pseudo-PHY MII Register 16: Register Set Access Control Bit Definition**

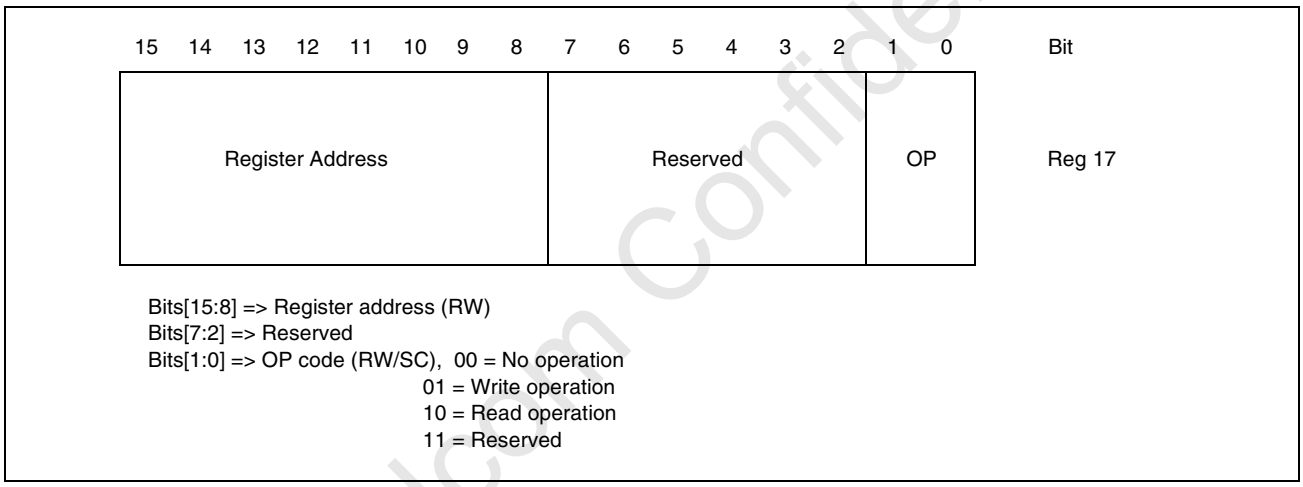


**Figure 20: Pseudo-PHY MII Register 17: Register Set Read/Write Control Bit Definition**

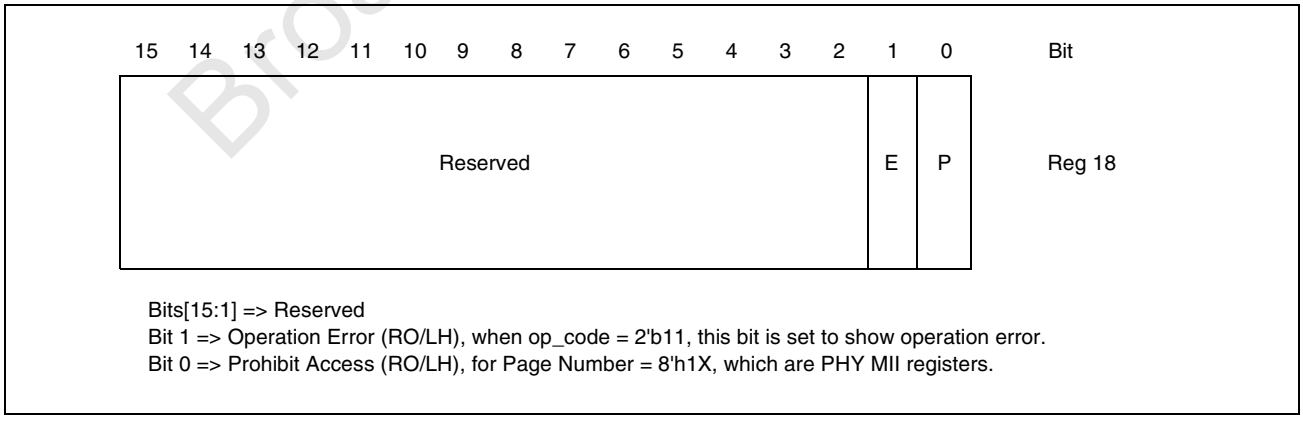


**Figure 21: Pseudo-PHY MII Register 18: Register Access Status Bit Definition**

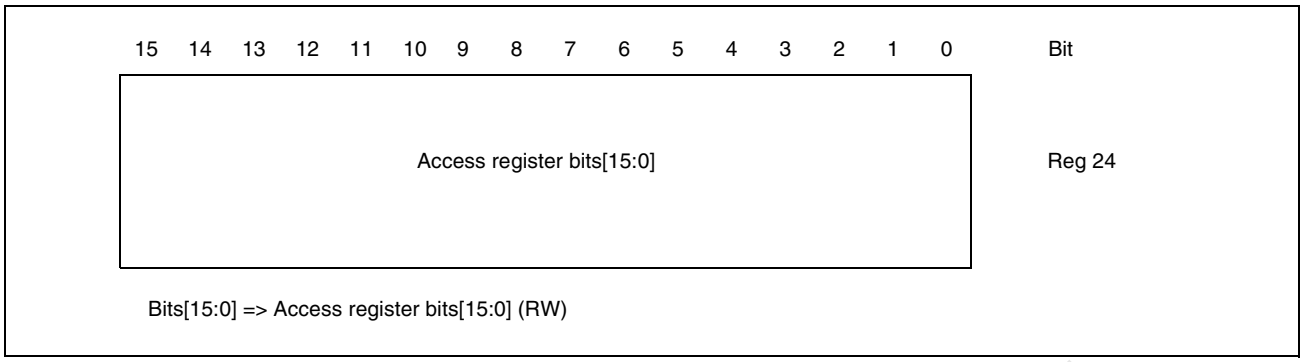


**Figure 22: Pseudo-PHY MII Register 24: Access Register Bit Definition**

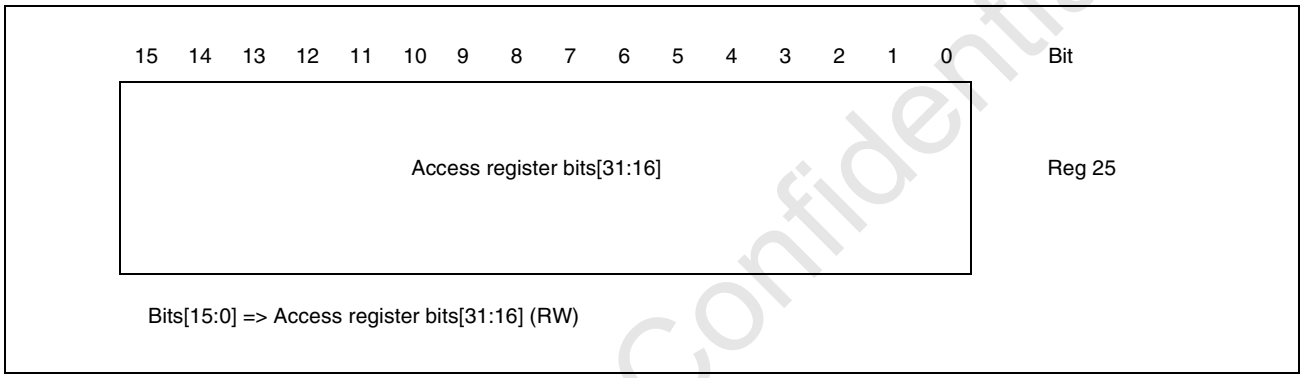


**Figure 23: Pseudo-PHY MII Register 25: Access Register Bit Definition**

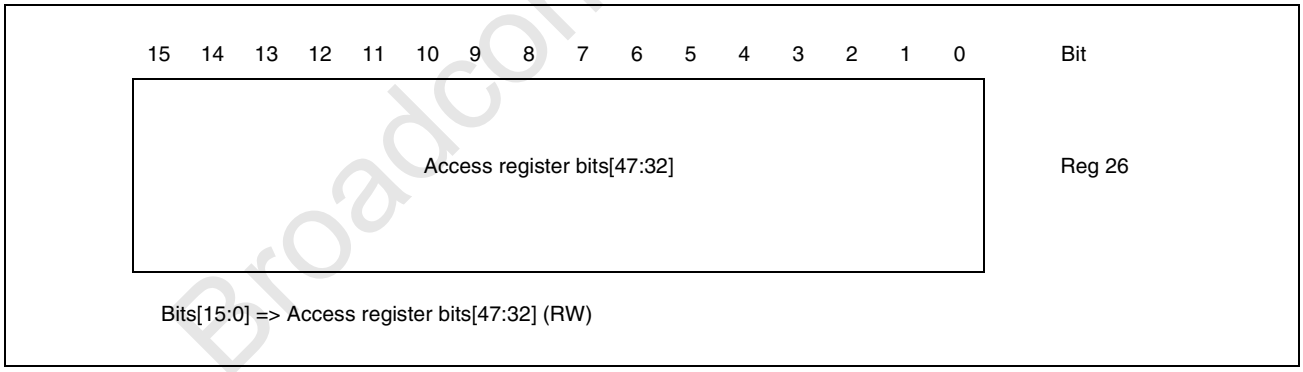


**Figure 24: Pseudo-PHY MII Register 26: Access Register Bit Definition**

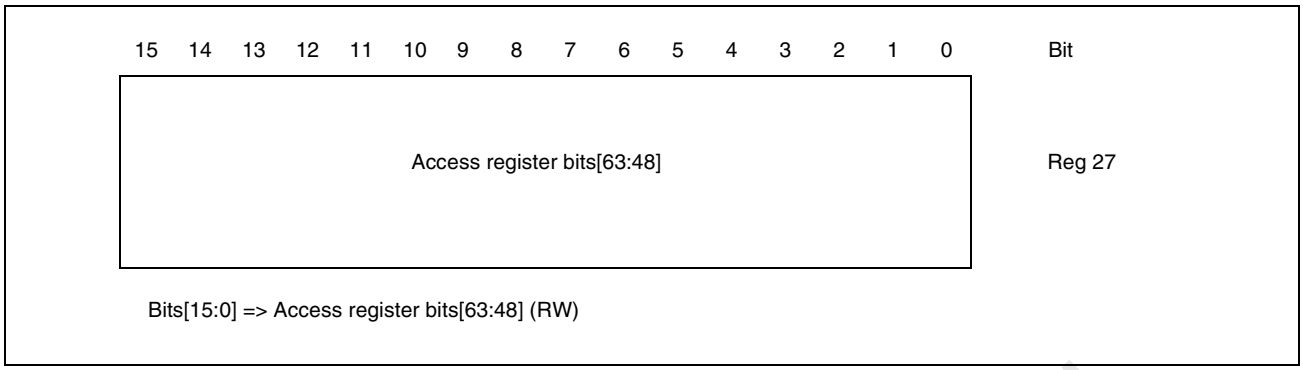


**Figure 25: Pseudo-PHY MII Register 27: Access Register Bit Definition**

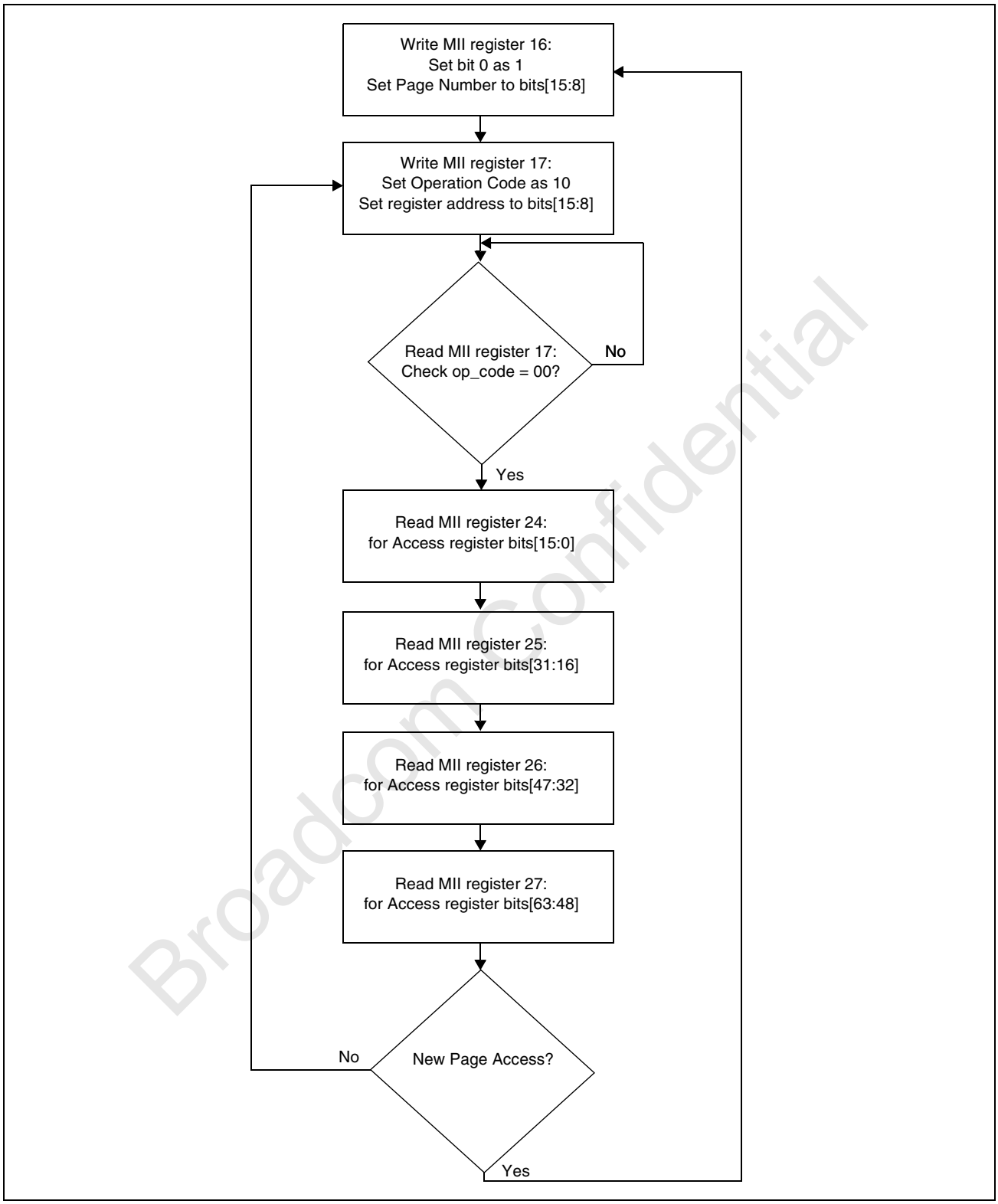




**Figure 26: Read Access to the Register Set via the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path**

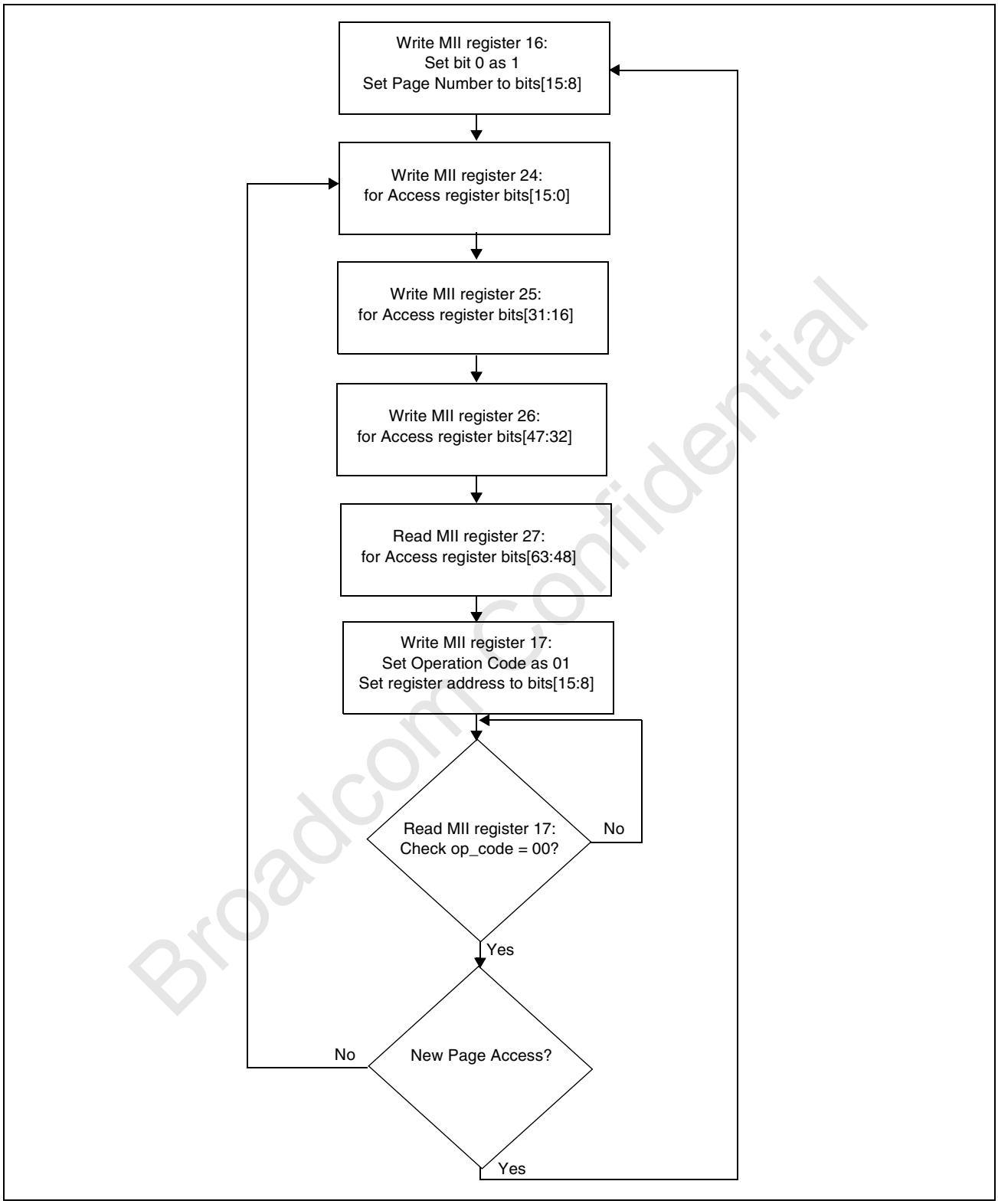




**Figure 27: Write Access to the Register Set via the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path**

Table 24 summarizes the complete management frame format.

***Table 24: MII Management Frame Format***

| *Operation* | *PRE* | *ST* | *OP* | *PHYAD* | *REGAD* | *TA* | *Data* | *Direction* |
|---|---|---|---|---|---|---|---|---|
| Read | 1 ... 1 | 01 | 10 | AAAAA | RRRRR | ZZ<br>Z0 | Z ... Z<br>D ... D | Driven by master<br>Driven by slave |
| Write | 1 ... 1 | 01 | 01 | AAAAA | RRRRR | 10 | D ... D | Driven to master |

See "MDC/MDIO Interface" on page 69 for more information regarding the timing requirements.

# LED Interfaces

The BCM5387 provides visibility per-port of link status, port speed, duplex mode, combined transmit and receive activity, and collision. Both a "Parallel LED Interface" on page 77 and "Serial LED Interface" on page 79 are supplied to drive the status to the LEDs. The parallel interface provides the lowest-cost solution for implementing LEDs. If multiple LED signals cause congestion, the serial mode is more appropriate. Combinations of serial and parallel status can also be effective. Additionally, the "LED Control Register (Page 00h: Address 012h)" on page 99 allows the parallel LEDs to be individually configured to on, off, and blinking states.

During power-on and reset, the parallel LED signals are driven low, and the serial interface shifts a continuous low value for 1.34s.

## Parallel LED Interface

Four pins per-port are provided for directly driving LED status: LEDA-LEDD. The LEDMODE[2:0] configuration signals control the LED mode type driven by each pin. Table 25 on page 77 describes the selectable mode types, and Table 26 on page 78 gives a complete LED mode matrix for the parallel LED interface.

***Table 25: Parallel LED Mode Matrix***

| *Input Control Pin LEDMODE[2:0]* | *LED Outputs LEDA* | *LED Outputs LEDB* | *LED Outputs LEDC* | *LED Outputs LEDD* |
|---|---|---|---|---|
| 000 | LNK/ACT | DUPLEX | SPEED100 | SPEED1000 |
| 001 | LNK/ACT/SPD | DUPLEX | SPEED100 | SPEED1000 |
| 010 | LNK | ACT | SPEED100 | SPEED1000 |
| 011 | LNKG/ACTF | LNKF/ACTG | DPX/COL | SPEED1000 |
| 100 | LNK/ACT | DUPLEX | SPEED100 | SPEED1000 |
| 101 | LNK/ACT/SPD | DUPLEX | COL | SPEED1000 |
| 110 | LNK | ACT | SPEED100 | SPEED1000 |
| 111 | LNK/ACT | DPX/COL | SPEED100 | SPEED1000 |

*Table 26: Parallel LED Mode Types*

| *Name* | *Description* |
|---|---|
| LNK | Link indicator. Low when link is established. High when link is off. |
| LNK/ACT | Link and activity indicator. Low when link is established. Blinking at 12 Hz when link is up and port is transmitting and receiving. |
| LNK/ACT/SPD | Link, activity, and speed indicator. Low when link is up. Blinking at 3 Hz when port has activity (TX or RX) in 10 Mb mode. Blinking at 6 Hz when there is activity at 100 Mb mode, and blinking at 12 Hz when activity is in 1000 Mb mode. |
| LNKG/ACTF | 1G link, 10/100 activity indicator. Low when 1000 Mb link is up. Blinking at 12 Hz when there is activity in 10 Mb/100 Mb mode. High in all other cases. See Figure 28 on page 78 for more information. |
| LNKF/ACTG | 10/100 link, 1G activity indicator. Low when 10 Mb/100 Mb link is up. Blinking at 12 Hz when there is activity in 1000 Mb mode. High in all other cases. See Figure 28 on page 78 for more information. |
| DUPLEX | Duplex mode indicator. High for half-duplex or no link and low for full-duplex and link. |
| DPX/COL | Duplex and collision indicator. Blinking when collision is detected. Low for full-duplex and link. |
| ACT | Activity indicator. Low for 42 ms when transmit or receive activity is detected during previous 42 ms interval. High during no activity or no link. |
| COLSN | Collision indicator. Low for 42 ms when collision is detected during the previous 42 ms interval. High in the absence of collisions or no link. |
| SPEED100 | 100 Mbps speed indicator. Low for 100 Mbps link; otherwise, high. |
| SPEED1000 | 1000 Mbps speed indicator. Low for link at 1000 Mbps, high for all other conditions. |

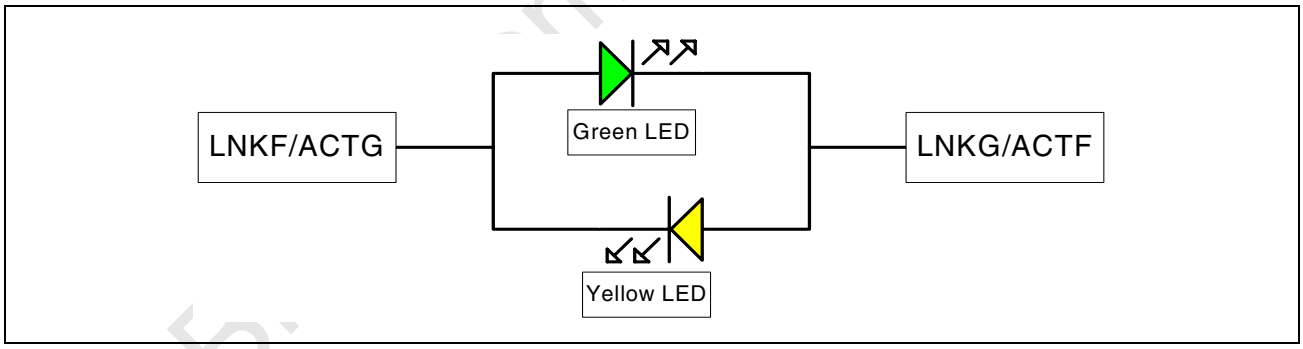


**Figure 28: Bicolor Link/Act LED Scheme**

# Serial LED Interface

A two-pin serial interface, LEDDATA and LEDCLK, provides data and clock to enable external shift registers to capture the LED status indications from the BCM5387 for each port. The status encapsulated within the shift sequence is configured by the LEDMODE[2:0] configuration signals. The configuration signals select both the number of status bits per port and the status type of each bit.

The LEDCLK is generated by dividing the 25-MHz input clock by 16, providing a 640-ns clock period. The LEDDATA outputs are generated on the falling edge of the LEDCLK and have adequate setup and hold time to be clocked externally on the rising edge of LEDCLK.

The first two bits in the sequence are RESVD and $\overline{\text{LEDERR}}$. Next follows an 8-bit Load Status word. The following shift sequence is sequential per port status words. Each port status word contains up to 5-bits for the designated status. Port 0 status word is shifted out first, followed by Port 1 and then the remaining serial ports. The shift sequence is repeated every 42 ms.

Refer to Figure 29 for an illustration of the serial LED shift sequence, Figure 30 on page 80 for an example circuit, Table 28 on page 81 for LED status type, and Table 27 on page 81 for LED mode matrix.

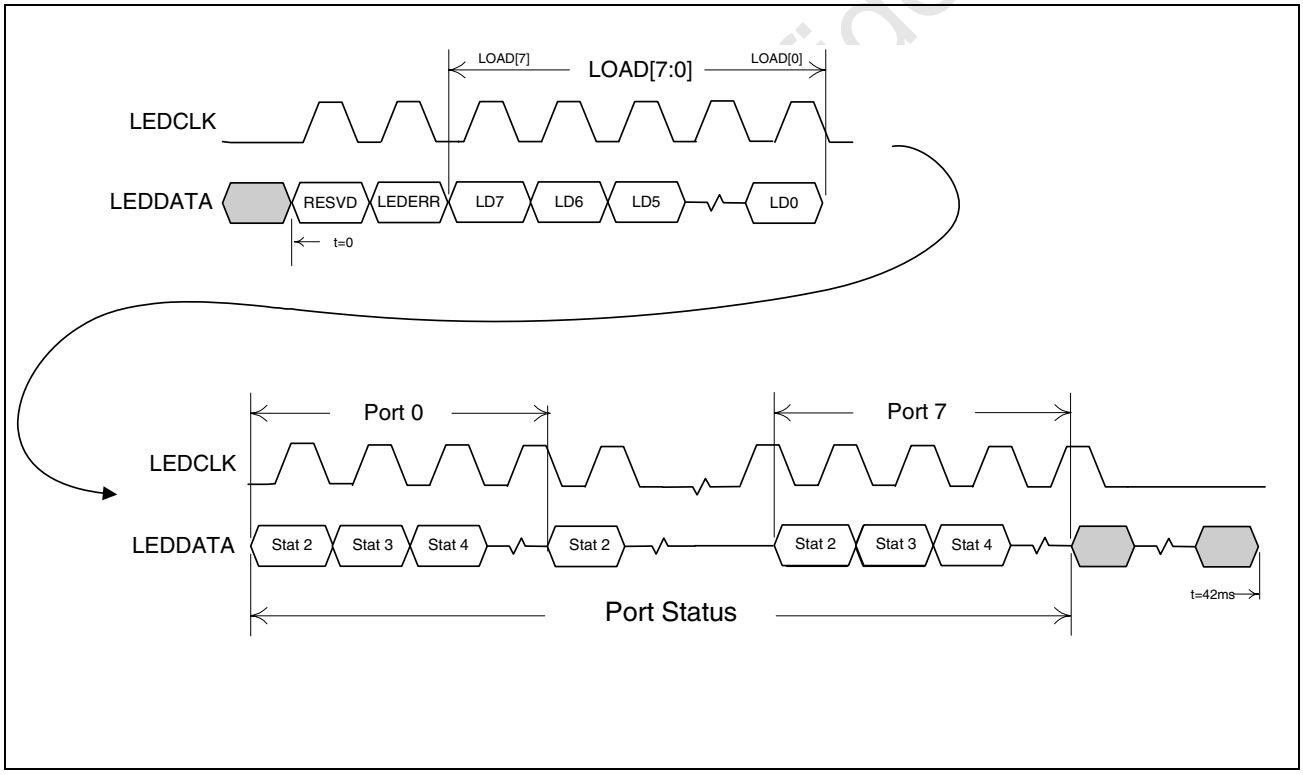


**Figure 29: Serial LED Shift Sequence**

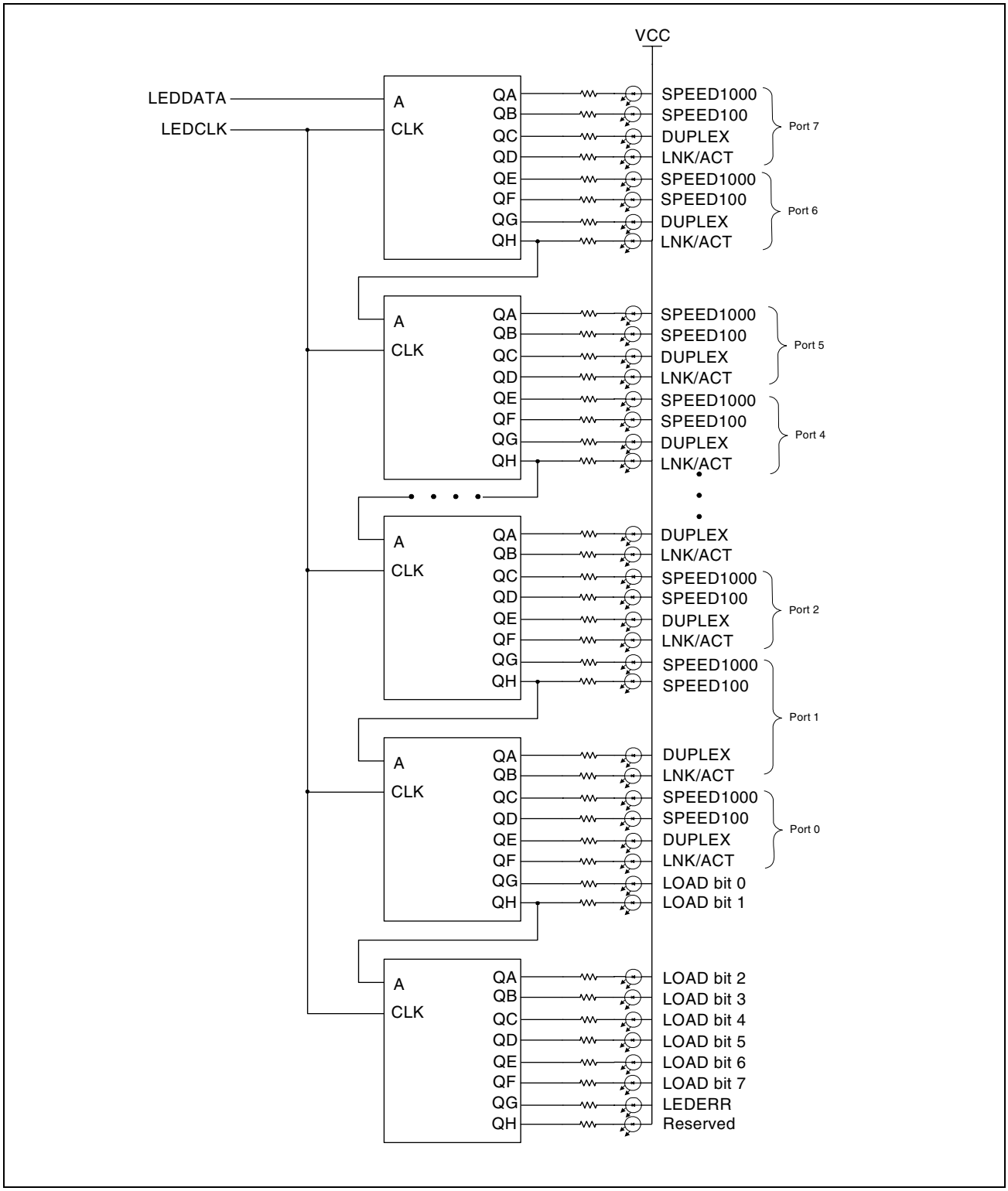


**Figure 30: Example External Circuit for Serial LED Mode (LEDMODE[2:0] = 000)**

*Table 27: Serial LED Mode Matrix*

| LEDMODE | stat0 | stat1 | stat2 | stat3 | stat4 | stat5 | stat6 |
|---|---|---|---|---|---|---|---|
| 000 | RESVD LEDERR | LOAD | LNK/ACT | DUPLEX | SPEED100 | SPEED1000 | — |
| 001 | RESVD LEDERR | LOAD | LNK/ACT/SPD | DUPLEX | — | — | — |
| 010 | RESVD LEDERR | LOAD | LNK | ACT | SPEED100 | SPEED1000 | DUPLEX |
| 011 | RESVD LEDERR | LOAD | LNKG/ACTF | LNKF/ACTG | DPX/COL | — | — |
| 100 | RESVD LEDERR | LOAD | LNK/ACT | DUPLEX | SPEED100 | SPEED1000 | COLSN |
| 101 | RESVD LEDERR | LOAD | LNK/ACT/SPD | DUPLEX | COLSN | — | — |
| 110 | RESVD LEDERR | LOAD | DUPLEX | COLSN | — | — | — |
| 111 | RESVD LEDERR | LOAD | LNK/ACT | DPX/COL | SPEED100 | SPEED1000 | — |

*Table 28: Serial LED Status Types*

| Name | Description |
|---|---|
| LEDERR | Error indication. Internal memory fails self-test during power-on reset. Low if failure occurs. |
| LOAD | Bandwidth utilization indicator. 8-bit binary value indicating the percentage of total switch bandwidth utilized over a 42 ms interval for packet data. See Table 29 on page 82 for more information. |
| LNK | Link indicator. Low when link is established. High when link is off. |
| LNK/ACT | Link and activity indicator. Low when link is established. Blinking at 12 Hz when link is up and port is transmitting and receiving. |
| LNK/ACT/SPD | Link, activity, and speed indicator. Low when link is up. Blinking at 3 Hz when port is transmitting or receiving in 10 Mb mode. Blinking at 6 Hz when port is transmitting or receiving in 100 Mb mode and blinking at 12 Hz when in 1000 Mb mode. |
| LNKG/ACTF | 1000M link, 10/100 activity indicator. Low when 1000 Mb link is up. Blinking at 12 Hz when there is activity in 10 Mb/100 Mb mode. High in all other cases. See Figure 28 on page 78 for more information. |
| LNKF/ACTG | 10/100 Link, 1G activity indicator. Low when 10 Mb/100 Mb link is up. Blinking at 12 Hz when there is activity in 1000 Mb mode. High in all other cases. See Figure 28 on page 78 for more information. |
| DUPLEX | Duplex mode indicator. High for half-duplex or no link, and low for full-duplex and link. |
| DPX/COL | Duplex and collision indicator. Blinking when collision is detected. Low for full-duplex and link. |

*Table 28: Serial LED Status Types (Cont.)*

| Name | Description |
|---|---|
| ACT | Activity indicator. Low for 42 ms when transmit or receive activity is detected during previous 42 ms interval. High during no activity or no link. |
| COLSN | Collision indicator. Low for 42 ms when collision is detected during the previous 42 ms interval. High in the absence of collisions or no link. |
| SPEED100 | 100 Mbps speed indicator. Low for 100 Mbps link; otherwise, high. |
| SPEED1000 | 1000 Mbps speed indicator. Low for link at 1000 Mbps, high for all other conditions. |

The load meter LEDs provide a bar graph indication of the percentage of total available bandwidth of the switch utilized by packet data over a periodic interval of 42 ms. The bar graph scale is shown in Table 29.

*Table 29: Load Meter LED Decode*

| Load[7:0] | Number of LEDs On | Bandwidth (%) |
|---|---|---|
| 00000000 | 8 | > 50.0% |
| 10000000 | 7 | 25.0–50.0% |
| 11000000 | 6 | 12.5–25.0% |
| 11100000 | 5 | 6.25–12.5% |
| 11110000 | 4 | 3.13–6.25% |
| 11111000 | 3 | 1.56–3.13% |
| 11111100 | 2 | 0.78–1.56% |
| 11111110 | 1 | 0.49–0.78% |
| 11111111 | 0 | < 0.49% |

# Section 5: Hardware Signal Definition Table

## I/O Signal Types

The following conventions are used to identify the I/O types shown in Table 30. The I/O pin type is useful in referencing the DC-pin characteristics in "Electrical Characteristics" on page 187.

***Table 30: I/O Signal Type Definitions***

| *Abbreviation* | *Description* |
|---|---|
| 3T | 3.3V tolerant |
| A | Analog pin type |
| B | Bias pin type |
| CS | Continuously sampled |
| D | Digital pin type |
| DNC | Do not connect |
| DPD | Digital Pull Down |
| G | RGMII pin type |
| GND | Ground |
| I | Input |
| I/O | Bidirectional |
| $I_{PU}$ | Input with internal pullup |
| $O_{3S}$ | Three-state output |
| OD | Open drain |
| $O_{DO}$ | Open-drain output |
| OT | Tristateable signal |
| O | Output |
| PD | Internal pulldown |
| SOR | Sample on reset |
| PWR | Power pin supply |
| PU | Internal pullup |
| XT | Crystal pin type |

# Signal Descriptions

*Table 31: Signal Descriptions*

| *Signal Name* | *Type* | *Description* |
|---|---|---|
| **Serial Interface** | | |
| SGRX-{0:4}<br>SGRX+{0:4} | $I_A$ | **Serial Transmit/Receive Pairs**. Differential Serial input and output data pairs. |
| SGTX-{0:4}<br>SGTX+{0:4} | $O_A$ | |
| SD{0:4} | $I_{PD,DPD}$ | **Serial Signal Detection**. |
| **Clock/Reset** | | |
| $\overline{\text{RESET}}$ | $I_{PU,D}$ | **Hardware Reset Input**. Active low Schmitt-triggered input. Resets the BCM5387. |
| XTALI | $I_{XT}$ | **25-MHz Crystal Oscillator Input/Output**. A continuous 25-MHz reference clock must be supplied to the BCM5387 by connecting a 25-MHz crystal between these two pins or by driving XTALI with an external 25-MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTALO unconnected. The maximum XTALI input voltage is 2.5V. |
| XTALO | $O_{XT}$ | |
| **IMP Interface** | | |
| TXCLK | $O_D$ | **GMII Transmit Clock**. This clock is driven to synchronize the transmit data in GMII mode at 125 MHz (1000 Mbps mode only).<br>**RGMII Transmit Clock**. This clock is driven to synchronize the transmit data in RGMII mode: 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. In RGMII mode, both edges of the clock are used to align with TXD[3:0].<br>**RvMII Receive Clock**. Synchronizes the TXD[3:0] in RvMII mode and connects to the MAC/Management Entity RXC. In 100 Mbps mode, this output is 25 MHz. In 10 Mbps mode this output is 2.5 MHz. |
| TXD[3:0] | $O_D$ | **GMII Transmit Data Output (first nibble)**. Data bits TXD[3:0] are clocked on the rising edge of TXCLK.<br>**RGMII Transmit Data Output**. For 1000 Mbps operation, data bits TXD[3:0] are clocked on the rising edge of TXCLK, and data bits TXD[7:4] are clocked on the falling edge of TXCLK. For 10 Mbps and 100 Mbps, data bits TXD[3:0] are clocked on the rising edge of TXCLK.<br>**RvMII Receive Data Output**. Clocked on the rising edge of TXCLK and connected to the RXD pins of the external MAC/Management entity. |
| TXD[7:4] | $O_D$ | **GMII Transmit Data Output (second nibble)**. Data bits[7:4] are clocked on the rising edge of TXCLK. |

*Table 31: Signal Descriptions (Cont.)*

| Signal Name | Type | Description |
|---|---|---|
| TXEN | $O_D$ | **GMII Transmit Enable**. Active high. TXEN indicates the data on the TXD pins are encoded and transmitted.<br>**RGMII Transmit Control**. On the rising edge of TXCLK, TXEN indicates that a transmit frame is in progress, and the data present on the TXD[3:0] output pins is valid. On the falling edge of TXCLK, TXEN is a derivative of GMII mode TXEN and TXER signals.<br>**RvMII Receive Data Valid**. Active high. Connected to RXDV pin of MAC/Management entity. Indicates that a receive frame is in progress, and the data present on the TXD[3:0] output pins is valid. |
| TXER | $O_D$ | **GMII Transmit Error**. Active high. Asserting TXER when TXEN is high indicates a transmission error. TXER is also used to indicate Carrier Extension when operating in half-duplex mode. |
| RXCLK | $I_D$ | **GMII Receive Clock**. 125 MHz (1000 Mbps operation only)<br>**RGMII Receive Clock**. 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. Data bits RXD[3:0] are clocked in on the rising edge of the RXCLK, and data bits RXD[7:4] are clocked in on the falling edge of the RXCLK. |
| | $O_D$ | **RvMII Transmit Clock**. Synchronizes the RXD[3:0] in RvMII mode and connects to the MAC/Management entity TXC. 25 MHz for 100 Mbps mode, and 2.5 MHz for 10 Mbps mode. |
| RXD[3:0] | $I_D$ | **GMII Receive Data Inputs (first nibble)**. Data bits RXD[3:0] are clocked on the rising edge of RXCLK.<br>**RGMII Receive Data Inputs**. For 1000 Mbps operation, data bits RXD[3:0] are clocked-out on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mbps and 100 Mbps modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK.<br>**RvMII Transmit Data Inputs**. Clocked on the rising edge of RXCLK and connected to the TXD pins of the external MAC/Management entity. |
| RXD[7:4] | $I_D$ | **GMII Receive Data Outputs (second nibble)**. Data bits RXD[7:4] are clocked out on the rising edge of RXCLK. |
| RXDV | $I_D$ | **GMII Receive Data Valid**. Active high. RXDV indicates that a receive frame is in progress, and the data present on the RXD output pins are valid.<br>**RGMII Receive Data Valid**. Functional equivalent of GMII RXDV on the rising edge of RXCLK and functional equivalent of a logical derivative of GMII RXDV and RXER on the falling edge of RXCLK.<br>**RvMII Transmit Enable**. Active high. Indicates the data on the RXD[3:0] pins are encoded and transmitted. Connects to the TXEN of the external MAC/Management entity. |
| RXER | $I_D$ | **GMII Receive Error**. Indicates an error during the receive frame. |
| **MDC/MDIO Interface** | | |
| MDIO | $I/O_{PU,D}$ | **Management Data I/O**. In master mode, this serial input/output data signal is used to read from and write to the MII registers of the external transceivers. In slave mode, it is used by an external entity to read/write to the switch registers via the Pseudo-PHY. See MDC/MDIO interface for more information. |

*Table 31: Signal Descriptions (Cont.)*

| *Signal Name* | *Type* | *Description* |
|---|---|---|
| MDC | $I/O_{PU,D}$ | **Management Data Clock**. In master mode, this 2.5 MHz clock sourced by the BCM5387 to the external PHY device. In slave mode, it is sourced by an external entity. |
| **LED Interface** | | |
| $\overline{\text{LEDA}}${4:0}<br>$\overline{\text{LEDB}}${4:0}<br>$\overline{\text{LEDC}}${4:0}<br>$\overline{\text{LEDD}}${4:0} | $O_D$ | **Parallel LED Indicators**. These indicator pins represent port status conditions depending on how they are programmed via the LEDMODE[2:0] pins. See "LED Interfaces" on page 77 for a functional description of these signals. |
| LEDCLK | $O_{PD}$ | **LED Shift Clock**. This clock is periodically active to enable LEDDATA to shift into external registers. |
| LEDDATA | $O_{PD}$ | **Serial LED Data Output**. Serial LED data for all ports is shifted out when LEDCLK is active. LEDMODE[2:0] pins set the serial data content. See LED interface for a functional description of this signal. |
| **Programming Interfaces** | | |
| SCK | $I_{PD,DPD}$ | **SPI Serial Clock**. Clock input to the BCM5387 SPI interface supplied by the SPI master. Supports up to 2 MHz. Enabled if CPU_EPROM_SEL is high during power-on reset. |
| | $O_{PD}$ | **EEPROM Serial Clock**. Clock output to an external EEPROM device. Enabled if CPU_EPROM_SEL is low during power-on reset.<br>See programming interfaces for more information. |
| $\overline{\text{SS/CS}}$ | $I_{PU,D}$ | **SPI Slave Select**. Active low signal which enables an SPI interface read or write operation. Enabled if CPU_EPROM_SEL is high during power-on reset. |
| | $O_{PU}$ | **EEPROM Chip Select**. Active high control signal that enables a read operation from an external EEPROM device. Enabled if CPU_EPROM_SEL is low during power-on reset.<br>See Programming interfaces for more information. |
| MOSI/DI | $I_{PD,3T,DPD}$ | **SPI Master-Out/Slave-In**. Input signal which receives control and address information for the SPI interface, as well as serial data during write operations. Enabled if CPU_EPROM_SEL is high during power-on reset. |
| | $O_{PD}$ | **EEPROM Data In**. Serial data input to an external EEPROM device. Enabled if CPU_EPROM_SEL is low during power-on reset.<br>See programming interfaces for more information. |
| MISO/DO | $O_{PD}$ | **SPI Master-In/Slave-Out**. Output signal which transmits serial data during an SPI interface read operation. Enabled if CPU_EPROM_SEL is high during power-on reset. |
| | $I_{PD}$ | **EEPROM Data Out**. Serial data output to an external EEPROM device. Enabled if CPU_EPROM_SEL is low during power-on reset.<br>See programming interfaces for more information. |

*Table 31: Signal Descriptions (Cont.)*

| Signal Name | Type | Description |
|---|---|---|
| **Configuration Pins** | | |
| AUTO_POLL | $I_{PD,SOR,DPD}$ | **Automatic PHY Polling Enable**.<br>0 = Enable external PHY polling.<br>1 = Disable external PHY polling.<br>See "MDC/MDIO Interface" on page 69 for more information. |
| BC_SUPP_EN | $I_{PD,SOR,DPD}$ | **Broadcast Suppression Enable**.<br>0 = Disable rate-based broadcast suppression.<br>1 = Enable rate-based broadcast suppression.<br>See "Rate Control" on page 29 for more information. |
| CLK_FREQ1 | $I_{PU,SOR,D}$ | **System Clock Selection**.<br>Determines rate of system clock.<br>00 = 100 MHz<br>01 = 104 MHz<br>10 = 113 MHz (normal operation)<br>11 = 125 MHz |
| CLK_FREQ0 | $I_{PD,SOR,DPD}$ | |
| CPU_EPROM_SEL | $I_{PU,SOR,D}$ | **CPU or EEPROM Interface Selection**.<br>CPU_EPROM_SEL = 0: Enable EEPROM interface.<br>CPU_EPROM_SEL = 1: Enable SPI interface.<br>See "Programming Interfaces" on page 61 for more information. |
| ENFDXFLOW | $I_{PU,SOR,D}$ | **Enable Automatic Full-Duplex Flow Control**. In combination with the results of auto-negotiation, sets the flow control mode. Refer to "Flow Control" on page 44 for more information. |
| ENHDXFLOW | $I_{PU,SOR,D}$ | **Enable Automatic Backpressure**. When this pin is pulled high, it enables half-duplex backpressure flow control when a port is configured to half-duplex. Refer to "Flow Control" on page 44 for more information. |
| EEPROM_EXT[1:0] | $I_{PD,SOR,DPD}$ | **Extended EEPROM Interface Selection**.<br>EEPROM_EXT[1:0] = 00: Supports 93C46 EEPROM<br>EEPROM_EXT[1:0] = 01: Supports 93C56 EEPROM<br>EEPROM_EXT[1:0] = 10: Supports 93C66 EEPROM<br>EEPROM_EXT[1:0] = 11: Supports 93C86 EEPROM<br>See "EEPROM Interface" on page 67 for more information. |
| HW_FWDG_EN | $I_{PD,DPD}$ | **Forwarding Enable**. Active high. If this pin is pulled low at power-up, frame forwarding is disabled. |
| LEDMODE[2:0]<br>• LEDMODE[2]<br>• LEDMODE[1]<br>• LEDMODE[0] | <br>$I_{PU,SOR,D}$<br>$I_{PD,SOR,DPD}$<br>$I_{PD,SOR,DPD}$ | **LED Mode**. These pins configure the LED mode for the LED outputs during power-on reset. Sets the default for register value Page 00, Offset 0Bh, bits[1:0]. See "LED Interfaces" on page 77 for more information. |

*Table 31: Signal Descriptions (Cont.)*

| Signal Name | Type | Description |
|---|---|---|
| MODE[1:0] | $I_{PD,SOR,DPD}$ | **IMP Port Mode**. Sets the mode of the IMP port based on the value of the pins at power-on reset.<br>00 = RGMII mode<br>01 = GMII mode<br>10 = RvMII mode<br>11 = Reserved |
| QoS_EN | $I_{PD,SOR,DPD}$ | **QoS Enable**.<br>QoS_EN = 0: Disable QoS function.<br>QoS_EN = 1: Enable QoS function.<br>See "Quality of Service" on page 22 for more information. |
| QoS_FC_OFF | $I_{PU,SOR,D}$ | **QoS Flow Control Off**.<br>0 = Enable flow control when QoS is enabled.<br>1 = Disable flow control when QoS is enabled.<br>See "Quality of Service" on page 22 for more information. |
| RXC_DELAY | $I_{PD,SOR,DPD}$ | **RXCLK Clock Timing Delay**. Active high. This pin enables the RXCLK to data-sampling timing delay. The input delayed timing mode can be programmed in the "IMP RGMII Control Register (Page 00h: Address 060h)" on page 106. See "RGMII Interface Timing" on page 194 for more information. |
| TXC_DELAY | $I_{PD,SOR,DPD}$ | **TXCLK Clock Timing Delay**. Active high. This pin enables the TXCLK to Data timing delay in RGMII mode. The output delayed timing mode can be programmed in the "IMP RGMII Control Register (Page 00h: Address 060h)" on page 106. See "RGMII Interface Timing" on page 194 for more information. This pin is to be floating or set low when operating in GMII or RvMII mode. |
| **Power** | | |
| PLLAVDD2<br>PLLAVDD | PWR<br>PWR | **Phase Lock Loop Analog VDD 2**. +1.2V. Second phase lock loop (for system clock and IMP transmit clock) analog VDD.<br>**Phase Lock Loop Analog VDD**. +1.2V. 1st phase lock loop (for SerDes clock) analog VDD. |
| PLLDVDD | PWR | **Phase Lock Loop Digital VDD**.+1.2V. |
| XTALVDD | PWR | **XTAL VDD**. +2.5V. |
| SAVDD | PWR | **SerDes Analog VDD**. +1.2V |
| DVDD | PWR | **Digital Core VDD**. +1.2V. |
| OVDD2<br>OVDD | PWR<br>PWR | **Digital Periphery VDD 2**.+2.5V.<br>**Digital Periphery VDD**. +2.5V (RGMII) or 3.3V (GMII). |
| GND | PWR | **Ground**. 0.0V. |
| **No Connect** | | |
| DNC | DNC | **Do Not Connect**. For test purposes only and should not be connected. |

# Section 6: Pin Assignment

## Pin Assignment by Pin Number

*Table 32: Pin Assignment (Sorted by Pin Number)*

| Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin |
|---|---|---|---|---|---|---|---|
| SGRX-{0} | A01 | PLLAVDD2 | C04 | DVDD | E07 | GND | G10 |
| SGRX+{0} | A02 | GND | C05 | OVDD2 | E08 | GND | G11 |
| GND | A03 | DNC | C06 | DVDD | E09 | OVDD | G12 |
| SAVDD | A04 | DNC | C07 | OVDD2 | E10 | RXD6 | G13 |
| RESET | A05 | DNC | C08 | DVDD | E11 | RXD7 | G14 |
| MODE0 | A06 | DNC | C09 | OVDD2 | E12 | GND | G15 |
| EEPROM_EXT1 | A07 | GND | C10 | RXER | E13 | DVDD | G16 |
| EEPROM_EXT0 | A08 | LEDMODE2 | C11 | RXD0 | E14 | XTALO | H01 |
| QOS_FC_OFF | A09 | GND | C12 | DVDD | E15 | XTALI | H02 |
| ENHDXFLOW | A10 | DVDD | C13 | GND | E16 | SGTX+{3} | H03 |
| BC_SUPP_EN | A11 | GND | C14 | GND | F01 | SGTX-{3} | H04 |
| CLK_FREQ1 | A12 | DNC | C15 | SAVDD | F02 | SAVDD | H05 |
| DNC | A13 | DNC | C16 | SGTX-{2} | F03 | GND | H06 |
| LEDMODE1 | A14 | GND | D01 | SGTX+{2} | F04 | GND | H07 |
| DNC | A15 | SAVDD | D02 | SAVDD | F05 | GND | H08 |
| TXC_DELAY | A16 | SGTX-{1} | D03 | GND | F06 | GND | H09 |
| GND | B01 | SGTX+{1} | D04 | GND | F07 | GND | H10 |
| SAVDD | B02 | DVDD | D05 | GND | F08 | GND | H11 |
| SGTX-{0} | B03 | DNC | D06 | GND | F09 | OVDD | H12 |
| SGTX+{0} | B04 | DNC | D07 | GND | F10 | TXD3 | H13 |
| MODE1 | B05 | DNC | D08 | GND | F11 | TXD1 | H14 |
| HW_FWDG_EN | B06 | DNC | D09 | OVDD | F12 | TXD0 | H15 |
| GND | B07 | DNC | D10 | RXD1 | F13 | TXD2 | H16 |
| DVDD | B08 | DNC | D11 | RXD3 | F14 | SGRX-{4} | J01 |
| GND | B09 | DNC | D12 | RXD4 | F15 | SGRX+{4} | J02 |
| ENFDXFLOW | B10 | DNC | D13 | RXD5 | F16 | DNC | J03 |
| QOS_EN | B11 | RXDV | D14 | SGRX-{3} | G01 | XTALVDD | J04 |
| CLK_FREQ0 | B12 | RXCLK | D15 | SGRX+{3} | G02 | SAVDD | J05 |
| CPU_EPROM_SEL | B13 | RXD2 | D16 | GND | G03 | GND | J06 |
| LEDMODE0 | B14 | SGRX-{2} | E01 | PLLAVDD | G04 | GND | J07 |
| AUTO_POLL | B15 | SGRX+{2} | E02 | SAVDD | G05 | GND | J08 |
| RXC_DELAY | B16 | GND | E03 | GND | G06 | GND | J09 |
| SGRX-{1} | C01 | SAVDD | E04 | GND | G07 | GND | J10 |
| SGRX+{1} | C02 | SAVDD | E05 | GND | G08 | GND | J11 |
| GND | C03 | OVDD2 | E06 | GND | G09 | OVDD | J12 |

| Signal Name | Pin |
|---|---|
| TXER | J13 |
| TXD6 | J14 |
| TXD5 | J15 |
| TXD4 | J16 |
| PLLDVDD | K01 |
| GND | K02 |
| SGTX+{4} | K03 |
| SGTX-{4} | K04 |
| SAVDD | K05 |
| GND | K06 |
| GND | K07 |
| GND | K08 |
| GND | K09 |
| GND | K10 |
| GND | K11 |
| OVDD2 | K12 |
| DNC | K13 |
| GND | K14 |
| DVDD | K15 |
| GND | K16 |
| DNC | L01 |
| DNC | L02 |
| GND | L03 |
| DNC | L04 |
| SAVDD | L05 |
| GND | L06 |
| GND | L07 |
| GND | L08 |
| GND | L09 |
| GND | L10 |
| GND | L11 |
| DVDD | L12 |
| DNC | L13 |
| MDIO | L14 |
| TXCLK | L15 |
| TXD7 | L16 |
| GND | M01 |
| SAVDD | M02 |
| DNC | M03 |
| DNC | M04 |
| SAVDD | M05 |
| GND | M06 |
| DVDD | M07 |

| Signal Name | Pin |
|---|---|
| OVDD2 | M08 |
| DVDD | M09 |
| OVDD2 | M10 |
| DVDD | M11 |
| OVDD2 | M12 |
| DVDD | M13 |
| DNC | M14 |
| DNC | M15 |
| TXEN | M16 |
| DNC | N01 |
| DNC | N02 |
| SD{4} | N03 |
| SD{0} | N04 |
| LEDA0 | N05 |
| LEDC0 | N06 |
| LEDD0 | N07 |
| LEDB0 | N08 |
| DVDD | N09 |
| GND | N10 |
| DVDD | N11 |
| GND | N12 |
| GND | N13 |
| MISO/DO | N14 |
| MDC | N15 |
| DNC | N16 |
| GND | P01 |
| SAVDD | P02 |
| DNC | P03 |
| DNC | P04 |
| DNC | P05 |
| LEDC1 | P06 |
| LEDD2 | P07 |
| LEDA2 | P08 |
| LEDD4 | P09 |
| LEDB4 | P10 |
| DNC | P11 |
| DNC | P12 |
| DNC | P13 |
| SCK | P14 |
| LEDDATA | P15 |
| DNC | P16 |
| DNC | R01 |
| DNC | R02 |

| Signal Name | Pin |
|---|---|
| SD{1} | R03 |
| SD{2} | R04 |
| LEDD1 | R05 |
| LEDB1 | R06 |
| LEDC2 | R07 |
| LEDD3 | R08 |
| LEDA3 | R09 |
| LEDA4 | R10 |
| DNC | R11 |
| DNC | R12 |
| DNC | R13 |
| DNC | R14 |
| $\overline{SS}$/CS | R15 |
| LEDCLK | R16 |
| GND | T01 |
| SD{3} | T02 |
| DNC | T03 |
| DNC | T04 |
| DNC | T05 |
| LEDA1 | T06 |
| LEDB2 | T07 |
| LEDC3 | T08 |
| LEDB3 | T09 |
| LEDC4 | T10 |
| DNC | T11 |
| DNC | T12 |
| DNC | T13 |
| DNC | T14 |
| DNC | T15 |
| MOSI/DI | T16 |

# Pin Assignment by Signal Name

*Table 33: Pin Assignment (Sorted by Signal Name)*

| Signal Name | Pin |
|---|---|
| AUTO_POLL | B15 |
| BC_SUPP_EN | A11 |
| CLK_FREQ0 | B12 |
| CLK_FREQ1 | A12 |
| CPU_EPROM_SEL | B13 |
| DNC | A13 |
| DNC | A15 |
| DNC | C06 |
| DNC | C07 |
| DNC | C08 |
| DNC | C09 |
| DNC | C15 |
| DNC | C16 |
| DNC | D06 |
| DNC | D07 |
| DNC | D08 |
| DNC | D09 |
| DNC | D10 |
| DNC | D11 |
| DNC | D12 |
| DNC | D13 |
| DNC | J03 |
| DNC | K13 |
| DNC | L01 |
| DNC | L02 |
| DNC | L04 |
| DNC | L13 |
| DNC | M03 |
| DNC | M04 |
| DNC | M14 |
| DNC | M15 |
| DNC | N01 |
| DNC | N02 |
| DNC | N16 |
| DNC | P03 |
| DNC | P04 |
| DNC | P05 |
| DNC | P11 |
| DNC | P12 |
| DNC | P13 |
| DNC | P16 |
| DNC | R01 |
| DNC | R02 |
| DNC | R11 |
| DNC | R12 |
| DNC | R13 |
| DNC | R14 |
| DNC | T03 |
| DNC | T04 |
| DNC | T05 |
| DNC | T11 |
| DNC | T12 |
| DNC | T13 |
| DNC | T14 |
| DNC | T15 |
| DVDD | B08 |
| DVDD | C13 |
| DVDD | D05 |
| DVDD | E07 |
| DVDD | E09 |
| DVDD | E11 |
| DVDD | E15 |
| DVDD | G16 |
| DVDD | K15 |
| DVDD | L12 |
| DVDD | M07 |
| DVDD | M09 |
| DVDD | M11 |
| DVDD | M13 |
| DVDD | N09 |
| DVDD | N11 |
| EEPROM_EXT0 | A08 |
| EEPROM_EXT1 | A07 |
| ENFDXFLOW | B10 |
| ENHDXFLOW | A10 |
| GND | A03 |
| GND | B01 |
| GND | B07 |
| GND | B09 |
| GND | C03 |
| GND | C05 |
| GND | C10 |
| GND | C12 |
| GND | C14 |
| GND | D01 |
| GND | E03 |
| GND | E16 |
| GND | F01 |
| GND | F06 |
| GND | F07 |
| GND | F08 |
| GND | F09 |
| GND | F10 |
| GND | F11 |
| GND | G03 |
| GND | G06 |
| GND | G07 |
| GND | G08 |
| GND | G09 |
| GND | G10 |
| GND | G11 |
| GND | G15 |
| GND | H06 |
| GND | H07 |
| GND | H08 |
| GND | H09 |
| GND | H10 |
| GND | H11 |
| GND | J06 |
| GND | J07 |
| GND | J08 |
| GND | J09 |
| GND | J10 |
| GND | J11 |
| GND | K02 |
| GND | K06 |
| GND | K07 |
| GND | K08 |
| GND | K09 |
| GND | K10 |
| GND | K11 |
| GND | K14 |
| GND | K16 |
| GND | L03 |
| GND | L06 |
| GND | L07 |
| GND | L08 |
| GND | L09 |
| GND | L10 |
| GND | L11 |
| GND | M01 |
| GND | M06 |
| GND | N10 |
| GND | N12 |
| GND | N13 |
| GND | P01 |
| GND | T01 |
| HW_FWDG_EN | B06 |
| LEDA0 | N05 |
| LEDA1 | T06 |
| LEDA2 | P08 |
| LEDA3 | R09 |
| LEDA4 | R10 |
| LEDB0 | N08 |
| LEDB1 | R06 |
| LEDB2 | T07 |
| LEDB3 | T09 |
| LEDB4 | P10 |
| LEDC0 | N06 |
| LEDC1 | P06 |
| LEDC2 | R07 |
| LEDC3 | T08 |
| LEDC4 | T10 |
| LEDCLK | R16 |
| LEDD0 | N07 |
| LEDD1 | R05 |

| Signal Name | Pin |
|---|---|
| LEDD2 | P07 |
| LEDD3 | R08 |
| LEDD4 | P09 |
| LEDDATA | P15 |
| LEDMODE0 | B14 |
| LEDMODE1 | A14 |
| LEDMODE2 | C11 |
| MDC | N15 |
| MDIO | L14 |
| MISO/DO | N14 |
| MODE0 | A06 |
| MODE1 | B05 |
| MOSI/DI | T16 |
| OVDD | F12 |
| OVDD | G12 |
| OVDD | H12 |
| OVDD | J12 |
| OVDD2 | E06 |
| OVDD2 | E08 |
| OVDD2 | E10 |
| OVDD2 | E12 |
| OVDD2 | K12 |
| OVDD2 | M08 |
| OVDD2 | M10 |
| OVDD2 | M12 |
| PLLAVDD | G04 |
| PLLAVDD2 | C04 |
| PLLDVDD | K01 |
| QOS_EN | B11 |
| QOS_FC_OFF | A09 |
| RESET | A05 |
| RXC_DELAY | B16 |
| RXCLK | D15 |
| RXD0 | E14 |
| RXD1 | F13 |
| RXD2 | D16 |
| RXD3 | F14 |
| RXD4 | F15 |
| RXD5 | F16 |
| RXD6 | G13 |
| RXD7 | G14 |
| RXDV | D14 |
| RXER | E13 |

| Signal Name | Pin |
|---|---|
| SAVDD | A04 |
| SAVDD | B02 |
| SAVDD | D02 |
| SAVDD | E04 |
| SAVDD | E05 |
| SAVDD | F02 |
| SAVDD | F05 |
| SAVDD | G05 |
| SAVDD | H05 |
| SAVDD | J05 |
| SAVDD | K05 |
| SAVDD | L05 |
| SAVDD | M02 |
| SAVDD | M05 |
| SAVDD | P02 |
| SCK | P14 |
| SD{0} | N04 |
| SD{1} | R03 |
| SD{2} | R04 |
| SD{3} | T02 |
| SD{4} | N03 |
| SGRX-{0} | A01 |
| SGRX-{1} | C01 |
| SGRX-{2} | E01 |
| SGRX-{3} | G01 |
| SGRX-{4} | J01 |
| SGRX+{0} | A02 |
| SGRX+{1} | C02 |
| SGRX+{2} | E02 |
| SGRX+{3} | G02 |
| SGRX+{4} | J02 |
| SGTX-{0} | B03 |
| SGTX-{1} | D03 |
| SGTX-{2} | F03 |
| SGTX-{3} | H04 |
| SGTX-{4} | K04 |
| SGTX+{0} | B04 |
| SGTX+{1} | D04 |
| SGTX+{2} | F04 |
| SGTX+{3} | H03 |
| SGTX+{4} | K03 |
| $\overline{SS}$/CS | R15 |
| TXC_DELAY | A16 |

| Signal Name | Pin |
|---|---|
| TXCLK | L15 |
| TXD0 | H15 |
| TXD1 | H14 |
| TXD2 | H16 |
| TXD3 | H13 |
| TXD4 | J16 |
| TXD5 | J15 |
| TXD6 | J14 |
| TXD7 | L16 |
| TXEN | M16 |
| TXER | J13 |
| XTALI | H02 |
| XTALO | H01 |
| XTALVDD | J04 |

# Section 7: Register Definitions

## Register Definition

The BCM5387 register set can be accessed through the “Programming Interfaces” on page 61. The register space is organized into pages, each containing a certain set of registers. Table 34 on page 94 lists the pages defined in the BCM5387. To access a page, the page register (0xFF) is written with the page value. The registers contained in the page can then be accessed by their address. See “Programming Interfaces” on page 61 for more information.

## Register Notations

In the register description tables, the following notation in the R/W column is used to describe the ability to read or to write:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Clear on read

Reserved bits must be written as the default value and ignored when read.

# Global Page Register

***Table 34: Global Page Register Map***

| *Page* | *Description* |
|---|---|
| 00h | "Page 00h: Control Registers" on page 95 |
| 01h | "Page 01h: Status Registers" on page 109 |
| 02h | "Page 02h: Management/Mirroring Registers" on page 113 |
| 03h | Reserved |
| 04h | "Page 04h: ARL Control Register" on page 120 |
| 05h | "Page 05h: ARL/VTBL Access Registers" on page 124 |
| 06h–0Fh | Reserved |
| 010h–017h | "Page 010h–017h: Internal Serial Port Registers" on page 135 |
| 018h–01Fh | Reserved |
| 020h–028h | "Page 020h-027h: Port MIB Registers" on page 153 |
| 029h–02Fh | Reserved |
| 030h | "Page 030h: QoS Registers" on page 158 |
| 031h | "Page 031h: Port-Based VLAN Registers" on page 165 |
| 032h | "Page 032h: Trunking Registers" on page 166 |
| 033h | Reserved |
| 034h | "Page 034h: IEEE 802.1Q VLAN Registers" on page 168 |
| 035h–03Fh | Reserved |
| 040h | "Page 040h: Jumbo Frame Control Register" on page 175 |
| 041h | "Page 041h: Broadcast Storm Suppression Register" on page 178 |
| 042h–07Fh | Reserved |
| 080h–087h | "Page 080-087h: External PHY Registers (Serial Ports)" on page 183 |
| 088h–0EFh | Reserved |
| Maps to all pages | "Global Registers" on page 185 |

# Page 00h: Control Registers

*Table 35: Control Registers (Page 00h)*

| Address | Bits | Register Name |
|---|---|---|
| 00h-07h | 8/port | "Port Traffic Control Register (Page 00h: Address 00h)" on page 96 |
| 08h | 8 | "IMP Traffic Control Register (Page 00h: Address 08h)" on page 97 |
| 09h–0Ah | – | Reserved |
| 0Bh | 8 | "Switch Mode Register (Page 00h: Address 0Bh)" on page 98 |
| 0Ch–0Dh | – | Reserved |
| 0Eh | 8 | "IMP Port State Override Register (Page 00h: Address 0Eh)" on page 98 |
| 0Fh–011h | – | Reserved |
| 012h–019h | 16/LED | "LED Control Register (Page 00h: Address 012h)" on page 99 |
| 01Ah–020h | – | Reserved |
| 021h | 8 | "Port Forward Control Register (Page 00h: Address 021h)" on page 100 |
| 022h–023h | – | Reserved |
| 024h–025h | 16 | "Protected Port Selection Register (Page 00h: Address 24h)" on page 100 |
| 026h–02Eh | – | Reserved |
| 02Fh | 8 | "Reserved Multicast Control Register (Page 00h: Address 02Fh)" on page 101 |
| 030h–031h | – | Reserved |
| 02h–033h | 16 | "Unicast Lookup Failed Forward Map Register (Page 00h: Address 032h)" on page 102 |
| 034h–035h | 16 | "Multicast Lookup Failed Forward Map Register (Page 00h: Address 034h)" on page 103 |
| 036h–04Fh | – | Reserved |
| 050h–057h | 8/port | "External PHY Scan Result Register (Page 00h: Address 050h)" on page 104 |
| 058h–05Fh | 8/port | "Port State Override Register (Page 00h: Address 058h)" on page 105 |
| 060h | 8 | "IMP RGMII Control Register (Page 00h: Address 060h)" on page 106 |
| 061h–06Fh | – | Reserved |
| 070h–077h | 8/port | "MDIO/MDC Port Address Register (Page 00h: Address 070h)" on page 107 |
| 078h–079h | – | Reserved |
| 080h | 8 | "Pause Frame Detection Control Register (Page 00h: Address 080h)" on page 107 |
| 081h–087h | – | Reserved |
| 088h | 8 | "Fast-Aging Control Register (Page 00h: Address 088h)" on page 108 |
| 089h | 8 | "Fast-Aging Port Control Register (Page 00h: Address 089h)" on page 108 |
| 08Ah–08Bh | 16 | "Fast-Aging VID Control Register (Page 00h: Address 08Ah)" on page 108 |

*Table 35: Control Registers (Page 00h) (Cont.)*

| Address | Bits | Register Name |
|---|---|---|
| 08Ch–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, Bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

# Port Traffic Control Register (Page 00h: Address 00h)

*Table 36: Port Traffic Control Register Address Summary*

| Address | Description |
|---|---|
| 00h | Port 0 |
| 01h | Port 1 |
| 02h | Port 2 |
| 03h | Port 3 |
| 04h | Port 4 |
| 05h | Reserved |
| 06h | Reserved |
| 07h | Reserved |

*Table 37: Port Control Register (Page 00h: Address 00h–07h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:5 | STP_STATE[2:0] | R/W | CPU writes the current computed states of its spanning tree algorithm for a given port.<br>000 = No spanning tree (default for unmanaged mode).<br>001 = Disabled state (default for managed mode).<br>010 = Blocking state.<br>011 = Listening state.<br>100 = Learning state.<br>101 = Forwarding state.<br>110–111= Reserved. | HW_FWDG_EN |
| 4:2 | Reserved | – | – | 000 |
| 1 | TX_DISABLE | R/W | 0 = Enable the transmit function of the port at the MAC level.<br>1 = Disable the transmit function of the port at the MAC level. | 0 |

*Table 37: Port Control Register (Page 00h: Address 00h–07h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 0 | RX_DISABLE | R/W | 0 = Enable the receive function of the port at the MAC level.<br>1 = Disable the receive function of the port at the MAC level. | 0 |

# IMP Traffic Control Register (Page 00h: Address 08h)

*Table 38: IMP Port Control Register (Page 00h: Address 08h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:5 | Reserved | R/W | – | 000 |
| 4 | RX_UCST_EN | R/W | Receive Unicast Enable.<br>Enables the receipt of unicast frames on the IMP when the IMP is configured as the Frame Management port, and the frame is flooded due to no matching address table entry.<br>When cleared, unicast frames that meet the Mirror Ingress/Egress Rules are forwarded to the Frame Management port. | 0 |
| 3 | RX_MCST_EN | R/W | Receive Multicast Enable.<br>Enables the receipt of multicast frames on the IMP, when the IMP is configured as the Frame Management port, and the frame was flooded due to no matching address table entry.<br>When cleared, multicast frames that meet the Mirror Ingress/Egress Rules are forwarded to the Frame Management port. | 0 |
| 2 | RX_BCST_EN | R/W | Receive Broadcast Enable.<br>Enables the receipt of broadcast frames on the IMP.<br>When cleared, multicast frames that meet the Mirror Ingress/Egress Rules are forwarded to the Frame Management port. | 0 |
| 1:0 | Reserved | R/W | – | 0 |

# Switch Mode Register (Page 00h: Address 0Bh)

*Table 39: Switch Mode Register (Page 00h: Address 0Bh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:2 | Reserved | RO | – | 01 |
| 1 | SW_FWDG_EN | R/W | Software Forwarding Enable.<br>SW_FWDG_EN = 1: Frame forwarding is enabled.<br>SW_FWDG_EN = 0: Frame forwarding is disabled.<br>Managed switch implementations should be configured to disable forwarding on power-on to allow the processor to configure the internal address table and other parameters before frame forwarding is enabled. | HW_FWDG_EN |
| 0 | SW_FWDG_MODE | R/W | Software Forwarding Mode.<br>0 = Unmanaged mode.<br>1 = Managed mode.<br>The ARL treats reserved multicast addresses differently depending on this selection. See Table 3 for a precise definition. | ~HW_FWDG_EN |

# IMP Port State Override Register (Page 00h: Address 0Eh)

*Table 40: IMP Port State Override Register (Page 00h: Address 0Eh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | MII_SW_OR | R/W | MII Software Override.<br>0 = Use MII hardware pin status.<br>1 = Use contents of this register. | 0 |
| 6 | Reserved | R/W | Reserved. | 0 |
| 5 | Tx Flow Control Capability | RO | Link Partner Flow Control Capability.<br>0 = Not PAUSE capable.<br>1 = PAUSE capable. | 0 |
| 4 | Rx Flow Control Capability | R/W | Link Partner Flow Control Capability.<br>0 = Not PAUSE-capable.<br>1 = PAUSE-capable. | 0 |
| 3:2 | SPEED | R/W | Speed.<br>00 = 10 Mbps.<br>01 = 100 Mbps.<br>10 = 1000 Mbps. | 10 |
| 1 | FDX | R/W | Full-duplex.<br>0 = Half-duplex.<br>1 = Full-duplex. | 1 |

*Table 40: IMP Port State Override Register (Page 00h: Address 0Eh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 0 | LINK | R/W | Link Status.<br>0 = Link fail.<br>1 = Link pass. | 0 |

# LED Control Register (Page 00h: Address 012h)

*Table 41: LED Control Register Address Summary*

| Address | Description |
|---|---|
| 012h–013h | LED A |
| 014h–015h | LED B |
| 016h–017h | LED C |
| 018h–019h | LED D |

*Table 42: LED Control Register (Page 00h: Address 012h–019h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:10 | Reserved | RO | – | b'111111 |
| 9:0 | LED Control | R/W | Software Control for Parallel.<br>For testing purposes, the mode of each LED can be controlled for each port based on the mapping below:<br>• Bits[9:8] = Port 4<br>• Bits[7:6] = Port 3<br>• Bits[5:4] = Port 2<br>• Bits[3:2] = Port 1<br>• Bits[1:0] = Port 0<br>The value of the bits controls the operation:<br>• 11 = Normal mode<br>• 10 = Flash mode<br>• 01 = On mode<br>• 00 = Off mode | 3FFh |

See “LED Interfaces” on page 77 for more information.

# Port Forward Control Register (Page 00h: Address 021h)

*Table 43: Port Forward Control Register (Page 00h: Address 021h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | MCST_DFL_FWD | R/W | 1 = Forward multicast packets according to Table 7 on page 38 if fail ARL table lookup.<br>0 = Flood multicast packet if fail ARL table lookup. | 0 |
| 6 | UNI_DFL_FWD | R/W | 1 = Forward multicast packets according to Table 7 on page 38 if fail ARL table lookup.<br>0 = Flood unicast packet if fail ARL table lookup. | 0 |
| 5:1 | Reserved | R/W | – | 0 |
| 0 | ARL_MULTICAST | R/W | 1 = Enable 4K IP multicast address scheme.<br>0 = Disable 4K IP multicast address scheme. | 0 |

See "Address Management" on page 33 for more information.

# Protected Port Selection Register (Page 00h: Address 24h)

*Table 44: Protected Port Selection Register (Page 00h: Address 024h-025h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8 | PORT_SELECT | R/W | Protected Port Selection.<br>Bit 8: IMP port<br>1 = Port protected. Cannot send/receive to other protected ports.<br>0 = Port is not protected. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | PORT_SELECT | R/W | Protected Port Selection.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

See "Protected Ports" on page 31 for more information.

# Reserved Multicast Control Register (Page 00h: Address 02Fh)

*Table 45: Reserved Multicast Control Register (Page 00h: Address 02Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Multicast Learning | R/W | Multicast Learning Enable.<br>0 = Do not learn unicast source addresses of frames that have a reserved multicast destination address.<br>1 = Learn unicast source addresses even from frames that have a reserved multicast destination address.<br>See "Address Management" on page 33 for more information. | 0 |
| 6:5 | Reserved | R/W | – | 0 |
| 4 | En_mul_4 | R/W | Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-20 ~ 01-80-C2-00-00-2F.<br>0 = Forward.<br>1 = Drop. | 0 |
| 3 | En_Mul_3 | R/W | Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-11 ~ 01-80-C2-00-00-1F.<br>0 = Forward.<br>1 = Drop. | 0 |
| 2 | En_Mul_2 | R/W | Specifies if packets with the destination address below are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-10.<br>0 = Forward.<br>1 = Drop. | 0 |
| 1 | En_mul_1 | R/W | Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F.<br>0 = Forward.<br>1 = Drop. | 1 |

*Table 45: Reserved Multicast Control Register (Page 00h: Address 02Fh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 0 | En_Mul_0 | R/W | Specifies if packets with the destination address below are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-00.<br>0 = Forward.<br>1 = Drop. | 0 |

See "Multicast Addresses" on page 37 for more information.

## Unicast Lookup Failed Forward Map Register (Page 00h: Address 032h)

*Table 46: Unicast Lookup Failed Forward Map Register (Page 00h: Address 032h-033h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8 | UNI_DFL_MAP | R/W | Unicast Lookup Failed Forward Map.<br>Bit 8: IMP port<br>When the UNICAST_DROP_EN is enabled in the "Port Forward Control Register (Page 00h: Address 021h)" on page 100 and a unicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped.<br>0 = Do not forward a unicast lookup failure to this port.<br>1 = Forward a unicast lookup failure to this port. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | UNI_DFL_MAP | R/W | Unicast Lookup Failed Forward Map.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

See "Unicast Addresses" on page 35 for more information

# Multicast Lookup Failed Forward Map Register (Page 00h: Address 034h)

*Table 47: Multicast Lookup Failed Forward Map Register (Page 00h: Address 034h-035h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8 | MCST_DFL_MAP | R/W | Multicast Lookup Failed Forward Map.<br>Bit 8: IMP port<br>When the MULTICAST_DROP_EN is enabled in the "Port Forward Control Register (Page 00h: Address 021h)" on page 100 and a multicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped.<br>0 = Do not forward a multicast lookup failure to this port.<br>1 = Forward a multicast lookup failure to this port. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | MCST_DFL_MAP | R/W | Multicast Lookup Failed Forward Map.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

See "Multicast Addresses" on page 37 for more information.

# External PHY Scan Result Register (Page 00h: Address 050h)

*Table 48: External PHY Scan Result Register Address Summary*

| Address | Description |
|---|---|
| 50h | Port 0 |
| 51h | Port 1 |
| 52h | Port 2 |
| 53h | Port 3 |
| 54h | Port 4 |
| 55h | Reserved |
| 56h | Reserved |
| 57h | Reserved |

*Table 49: External PHY Scan Result Register (Page 00h: Address 050h–057h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | RO | – | 0 |
| 6 | SCAN_TIMEOUT_ERROR | RO | This bit is asserted if there is no appropriate response from the external PHY for over 1 ms during register scan. | 0 |
| 5 | TX_FLOW_CONTROL | RO | Reports the result of the external PHY scan for transmit flow control.<br>0 = Flow control enabled for transmit traffic.<br>1 = Flow control disabled for transmit traffic. | 0 |
| 4 | RX_FLOW_CONTROL | RO | Reports the result of the external PHY scan for receive flow control.<br>0 = Flow control enabled for receive traffic.<br>1 = Flow control disabled for receive traffic | 0 |
| 3:2 | SPEED | RO | Reports the result of the external PHY scan for speed settings.<br>00 = 10 Mbps.<br>01 = 100 Mbps.<br>10 = 1000 Mbps.<br>11 = Illegal state. | 0 |
| 1 | Duplex_Mode | RO | Reports the result of the external PHY scan for duplex mode.<br>0 = Half-duplex.<br>1 = Full-duplex. | 0 |
| 0 | Link_State | RO | Reports the result of the external PHY scan for link state.<br>1 = Link up.<br>0 = Link down. | 0 |

For more information, see "MDC/MDIO Interface" on page 69.

# Port State Override Register (Page 00h: Address 058h)

***Table 50: Port State Override Register Address Summary***

| *Address* | *Description* |
|---|---|
| 58h | Port 0 |
| 59h | Port 1 |
| 5Ah | Port 2 |
| 5Bh | Port 3 |
| 5Ch | Port 4 |
| 5Dh | Reserved |
| 5Eh | Reserved |
| 5Fh | Reserved |

***Table 51: Port State Override Register (Page 00h: Address 058h–50Fh)***

| *Bit* | *Name* | *R/W* | *Description* | *Default* |
|---|---|---|---|---|
| 7 | External PHY Scan Enable | R/W | Writing 1 to this bit allows the port to scan the attached external PHY. Writing 0 to this bit disables this operation.<br>Default is set to the inversion of the ~AUTO_POLL pin strap value. | ~AUTO_POLL |
| 6 | Software Override | R/W | Writing 1 to this bit allows the values of the bits[5:0] to be written to the external PHY. Writing 0 to this bit prevents these values from overriding the present external PHY conditions. | 0 |
| 5 | Tx Flow Control Enable | R/W | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1.<br>0 = Flow control enable for transmit traffic.<br>1 = Flow control disable for transmit traffic. | 0 |
| 4 | Rx Flow Control Enable | R/W | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1.<br>0 = Flow control enabled for receive traffic.<br>1 = Flow control disabled for receive traffic. | 0 |

*Table 51: Port State Override Register (Page 00h: Address 058h–50Fh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 3:2 | Speed | R/W | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1.<br>00 = 10 Mbps.<br>01 = 100 Mbps.<br>10 = 1000 Mbps.<br>11 = Illegal state. | 10 |
| 1 | Duplex Mode | R/W | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1.<br>0 = Half-duplex.<br>1 = Full-duplex. | 1 |
| 0 | Link State | R/W | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written 1.<br>1 = Link up.<br>0 = Link down. | 1 |

For more information, see "MDC/MDIO Interface" on page 69.

## IMP RGMII Control Register (Page 00h: Address 060h)

*Table 52: IMP RGMII Control Register (Page 00h: Address 060h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:2 | Reserved | RO | – | 00h |
| 1 | RXC_DELAY | R/W | RGMII RXCLK to Data Sample Delay.<br>Writing 1 to this bit delays the sampling of receive data. See "RGMII Interface Timing" on page 194 for more information. | RXC_DELAY |
| 0 | TXC_DELAY | R/W | RGMII TXCLK to Data Delay.<br>Writing 1 to this bit delays the output clock with respect to data. See "RGMII Interface Timing" on page 194 for more information. | TXC_DELAY |

# MDIO/MDC Port Address Register (Page 00h: Address 070h)

*Table 53: MDIO/MDC Port Address Register Address Summary*

| Address | Description |
|---|---|
| 70h | Port 0 |
| 71h | Port 1 |
| 72h | Port 2 |
| 73h | Port 3 |
| 74h | Port 4 |
| 75h | Reserved |
| 76h | Reserved |
| 77h | Reserved |

*Table 54: MDIO/MDC Port Address Register (Page 00h: Address 070h–077h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:5 | Reserved | RO | – | – |
| 4:0 | MDIO_ADDR | R/W | MDIO/MDC Port Address.<br>Writing to these bits sets the MDIO/MDC address of the respective port. The MDIO/MDC address (PHY Address) is used for auto-polling.<br>Default addresses correspond to port number.<br>See "MDC/MDIO Interface" on page 69 for more information. | |

# Pause Frame Detection Control Register (Page 00h: Address 080h)

*Table 55: Pause Frame Detection Control Register (Page 00h: Address 080h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:1 | Reserved | RO | – | 0 |
| 0 | PAUSE_IGNORE_DA | R/W | 0 = Check DA field on Pause Frame detection.<br>1 = Ignore DA field on Pause Frame detection. | 0 |

# Fast-Aging Control Register (Page 00h: Address 088h)

*Table 56: Fast-Aging Control Register (Page 00h: Address 088h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Fast Age Start/Done | R/W | Fast Age Start/Done.<br>1 = Starts the fast aging.<br>0 = Fast aging is not in process.<br>When fast aging is done, the control bit is automatically cleared. | 0 |
| 6:1 | Reserved | R/W | – | 0 |
| 0 | Static Fast Aging | R/W | Fast Age Static Entries.<br>1 = All entries, including static, are fast-aged.<br>0 = Only dynamic entries are fast-aged. | 0 |

# Fast-Aging Port Control Register (Page 00h: Address 089h)

*Table 57: Fast-Aging Port Control Register (Page 00h: Address 089h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Fast Age All Ports | R/W | Fast Age All Ports Enable.<br>1 = All ports are subject to fast aging.<br>0 = One port selected via bits[3:0] subjected to fast aging. | 1 |
| 6:4 | Reserved | R/W | – | 0 |
| 3:0 | Fast Age Single Port | R/W | Fast Age Single Port Select.<br>Writing bits[3:0] selects the port to be fast aged. | 0 |

# Fast-Aging VID Control Register (Page 00h: Address 08Ah)

*Table 58: Fast-Aging VID Control Register (Page 00h: Address 08Ah-08Bh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Fast Age All VID | R/W | Fast Age All VID Enable.<br>1 = All VIDs are subject to fast aging.<br>0 = One VID selected via bits[11:0] subjected to fast aging. | 1 |
| 14:12 | Reserved | R/W | — | 0 |
| 11:0 | Fast Age Single VID | R/W | Fast Age Single VID Select.<br>Writing bits[11:0] selects the VID to be fast aged | 0 |

# Page 01h: Status Registers

*Table 59: Status Registers (Page 01h)*

| Address | Bits | Register Name |
|---|---|---|
| 00h–01h | 16 | "Link Status Summary (Page 01h: Address 00h)" on page 109 |
| 02h–03h | 16 | "Link Status Change (Page 01h: Address 02h)" on page 110 |
| 04h–07h | 32 | "Port Speed Summary (Page 01h: Address 04h)" on page 110 |
| 08h–09h | 16 | "Duplex Status Summary (Page 01h: Address 08h)" on page 111 |
| 0Ah–0Dh | 32 | "Pause Status Summary (Page 01h: Address 0Ah)" on page 111 |
| 0Eh–0Fh | 16 | "Source Address Change Register (Page 01h: Address 0Eh)" on page 112 |
| 010h–045h | 48/port | "Last Source Address Register (Page 01h: Address 010h)" on page 112 |
| 046h–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

## Link Status Summary (Page 01h: Address 00h)

*Table 60: Link Status Summary Register (Page 01h: Address 00h–01h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8 | LINK_STATUS | RO | Link status.<br>Bit 8: IMP port.<br>0 = Link fail<br>1 = Link pass | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | LINK_STATUS | R/W | Link status.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

# Link Status Change (Page 01h: Address 02h)

*Table 61: Link Status Change Register (Page 01h: Address 02h–03h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8 | LINK_STATUS_CHANGE | RO | Link Status Change.<br>Bit 8: IMP port<br>Upon change of link status, a bit remains set until cleared by a read operation.<br>0 = Link status constant<br>1 = Link status change | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | LINK_STATUS_CHANGE | RO | Link Status Change.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

# Port Speed Summary (Page 01h: Address 04h)

*Table 62: Port Speed Summary Register (Page 01h: Address 04h–07h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:18 | Reserved | PO | Reserved. | 0 |
| 17:16 | PORT_SPEED | RO | Port Speed.<br>The speed of each port is reported based on the mapping below:<br>• Bits[17:16] = IMP port. | 0 |
| 15:10 | Reserved | RO | – | 0 |
| 9:0 | PORT_SPEED | RO | Port Speed.<br>The speed of each port is reported based on the mapping below:<br>• Bits[9:8] = Port 4.<br>• Bits[7:6] = Port 3.<br>• Bits[5:4] = Port 2.<br>• Bits[3:2] = Port 1.<br>• Bits[1:0] = Port 0.<br>The value of the bits are:<br>• 00 = 10 Mbps.<br>• 01 = 100 Mbps.<br>• 10 = 1000 Mbps.<br>• 11 = Illegal state. | 0 |

# Duplex Status Summary (Page 01h: Address 08h)

*Table 63: Duplex Status Summary Register (Page 01h: Address 08h–09h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8 | DUPLEX_STATE | RO | Duplex State.<br>Bit 8: IMP port<br>0 = Half-duplex.<br>1 = Full-duplex. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | DUPLEX_STATE | RO | Duplex State.<br>Bits[4:0] correspond to ports [4:0], respectively.<br>0 = Half-duplex.<br>1 = Full-duplex. | 0 |

# Pause Status Summary (Page 01h: Address 0Ah)

*Table 64: PAUSE Status Summary Register (Page 01h: Address 0Ah–0Dh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:18 | Reserved | RO | Reserved. | 0 |
| 17 | PAUSE_STATE | RO | Pause State.<br>Receive pause capability.<br>• Bit 17: IMP port. | 0 |
| 16:14 | Reserved | RO | – | 0 |
| 13:9 | PAUSE_STATE | RO | Pause State.<br>Receive pause capability.<br>• Bits[13:9] correspond to ports [4:0], respectively. | 0 |
| 8 | PAUSE_STATE | RO | Transmit pause capability.<br>• Bit 8: IMP port. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | PAUSE_STATE | RO | Transmit pause capability.<br>• Bits[4:0] correspond to ports [4:0], respectively.<br>– 0 = Disabled.<br>– 1 = Enabled. | 0 |

# Source Address Change Register (Page 01h: Address 0Eh)

*Table 65: Source Address Change Register (Page 01h: Address 0Eh–0Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8 | SRC_ADDR_CHANGE | RC | Source Address Change.<br>Bit 8: IMP port.<br>The value of this bit is 1 if a change in the source address is detected on the given port.<br>The bit remains set until cleared by a read operation.<br>0 = No change in source address since last read.<br>1 = Source address has changed since last read. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | SRC_ADDR_CHANGE | RO | Source Address Change.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

# Last Source Address Register (Page 01h: Address 010h)

*Table 66: Last Source Address Register Address Summary*

| Address | Description |
|---|---|
| 010h–015h | Port 0 |
| 016h–01Bh | Port 1 |
| 01Ch–021h | Port 2 |
| 022h–027h | Port 3 |
| 028h–02Dh | Port 4 |
| 02Eh–033h | Reserved |
| 034h–039h | Reserved |
| 03Ah–03Fh | Reserved |
| 040h–045h | IMP port |

*Table 67: Last Source Address (Page 01h: Address 010h–045h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:0 | LAST_SOURCE_ADD | R/W | The 48-bit source address detected on the last packet ingressed. | 0 |

# Page 02h: Management/Mirroring Registers

*Table 68: Aging/Mirroring Registers (Page 02h)*

| Address | Bits | Register Name |
|---|---|---|
| 00h | 8 | "Global Management Configuration Register (Page 02h: Address 00h)" on page 114 |
| 01h–03h | – | Reserved |
| 04h–05h | 16 | "RMON MIB Steering Register (Page 02h: Address 04h)" on page 114 |
| 06h–09h | 32 | "Aging Time Control Register (Page 02h: Address 06h)" on page 115 |
| 0Ah–0Fh | – | Reserved |
| 010h–011h | 16 | "Mirror Capture Control Register (Page 02h: Address 010h)" on page 115 |
| 012h–013h | 16 | "Ingress Mirror Control Register (Page 02h: Address 012h)" on page 116 |
| 014h–015h | 16 | "Ingress Mirror Divider Register (Page 02h: Address 014h)" on page 117 |
| 016h–01Bh | 48 | "Ingress Mirror MAC Address Register (Page 02h: Address 016h)" on page 117 |
| 01Ch–01Dh | 16 | "Egress Mirror Control Register (Page 02h: Address 01Ch)" on page 118 |
| 01Eh–01Fh | 16 | "Egress Mirror Divider Register (Page 02h: Address 01Eh)" on page 119 |
| 020h–025h | 48 | "Egress Mirror MAC Address Register (Page 02h: Address 020h)" on page 119 |
| 026h–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

# Global Management Configuration Register (Page 02h: Address 00h)

*Table 69: Global Management Configuration Register (Page 02h: Address 00h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | IMP Port Enable | R/W | IMP Port Enable.<br>0 = No frame management port.<br>1 = IMP port enabled for frame management.<br>These bits are ignored when SW_FWD_MODE = Unmanaged in the "Switch Mode Register (Page 00h: Address 0Bh)" on page 98. | 0 |
| 6:4 | Reserved | R/W | – | 0 |
| 3 | IGMP IP Enable | R/W | IGMP Snooping Enable.<br>1 = IGMP snooping enabled.<br>0 = IGMP snooping disabled.<br>Incoming frames with a value of 2 in the protocol field of the IP header are forwarded to the IMP port.<br>See "IGMP Snooping" on page 33 for more information. | 0 |
| 2 | Reserved | R/W | – | 0 |
| 1 | Receive BPDU | R/W | Receive BPDU Enable.<br>Enables all ports to receive BPDUs and forwards to the IMP port. This bit must be set to globally allow BPDUs to be received. | 0 |
| 0 | Reset MIB | R/W | Reset MIB Counters.<br>Resets all MIB counters for all ports to 0 (pages 20h-28h). This bit must be set and then cleared in successive write cycles to activate the reset operation. | 0 |

# RMON MIB Steering Register (Page 02h: Address 04h)

*Table 70: RMON MIB Steering Register (Page 02h: Address 04h–05h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:8 | Reserved | R/W | – | 0 |
| 7:0 | Override RMON Receive | R/W | Override RMON Receive.<br>Forces the RMON packet size bucket counters from the normal default of snooping on the receive side of the MAC to the transmit side. This allows the RMON bucket counters to snoop either transmit or receive, allowing full-duplex MAC support. | 0 |
| 6:5 | Reserved | RO | – | 0 |

*Table 70: RMON MIB Steering Register (Page 02h: Address 04h–05h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 4:0 | Override RMON Receive | R/W | Override RMON Receive.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

## Aging Time Control Register (Page 02h: Address 06h)

*Table 71: Aging Time Control Register (Page 02h: Address 06h–09h)*

| BIt | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:21 | Reserved | RO | – | – |
| 20 | Age Change | R/W | Age Change Enable.<br>1 = Set age time via bits[19:0].<br>0 = Age time default 300 ns. | 0 |
| 19:0 | AGE_TIME | R/W | Specifies the aging time in seconds for dynamically learned addresses. Maximum age time is 1,048,575 s. Setting the AGE_TIME to 0 disables the aging process. For more information on ARL table aging, see "Address Aging" on page 41. | 300d |

## Mirror Capture Control Register (Page 02h: Address 010h)

*Table 72: Mirror Capture Control Register (Page 02h: Address 010h–011h)*

| BIt | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Mirror Enable | R/W | Global Mirror Enable.<br>0 = Disable L.<br>1 = Enable L. | 0 |
| 14 | BLK_NOT_MIR | R/W | When enabled, all traffic to MIRROR_CAPTURE_PORT is blocked, except for mirror traffic.<br>Nonmirror traffic disable.<br>0 = No traffic blocking on Mirror Capture port.<br>1 = Traffic to Mirror Capture port blocked unless mirror traffic. | 0 |
| 13:6 | Reserved | RO | — | 0 |
| 5:4 | Reserved | R/W | Value must be 0. | 0 |
| 3:0 | Capture Port | R/W | Mirror Capture Port ID.<br>Binary value identifies the single unique port that is designated as the port where all ingress and/or egress traffic is mirrored. | 0 |

For additional information about port mirroring, see "Port Mirroring" on page 31.

# Ingress Mirror Control Register (Page 02h: Address 012h)

*Table 73: Ingress Mirror Control Register (Page 02h: Address 012h–013h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:14 | IN_MIRROR_FILTER | R/W | Ingress Mirror Filter.<br>Filters frames that are to be forwarded to the Mirror Capture port, specified in "Mirror Capture Control Register (Page 02h: Address 010h)" on page 115.<br>00 = Mirror all ingress frames.<br>01 = Mirror all ingress frames with DA = IN_MIRROR_MAC.<br>10 = Mirror all ingress frames with SA = IN_MIRROR_MAC.<br>11 = Reserved.<br>IN_MIRROR_MAC is specified in "Ingress Mirror MAC Address Register (Page 02h: Address 016h)" on page 117. | 0 |
| 13 | IN_DIV_EN | R/W | Ingress Divider Enable.<br>The ingress divider mirrors every $n^{th}$ ingress frame that has passed through the IN_MIRROR_FILTER (n represents the IN_MIRROR_DIV defined in "Ingress Mirror Divider Register (Page 02h: Address 014h)" on page 117).<br>0 = Disable Ingress Divider feature.<br>1 = Enable Ingress Divider feature. | 0 |
| 12:9 | Reserved | R/W | – | 0 |
| 8 | IN_MIRROR_MASK | R/W | Ingress Mirror Port Mask.<br>Bit 8: IMP port.<br>Ports with the corresponding bit set to 1 have ingress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an Ingress Mirror port, severe congestion and/or frame loss may occur if excessive bandwidth from the ingress mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter via bits [15:14] or divider via bit 13 may be helpful. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | IN_MIRROR_MASK | R/W | Ingress Mirror Port Mask.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

For additional information about port mirroring, see "Port Mirroring" on page 31.

# Ingress Mirror Divider Register (Page 02h: Address 014h)

*Table 74: Ingress Mirror Divider Register (Page 02h: Address 014h–015h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:10 | Reserved | RO | – | 0 |
| 9:0 | IN_MIRROR_DIV | R/W | Ingress Mirror Divider.<br>Receive frames that have passed the IN_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the IN_DIV_EN bit in the "Ingress Mirror Control Register (Page 02h: Address 012h)" on page 116 is set, frames that pass the IN_MIRROR_FILTER rule are further divided by n, where n = IN_MIRROR_DIV + 1. | 0 |

For additional information about port mirroring, see "Port Mirroring" on page 31.

# Ingress Mirror MAC Address Register (Page 02h: Address 016h)

*Table 75: Ingress Mirror MAC Address Register (Page 02h: Address 016h–01Bh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:0 | IN_MIRROR_MAC | R/W | Ingress Mirror MAC Address.<br>MAC address that is compared against ingress frames in accordance with the IN_MIRROR_FILTER rules in "Ingress Mirror Control Register (Page 02h: Address 012h)" on page 116. | 0 |

For additional information about port mirroring, see "Port Mirroring" on page 31.

# Egress Mirror Control Register (Page 02h: Address 01Ch)

*Table 76: Egress Mirror Control Register (Page 02h: Address 01Ch–01Dh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:14 | OUT_MIRROR_FILTER | R/W | Egress Mirror Filter.<br>Filters egress frames that are forwarded to the Mirror Capture port, specified in "Mirror Capture Control Register (Page 02h: Address 010h)" on page 115.<br>00 = Mirror all egress frames.<br>01 = Mirror all egress frames with DA = OUT_MIRROR_MAC.<br>10 = Mirror all egress frames with SA = OUT_MIRROR_MAC.<br>11 = Reserved.<br>OUT_MIRROR_MAC is specified in "Egress Mirror MAC Address Register (Page 02h: Address 020h)" on page 119. | 0 |
| 13 | OUT_DIV_EN | R/W | Egress Divider Enable.<br>The Egress Divider mirrors every $n^{th}$ egress frame that has passed through the OUT_MIRROR_FILTER (n represents the OUT_MIRROR_DIV defined in "Egress Mirror Divider Register (Page 02h: Address 01Eh)" on page 119).<br>0 = Disable Egress Divider feature.<br>1 = Enable Egress Divider feature. | 0 |
| 12:8 | Reserved | R/W | – | 0 |
| 8 | OUT_MIRROR_MASK | R/W | Egress Mirror Port Mask.<br>Bit 8: IMP port.<br>Ports with the corresponding bit set to 1 have egress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an Egress Mirror port, severe congestion and/or frame loss may occur if excessive bandwidth from the egress mirrored port(s) is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter via bits[15:14] or a divider via bit 13 may be helpful. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | OUT_MIRROR_MASK | R/W | Egress Mirror Port Mask.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

For additional information about port mirroring, see "Port Mirroring" on page 31.

# Egress Mirror Divider Register (Page 02h: Address 01Eh)

*Table 77: Egress Mirror Divider Register (Page 02h: Address 01Eh–01Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:10 | Reserved | RO | – | 0 |
| 9:0 | OUT_MIRROR_DIV | R/W | Egress Mirror Divider.<br>Egressed frames that have passed the OUT_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the OUT_DIV_EN bit in the "Egress Mirror Control Register (Page 02h: Address 01Ch)" on page 118 is set, frames that pass the OUT_MIRROR_FILTER rule are further divided by n, where n = OUT_MIRROR_DIV + 1. | 0 |

For additional information about port mirroring, see "Port Mirroring" on page 31.

# Egress Mirror MAC Address Register (Page 02h: Address 020h)

*Table 78: Egress Mirror MAC Address Register (Page 02h: Address 020h–025h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:0 | OUT_MIRROR_MAC | R/W | Egress Mirror MAC Address.<br>MAC address that is compared against egress frames in accordance with the OUT_MIRROR_FILTER rules defined in "Egress Mirror Control Register (Page 02h: Address 01Ch)" on page 118. | 0 |

For additional information about port mirroring, see "Port Mirroring" on page 31.

# Page 04h: ARL Control Register

*Table 79: ARL Control Registers (Page 04h)*

| Address | Bits | Register Name |
|---|---|---|
| 00h | 8 | "Global ARL Configuration Register (Page 04h: Address 00h)" on page 120 |
| 01h–03h | – | Reserved |
| 04h–09h | 48 | "BPDU Multicast Address Register (Page 04h: Address 04h)" on page 121 |
| 010h–015h | 48 | "Multiport Address 1 Register (Page 04h: Address 010h)" on page 121 |
| 016h–019h | 32 | "Multiport Vector 1 Register (Page 04h: Address 016h)" on page 122 |
| 01Ah–01Fh | – | Reserved |
| 020h–025h | 48 | "Multiport Address 2 Register (Page 04h: Address 020h)" on page 122 |
| 026h–029h | 32 | "Multiport Vector 2 Register (Page 04h: Address 026h)" on page 123 |
| 02Ah–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

## Global ARL Configuration Register (Page 04h: Address 00h)

*Table 80: Global ARL Configuration Register (Page 04h: Address 00h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:5 | Reserved | RO | – | 0 |
| 4 | Multiport Address | R/W | Multiport Address Enable.<br>When set by the host, enables multiport addressing.<br>Note that if only one multiport address is required, the host should write both multiport address/vector entries to the same value.<br>0 = Disable multiport address registers.<br>1 = Enable multiport address registers.<br>See "Using the Multiport Addresses" on page 42 for more information. | 0 |
| 3:1 | Reserved | RO | – | – |

*Table 80: Global ARL Configuration Register (Page 04h: Address 00h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 0 | Hash Disable | R/W | Hash Function Disable.<br>Disables the hash function of the ARL table so that entries are directly mapped to the table, instead of being hashed to an index.<br>1 = Disable hash function.<br>0 = Enable hash function.<br>For more information see "Address Table Organization" on page 34. | 0 |

## BPDU Multicast Address Register (Page 04h: Address 04h)

*Table 81: BPDU Multicast Address Register (Page 04h: Address 04h-09h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:0 | BPDU_MC_ADDR | R/W | BPDU Multicast Address 1.<br>Defaults to the IEEE 802.1 defined reserved multicast address for the bridge group address. Programming to an alternate value allows support of proprietary protocols in place of the normal spanning tree protocol. Frames with a matching DA to this address are forwarded to the designated management port. | 01-80-c2-00-00-00 |

## Multiport Address 1 Register (Page 04h: Address 010h)

*Table 82: Multiport Address 1 Register (Page 04h: Address 010h–015h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:0 | MPORT_ADDR_1 | R/W | Multiport Address 1.<br>48-bit MAC Address. Allows frames with a matching destination address to be forwarded to any programmable group of ports, as defined in the bit map in the "Multiport Vector 1 Register (Page 04h: Address 016h)" on page 122.<br>Must be enabled using the MPORT_ADDR_EN bit in the "Global ARL Configuration Register (Page 04h: Address 00h)" on page 120.<br>See "Using the Multiport Addresses" on page 42 for more information. | 0 |

# Multiport Vector 1 Register (Page 04h: Address 016h)

*Table 83: Multiport Vector 1 Register (Page 04h: Address 016h–019h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:9 | Reserved | RO | – | 0 |
| 8 | MPORT_VCTR_1 | R/W | Multiport Vector 1.<br>Bit 8: IMP port.<br>Ports with the corresponding bit set to 1 are forwarded to all frames with a destination address matching that of the "Multiport Address 1 Register (Page 04h: Address 010h)" on page 121.<br>See "Using the Multiport Addresses" on page 42 for more information. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | MPORT_VCTR_1 | R/W | Multiport Vector 1.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

# Multiport Address 2 Register (Page 04h: Address 020h)

*Table 84: Multiport Address 2 Register (Page 04h: Address 020h–025h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:0 | MPORT_ADDR_2 | R/W | Multiport Address 2.<br>48-bit MAC Address. Allows frames with a matching destination address to be forwarded to any programmable group of ports, as defined in the bit map in the "Multiport Vector 2 Register (Page 04h: Address 026h)" on page 123.<br>Must be enabled using the MPORT_ADDR_EN bit in the "Global ARL Configuration Register (Page 04h: Address 00h)" on page 120.<br>See "Using the Multiport Addresses" on page 42 for more information. | 0 |

# Multiport Vector 2 Register (Page 04h: Address 026h)

*Table 85: Multiport Vector 2 Register (Page 04h: Address 026h–029h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:9 | Reserved | RO | – | 0 |
| 8 | MPORT_VCTR_2 | R/W | Multiport Vector 2.<br>Bit 8: IMP port<br>Ports with the corresponding bit set to 1 are forwarded to all frames with a destination address matching that of the "Multiport Address 2 Register (Page 04h: Address 020h)" on page 122.<br>See "Using the Multiport Addresses" on page 42 for more information. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 8:0 | MPORT_VCTR_2 | R/W | Multiport Vector 2.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

# Page 05h: ARL/VTBL Access Registers

*Table 86: ARL/VTBL Access Registers (Page 05h)*

| Address | Bits | Register Name |
|---|---|---|
| 00h | 8 | "ARL Table Read/Write Control Register (Page 05h: Address 00h)" on page 125 |
| 01h–0Fh | – | Reserved |
| 02h–07h | 48 | "MAC Address Index Register (Page 05h: Address 02h)" on page 125 |
| 08h–09h | 16 | "VLAN ID Index Register (Page 05h: Address 08h)" on page 126 |
| 0Ah–0Fh | – | Reserved |
| 010h–017h | 64 | "ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h)" on page 126 |
| 018h–019h | 16 | "ARL Table Data Entry 0 Register (Page 05h: Address 018h)" on page 127 |
| 01Ah–01Fh | – | Reserved |
| 020h–027h | 64 | "ARL Table MAC/VID Entry 1 Register (Page 05h: Address 20h)" on page 128 |
| 028h–029h | 16 | "ARL Table Data Entry 1 Register (Page 05h: Address 028h)" on page 129 |
| 030h | 8 | "ARL Table Search Control Register (Page 05h: Address 030h)" on page 130 |
| 031h–032h | – | Reserved |
| 033h–03Ah | 64 | "ARL Table Search MAC/VID Result Register (Page 05h: Address 033h)" on page 131 |
| 03Bh–03Ch | 16 | "ARL Table Search Data Result Register (Page 05h: Address 03Bh)" on page 132 |
| 03Dh–05Fh | – | Reserved |
| 060h | 8 | "VLAN Table Read/Write Control Register (Page 05h: Address 060h)" on page 133 |
| 061h–062h | 16 | "VLAN Table Address Index Register (Page 05h: Address 061h)" on page 134 |
| 063h–066h | 32 | "VLAN Table Entry Register (Page 05h: Address 063h)" on page 134 |
| 067h–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

# ARL Table Read/Write Control Register (Page 05h: Address 00h)

*Table 87: ARL Table Read/Write Control Register (Page 05h: Address 00h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | START/DONE | R/W (SC) | Start/Done Command.<br>Write as 1 to initiate a read/write command to the ARL table. The bit returns to 0 to indicate that a read/write operation is complete. | 0 |
| 6:1 | Reserved | RO | – | – |
| 0 | ARL_R/W | R/W | ARL Table Read/Write Bit.<br>Specifies whether the ARL command is a read or write operation.<br>1 = Read<br>0 = Write | 0 |

For more information, see "Accessing the ARL Table Entries" on page 39.

# MAC Address Index Register (Page 05h: Address 02h)

*Table 88: MAC Address Index Register (Page 05h: Address 02h–07h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:0 | MAC_ADDR_INDX | R/W | MAC Address Index.<br>The ARL table read/write command uses this 48-bit address to index the ARL table. When IEEE 802.1Q is enabled, the ARL table is indexed by a combined hash of the MAC_ADDR_INDX and the VID_TBL_INDX, defined in the "VLAN ID Index Register (Page 05h: Address 08h)" on page 126.<br>For more information, see "Accessing the ARL Table Entries" on page 39. | 0 |

# VLAN ID Index Register (Page 05h: Address 08h)

*Table 89: VLAN ID Index Register (Page 05h: Address 08h–09h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:12 | Reserved | R/W | – | 0 |
| 11:0 | VID_INDX | R/W | VLAN ID Index.<br>When IEEE 802.1Q is enabled, the VLAN ID Index is used with the MAC_ADDR_INDX, defined in the "MAC Address Index Register (Page 05h: Address 02h)" on page 125, to form the hash index for which status is to be read or written.<br>For more information, see "Accessing the ARL Table Entries" on page 39. | 0 |

# ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h)

*Table 90: ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h–017h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 63:60 | Reserved | RO | – | 0 |
| 59:48 | VID0 | R/W | VID Entry 0.<br>The VID field is either read from or written to the ARL table entry 0. The VID is a "don't-care" field when IEEE 802.1Q is disabled. | 0 |
| 47:0 | MACADDR0 | R/W | MAC Address Entry 0.<br>The 48-bit MAC Address field to be either read from or written to the ARL table entry 0. | 0 |

**Note:** Together, the "ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h)" on page 126 and the "ARL Table Data Entry 0 Register (Page 05h: Address 018h)" on page 127 compose a complete entry in the ARL table. For more information, see "Accessing the ARL Table Entries" on page 39.

# ARL Table Data Entry 0 Register (Page 05h: Address 018h)

*Table 91: ARL Table Data Entry 0 Register (Page 05h: Address 018h–019h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | VALID0 | R/W | Valid Bit Entry 0.<br>Write this bit to 1 to indicate that a valid MAC address is stored in the MACADDR0 field defined in the "ARL Table MAC/VID Entry 0 Register (Page 05h: Address 010h)" on page 126 and that the entry has not aged out. Reset when an entry is empty.<br>This information is read from or written to the ARL table during a read/write command. | 0 |
| 14 | STATIC0 | R/W | Static Bit Entry 0.<br>Write this bit to 1 to indicate that the entry is controlled by the external register control. When cleared, the internal learning and aging process controls the validity of the entry.<br>This information is read from or written to the ARL table during a read/write command. | 0 |
| 13 | AGE0 | R/W | Age Bit Entry 0.<br>Write this bit to 1 to indicate that an address entry has been learned or accessed. This bit is set to 0 by the internal aging algorithm. If the internal aging process detects a valid entry has remained unused for the period set by the AGE_TIME (defined in the "Aging Time Control Register (Page 02h: Address 06h)" on page 115) and the entry has not been marked as Static, the entry has the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.<br>This information is read from or written to the ARL table during a read/write command. | 0 |
| 12:10 | PRIORITY0 | R/W | Priority Bit for MAC-Based QoS Entry 0.<br>These bits define the priority field for MAC-based QoS packets.<br>This information is read from or written to the ARL table during a read/write command. | 0 |
| 9 | Reserved | R/W | — | – |

*Table 91: ARL Table Data Entry 0 Register (Page 05h: Address 018h–019h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 8:4 | FWD_PRT_MAP0 | R/W | Forward Port Map Entry 0.<br>For multicast entries, these bits define the forward port map. These bits and bits[3:0] compose the entire port map.<br>Bit 4: Port 4.<br>Bits[7:5]: Reserved.<br>Bit 8: IMP port.<br>For unicast entries, these bits are reserved.<br>This information is read from or written to the ARL table during a read/write command. | 00h |
| 3:0 | FWD_PRT_MAP0 | R/W | Forward Port Map Entry 0.<br>For multicast entries, these bits define the forward port map. These bits and bits[8:4] compose the entire port map.<br>Bits[3:0] correspond to ports [3:0], respectively. | 0 |
| | PORTID0 | R/W | Port Identification Entry 0.<br>For unicast entries, these bits define the port number associated with the entry of the ARL table.<br>This information is read from or written to the ARL table during a read/write command. | – |

# ARL Table MAC/VID Entry 1 Register (Page 05h: Address 20h)

*Table 92: ARL Table MAC/VID Entry 1 Register (Page 05h: Address 20h–27h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 63:60 | Reserved | RO | — | 0 |
| 59:48 | VID1 | R/W | VID Entry 1.<br>The VID field to be either read from or written to the ARL table entry 0. The VID is a don't-care field when IEEE 802.1Q is disabled. | 0 |
| 47:0 | MACADDR1 | R/W | MAC Address Entry 1.<br>The 48-bit MAC Address field to be either read from or written to the ARL table entry 1. | 0 |

**Note:** Together, the "ARL Table MAC/VID Entry 1 Register (Page 05h: Address 20h)" on page 128 and the "ARL Table Data Entry 1 Register (Page 05h: Address 028h)" on page 129 compose a complete entry in the ARL table. For more information, see "Accessing the ARL Table Entries" on page 39.

# ARL Table Data Entry 1 Register (Page 05h: Address 028h)

*Table 93: ARL Table Data Entry 1 Register (Page 05h: Address 028h–029h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | VALID1 | R/W | Valid Bit Entry 1.<br>Write this bit to 1 to indicate that a valid MAC address is stored in the MACADDR0 field defined in the "ARL Table MAC/VID Entry 1 Register (Page 05h: Address 20h)" on page 128 and that the entry has not aged out. Reset when an entry is empty.<br>This information is read from or written to the ARL table during a read/write command. | 0 |
| 14 | STATIC1 | R/W | Static Bit Entry 1.<br>Write this bit to 1 to indicate that the entry is controlled by the external register control. When cleared, the internal learning and aging process controls the validity of the entry.<br>This information is read from or written to the ARL table during a read/write command. | 0 |
| 13 | AGE1 | R/W | Age Bit Entry 1.<br>Write this bit to 1 to indicate that an address entry has been learned or accessed. This bit is set to 0 by the internal aging algorithm. If the internal aging process detects a valid entry has remained unused for the period set by the AGE_TIME (defined in the "Aging Time Control Register (Page 02h: Address 06h)" on page 115) and the entry has not been marked as Static, the entry has the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.<br>This information is read from or written to the ARL table during a read/write command. | 0 |
| 12:10 | PRIORITY1 | R/W | Priority Bit for MAC-Based QoS entry 1.<br>These bits define the priority field for MAC-based QoS packets.<br>This information is read from or written to the ARL table during a read/write command. | 0 |
| 9 | Reserved | R/W | — | – |
| 8:4 | FWD_PRT_MAP 1 | R/W | Forward Port Map Entry 1.<br>For multicast entries, these bits define the forward port map. These bits and bits[3:0] compose the entire port map.<br>Bit 4: Port 4.<br>Bits[7:5]: Reserved.<br>Bit 8: IMP port.<br>For unicast entries, these bits are reserved.<br>This information is read from or written to the ARL table during a read/write command. | 00h |

*Table 93: ARL Table Data Entry 1 Register (Page 05h: Address 028h–029h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 3:0 | FWD_PRT_MAP 1 | R/W | Forward Port Map Entry 1.<br>For multicast entries: these bits define the forward port map. These bits and bits[8:4] compose the entire port map.<br>Bits[3:0] correspond to ports [3:0], respectively. | 0 |
| | PORTID1 | R/W | Port Identification Entry 1.<br>For unicast entries: these bits define the port number associated with the entry of the ARL table.<br>This information is read from or written to the ARL table during a read/write command. | 0h |

## ARL Table Search Control Register (Page 05h: Address 030h)

*Table 94: ARL Table Search Control Register (Page 05h: Address 030h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | START/DONE | R/W (SC) | Start/Done.<br>Write as 1 to initiate a sequential search of the ARL table. Each entry found by the search is returned to the "ARL Table Search Data Result Register (Page 05h: Address 03Bh)" on page 132 and the "ARL Table Search MAC/VID Result Register (Page 05h: Address 033h)" on page 131. Reading the "ARL Table Search Data Result Register (Page 05h: Address 03Bh)" on page 132 allows the ARL table search to continue. The BCM5387 clears this bit when the ARL table search is complete. | 0 |
| 6:1 | Reserved | RO | — | 0 |
| 0 | ARL_SR_VALID | RC | ARL Search Result Valid.<br>Set by the BCM5387 to indicate that an ARL entry is found by the ARL table search. The found entry is available in the "ARL Table Search Data Result Register (Page 05h: Address 03Bh)" on page 132. This bit automatically returns to 0 after the ARL Search Result register is read. | 0 |

For more information, see "Accessing the ARL Table Entries" on page 39.

# ARL Search Address Register (Page 05h: Address 031h)

*Table 95: ARL Search Address Register (Page 05h: Address 031h–302h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | ARL_ADDR_VALID | R/W (SC) | ARL Address Valid.<br>Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry that is currently being accessed. Intended for factory test/diagnostic use only. | 0 |
| 14:0 | ARL_ADDR | | ARL Address.<br>14-bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location.Intended for factory test/ diagnostic use only. | 0 |

# ARL Table Search MAC/VID Result Register (Page 05h: Address 033h)

*Table 96: ARL Table Search MAC/VID Result Register (Page 05h: Address 033h–03Ah)*

| BIt | Name | R/W | Description | Default |
|---|---|---|---|---|
| 63:60 | Reserved | RO | — | 0 |
| 59:48 | ARL_SR_VID | RO | ARL Search VID Result.<br>These bits store the VID of the ARL table entry found by the ARL Table Search function. | 0 |
| 47:0 | ARL_SR_MAC | RO | ARL Search MAC Address Result.<br>These bits store the MAC address of the ARL table entry found by the ARL Table Search function. | 0 |

For more information, see “Accessing the ARL Table Entries” on page 39.

# ARL Table Search Data Result Register (Page 05h: Address 03Bh)

*Table 97: ARL Table Search Data Result Register (Page 05h: Address 03Bh–03Ch)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | ARL_SR_VALID | RO | ARL Search Valid Bit Result.<br>This bit stores the Valid bit of the ARL table entry found by the ARL Table Search function. Reading this register clears the data from the register and allows the ARL Table Search function to continue searching. | 0 |
| 14 | ARL_SR_STATIC | RO | ARL Search Static Bit Result.<br>This bit stores the Static bit of the ARL table entry found by the ARL Table Search function. Reading this register clears the data from the register and allows the ARL Table Search function to continue searching. | 0 |
| 13 | ARL_SR_AGE | RO | ARL Search Age Bit Result.<br>This bit stores the Age bit of the ARL table entry found by the ARL Table Search function. Reading this register clears the data from the register and allows the ARL Table Search function to continue searching. | 0 |
| 12:10 | ARL_SR_PRI | RO | ARL Search Priority Bits Result.<br>These bits store the priority bits of the ARL table entry found by the ARL Table Search function. Reading this register clears the data from the register and allows the ARL Table Search function to continue searching. | 0 |
| 9 | Reserved | RO | — | 0 |
| 8:4 | FWD_PRT_MAP | R/W | Forward Port Map Entry.<br>For multicast entries, these bits define the forward port map. These bits and bits[3:0] compose the entire port map.<br>Bit 4: Port 4.<br>Bits[7:5]: Reserved.<br>Bit 8: IMP port.<br>For unicast entries, these bits are reserved.<br>This information is read from or written to the ARL table during a read/write command. | 00h |

*Table 97: ARL Table Search Data Result Register (Page 05h: Address 03Bh–03Ch) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 3:0 | FWD_PRT_MAP | R/W | Forward Port Map Entry.<br>For multicast entries: these bits define the forward port map. These bits and bits[8:4] compose the entire port map.<br>Bits[3:0] correspond to ports [3:0], respectively. | 0 |
| | PORTID | R/W | Port Identification Entry.<br>For unicast entries: these bits define the port number associated with the entry of the ARL table.<br>This information is read from or written to the ARL table during a read/write command. | |

For more information, see "Accessing the ARL Table Entries" on page 39.

# VLAN Table Read/Write Control Register (Page 05h: Address 060h)

*Table 98: VLAN Table Read/Write Control Register (Page 05h: Address 060h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | START/DONE | R/W (SC) | Start/Done Command.<br>Write as 1 to initiate a read/write command to the VLAN table. The bit returns to 0 to indicate that the read/write operation is complete. | 0 |
| 6:1 | Reserved | RO | – | – |
| 0 | VTBL_R/W | R/W | VTBL Read/Write.<br>Specifies whether the current VLAN table read/write command is a read or write operation.<br>1 = Read.<br>0 = Write. | 0 |

See "Programming the VLAN Table" on page 27 for more information.

# VLAN Table Address Index Register (Page 05h: Address 061h)

*Table 99: VLAN Table Address Index Register (Page 05h: Address 061h–062h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:12 | Reserved | RO | — | 0 |
| 11:0 | VTBL_ADDR_INDX | R/W | VLAN Table Address Index.<br>The current VLAN table read/write uses this 12-bit address to index the VLAN table. | – |

See "Programming the VLAN Table" on page 27 for more information.

# VLAN Table Entry Register (Page 05h: Address 063h)

*Table 100: VLAN Table Entry Register (Page 05h: Address 063h–066h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:19 | Reserved | RO | — | 0 |
| 18 | VALID | R/W | VLAN Table VALID Bit.<br>This bit is written 1 to indicate that a valid VLAN entry is stored in the VLAN table.<br>This bit is a part of the VLAN table entry that is written/read to the VLAN table. | 0 |
| 17 | UNTAG_MAP | R/W | Untagged Port Map.<br>Bit 17: IMP port.<br>Ports written to 1 are designated as untagged VLAN ports. VLAN-tagged frames destined for these ports are untagged before they are forwarded.<br>**Note**: When the IEEE 802.1Q feature is enabled, frames sent via the CPU shall be tagged. | 0 |
| 16:14 | Reserved | RO | – | 0 |
| 13:9 | UNTAG_MAP | R/W | Untagged Port Map.<br>Bits[13:9] correspond to ports [4:0], respectively. | 0 |
| 8 | FWD_MAP | R/W | Forward Port Map.<br>Bit 8: IMP port.<br>Ports written to 1 are designated as capable of receiving VLAN-tagged frames. | 0 |
| 7:5 | Reserved | RO | – | 0 |
| 4:0 | FWD_MAP | R/W | Forward Port Map.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

See "Programming the VLAN Table" on page 27 for more information.

# Page 010h–017h: Internal Serial Port Registers

**Note:** These registers correspond to the configuration of the internal Serdes transceiver. These registers can be read/written via SPI or EEPROM. Alternatively, these registers can be read/written via MDC/MDIO slave mode. When accessed via slave mode, the internal Serdes ports have a PHY address corresponding to their port number. Each register is accessed via the MDC/MDIO register address specified in the table below.

*Table 101: Internal Serial Port Page Summary*

| Page | Description |
|---|---|
| 010h | Port 0 |
| 011h | Port 1 |
| 012h | Port 2 |
| 013h | Port 3 |
| 014h | Port 4 |
| 015h | Reserved |
| 016h | Reserved |
| 017h | Reserved |

*Table 102: Internal Serial Port Registers (Page 010h–017h)*

| MCD/MDIO Register Address | SPI Register Address | Bits | IEEE Register Name |
|---|---|---|---|
| 00h | 00h–01h | 16 | "MII Control Register (Page 010h-017h: Address 00h)" on page 137 |
| 01h | 02h–03h | 16 | "MII Status Register (Page 010h-017h: Address 02h)" on page 138 |
| 02h–03h | 04h–07h | – | Reserved |
| 04h | 08h–09h | 16 | "Auto-Negotiation Advertisement Register (Page 010h-017h: Address 08h)" on page 139 |
| 05h | 0Ah–0Bh | 16 | "Auto-Negotiation Link Partner Ability Register (Page 010h-017h: Address 0Ah)" on page 140 |
| 06h | 0Ch–0Dh | 16 | "Auto-Negotiation Expansion Register (Page 010h-017h: Address 0Ch)" on page 141 |
| 07h-0Eh | 0Eh–01Dh | – | Reserved |
| 0Fh | 01Eh–01Fh | 16 | "Extended Status Register (Page 010h-017h: Address 01Eh)" on page 142 |
| 010h | 020h–021h | 16 | • "SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h, Block 0)" on page 142<br>• "Analog Transmit Register (Page 010h-017h: Address 020h, Block 1)" on page 144 |

*Table 102: Internal Serial Port Registers (Page 010h–017h) (Cont.)*

| MCD/MDIO Register Address | SPI Register Address | Bits | IEEE Register Name |
|---|---|---|---|
| 011h | 022h–023h | 16 | "SerDes/SGMII Control 2 Register (Page 010h-017h: Address 022h)" on page 144 |
| 012h | 024h–025h | 16 | "SerDes/SGMII Control 3 Register (Page 010h-017h: Address 024h)" on page 145 |
| 013h | 026h–027h | – | Reserved |
| 014h | 028h–029h | 16 | "SerDes/SGMII Status 1 Register (Page 010h-017h: Address 028h)" on page 146 |
| 015h | 02Ah–02Bh | 16 | "SerDes/SGMII Status 2 Register (Page 010h-017h: Address 02Ah)" on page 147 |
| 016h | 02Ch–02Dh | 16 | "SerDes/SGMII Status 3 Register (Page 010h-017h: Address 02Ch)" on page 148 |
| 017h | 02Eh–02Fh | 16 | "BER/CRC Error Counter Register (Page 010h-017h: Address 02Eh)" on page 149 |
| 018h | 030h-031h | 16 | "PRBS Control Register (Page 010h-017h: Address 030h)" on page 149 |
| 019h | 032h-033h | 16 | "PRBS Status Register (Page 010h-017h: Address 032h)" on page 150 |
| 01Ah | 034h-035h | 16 | "Pattern Generator Control Register (Page 010h-017h: Address 034h)" on page 150 |
| 01Bh | 036h-037h | 16 | "Pattern Generator Status Register (Page 010h-017h: Address 036h)" on page 152 |
| 1Ah | 38h-39h | – | Reserved |
| 01Ch | 03Ah-03Bh | 16 | "Force Transmit 1 Register (Page 010h-017h: Address 03Ah)" on page 152 |
| 01Dh | 03Ch-03Dh | 16 | "Force Transmit 2 Register (Page 010h-017h: Address 03Ch)" on page 152 |
| 01Eh | 03Eh-3Fh | 16 | "Block Address Number (Page 010h-017h: Address 03Eh)" on page 153 |
| – | 40h-EFh | – | Reserved |
| – | 0F0h–0F7h | 64 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| – | 0F8h–0FDh | – | Reserved |
| – | 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| – | 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

# MII Control Register (Page 010h-017h: Address 00h)

*Table 103: MII Control Register (Page 010h-017h: Address 00h-01h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reset | R/W | SerDes/SGMII Port Reset.<br>0 = Normal operation.<br>1 = Port reset. | 0 |
| 14 | Internal Loopback | R/W | Loopback Enable.<br>0 = Normal operation.<br>1 = Loopback enable. | 0 |
| 13 | Speed Selection (LSB) | R/W | Speed Select Bits [6, 13]<br>1X = 1000 Mbps.<br>01 = 100 Mbps.<br>00 = 10 Mbps.<br>Used in SGMII Mode only. Ignored when in SerDes Mode. | 0 |
| 12 | Auto-Neg Enable | R/W | Auto-negotiation Enable (AN).<br>0 = Disable.<br>1 = Enable AN. | 1 |
| 11 | Powerdown | R/W | Power Down Enable.<br>Powerdown will disable the port conserving power consumption. MDC/MDIO and SPI access is still available.<br>0 = Normal operation.<br>1 = Low-power mode enable. | 0 |
| 10 | Reserved | RO | Reserved. Write 0, ignore read. | 0 |
| 9 | Restart Autoneg | R/W | Restart AN.<br>0 = Normal operation.<br>1 = Restart the AN process. | 0 |
| 8 | Duplex | R/W | Full-duplex.<br>0 = Half-duplex.<br>1 = Full-duplex. | 1 |
| 7 | Collision Test Enable | R/W | Collision Test Enable.<br>0 = Normal operation.<br>1 = Collision test mode enable. | 0 |
| 6 | Speed Selection (MSB) | R/W | Speed Select Bits [6, 13]<br>1X = 1000 Mbps.<br>01 = 100 Mbps.<br>00 = 10 Mbps.<br>Used in SGMII Mode only. Ignored when in SerDes Mode. | 1 |
| 5:0 | Reserved | RO | Reserved. Write 0, ignore read. | 00 |

# MII Status Register (Page 010h-017h: Address 02h)

*Table 104: MII Status Register (Page 010h-017h: Address 02h-03h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | 100BASE-T4 Capable | RO | 0 = Not capable.<br>1 = 100BASE-T4 capable. | 0 |
| 14 | 100BASE-X Full-duplex Capable | RO | 0 = Not capable.<br>1 = 100BASE-X full-duplex capable. | 0 |
| 13 | 100BASE-X Half-duplex Capable | RO | 0 = Not capable.<br>1 = 100BASE-X half-duplex capable. | 0 |
| 12 | 10BASE-T Full-duplex Capable | RO | 0 = Not capable.<br>1 = 10BASE-T full-duplex capable. | 0 |
| 11 | 10BASE-T Half-duplex Capable | RO | 0 = Not capable.<br>1 = 10BASE-T half-duplex capable. | 0 |
| 10 | 100BASE-T2 Full-duplex Capable | RO | 0 = Not capable.<br>1 = 100BASE-T2 full-duplex capable. | 0 |
| 9 | 100BASE-T2 Half-duplex Capable | RO | 0 = Not capable.<br>1 = 100BASE-T2 half-duplex capable. | 0 |
| 8 | Extended Status | RO | 0 = No extended status.<br>1 = Extended status in register 0F. | 1 |
| 7 | Reserved | RO | Reserved. Write 0, ignore read. | 0 |
| 6 | Management Frames Preamble Suppression | RO | 0 = PHY does not accept management frames with preamble suppressed.<br>1 = PHY accepts management frames with preamble suppressed. | 1 |
| 5 | Auto-negotiation Complete | RO | Auto-negotiation complete.<br>0 = Not done.<br>1 = AN complete. | 0 |
| 4 | Remote Fault | RO | Remote Fault.<br>0 = No fault detected.<br>1 = Remote fault detected. | 0 |
| 3 | Auto-negotiation Ability | RO | Auto-negotiation Ability.<br>0 = Not capable of AN.<br>1 = AN capable. | 1 |
| 2 | Link Status | ROLL | Link Status.<br>0 = Link fail since last read.<br>1 = No link fail since last read. | 0 |
| 1 | Jabber Detect | RO | Jabber Detect.<br>0 = Not detected.<br>1 = Jabber detected. | 0 |

*Table 104: MII Status Register (Page 010h-017h: Address 02h-03h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 0 | Extended Capability | RO | Extended Capability.<br>0 = Supports basic register set only.<br>1 = Extended register capabilities supported. | 1 |

# Auto-Negotiation Advertisement Register (Page 010h-017h: Address 08h)

*Table 105: Auto-Negotiation Advertisement Register (Page 010h-017h: Address 08h-09h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Next Page | RO | Next page.<br>1 = Next page ability supported<br>0 = Next page ability not supported | 0 |
| 14 | Reserved | RO | Reserved. Write 0, ignore read. | 0 |
| 13:12 | Remote Fault | R/W | Remote Fault.<br>00 = No fault.<br>01 = Link failure.<br>10 = Offline.<br>11 = AN error. | 00 |
| 11:9 | Reserved | RO | Reserved. Write 0, ignore read. | 000 |
| 8:7 | Pause Capable | R/W | Pause.<br>00 = No pause.<br>01 = Symmetric pause.<br>10 = Asymmetric pause towards link partner.<br>11 = Both symmetric and asymmetric pause towards local device. | 11 |
| 6 | Half-duplex Capable | R/W | Half-duplex.<br>0 = Do not advertise half-duplex.<br>1 = Advertise half-duplex. | 1 |
| 5 | Full-duplex Capable | R/W | Full-duplex.<br>0 = Do not advertise full-duplex.<br>1 = Advertise full-duplex. | 1 |
| 4:0 | Reserved | RO | Reserved. Write 0, ignore read. | 00 |

# Auto-Negotiation Link Partner Ability Register (Page 010h-017h: Address 0Ah)

*Table 106: Auto-Negotiation Link Partner Ability Register (Page 010h-017h: Address 0Ah-0Bh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Next Page/Link | RO | When link partner configured to SerDes mode (bit 0 = 0):<br>1 = Link partner is next page capable.<br>0 = Link partner is not next page capable.<br>When link partner configured to SGMII mode (bit 0 = 1).<br>1 = Link.<br>0 = No link. | 0 |
| 14 | Acknowledge | RO | Reserved. Write 0, ignore read. | 0 |
| 13:12 | Remote Fault/ Duplex | RO | When link partner configured to SerDes mode (bit 0 = 0), these bits indicate advertised remote fault setting of link partner:<br>00 = No Fault.<br>01 = Link failure.<br>10 = Offline.<br>11 = AN error.<br>When link partner configured to SGMII mode (bit 0 = 1), these bits indicate advertised duplex of link partner:<br>x1 = Full-duplex.<br>x0 = Half-duplex. | 00 |
| 11:10 | Speed | | When link partner configured to SerDes mode (bit 0 = 0), these bits are reserved.<br>When link partner configured to SGMII mode (bit 0 = 1), indicates advertised link speed of link partner:<br>1x = 1000M.<br>01 = 100M.<br>00 = 10M. | 00 |
| 9 | Reserved | RO | Reserved. Write 0, ignore read. | 0 |
| 8:7 | Pause Capable | RO | When link partner configured to SerDes mode (bit 0 = 0), indicates link partner pause capabilities:<br>00 = No pause.<br>01 = Symmetric pause.<br>10 = Asymmetric pause towards link partner.<br>11 = Both symmetric and asymmetric pause towards local device.<br><br>When link partner configured to SGMII mode (bit 0 = 1), these bits are reserved. | 0 |

*Table 106: Auto-Negotiation Link Partner Ability Register (Page 010h-017h: Address 0Ah-0Bh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 6 | Half-duplex Capable | RO | When link partner configured to SerDes mode (bit 0 = 0), indicates link partner advertised half-duplex capability:<br>0 = Not half-duplex capable.<br>1 = half-duplex capable.<br><br>When link partner configured to SGMII mode (bit 0 = 1), this bit is reserved. | 0 |
| 5 | Full-duplex Capable | RO | When link partner configured to SerDes mode (bit 0 = 0), indicates link partner advertised full-duplex capability:<br>0 = Not full-duplex capable.<br>1 = Full-duplex capable.<br><br>When link partner configured to SGMII mode (bit 0 = 1), this bit is reserved. | 0 |
| 4:1 | Reserved | RO | Reserved. Write 0, ignore read. | 0 |
| 0 | Serial Mode | RO | SGMII mode.<br>Indicates SerDes/SGMII link partner configuration.<br>0 = SerDes mode.<br>1 = SGMII mode. | 0 |

# Auto-Negotiation Expansion Register (Page 010h-017h: Address 0Ch)

*Table 107: Auto-Negotiation Expansion Register (Page 010h-017h: Address 0Ch-0Dh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:3 | Reserved | RO | Reserved. Write 0, ignore read. | 0000 |
| 2 | Next Page Capable | RO | Next Page Ability.<br>0 = Local device is not next-page able.<br>1 = Local device is next-page able. | 0 |
| 1 | Page Received | RO | Page Received.<br>0 = New link code word has not been received.<br>1 = New link code word has been received. | 0 |
| 0 | Reserved | RO | Reserved. Write 0, ignore read. | 0 |

# Extended Status Register (Page 010h-017h: Address 01Eh)

*Table 108: Extended Status Register (Page 010h-017h: Address 01Eh-01Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | 1000BASE-X Full-duplex Capable | RO | 0 = Not capable.<br>1 = 1000BASE-X full-duplex capable. | 1 |
| 14 | 1000BASE-X Half-duplex Capable | RO | 0 = Not capable.<br>1 = 1000BASE-X half-duplex capable. | 1 |
| 13 | 1000BASE-T Full-duplex Capable | RO | 0 = Not capable.<br>1 = 1000BASE-T full-duplex capable. | 0 |
| 12 | 1000BASE-T Half-duplex Capable | RO | 0 = Not capable.<br>1 = 1000BASE-T half-duplex capable. | 0 |
| 11:0 | Reserved | RO | Reserved. Write 0, ignore read. | 000 |

# SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h, Block 0)

*Table 109: SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h-021h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | RO | Reserved. Write 0, ignore read. | 0 |
| 14 | Signal Detect Filter | R/W | Filtering the Signal Detect pin adds hysteresis to the signal to stabilize the readings near the threshold. The status of resulting signal detect, regardless of whether the filter is active, is recorded via "SerDes/SGMII Status 3 Register (Page 010h-017h: Address 02Ch)" on page 148, bit 9.<br>0 = Filter signal detect from pin before using for synchronization.<br>1 = Disable filter for signal detect. | 0 |
| 13 | Global Write | R/W | MDC/MDIO commands addressed to PHYAD 00 will affect all ports that have the Global Write enabled.<br>0 = Normal operation.<br>1 = Global Write Enabled. | 0 |
| 12 | SerDes TX Amplitude Override | R/W | 1 = Override SerDes transmit amplitude from Block 1, Register 20h bit 14. Bits[15:12] program transmit amplitude.<br>0 = Normal operation. Block 1, Register 20h bit 14 internally set based on SGMII or Serdes mode. | 0 |

*Table 109: SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h-021h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 11 | Counter Select | R/W | Error Counter Register Definition<br>Configures the type of events counted in "BER/CRC Error Counter Register (Page 010h-017h: Address 02Eh)" on page 149.<br>0 = Select CRC errors.<br>1 = Select received packets. | 0 |
| 10 | Remote Loopback | R/W | Remote loopback operates in all available speeds.<br>0 = Normal operation.<br>1 = Enable remote loopback. | 0 |
| 9 | Reserved | R/W | Write as 0, ignore on read. | 0 |
| 8 | Comma Detection | R/W | 0 = Disable comma detection.<br>1 = Enable comma detection. | 1 |
| 7 | CRC Checker | R/W | 0 = Enable CRC checker.<br>1 = Disable CRC checker. | 1 |
| 6 | Reserved | R/W | Write as 0, ignore on read | 0 |
| 5 | SGMII Master | R/W | This bit configures the port to operate in Master mode (typical of PHY device) to allow testing link conditions between two switch ports.<br>0 = Normal operation.<br>1 = SGMII mode operates in Master (PHY) mode. If auto-negotiation is enabled, then the local device sends out the following auto-negotiation code word.<br>[15] = 1.<br>[14] = ACK.<br>[13] = 0.<br>[12] = Register 0, Bit 8.<br>[11] = Register 0, Bit 6.<br>[10] = Register 0, Bit 13.<br>[9:0] = 0000000001. | 0 |
| 4 | Autodetect Enable | R/W | 0 = Disable auto-detection (SerDes or SGMII mode is set according to bit 0 of this register).<br>1 = Enable auto-detection (SerDes and SGMII mode switches each time an auto-negotiation page is received with the wrong selector field in bit 0.) | 1 |
| 3 | Signal Detect Inversion | R/W | 0 = Use signal detect from pin.<br>1 = Invert signal detect from pin. | 0 |
| 2 | Signal Detect Enable | R/W | 0 = Ignore signal detect from pin.<br>1 = Signal detect from pin must be set to achieve synchronization. In SGMII the signal detect is always ignored, regardless of the setting of this bit. | 0 |
| 1 | Reserved | R/W | Write as 0, ignore on read | 0 |
| 0 | Serdes/SGMII Mode Select | R/W | 0 = SGMII mode.<br>1 = SerDes mode | 0 |

# Analog Transmit Register (Page 010h-017h: Address 020h, Block 1)

*Table 110: Analog Transmit Register (Page 010h-017h: Address 020h-021h, Block 1)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:12 | Voltage Output Levels | R/W | This setting may need to be changed from the default value if the transmitter is required to drive long trace lengths.<br>If Block 0, Register 20h, bit 12 is set to 1, the bits control the output voltage level from 0 mV to 750 mV in 16 equal steps (before any loss or variations in resistance). This is approximate. The actual voltage swing can be found by measuring the device on the board.<br>If Block 0, Register 20h, bit 12 is set to 0, then bit 14 is internally set based on SGMII or SerDes mode. Only bits 15, 13, and 12 can be programmed. All four bits determine transmit amplitude. | Ch |
| 11:9 | Reserved | R/W | Reserved | 100 |
| 8:6 | Pre-emphasis Coef | R/W | Pre-emphasis coefficient. This setting may need to be changed from the default value if the transmitter is required to drive long trace lengths.<br>It allows eight possible combinations, ranging from 0% to 50%. 0x7 is 50% and 0x0 is 0%. The granularity is roughly linear across the eight settings. | 0 |
| 5:0 | Reserved | R/W | Reserved | 10h |

# SerDes/SGMII Control 2 Register (Page 010h-017h: Address 022h)

*Table 111: SerDes/SGMII Control 2 Register (Page 010h-017h: Address 022h-023h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | RO | Reserved. Write as 0, ignore read. | 0 |
| 14 | BER Counter Clear | SC | 1 = Clear bit-error-rate counter "BER/CRC Error Counter Register (Page 010h-017h: Address 02Eh)" on page 149, bits[15:8].<br>0 = Normal operation. | 0 |
| 13 | Transmit Idle Test Sequence | R/W | This bit activates a transmit idle test sequence for testing purposes. The 16-stage, 10-bit transmit test sequence is forced regardless of link conditions. Setting Force Transmit 1/2 in addition to this bit can modify the idle test sequence.<br>"Force Transmit 1 Register (Page 010h-017h: Address 03Ah)" on page 152, bits [9:0] will override k28.5 for stage 5 (17Ch)<br>"Force Transmit 2 Register (Page 010h-017h: Address 03Ch)" on page 152, bits [9:0] will override D16.2 for stage 6 (289h).<br>1 = Enable transmit idle test sequence.<br>0 = Normal operation. | 0 |
| 12:6 | Reserved | R/W | Reserved. Write as 0, ignore read. | 00 |

*Table 111: SerDes/SGMII Control 2 Register (Page 010h-017h: Address 022h-023h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 5 | Force Transmit | R/W | 1 = Allow packets to be transmitted regardless of the condition of the link or synchronization.<br>0 = Normal operation. | 0 |
| 4 | Remote Fault Sense | R/W | 0 = Automatically detect remote faults and send remote fault status to link partner via auto-negotiation when SerDes mode is selected. SGMII does not support remote faults.<br>1 = Disable automatic sensing of remote faults, such as auto-negotiation error. | 0 |
| 3 | Reserved | R/W | | 0 |
| 2 | Stable Link Filter | R/W | This bit forces the constant sync status for 10 ms before establishing link. This prevents potential false-link events in SerDes applications not using Auto-negotiation or the Signal Detect pin.<br>0 = Normal operation.<br>1 = Sync status must be set for a solid 10 ms before a valid link is established when auto-negotiation is disabled. | 0 |
| 1 | False Link Disable | R/W | 0 = Normal operation.<br>1 = Do not allow link to be established when auto-negotiation is disabled and receiving auto-negotiation code words. The link is only established in this case after idles are received. (This bit does not need to be set, if bit 0 is set.). | 0 |
| 0 | Parallel Detect | R/W | 0 = Disable.<br>1 = Enable parallel detection. (This turns auto-negotiation on and off as needed to properly link up with the link partner. The idles and auto-negotiation code words received from the link partner are used to make this decision). | 1 |

## SerDes/SGMII Control 3 Register (Page 010h-017h: Address 024h)

*Table 112: SerDes/SGMII Control 3 Register (Page 010h-017h: Address 024h-025h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:14 | Reserved | RO | Reserved. Write 0, ignore read. | 00 |
| 13 | Carrier Sense Disable | R/W | 0 = Normal operation.<br>1 = Disable generating CRS from transmitting in half-duplex mode. Only receiving generates CRS. | 0 |
| 12:3 | Reserved | R/W | Reserved. Write as 0, ignore read. | 000h |
| 2:1 | FIFO Elasticity | R/W | 00 = Supports packets up to 5 KB.<br>01 = Supports packets up to 10 KB.<br>1X = Supports packets up to 13.5 KB. | 01 |
| 0 | Reserved | RO | Reserved. Write 0, ignore read. | 0 |

# SerDes/SGMII Status 1 Register (Page 010h-017h: Address 028h)

*Table 113: SerDes/SGMII Status 1 Register (Page 010h-017h: Address 028h-029h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Transmit FIFO status | RO | 0 = No transmit FIFO error detected since last read.<br>1 = Transmit FIFO error detected since last read. | 0 |
| 14 | Receive FIFO status | RO | 0 = No receive FIFO error detected since last read.<br>1 = Receive FIFO error detected since last read. | 0 |
| 13 | False Carrier status | RO | 0 = No false carrier detected since last read.<br>1 = False carrier detected since last read. | 0 |
| 12 | CRC Error status | RO | 0 = No CRC error detected since last read or detection is disabled via "SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h, Block 0)" on page 142, bit 7.<br>1 = CRC error detected since last read. | 0 |
| 11 | Transmit Error Status | RO | 0 = No transmit error code detected since last read.<br>1 = Transmit error code detected since last read (rx_data_error state in PCS receive FSM). | 0 |
| 10 | Receive Error Status | RO | 0 = No receive error since last read.<br>1 = Receive error since last read (early_end state in PCS receive FSM). | 0 |
| 9 | Carrier Extension Status | RO | 0 = No carrier extend error since last read.<br>1 = Carrier extend error since last read (extend_err in PCS receive FSM). | 0 |
| 8 | Early End Extension status | RO | 0 = No early end extension since last read.<br>1 = Early end extension since last read (early_end_ext in PCS receive FSM). | 0 |
| 7 | Link Change status | RO | 0 = Link status has not changed since last read.<br>1 = Link status has changed since last read. | 0 |
| 6 | Receive Pause status | RO | 0 = Disable pause receive.<br>1 = Enable pause receive. | 0 |
| 5 | Transmit Pause status | RO | 0 = Disable pause transmit.<br>1 = Enable pause transmit. | 0 |
| 4:3 | Speed status | RO | 00 = 10 Mbps.<br>01 = 100 Mbps.<br>1X = 1000 Mbps. | 0 |
| 2 | Duplex status | RO | 0 = Half-duplex.<br>1 = Full-duplex. | 0 |
| 1 | Link status | RO | 0 = Link is down.<br>1 = Link is up. | 0 |
| 0 | SGMII/SerDes status | RO | 0 = SerDes mode<br>1 = SGMII mode. | 0 |

# SerDes/SGMII Status 2 Register (Page 010h-017h: Address 02Ah)

*Table 114: SerDes/SGMII Status 2 Register (Page 010h-017h: Address 02Ah-02Bh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | SGMII/SerDes Mode Change | RO | 0 = SGMII/SerDes mode has not changed since last read (fixed in SGMII or SerDes mode).<br>1 = SGMII/SerDes mode has changed since last read.<br>***Note:*** This bit is useful when auto-detection is enabled in "SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h, Block 0)" on page 142, bit 4. | 0 |
| 14 | Consistency mismatch | RO | A consistency mismatch results from incompatibilities represented in the link code word of the local and remote link partners. SerDes or SGMII mode.<br>0 = Consistency mismatch has not been detected since last read.<br>1 = Consistency mismatch detected since last read. | 0 |
| 13 | Auto-negotiation Resolution Error | RO | 0 = Auto-negotiation had error since last read.<br>1 = Auto-negotiation has not had error since last read. | 0 |
| 12 | SGMII selector mismatch | RO | A SGMII selector mismatch occurs when the auto-negotiation page received from the link partner has bit 0 = 0 while local device is in SGMII mode.<br>0 = SGMII selector mismatch not detected since last read.<br>1 = SGMII selector mismatch detected since last read. | 0 |
| 11 | Sync Status Failure | RO | 0 = SYNC_STATUS has not failed since last read.<br>1 = SYNC_STATUS has failed since last read (synchronization has been lost). | 0 |
| 10 | Sync Status Ok | RO | 0 = SYNC_STATUS ok has not been detected since last read.<br>1 = SYNC_STATUS ok detected since last read (synchronization has been achieved). | 0 |
| 9 | Rudi_C | RO | 0 = rudi_c has not been detected since last read.<br>1 = rudi_c detected since last read. | 0 |
| 8 | Rudi_I | RO | 0 = rudi_i has not been detected since last read.<br>1 = rudi_i detected since last read. | 0 |
| 7 | Rudi_Invalid | RO | 0 = rudi_invalid has not been detected since last read.<br>1 = rudi_invalid detected since last read. | 0 |
| 6 | Sync Loss | RO | 0 = Failure condition has not been detected since last read.<br>1 = A valid link went down due to a loss of synchronization for over 10 ms. | 0 |
| 5 | Idle Detect | RO | 0 = Idle detect state not entered since last read.<br>1 = Idle detect state in auto-negotiation fsm entered since last read. | 0 |
| 4 | Acknowledge Complete | RO | 0 = Complete acknowledge state not entered since last read.<br>1 = Complete acknowledge state in auto-negotiation fsm entered since last read. | 0 |

*Table 114: SerDes/SGMII Status 2 Register (Page 010h-017h: Address 02Ah-02Bh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 3 | Acknowledge Detect State | RO | 0 = Acknowledge detect state not entered since last read.<br>1 = Acknowledge detect state in auto-negotiation fsm entered since last read. | 0 |
| 2 | Ability Detect State | RO | 0 = Ability detect state not entered since last read.<br>1 = Ability detect state in auto-negotiation fsm entered since last read. | 0 |
| 1 | An_disable_link_ok State | RO | 1 = an_disable_link_ok state in auto-negotiation fsm entered since last read.<br>0 = an_disable_link_ok not entered since last read. | 0 |
| 0 | An_enable State | RO | 0 = an_enable state has not been entered since last read.<br>1 = an_enable state in auto-negotiation fsm entered since last read. | 0 |

## SerDes/SGMII Status 3 Register (Page 010h-017h: Address 02Ch)

*Table 115: SerDes/SGMII Status 3 Register (Page 010h-017h: Address 02Ch–02Dh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:10 | Reserved | RO | Reserved. Write as 0, ignore read. | 0 |
| 9 | Signal Detect Filter Output | | This bit represents the output of the Signal Detect filter, regardless of whether the filter is active or not. This status signal is still valid when "SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h, Block 0)" on page 142 bit [14] is 1. Noise pulses less than 16 ns wide are still removed when even the filter is disabled.<br>0 = Output of signal detect filter is not set.<br>1 = Output of signal detect filter is set.<br>This signal is used for the PCS synchronization. When the Signal Detect signal is disabled ("SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h, Block 0)" on page 142, bit [2] is 0, then the output of the filter is forced high. | 0 |
| 8 | Signal Detect Inversion Output | | This status signal is the signal detect result when "SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h, Block 0)" on page 142, bit [3] is 0; otherwise, it is the inversion of the signal detect.<br>0 = Output of signal detect inversion is not set.<br>1 = Output of signal detect inversion is set.<br>This is the only valid Signal Detect status bit when the port is powered down from "MII Control Register (Page 010h-017h: Address 00h)" on page 137, bit [11]. | 0 |
| 7 | Signal Detect Change | | 0 = Signal detect has not changed since last read.<br>1 = Signal detect has changed since last read.<br>**Note**: The signal detect change is based on a change in bit [9] of this register. | 0 |
| 6 | Signal Detect | RO | Signal detect direct from pin. | 0 |

*Table 115: SerDes/SGMII Status 3 Register (Page 010h-017h: Address 02Ch–02Dh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 5 | Analog Signal Detect | RO | Analog signal detect status bit. | 0 |
| 4:0 | Reserved | RO | Reserved. Write as 0, ignore read. | 0 |

## BER/CRC Error Counter Register (Page 010h-017h: Address 02Eh)

*Table 116: BER/CRC Error Counter Register (Page 010h–017h: Address 02Eh-02Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:8 | Bit Error Rate (BER) Counter | RO | Number of invalid code groups detected while sync_status = 1.<br>Freezes at FFh.<br>Write "Analog Transmit Register (Page 010h-017h: Address 020h, Block 1)" on page 144, bit [14] = 1 in order to clear. | 00h |
| 7:0 | CRC Error/ Receive Packet Counter | R/W CR | Number of CRC errors detected since last read. Freezes at FFh.<br>When "SerDes/SGMII Control 1 Register (Page 010h-017h: Address 020h, Block 0)" on page 142, bit 11 is set, the counter detects the number of received packets instead of CRC errors. | 00h |

## PRBS Control Register (Page 010h-017h: Address 030h)

*Table 117: PRBS Control Register (Page 010h–017h: Address 030h-031h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:4 | Reserved | R/W | Write as 0, ignore on read | 000h |
| 3:2 | PRBS Order | R/W | 11 = x(n) = 1 + x(28) + x(31)<br>10 = x(n) = 1 + x(18) + x(23)<br>01 = x(n) = 1 + x(14) + x(15)<br>00 = x(n) = 1 + x(6) + x(7) | 00 |
| 1 | Invert PRBS Order | R/W | 1 = Invert polynomial sequence<br>0 = Normal operation | 0 |
| 0 | PRBS Enable | R/W | 1 = Enable PRBS<br>0 = Disable PRBS | 0 |

# PRBS Status Register (Page 010h-017h: Address 032h)

*Table 118: PRBS Status Register (Page 010h–017h: Address 032h-033h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:13 | PRBS Error State | RO<br>CR | Grey coded FSM:<br>100 = 1024 or more errors<br>101 = 512-1023 errors<br>111 = 256-511 errors<br>110 = 128-255 errors<br>010 = 64-127 errors<br>011 = 32-63 errors<br>001 = 1-31 errors<br>000 = No errors | 000 |
| 12 | PRBS Lost Lock | RO<br>LH | 1 = PRBS has lost lock since last read<br>0 = PRBS has not lost lock since last read | 0 |
| 11 | PRBS Locked | RO | 1 = PRBS monitor is locked<br>0 = PRBS monitor is not locked | 0 |
| 10:0 | PRBS Errors | RO<br>CR | Number of PRBS errors detected while locked. Freezes at 7FFh.<br>**Note**: Counter is not synchronized to read status clock. The counter might increment while reading, causing inaccurate results. The PRBS should be disabled before reading the 11-bit error counter. | 000h |

# Pattern Generator Control Register (Page 010h-017h: Address 034h)

*Table 119: Pattern Generator Control Register (Page 010h–017h: Address 034h-035h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | R/W | Write as 0, ignore on read | 0 |
| 14 | TXER | R/W | 1 = Set txer = 1 during CRC portion of packet<br>0 = Normal operation | 0 |
| 13 | Skip CRC | R/W | 1 = Do not append 32-bit CRC to end of packet<br>0 = Normal operation | 0 |
| 12 | CRC Checker Enable | R/W | 1 = Enable CRC checker to detect CRC errors on packets of any size (1 byte or more)<br>0 = Normal operation (CRC checker only detects CRC errors on packets of at least 72 bytes) | 0 |

*Table 119: Pattern Generator Control Register (Page 010h–017h: Address 034h-035h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 11:9 | IPG Select | R/W | 000 = Invalid<br>001 = ipg of 6 bytes<br>010 = ipg of 10 bytes<br>011 = ipg of 14 bytes<br>100 = ipg of 18 bytes<br>101 = ipg of 22 bytes<br>110 = ipg of 26 bytes<br>111 = ipg of 30 bytes | 100 |
| 8:3 | Packet Size | R/W | 000000 = Invalid<br>000001 = 256 bytes<br>000010 = 512 bytes<br>000011 = 768 bytes<br>000100 = 1024 bytes<br>...<br>111111 = 16,128 bytes | 000100 |
| 2 | Single Pass Mode | R/W | 1 = Only send 1 packet and stop<br>0 = Send packets while bit 1 of this register is set | 0 |
| 1 | Run Pattern Generator | R/W | 1 = A rising edge on this bit while the pattern generator is in the idle state will start sending packets. If the single pass mode is set, then a single packet will be sent and the idle state will be entered. If the single pass mode is not set, then packets will be sent until this bit is cleared. At this point, the current packet will finish transmitting and then enter the idle state.<br>**Note**: A valid link must be established prior to sending packets.<br>0 = Do not send packets | 0 |
| 0 | Select Pattern Generator Data | R/W | 1 = Send idles or pattern generator data into transmit fifo (ignore MAC transmit data).<br>0 = Normal operation. | 0 |

# Pattern Generator Status Register (Page 010h-017h: Address 036h)

*Table 120: Pattern Generator Status Register (Page 010h–017h: Address 036h-037h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:4 | Reserved | R/W | Write as 0, ignore on read | 000h |
| 3 | Pattern Generator Active | RO | 1 = Pattern generator is still sending packets<br>0 = Pattern generator is idle | 0 |
| 2:0 | Pattern Generator FSM | RO | 000 = Idle<br>001 = Transmit preamble<br>011 = Transmit sfd<br>010 = Transmit data<br>110 = Transmit crc<br>100 = ipg<br>101 = ipg 2 (allows fsm to be grey-coded) | 000 |

# Force Transmit 1 Register (Page 010h-017h: Address 03Ah)

*Table 121: Force Transmit 1 Register (Page 010h–017h: Address 03Ah-30Bh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:11 | Reserved | R/W | Write as 0, ignore on read | 00h |
| 10 | Force Transmit | R/W | This bit enables a test transmit mode of two alternating patterns. Additionally, can be used in conjunction with the Transmit Idle Test via "Analog Transmit Register (Page 010h-017h: Address 020h, Block 1)" on page 144, bit 13.<br>1 = Provide alternating bit[9:0] from this register and "Force Transmit 2 Register (Page 010h-017h: Address 03Ch)" on page 152, bits[9:0] to SerDes analog transmitter.<br>0 = Normal operation. | 0 |
| 9:0 | Force Transmit Data 1 | R/W | Value in this register will be provided to SerDes analog transmitter every other clock cycle when bit 10 is set | 17Ch |

# Force Transmit 2 Register (Page 010h-017h: Address 03Ch)

*Table 122: Force Transmit 2 Register (Page 010h–017h: Address 03Ch-03Dh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:10 | Reserved | R/W | Write as 0, ignore on read | 00h |
| 9:0 | Force Transmit Data 2 | R/W | Value in this register will be provided to SerDes analog transmitter every other clock cycle when "Force Transmit 1 Register (Page 010h-017h: Address 03Ah)" on page 152, bit 10 is set. | |

## Block Address Number (Page 010h-017h: Address 03Eh)

*Table 123: Block Address Number (Page 010h-017h: Address 03Eh-03Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:1 | Reserved | RO | Reserved | 0 |
| 0 | Block Number | R/W | Block 1 and Block 0 selected via this bit.<br>0 = Block 0 Active<br>1 = Block 1 Active | 0 |

# Page 020h-027h: Port MIB Registers

*Table 124: Port MIB Registers Page Summary*

| Page | Description |
|---|---|
| 020h | Port 0 |
| 021h | Port 1 |
| 022h | Port 2 |
| 023h | Port 3 |
| 024h | Port 4 |
| 025h | Reserved |
| 026h | Reserved |
| 027h | Reserved |

*Table 125: Page 020h–027h Port MIB Registers*

| Address | Bits | Name | Description |
|---|---|---|---|
| 00h–07h | 64 | TxOctets | The total number of good bytes of data transmitted by a port (excluding preamble, but including FCS). |
| 08h–0Bh | 32 | TxDropPkts | This counter is incremented every time a transmit packet is dropped due to lack of resources (e.g., transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters. |
| 0Ch–0Fh | 32 | TxQoSPKT | The total number of good packets transmitted on any queue, which is specified in MIB Queue Select register when QoS is enabled. |
| 010h–013h | 32 | TxBroadcastPkts | The number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets. |

***Table 125: Page 020h–027h Port MIB Registers (Cont.)***

| Address | Bits | Name | Description |
|---|---|---|---|
| 014h–017h | 32 | TxMulticastPkts | The number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. |
| 018h–01Bh | 32 | TxUnicastPkts | The number of good packets transmitted by a port that are addressed to a unicast address. |
| 01Ch–01Fh | 32 | TxCollisions | The number of collisions experienced by a port during packet transmissions. |
| 020h–023h | 32 | TxSingleCollision | The number of packets successfully transmitted by a port that experienced exactly one collision. |
| 024h–027h | 32 | TxMultiple Collision | The number of packets successfully transmitted by a port that experienced more than one collision. |
| 028h–02Bh | 32 | TxDeferredTransmit | The number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy. |
| 02Ch–02Fh | 32 | TxLateCollision | The number of times that a collision is detected later than 512 bit-times into the transmission of a packet. |
| 030h–033h | 32 | TxExcessiveCollision | The number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts. |
| 034h–037h | 32 | TxFrameInDisc? | The number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue. (Not maintained or reported in the MIB counters and located in the Congestion Management registers [Page 0Ah].) This attribute only increments if a network device is not acting in compliance with a flow-control request, or the BCM5387 internal flow control/buffering scheme has been misconfigured. |
| 038h–03Bh | 32 | TxPausePkts | The number of PAUSE events on a given port. |
| 03Ch–043h | 64 | TxQoSOctets | The total number of good bytes transmitted on any queue, which is specified in MIB Queue Select register when QoS is enabled. |
| 044h–04Bh | 64 | RxOctets | The number of bytes of data received by a port (excluding preamble, but including FCS), including bad packets. |
| 04Ch–04Fh | 32 | RxUndersizePkts | The number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS). |

***Table 125: Page 020h–027h Port MIB Registers (Cont.)***

| *Address* | *Bits* | *Name* | *Description* |
|---|---|---|---|
| 050h–053h | 32 | RxPausePkts | The number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88-08h), have a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (00-01), be a minimum of 64 bytes in length (excluding preamble but including FCS), and have a valid CRC. Although an IEEE 802.3 compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a non-compliant transmitting device on the network. |
| 054h–057h | 32 | Pkts64Octets | The number of packets (including error packets) that are 64 bytes long. |
| 058h–05Bh | 32 | Pkts65to127Octets | The number of packets (including error packets) that are between 65 and 127 bytes long. |
| 05Ch–05Fh | 32 | Pkts128to255Octets | The number of packets (including error packets) that are between 128 and 255 bytes long. |
| 060h–063h | 32 | Pkts256to511Octets | The number of packets (including error packets) that are between 256 and 511 bytes long. |
| 064h–067h | 32 | Pkts512to1023Octets | The number of packets (including error packets) that are between 512 and 1023 bytes long. |
| 068h–06Bh | 32 | Pkts1024to1522Octets | The number of packets (including error packets) that are between 1024 and 1522 bytes long. |
| 06Ch–06Fh | 32 | RxOversizePkts | The number of good packets received by a port that are greater than 1522 bytes (tagged) and 1518 bytes (untagged). Note that this counter alone is incremented for packets in the range 1523-1536 bytes inclusive, whereas both this counter and the RxExcessSizeDisc counter are incremented for packets of 1537 bytes and higher. |
| 070h–073h | 32 | RxJabbers | The number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error. |
| 074h–077h | 32 | RxAlignmentErrors | The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and 1522 bytes, inclusive, and have a bad FCS with a non-integral number of bytes. |

***Table 125: Page 020h–027h Port MIB Registers (Cont.)***

| Address | Bits | Name | Description |
|---|---|---|---|
| 078h–07Bh | 32 | RxFCSErrors | The number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and 1522 bytes inclusive, and have a bad FCS with an integral number of bytes. |
| 07Ch–083h | 64 | RxGoodOctets | The total number of bytes in all good packets received by a port (excluding framing bits but including FCS). |
| 084h–087h | 32 | RxDropPkts | The number of good packets received by a port that were dropped due to lack of resources (e.g., lack of input buffers) or were dropped due to lack of resources before a determination of the validity of the packet was able to be made (e.g., receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxExcessSizeDisc, the RxAlignmentErrors, or the RxFCSErrors counters. |
| 088h–08Bh | 32 | RxUnicastPkts | The number of good packets received by a port that are addressed to a unicast address. |
| 08Ch–08Fh | 32 | RxMulticastPkts | The number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. |
| 090h–093h | 32 | RxBroadcastPkts | The number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets. |
| 094h–097h | 32 | RxSAChanges | The number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network. |
| 098h–09Bh | 32 | RxFragments | The number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error. |
| 09Ch–09Fh | 32 | RxExcessSizeDisc | The number of good packets received by a port that are greater than 1536 bytes (excluding framing bits but including the FCS) and were discarded due to excessive length. Note that the RxOversizePkts counter alone is incremented for packets in the range 1523-1536 bytes inclusive, whereas both this counter and the RxOversizePkts counter are incremented for packets of 1537 bytes and higher |
| 0A0h–0A3h | 32 | RXSymbolError | The total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter only increments once per carrier event and does not increment on detection of collision during the carrier event. |

***Table 125: Page 020h–027h Port MIB Registers (Cont.)***

| Address | Bits | Name | Description |
|---|---|---|---|
| 0A4h–0A7h | 32 | RXQOSPkt | The total number of good packets received in any priority, which is specified in MIB Queue Select register when QoS is enabled. |
| 0A8h–0AFh | 64 | RXQOSOctets | The total number of good bytes received in any priority, which is specified in MIB Queue Select register when QoS is enabled. |
| 0B0h–0B3h | 32 | Pkts1523to2047 | The number of packets (including error packets) that are between 1523 and 2047 bytes long. |
| 0B4h–0B7h | 32 | Pkts2048to4095 | The number of packets (including error packets) that are between 2048 and 4095 bytes long. |
| 0B8h–0BBh | 32 | Pkts4096to8191 | The number of packets (including error packets) that are between 4096 and 8191 bytes long. |
| 0BCh–0BFh | 32 | Pkts8192to9728 | The number of packets (including error packets) that are between 8192 and 9728 bytes long. |
| C0h–EFh | – | Reserved | |
| F0h–F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 | |
| F8h–FDh | – | Reserved | |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 | |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 | |

# Page 030h: QoS Registers

*Table 126: Page 030h QoS Registers*

| Address | Bits | Description |
|---|---|---|
| 00h | 8 | "QoS Global Control Register (Page 030h: Address 00h)" on page 159 |
| 01h–03h | – | Reserved |
| 04h–05h | 16 | "QoS IEEE 802.1p Enable Register (Page 030h: Address 04h)" on page 159 |
| 06h–07h | 16 | "QoS DiffServ Enable Register (Page 030h: Address 06h)" on page 160 |
| 08h–0Fh | – | Reserved |
| 010h–013h | 32 | "IEEE 802.1p Priority Map Register (Page 030h: Address 010h–013h)" on page 160 |
| 014h–02Fh | – | Reserved |
| 030h–035h | 48 | "DiffServ Priority Map 0 Register (Page 030h: Address 030h)" on page 161 |
| 036h–03Bh | 48 | "DiffServ Priority Map 1 Register (Page 030h: Address 036h)" on page 161 |
| 03Ch–041h | 48 | "DiffServ Priority Map 2 Register (Page 030h: Address 03Ch)" on page 162 |
| 042h–047h | 48 | "DiffServ Priority Map 3 Register (Page 030h: Address 042h)" on page 163 |
| 048h–04Fh | – | Reserved |
| 050h–061h | 16/port | "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163 |
| 062h–07Fh | – | Reserved |
| 080h | 8 | "TX Queue Control Register (Page 030h: Address 080h)" on page 164 |
| 081h | 8 | "TX Queue Weight Register (Page 030h: Address 081h)" on page 165, Queue 0 |
| 082h | 8 | "TX Queue Weight Register (Page 030h: Address 081h)" on page 165, Queue 1 |
| 083h | 8 | "TX Queue Weight Register (Page 030h: Address 081h)" on page 165, Queue 2 |
| 084h | 8 | "TX Queue Weight Register (Page 030h: Address 081h)" on page 165, Queue 3 |
| 085h–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

# QoS Global Control Register (Page 030h: Address 00h)

*Table 127: QoS Global Control Register (Page 030h: Address 00h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | R/W | – | 0 |
| 6 | PORT_QOS_EN | R/W | Port-based QoS Enable.<br>When port-based QoS is enabled, ingress frames are assigned a priority ID value based on the PORT_QOS_PRI bits in the "Default IEEE 802.1Q Tag Register (Page 034h, Address 010h)" on page 174. IEEE 802.1p and DiffServ priorities are disregarded if QoS_LAYER_SEL (bits[3:2]) is 00, 01 or 10. If QoS_LAYER_SEL=11, the highest available priority of port-based QoS, remapped IEEE 802.1p QoS, remapped DiffServ QoS, or MAC-based QoS applies.<br>0 = Disable port-based QoS.<br>1 = Enable port-based QoS.<br>See "Quality of Service" on page 22 for more information. | QoS_EN |
| 5:4 | Reserved | R/W | – | 0 |
| 3:2 | QOS_LAYER_SEL | R/W | QoS Priority Selection.<br>These bits determine which QoS priority scheme is associated with the frame. See "Frame Priority Decision Tree" on page 25 for details. | 0 |
| 1:0 | Reserved | R/W | – | 0 |

# QoS IEEE 802.1p Enable Register (Page 030h: Address 04h)

*Table 128: QoS IEEE 802.1P Enable Register (Page 030h: Address 04h–05h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8:0 | 802_1P_EN | R/W | QoS IEEE 802.1p Port Mask.<br>Bit 8: IMP port.<br>0 = Disable IEEE 802.1p priority for individual ports.<br>1 = Enable IEEE 802.1p priority for individual ports.<br>See "IEEE 802.1p QoS" on page 24 for more information. | 0 |
| 7:5 | RESERVED | RO | – | 0 |
| 4:0 | 802_1P_EN | R/W | QoS IEEE 802.1p Port Mask.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

See "Quality of Service" on page 22 for more information.

# QoS DiffServ Enable Register (Page 030h: Address 06h)

*Table 129: QoS DiffServ Enable Register (Page 030h: Address 06h–07h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | 0 |
| 8 | DIFFSERV_EN | R/W | DiffServ Port Mask.<br>Bit 8: IMP port.<br>0 = Disable DiffServ priority for individual ports.<br>1 = Enable DiffServ priority for individual ports.<br>See "DiffServ QoS" on page 25 for more information. | 0 |
| 7:5 | RESERVED | RO | – | 0 |
| 4:0 | DIFFSERV_EN | R/W | DiffServ Port Mask.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

See "Quality of Service" on page 22 for more information.

# IEEE 802.1p Priority Map Register (Page 030h: Address 010h)

These bits map the IEEE 802.1p priority level to one of the eight priority ID levels in the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163.

*Table 130: IEEE 802.1p Priority Map Register (Page 030h: Address 010h–013h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:24 | Reserved | RO | – | 0 |
| 23:21 | 1P _111_MAP | R/W | IEEE 802.1p Priority Tag Field 111 | 0 |
| 20:18 | 1P _110_MAP | R/W | IEEE 802.1p Priority Tag Field 110 | 0 |
| 17:15 | 1P _101_MAP | R/W | IEEE 802.1p Priority Tag Field 101 | 0 |
| 14:12 | 1P _100_MAP | R/W | IEEE 802.1p Priority Tag Field 100 | 0 |
| 11:9 | 1P _011_MAP | R/W | IEEE 802.1p Priority Tag Field 011 | 0 |
| 8:6 | 1P _010_MAP | R/W | IEEE 802.1p Priority Tag Field 010 | 0 |
| 5:3 | 1P _001_MAP | R/W | IEEE 802.1p Priority Tag Field 001 | 0 |
| 2:0 | 1P _000_MAP | R/W | IEEE 802.1p Priority Tag Field 000 | 0 |

See "Quality of Service" on page 22 for more information.

# DiffServ Priority Map 0 Register (Page 030h: Address 030h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163.

***Table 131: DiffServ Priority Map 0 Register (Page 030h: Address 030h–035h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:45 | DIFFSERV_ 001111_MAP | R/W | DiffServ DSCP Priority Tag Field 001111 | 0 |
| 44:42 | DIFFSERV_ 001110_MAP | R/W | DiffServ DSCP Priority Tag Field 001110 | 0 |
| 41:39 | DIFFSERV_ 001101_MAP | R/W | DiffServ DSCP Priority Tag Field 001101 | 0 |
| 38:36 | DIFFSERV_ 001100_MAP | R/W | DiffServ DSCP Priority Tag Field 001100 | 0 |
| 35:33 | DIFFSERV_ 001011_MAP | R/W | DiffServ DSCP Priority Tag Field 001011 | 0 |
| 32:30 | DIFFSERV_ 001010_MAP | R/W | DiffServ DSCP Priority Tag Field 001010 | 0 |
| 29:27 | DIFFSERV_ 001001_MAP | R/W | DiffServ DSCP Priority Tag Field 001001 | 0 |
| 26:24 | DIFFSERV_ 001000_MAP | R/W | DiffServ DSCP Priority Tag Field 001000 | 0 |
| 23:21 | DIFFSERV_ 000111_MAP | R/W | DiffServ DSCP Priority Tag Field 000111 | 0 |
| 20:18 | DIFFSERV_ 000110_MAP | R/W | DiffServ DSCP Priority Tag Field 000110 | 0 |
| 17:15 | DIFFSERV_ 000101_MAP | R/W | DiffServ DSCP Priority Tag Field 000101 | 0 |
| 14:12 | DIFFSERV_ 000100_MAP | R/W | DiffServ DSCP Priority Tag Field 000100 | 0 |
| 11:9 | DIFFSERV_ 000011_MAP | R/W | DiffServ DSCP Priority Tag Field 000011 | 0 |
| 8:6 | DIFFSERV_ 000010_MAP | R/W | DiffServ DSCP Priority Tag Field 000010 | 0 |
| 5:3 | DIFFSERV_ 000001_MAP | R/W | DiffServ DSCP Priority Tag Field 000001 | 0 |
| 2:0 | DIFFSERV_ 000000_MAP | R/W | DiffServ DSCP Priority Tag Field 000000 | 0 |

See "Quality of Service" on page 22 for more information.

# DiffServ Priority Map 1 Register (Page 030h: Address 036h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163.

***Table 132: DiffServ Priority Map 1 Register (Page 030h: Address 036h–03Bh)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:45 | DIFFSERV_ 011111_MAP | R/W | DiffServ DSCP Priority Tag Field 011111 | 0 |
| 44:42 | DIFFSERV_ 011110_MAP | R/W | DiffServ DSCP Priority Tag Field 011110 | 0 |
| 41:39 | DIFFSERV_ 011101_MAP | R/W | DiffServ DSCP Priority Tag Field 011101 | 0 |
| 38:36 | DIFFSERV_ 011100_MAP | R/W | DiffServ DSCP Priority Tag Field 011100 | 0 |
| 35:33 | DIFFSERV_ 011011_MAP | R/W | DiffServ DSCP Priority Tag Field 011011 | 0 |
| 32:30 | DIFFSERV_ 011010_MAP | R/W | DiffServ DSCP Priority Tag Field 011010 | 0 |
| 29:27 | DIFFSERV_ 011001_MAP | R/W | DiffServ DSCP Priority Tag Field 011001 | 0 |

*Table 132: DiffServ Priority Map 1 Register (Page 030h: Address 036h–03Bh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 26:24 | DIFFSERV_ 011000_MAP | R/W | DiffServ DSCP Priority Tag Field 011000 | 0 |
| 23:21 | DIFFSERV_ 010111_MAP | R/W | DiffServ DSCP Priority Tag Field 010111 | 0 |
| 20:18 | DIFFSERV_ 010110_MAP | R/W | DiffServ DSCP Priority Tag Field 010110 | 0 |
| 17:15 | DIFFSERV_ 010101_MAP | R/W | DiffServ DSCP Priority Tag Field 010101 | 0 |
| 14:12 | DIFFSERV_ 010100_MAP | R/W | DiffServ DSCP Priority Tag Field 010100 | 0 |
| 11:9 | DIFFSERV_ 010011_MAP | R/W | DiffServ DSCP Priority Tag Field 010011 | 0 |
| 8:6 | DIFFSERV_ 010010_MAP | R/W | DiffServ DSCP Priority Tag Field 010010 | 0 |
| 5:3 | DIFFSERV_ 010001_MAP | R/W | DiffServ DSCP Priority Tag Field 010001 | 0 |
| 2:0 | DIFFSERV_ 010000_MAP | R/W | DiffServ DSCP Priority Tag Field 010000 | 0 |

See "Quality of Service" on page 22 for more information.

## DiffServ Priority Map 2 Register (Page 030h: Address 03Ch)

These bits map the DiffServ priority level to one of the eight priority ID levels in the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163.

*Table 133: DiffServ Priority Map 2 Register (Page 030h: Address 03Ch–041h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:45 | DIFFSERV_ 101111_MAP | R/W | DiffServ DSCP Priority Tag Field 101111 | 0 |
| 44:42 | DIFFSERV_ 101110_MAP | R/W | DiffServ DSCP Priority Tag Field 101110 | 0 |
| 41:39 | DIFFSERV_ 101101_MAP | R/W | DiffServ DSCP Priority Tag Field 101101 | 0 |
| 38:36 | DIFFSERV_ 101100_MAP | R/W | DiffServ DSCP Priority Tag Field 101100 | 0 |
| 35:33 | DIFFSERV_ 101011_MAP | R/W | DiffServ DSCP Priority Tag Field 101011 | 0 |
| 32:30 | DIFFSERV_ 101010_MAP | R/W | DiffServ DSCP Priority Tag Field 101010 | 0 |
| 29:27 | DIFFSERV_ 101001_MAP | R/W | DiffServ DSCP Priority Tag Field 101001 | 0 |
| 26:24 | DIFFSERV_ 101000_MAP | R/W | DiffServ DSCP Priority Tag Field 101000 | 0 |
| 23:21 | DIFFSERV_ 100111_MAP | R/W | DiffServ DSCP Priority Tag Field 100111 | 0 |
| 20:18 | DIFFSERV_ 100110_MAP | R/W | DiffServ DSCP Priority Tag Field 100110 | 0 |
| 17:15 | DIFFSERV_ 100101_MAP | R/W | DiffServ DSCP Priority Tag Field 100101 | 0 |
| 14:12 | DIFFSERV_ 100100_MAP | R/W | DiffServ DSCP Priority Tag Field 100100 | 0 |
| 11:9 | DIFFSERV_ 100011_MAP | R/W | DiffServ DSCP Priority Tag Field 100011 | 0 |
| 8:6 | DIFFSERV_ 100010_MAP | R/W | DiffServ DSCP Priority Tag Field 100010 | 0 |
| 5:3 | DIFFSERV_ 100001_MAP | R/W | DiffServ DSCP Priority Tag Field 100001 | 0 |
| 2:0 | DIFFSERV_ 100000_MAP | R/W | DiffServ DSCP Priority Tag Field 100000 | 0 |

See "Quality of Service" on page 22 for more information.

# DiffServ Priority Map 3 Register (Page 030h: Address 042h)

These bits map the DiffServ priority level to one of the eight priority ID levels in the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163.

***Table 134: DiffServ Priority Map 3 Register (Page 030h: Address 042h–407h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 47:45 | DIFFSERV_ 111111_MAP | R/W | DiffServ DSCP Priority Tag Field 111111 | 0 |
| 44:42 | DIFFSERV_ 111110_MAP | R/W | DiffServ DSCP Priority Tag Field 111110 | 0 |
| 41:39 | DIFFSERV_ 111101_MAP | R/W | DiffServ DSCP Priority Tag Field 111101 | 0 |
| 38:36 | DIFFSERV_ 111100_MAP | R/W | DiffServ DSCP Priority Tag Field 111100 | 0 |
| 35:33 | DIFFSERV_ 111011_MAP | R/W | DiffServ DSCP Priority Tag Field 111011 | 0 |
| 32:30 | DIFFSERV_ 111010_MAP | R/W | DiffServ DSCP Priority Tag Field 111010 | 0 |
| 29:27 | DIFFSERV_ 111001_MAP | R/W | DiffServ DSCP Priority Tag Field 111001 | 0 |
| 26:24 | DIFFSERV_ 111000_MAP | R/W | DiffServ DSCP Priority Tag Field 111000 | 0 |
| 23:21 | DIFFSERV_ 110111_MAP | R/W | DiffServ DSCP Priority Tag Field 110111 | 0 |
| 20:18 | DIFFSERV_ 110110_MAP | R/W | DiffServ DSCP Priority Tag Field 110110 | 0 |
| 17:15 | DIFFSERV_ 100101_MAP | R/W | DiffServ DSCP Priority Tag Field 100101 | 0 |
| 14:12 | DIFFSERV_ 110100_MAP | R/W | DiffServ DSCP Priority Tag Field 110100 | 0 |
| 11:9 | DIFFSERV_ 110011_MAP | R/W | DiffServ DSCP Priority Tag Field 110011 | 0 |
| 8:6 | DIFFSERV_ 110010_MAP | R/W | DiffServ DSCP Priority Tag Field 110010 | 0 |
| 5:3 | DIFFSERV_ 110001_MAP | R/W | DiffServ DSCP Priority Tag Field 110001 | 0 |
| 2:0 | DIFFSERV_ 110000_MAP | R/W | DiffServ DSCP Priority Tag Field 110000 | 0 |

See "Quality of Service" on page 22 for more information.

# Ingress Port Priority ID Map Register (Page 030h: Address 050h)

All the bits in the following table map the priority ID to one of the TX Queues. The quantity of TX queues is set in the "TX Queue Control Register (Page 030h: Address 080h)" on page 164.

***Table 135: Ingress Port Priority ID Map Register Address Summary***

| Address | Description |
|---|---|
| 050h–051h | Port 0 |
| 052h–053h | Port 1 |
| 054h–055h | Port 2 |
| 056h–057h | Port 3 |
| 058h–059h | Port 4 |
| 05Ah–05Bh | Reserved |
| 05Ch–05Dh | Reserved |

*Table 135: Ingress Port Priority ID Map Register Address Summary (Cont.)*

| Address | Description |
|---|---|
| 05Eh–05Fh | Reserved |
| 060h–061h | IMP port |

*If QoS_EN = 1, the register default values of ports [3:0] are 11, and all other ports default to 00. If QoS_EN = 0, all values default to 00 for every port.

*Table 136: Ingress Port Priority ID Map Register (Page 030h: Address 050h–061h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:14 | PRI_111_QID | R/W | Priority ID 111 mapped to TX Queue ID | 00 |
| 13:12 | PRI_110_QID | R/W | Priority ID 110 mapped to TX Queue ID | 00 |
| 11:10 | PRI_101_QID | R/W | Priority ID 101 mapped to TX Queue ID | 00 |
| 9:8 | PRI_100_QID | R/W | Priority ID 100 mapped to TX Queue ID | 00 |
| 7:6 | PRI_011_QID | R/W | Priority ID 011 mapped to TX Queue ID | 00 |
| 5:4 | PRI_010_QID | R/W | Priority ID 010 mapped to TX Queue ID | 00 |
| 3:2 | PRI_001_QID | R/W | Priority ID 001 mapped to TX Queue ID | 00 |
| 1:0 | PRI_000_QID | R/W | Priority ID 000 mapped to TX Queue ID | 00 |

See "Quality of Service" on page 22 for more information.

## TX Queue Control Register (Page 030h: Address 080h)

*Table 137: TX Queue Control Register (Page 030h: Address 080h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:5 | Reserved | R/W | – | 0 |
| 4 | HQ_PREEMPT | R/W | High Queue Preempt.<br>When enabled, the highest queue is served first. If the highest queue is empty, frames from the lower queues are served in a weighted round-robin fashion. Queue weight is programmed in "TX Queue Weight Register (Page 030h: Address 081h)" on page 165. | 0 |
| 3:2 | TXQ_MODE | R/W | Transmit Queue Mode.<br>00 = Single-queue mode (no QoS).<br>01 = Two-queue mode (queue [0:1]).<br>10 = Three-queue mode (queue [0:2]).<br>11 = Four-queue mode (queue [0:3]).<br>Eight priority ID levels are mapped to the queues in "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163. | QoS_EN |
| 1:0 | Reserved | R/W | – | 0 |

See "Quality of Service" on page 22 for more information.

## TX Queue Weight Register (Page 030h: Address 081h)

*Table 138: TX Queue Weight Register Queue[0:3] (Page 030h: Address 081h–084h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:0 | QSERV_WEIGHT | R/W | Queue Weight Register.<br>The binary value of these bits sets the service weight of the given queue. The value of 1 allows the queue to send one packet for every round; the value of 4 allows the queue to send four packets for every round. It is suggested that the weight of each queue is Q3 > Q2 > Q1 > Q0 > 0.<br>**Note**: The maximum allowable transmit queue weight is 31h. Programming a higher weight than 31h can yield unexpected results. | Queue:<br>0: 0001<br>1: 0010<br>2: 0100<br>3: 1000 |

See "Quality of Service" on page 22 for more information.

# Page 031h: Port-Based VLAN Registers

*Table 139: Page 031h VLAN Registers*

| Address | Bits | Description |
|---|---|---|
| 00h–011h | 16/port | "Port-Based VLAN Control Register (Page 031h, Address 00h)" on page 165 |
| 01Fh–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

## Port-Based VLAN Control Register (Page 031h, Address 00h)

*Table 140: Port-Based VLAN Control Register Address Summary*

| Address | Description |
|---|---|
| 00h–01h | Port 0 |
| 02h–03h | Port 1 |
| 04h–05h | Port 2 |
| 06h–07h | Port 3 |
| 08h–09h | Port 4 |

*Table 140: Port-Based VLAN Control Register Address Summary (Cont.)*

| Address | Description |
|---|---|
| 0Ah–0Bh | Reserved |
| 0Ch–0Dh | Reserved |
| 0Eh–0Fh | Reserved |
| 010h–011h | IMP port |

*Table 141: Port VLAN Control Register (Page 031h, Address 00h–0Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | RO | – | — |
| 8 | FORWARD_MASK | R/W | VLAN Forwarding Mask.<br>Bit 8: IMP port.<br>0 = Disable VLAN forwarding to egress port.<br>1 = Enable VLAN forwarding to egress port. | b'1 |
| 7:5 | RESERVED | RO | – | b'111 |
| 4:0 | FORWARD_MASK | R/W | VLAN Forwarding Mask.<br>Bits[4:0] correspond to ports [4:0], respectively. | 1Fh |

For more information, see "Port-Based VLAN" on page 25.

# Page 032h: Trunking Registers

*Table 142: Page 032h Trunking Registers*

| Address | Bits | Description |
|---|---|---|
| 00h | – | Reserved |
| 01h | 8 | "MAC Trunking Control Register (Page 032h, Address 01h)" on page 167 |
| 02h–08Fh | – | Reserved |
| 090h–091h | 16 | "Trunking Group Register (Page 032h, Address 090h)" on page 167 |
| 92h–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

# MAC Trunking Control Register (Page 032h, Address 01h)

*Table 143: MAC Trunk Control Register (Page 032h, Address 01h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:4 | Reserved | R/W | – | 4'b0 |
| 3 | Trunking Mac Enable Bit | R/W | Trunking MAC Enable Bit<br>This bit enables the trunking feature.<br>1 = Enabled<br>0 = Disabled | 0 |
| 2 | Reserved | R/W | Reserved | 0 |
| 1:0 | TRK_HASH_INDX | R/W | Trunk Hash Index Selector.<br>00 = Use hash [DA,SA] to generate index.<br>01 = Use hash [DA] to generate index.<br>10 = Use hash [SA] to generate index.<br>11 = Illegal state. | 2'b0 |

See “Port Trunking/Aggregation” on page 28 for more information.

# Trunking Group Register (Page 032h, Address 090h)

*Table 144: Trunk Group Register (Page 032h, Address 090h–091h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:2 | Reserved | R/W | – | 0 |
| 1:0 | Trunk Group Enable | R/W | Trunk Group Enable.<br>1 = Enable trunk group.<br>0 = Disable trunk group.<br><br>Bit 0: Enable port 0-1 trunking group.<br>Bit 1: Enable port 2-3 trunking group. | 0 |

See “Port Trunking/Aggregation” on page 28 for more information.

# Page 034h: IEEE 802.1Q VLAN Registers

*Table 145: Page 034h IEEE 802.1Q VLAN Registers*

| Address | Bits | Description |
|---|---|---|
| 00h | 8 | "Global IEEE 802.1Q Register (Pages 034h, Address 00h)" on page 169 |
| 01h | 8 | "Global VLAN Control 1 Register (Page 034h, Address 01h)" on page 170 |
| 02h | 8 | "Global VLAN Control 2 Register (Page 034h, Address 02h)" on page 171 |
| 03h | 8 | "Global VLAN Control 3 Register (Page: 34h, Address 03h)" on page 171 |
| 04h | 8 | "Global VLAN Control 4 Register (Page 034h, Address 04h)" on page 172 |
| 05h | 8 | "Global VLAN Control 5 Register (Page 034h, Address 05h)" on page 173 |
| 07h-0Ah | 32 | "IEEE 802.1p Priority Remap Register (Page 034h, Address 07h)" on page 174 |
| 010h–021h | 16/port | "Default IEEE 802.1Q Tag Register (Page 034h, Address 010h)" on page 174 |
| 020h–0EFh | – | Reserved |
| 0F0h–0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| 0F8h–0FDh | – | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

# Global IEEE 802.1Q Register (Pages 034h, Address 00h)

*Table 146: Global IEEE 802.1Q Register (Pages 034h, Address 00h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Enable IEEE 802.1Q | R/W | Enable IEEE 802.1Q VLAN.<br>0 = Disable IEEE 802.1Q VLAN.<br>1 = Enable IEEE 802.1Q VLAN.<br>See "Programming the VLAN Table" on page 27 for more information. | 0 |
| 6:5 | VLAN Learning Mode | R/W | VLAN Learning Mode.<br>00 = SVL (Shared VLAN Learning mode) (MAC hash ARL table).<br>11 = IVL (Individual VLAN Learning mode) (MAC and VID hash ARL table).<br>10 = Illegal setting.<br>01 = Illegal setting. | 11 |
| 4 | Reserved | R/W | Reserved. | 0 |
| 3:2 | Frame Control | R/W | IEEE 802.1Q Frame Control.<br>00 = No change.<br>01 = Change priority (4 bits).<br>10 = Change VID (12 bits).<br>11 = Change priority and VID (16 bits). | 00 |
| 1:0 | Reserved | R/W | Reserved. | 10 |

See "IEEE 802.1Q VLAN" on page 26 for more information.

# Global VLAN Control 1 Register (Page 034h, Address 01h)

*Table 147: Global VLAN Control 1 Register (Page 034h, Address 01h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | R/W | Reserved. | 0 |
| 6 | Multicast Untag Check | R/W | Multicast VLAN Untagged Map Check Bypass.<br>1 = Multicast frames are not checked against the VLAN Untagged map.<br>0 = Multicast frames are checked against the VLAN Untagged map. | 0 |
| 5 | Multicast Forward Check | R/W | Multicast VLAN Forward Map Check Bypass.<br>1 = Multicast frames are not checked against the VLAN Forward map.<br>0 = Multicast frames are checked against the VLAN Forward map. | 0 |
| 4 | Reserved | R/W | Reserved. | 0 |
| 3 | Reserved Multicast Untag Check | R/W | Reserved Multicast (except GMRP and GVRP) VLAN Untagged Map Check bit.<br>1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN Untagged map.<br>0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN Untagged map. | 0 |
| 2 | Reserved Multicast Forward Check | R/W | Reserved Multicast (except GMRP and GVRP) VLAN Forward Map Check bit.<br>1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN Forward map.<br>0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN Forward map. | 0 |
| 1 | Reserved | R/W | Reserved. | 1 |
| 0 | Multiport Address VLAN Check | R/W | Multiport Address VLAN Table Check Enable bit.<br>Frames that are routed according to the Multiport Address entries can be checked against the VLAN table.<br>1 = Enable VLAN checking.<br>0 = Bypass all VLAN checking.<br>See Multiport Address for more information. | 0 |



For more information, see “IEEE 802.1Q VLAN” on page 26.

# Global VLAN Control 2 Register (Page 034h, Address 02h)

*Table 148: Global VLAN Control 2 Register (Page 034h, Address 02h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserved | R/W | Reserved. | 0 |
| 6 | GMRP/GVRP Untag Check | R/W | GMRP or GVRP VLAN Untag Map Check Bit.<br>1 = GMRP or GVRP frames are checked against the VLAN Untagged map.<br>0 = GMRP or GVRP frames are not checked against the VLAN Untagged map.<br>Does not apply to the frame management port. | 0 |
| 5 | GMRP/GVRP Forward Check | R/W | GMRP or GVRP VLAN Forward Map Check Bit.<br>1 = GMRP or GVRP frames are checked against the VLAN Forward map.<br>0 = GMRP or GVRP frames are not checked against the VLAN Forward map.<br>Does not apply to the frame management port. | 0 |
| 4 | Reserved | R/W | Reserved. | 1 |
| 3 | IMP Frame Untag Bypass | R/W | IMP Frame VLAN Untag Map Bypass.<br>1 = IMP frames are not checked against the VLAN Untagged map.<br>0 = IMP frames are checked against the VLAN Untagged map. | 0 |
| 2 | IMP Frame Forward Bypass | R/W | IMP Frame VLAN Forward Map Check Bit.<br>1 = IMP frames are not checked against the VLAN Forward map.<br>0 = IMP frames are checked against the VLAN Forward map. | 0 |
| 1:0 | Reserved | R/W | Reserved. | 00 |

For more information, see “IEEE 802.1Q VLAN” on page 26.

# Global VLAN Control 3 Register (Page: 34h, Address 03h)

*Table 149: Global VLAN Control 3 Register (Page: 34h, Address 03h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:0 | Drop Non 1Q Frames | R/W | Drop Non-1Q Frames.<br>When enabled, any frame without an IEEE 802.1Q tag is dropped by this port. | 0 |
| 6:5 | RESERVED | RO | – | 0 |
| 4:0 | Drop Non 1Q Frames | R/W | Drop Non-1Q Frames.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

# Global VLAN Control 4 Register (Page 034h, Address 04h)

*Table 150: Global VLAN Control 4 Register (Page 034h, Address 04h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:6 | Source Membership Check | R/W | Source Membership Check Bit.<br>Frames with a VID matching a corresponding entry in the VLAN table, can be checked for source membership. The source is a member only when the source address of the frame is included as a member in the corresponding VLAN entry.<br>00 = Forward frame, but do not learn the SA into the ARL table.<br>01 = Drop frame.<br>10 = Forward frame, and learn the SA into the ARL table.<br>11 = Forward frame to IMP, but not learn.<br>Does not apply to IMP port. | 11 |
| 5 | Forward GVRP to Management | R/W | Forward all GVRP frames to the Frame Management Port bit.<br>1 = GVRP frames are forwarded to the management port.<br>0 = GVRP frames are not forwarded to the management port. | 0 |
| 4 | Forward GMRP to Management | R/W | Forward All GMRP Frames to the Frame Management Port bit.<br>1 = GMRP frames are forwarded to the management port.<br>0 = GMRP frames are not forwarded to the management port. | 0 |
| 3:0 | Reserved | R/W | – | 0 |

For more information, see “IEEE 802.1Q VLAN” on page 26.

# Global VLAN Control 5 Register (Page 034h, Address 05h)

*Table 151: Global VLAN Control 5 Register (Page 034h, Address 05h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | Reserve MC Learning | R/W | Enable Reserved Multicast Address Learning.<br>1 = Reserved multicast frames are learned.<br>0 = Reserved multicast frames are not learned. | 0 |
| 6:5 | Reserved | R/W | – | 00 |
| 4 | Trunk Check Bypass | R/W | Trunk Check Bypass.<br>1 = Egress directed frames issued from the IMP port bypass trunk checking.<br>0 = Egress directed frames issued from the IMP port are subject to trunk checking and redirection. | 1 |
| 3 | Drop Invalid VID | R/W | Drop Frames With Invalid VID.<br>Frames with an invalid VID do not have a corresponding entry in the VLAN table.<br>1 = Ingress frames with invalid VID are dropped.<br>0 = Ingress frames with invalid VID are forwarded to the IMP port. | 0 |
| 2 | Reserved | R/W | Must Write 0. Ignore on read | 0 |
| 1 | Management CRC Check Bypass | R/W | Bypass CRC Check at the Frame Management Port.<br>Disables checking the inner and outer CRC of frames ingressed from the frame management port.<br>1 = CRC is ignored.<br>0 = CRC is checked. | 0 |
| 0 | CRC Generation | R/W | Enable CRC Generation At Egress Ports.<br>When IEEE 802.1Q is disabled, this bit determines if the inner and outer CRC is recalculated before being egressed at the frame management port.<br>1 = CRC recalculated.<br>0 = CRC not recalculated. | 0 |

For more information, see “IEEE 802.1Q VLAN” on page 26.

# IEEE 802.1p Priority Remap Register (Page 034h, Address 07h)

*Table 152: IEEE 802.1p Priority Remap Register (Page 034h, Address 07h-0Ah)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:24 | Reserved | RO | Reserved. | 0 |
| 23:0 | IEEE 802.1p Remap | R/W | IEEE 802.1p Priority Remap Bits.<br>The IEEE 802.1p Remap Enable bit of the "Global VLAN Control 2 Register (Page 034h, Address 02h)" on page 171 enables the remapping of IEEE 802.1p priorities as below:<br>• Bits[23:21]: IEEE 802.1p priority 111.<br>• Bits[20:18]: IEEE 802.1p priority 110.<br>• Bits[17:21]: IEEE 802.1p priority 101.<br>• Bits[14:12]: IEEE 802.1p priority 100.<br>• Bits[11:9]: IEEE 802.1p priority 011.<br>• Bits[8:6]: IEEE 802.1p priority 010.<br>• Bits[5:3]: IEEE 802.1p priority 001.<br>• Bits[2:0]: IEEE 802.1p priority 000.<br>See "Quality of Service" on page 22 for more information. | 0 |

For more information, see "IEEE 802.1Q VLAN" on page 26.

# Default IEEE 802.1Q Tag Register (Page 034h, Address 010h)

*Table 153: Default IEEE 802.1Q Tag Register Address Summary*

| Address | Description |
|---|---|
| 10h–11h | Port 0 |
| 12h–13h | Port 1 |
| 14h–15h | Port 2 |
| 16h–17h | Port 3 |
| 18h–19h | Port 4 |
| 1Ah–1Bh | Reserved |
| 1Ch–1Dh | Reserved |
| 1Eh–1Fh | Reserved |
| 20h–21h | IMP port (see note below) |

*Table 154: Default IEEE 802.1Q Tag Register (Page 034h, Address 010h–021h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:13 | DEFAULT_PRI/ PORT_QOS_PRI | R/W | Default IEEE 802.1Q Priority.<br>If an IEEE 802.1Q tag is added to an incoming non-IEEE 802.1Q frame, these bits are the default priority value for the new tag. See "IEEE 802.1Q VLAN" on page 26 for more information.<br><br>Port-based QoS Priority Map Bits.<br>When port-based QoS is enabled in the "QoS Global Control Register (Page 030h: Address 00h)" on page 159, these bits represent the priority ID for the ingress port. The priority ID determines the TX Queue for each frame based on the "Ingress Port Priority ID Map Register (Page 030h: Address 050h)" on page 163. | 000 |
| 12 | CFI | R/W | Conical Form Indicator. | 0 |
| 11:0 | DEFAULT_VID | R/W | Default IEEE 802.1Q VLAN ID.<br>If an IEEE 802.1Q tag is added to an incoming non-IEEE 802.1Q frame, then these bits are the default VID for the new tag. See "IEEE 802.1Q VLAN" on page 26 for more information. | 0 |

**Note:** The CPU shall always include the VLAN tag to all packets. The default VID from the Default IEEE 802.1Q Tag Register is not appended to management packets that are untagged or IEEE 802.1P priority tagged.

# Page 040h: Jumbo Frame Control Register

*Table 155: Page 040h Jumbo Frame Control Register*

| Address | Bits | Description |
|---|---|---|
| 00h | – | Reserved |
| 01h–04h | 32 | "Jumbo Frame Port Mask Register (Page 040h, Address 01h)" on page 176 |
| 05h–06h | 16 | "Jumbo MIB Good Frame Max Size Register (Page 040h, Address 05h)" on page 176 |
| 07h–EFh | – | Reserved |
| F0h–F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| F8h–FDh | – | Reserved |
| FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

# Jumbo Frame Port Mask Register (Page 040h, Address 01h)

*Table 156: Jumbo Frame Port Mask Registers (Page 040h, Address 01h-04h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:25 | Reserved | RO | – | 0 |
| 24 | 10_100_jumbo_en | R/W | 10/100 Speed Jumbo Frame Enable.<br>1 = Jumbo packets enabled at 1000/100/10 Mbps port speeds.<br>0 = Jumbo packets can be received and transmitted only in 1000 Mbps operation. | 0 |
| 23:8 | Reserved | R/W | – | 0 |
| 7 | JUMBO_PORT_MASK | R/W | Jumbo Frame Port Mask.<br>0 = Disable jumbo frame capability on the port.<br>1 = Enable jumbo frame capability on the port.<br>Jumbo frames can be ingressed and egressed only to the ports enabled via this port mask. Jumbo Frame Port Mask has no affect on the traffic of normal sized frames. See "Jumbo Frame Support" on page 28 for more information. | 0 |
| 6:5 | RESERVED | RO | – | 0 |
| 4:0 | JUMBO_PORT_MASK | R/W | Jumbo Frame Port Mask.<br>Bits[4:0] correspond to ports [4:0], respectively. | 0 |

# Jumbo MIB Good Frame Max Size Register (Page 040h, Address 05h)

*Table 157: Jumbo MIB Good Frame Max Size Registers (Page 040h, Address 05h-06h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 15:14 | Reserved | RO | – | 0 |

***Table 157: Jumbo MIB Good Frame Max Size Registers (Page 040h, Address 05h-06h)***

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 13:0 | MIB Good Max Frame Size | R/W | Good Frame Max Size.<br>Defines the Good Frame Max Size for MIB counter, which should be in the range ‘d9724 ~ ‘d1518.<br><br>Good Frame Length Range in MIB.<br>Tagged Packets: (Good Frame Max Size + 4) ~ 64 bytes.<br>Untagged Packets: Good Frame Max Size ~ 64 bytes.<br><br>The register setting affects the following MIB parameters:<br>• RxSAChange.<br>• RxGoodOctets.<br>• RxUnicastPkts.<br>• RxMulticastPkts.<br>• RxBroadcastPkts.<br>• RxOverSizePkts. | ‘d1518 |

# Page 041h: Broadcast Storm Suppression Register

*Table 158: Broadcast Storm Suppression Register (Page 041h)*

| Address | Bits | Description |
|---|---|---|
| 00h–03h | 32 | "Global Rate Control Register (Page 041h, Address 00h)" on page 178 |
| 04h–0Fh | – | Reserved |
| 10h–2Fh | 32/port | "Port Rate Control Register (Page 041h, Address 010h)" on page 180 |
| 30h–EFh | – | Reserved |
| F0h–F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, bytes 0-7 |
| F8h–FDh | – | Reserved |
| FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

## Global Rate Control Register (Page 041h, Address 00h)

*Table 159: Global Rate Control Register (Page 041h, Address 00h–03h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:17 | Reserved | RO | — | 0 |
| 16 | RATE_COUNT_IPG | R/W | Bit Rate Mode Selection.<br>0 = Rx Rate excludes IPG.<br>1 = Rx Rate includes IPG. | 0 |
| 15 | BUCK1_ BRM_SEL | R/W | Bit Rate Mode Selection.<br>0 = Absolute Bit Rate mode—The Rate Count in the "Port Rate Control Register (Page 041h, Address 010h)" on page 180 represents the incoming bit rate as an absolute data rate.<br>1 = Bit Rate Normalized to Link Speed mode—The Rate Count in the "Port Rate Control Register (Page 041h, Address 010h)" on page 180 represents the incoming bit rate normalized with respect to the Link Speed mode.<br>See "Rate Control" on page 29 for more details. | 0 |
| 14 | BUCK1_DRP_EN | R/W | Suppression Drop mode enabled.<br>0 = The Pause Frame/Jamming Frame is transmitted if the allowed bandwidth is exceeded for the types of packets indicated below in the Packet Type Mask.<br>1 = Incoming packets are dropped if the allowed bandwidth is exceeded for the types of packets indicated below in the Packet Type Mask. | 0 |

*Table 159: Global Rate Control Register (Page 041h, Address 00h–03h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 13:8 | BUCK1_PACKET_TYPE | R/W | Suppressed Packet Type Mask.<br>This bit mask determines the type of packets to be monitored by Bucket 1.<br>• 0 = Disable suppression for the corresponding packet type.<br>• 1 = Enable suppression for the corresponding packet type.<br>The bits in this bit field are defined as follows:<br>• Bit 8: Unicast.<br>• Bit 9: Multicast (multicast and destination lookup success).<br>• Bit 10: Ethernet broadcast packets (Length Type < 0600).<br>• Bit 11: Ethernet broadcast packets.(Length Type ≥ 0600).<br>• Bit 12: Reserved multicast address packets. (01-80-c2-00-00-10 only)<br>• Bit 13: Destination Lookup Failure.<br>See "Rate Control" on page 29 for more details. | 0 |
| 7 | BUCK0_ BRM_SEL | R/W | Bit rate Mode Selection.<br>0 = Absolute Bit Rate mode—The Rate Count in the "Port Rate Control Register (Page 041h, Address 010h)" on page 180 represents the incoming bit rate as an absolute data rate.<br>1 = Bit Rate Normalized to Link Speed mode—The Rate Count in the "Port Rate Control Register (Page 041h, Address 010h)" on page 180 represents the incoming bit rate normalized with respect to the Link Speed mode.<br>See "Rate Control" on page 29 for more details. | BC_SUPP_EN |
| 6 | BUCK0_DRP_EN | R/W | Suppression Drop Mode Enabled.<br>0 = The Pause Frame/Jamming Frame is transmitted if the allowed bandwidth is exceeded for the types of packets indicated below in the Packet Type Mask.<br>1 = Incoming packets are dropped if the allowed bandwidth is exceeded for the types of packets indicated below in the Packet Type Mask. | BC_SUPP_EN |

*Table 159: Global Rate Control Register (Page 041h, Address 00h–03h) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 5:0 | BUCK0_PACKET_TYPE | R/W | Suppressed Packet Type Mask.<br>This bit mask determines the type of packets to be monitored by Bucket 0.<br>0 = Disable suppression for the corresponding packet type.<br>1 = Enable suppression for the corresponding packet type.<br>The bits in this bit field are defined as follows:<br>Bit 0: Unicast.<br>Bit 1: Multicast (multicast and destination lookup success).<br>Bit 2: Ethernet broadcast packets (Length Type < 0600).<br>Bit 3: Ethernet broadcast packets.(Length Type ≥ 0600).<br>Bit 4: Reserved multicast address packets. (01-80-c2-00-00-10 only)<br>Bit 5: Destination LookUp Failure.<br>See "Rate Control" on page 29 for more details. | BC_SUPP_EN:<br>1: 001100<br>0: 000000 |

# Port Rate Control Register (Page 041h, Address 010h)

*Table 160: Port Rate Control Register Address Summary*

| Address | Description |
|---|---|
| 10h–13h | Port 0 |
| 14h–17h | Port 1 |
| 18h–1Bh | Port 2 |
| 1Ch–1Fh | Port 3 |
| 20h–23h | Port 4 |
| 24h–27h | Reserved |
| 28h–2Bh | Reserved |
| 2Ch–2Fh | Reserved |

*Table 161: Port Rate Control Register (Page 041h, Address 010h–02Fh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 31:24 | Reserved | RO | – | 0 |
| 23 | Enable Bucket1 | R/W | Enable Rate Control of the Ingress Port, Bucket 1.<br>1 = Enable.<br>0 = Disable. | 0 |

*Table 161: Port Rate Control Register (Page 041h, Address 010h–02Fh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 22 | Enable Bucket0 | R/W | Enable Rate Control of the Ingress Port, Bucket 0.<br>1 = Enable.<br>0 = Disable. | BC_SUPP_EN |
| 21:19 | BUCK1_SIZE | R/W | Bucket Size.<br>This bit determines the maximum size of bucket 1. This is specified on a per port basis.<br>000 = 16 KB.<br>001 = 20 KB.<br>010 = 28 KB.<br>011 = 40 KB.<br>100 = 76 KB.<br>101 = 140 KB.<br>110 = 268 KB.<br>111 = 500 KB.<br>See "Rate Control" on page 29 for more details. | 000 |
| 18:11 | BUCK1_Rate_Cnt | R/W | Rate Count.<br>The Rate Count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per-port basis. The programmed values of the Rate Count and the bit rate mode of the "Global Rate Control Register (Page 041h, Address 00h)" on page 178determine the bucket bit rate in KB. The bucket bit rate represents the average upper limit for incoming packets selected in the Suppressed Packet Type Mask in the "Global Rate Control Register (Page 041h, Address 00h)" on page 178. See "Rate Control" on page 29 for more details.<br>Values written to these bits must be with the ranges specified by Table 2 on page 30. Values outside these ranges are not valid. | 000 |
| 10:8 | BUCK0_SIZE | R/W | Bucket Size.<br>This bit determines the maximum size of bucket 0. This is specified on a per port basis.<br>000 = 16 KB.<br>001 = 20 KB.<br>010 = 28 KB.<br>011 = 40 KB.<br>100 = 76 KB.<br>101 = 140 KB.<br>110 = 268 KB.<br>111 = 500 KB.<br>See "Rate Control" on page 29 for more details. | 000 |

*Table 161: Port Rate Control Register (Page 041h, Address 010h–02Fh) (Cont.)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:0 | BUCK0_Rate_Cnt | R/W | Rate Count.<br>The Rate Count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the rate count and the bit rate mode of the "Global Rate Control Register (Page 041h, Address 00h)" on page 178 determine the bucket bit rate in KB. The bucket bit rate represents the average upper limit for incoming packets selected in the Suppressed Packet Type Mask in the "Global Rate Control Register (Page 041h, Address 00h)" on page 178. See "Rate Control" on page 29 for more details. | 10h |

# Page 080-087h: External PHY Registers (Serial Ports)

**Note:** Information on the external PHY registers should be obtained from the external PHY data sheet. Data is obtained by polling the registers of the external PHY via the "MDC/MDIO Interface Register Programming" on page 69. The actual values or meanings of these bits are controlled by the external PHY. The following table maps the MDC/MDIO register address (used in PHY data sheets) to the SPI register address (used to access these registers via SPI).

*Table 162: External PHY Registers (Serial Ports) Page Summary*

| Page | Description |
|---|---|
| 080h | Port 0 |
| 081h | Port 1 |
| 082h | Port 2 |
| 083h | Port 3 |
| 084h | Port 4 |
| 085h | Reserved |
| 086h | Reserved |
| 087h | Reserved |

*Table 163: External PHY Registers (Serial Ports) (Page 080h–087h)*

| MCD/MDIO Address | SPI Register Address | Bits | IEEE Register Name |
|---|---|---|---|
| 00h | 00h–01h | 16 | MII Control register |
| 01h | 02h–03h | 16 | MII Status register |
| 02h–03h | 04h–07h | 32 | PHY Identifier register |
| 04h | 08h–09h | 16 | Auto-negotiation Advertisement register |
| 05h | 0Ah–0Bh | 16 | Auto-negotiation Link Partner Ability register |
| 06h | 0Ch–0Dh | 16 | Auto-negotiation Expansion register |
| 07h | 0Eh–0Fh | 16 | Next Page Transmit register |
| 08h | 010h–011h | 16 | Link Partner Received Next Page register |
| 09h | 012h–013h | 16 | 1000BASE-T Control register |
| 0Ah | 014h–015h | 16 | 1000BASE-T Status register |
| 0Bh | 016h–017h | 16 | |
| 0Ch | 018h–019h | 16 | |
| 0Dh | 01Ah–01Bh | 16 | |
| 0Eh | 01Ch–01Dh | 16 | |

*Table 163: External PHY Registers (Serial Ports) (Page 080h–087h) (Cont.)*

| MCD/MDIO Address | SPI Register Address | Bits | IEEE Register Name |
|---|---|---|---|
| 0Fh | 01Eh–01Fh | 16 | IEEE Extended Status register |
| 010h | 020h–021h | 16 | |
| 011h | 022h–023h | 16 | |
| 012h | 024h–025h | 16 | |
| 013h | 026h–027h | 16 | |
| 014h | 028h–029h | 16 | |
| 015h | 02Ah–02Bh | 16 | |
| 016h | 02Ch–02Dh | 16 | |
| 017h | 02Eh–02Fh | 16 | |
| 018h | 030h–031h | 16 | |
| 019h | 032h–033h | 16 | |
| 01Ah | 034h–035h | 16 | |
| 01Bh | 036h–037h | 16 | |
| 01Ch | 038h–039h | 16 | |
| 01Dh | 03Ah–03Bh | 16 | |
| 01Eh | 03Ch–03Dh | 16 | |
| 01Fh | 03Eh–03Fh | 16 | |
| – | 40h-EFh | – | Reserved |
| – | 0F0h–0F7h | 8 | “SPI Data I/O Register (Global, Address 0F0h)” on page 185, bytes 0-7 |
| – | 0F8h–0FDh | – | Reserved |
| – | 0FEh | 8 | “SPI Status Register (Global, Address 0FEh)” on page 185 |
| – | 0FFh | 8 | “Page Register (Global, Address 0FFh)” on page 186 |

# Global Registers

*Table 164: Global Registers (Maps to All Pages)*

| Address | Bits | Description |
|---|---|---|
| 0F0h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, 0 |
| 0F1h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, 1 |
| 0F2h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, 2 |
| 0F3h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, 3 |
| 0F4h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, 4 |
| 0F5h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, 5 |
| 0F6h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, 6 |
| 0F7h | 8 | "SPI Data I/O Register (Global, Address 0F0h)" on page 185, 7 |
| 0F8–0FDh | — | Reserved |
| 0FEh | 8 | "SPI Status Register (Global, Address 0FEh)" on page 185 |
| 0FFh | 8 | "Page Register (Global, Address 0FFh)" on page 186 |

## SPI Data I/O Register (Global, Address 0F0h)

*Table 165: SPI Data I/O Register (Maps to All Registers, Address 0F0h–0F7h)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:0 | SPI Data I/O | R/W | SPI data bytes [7:0] | 0 |

## SPI Status Register (Global, Address 0FEh)

*Table 166: SPI Status Register (Maps to All Registers, Address 0FEh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7 | SPIF | RO | SPI Read/Write Complete Flag | 0 |
| 6 | Reserved | RO | – | 0 |
| 5 | RACK | RO (SC) | SPI Read Data Ready Acknowledgement (self-clearing) | 0 |
| 4:2 | Reserved | RO | – | 0 |
| 1 | RXRDY | RO | SMP Rx Ready Flag—should check every 8 bytes | 0 |
| 0 | TXRDY | RO | SMP Tx Ready Flag—should check every 8 bytes | 0 |

# Page Register (Global, Address 0FFh)

*Table 167: Page Register (Maps to All Registers, Address 0FFh)*

| Bit | Name | R/W | Description | Default |
|---|---|---|---|---|
| 7:0 | PAGE_REG | R/W | Binary value determines the value of the accessed register page. | 0 |

# Section 8: Electrical Characteristics

## Absolute Maximum Ratings

*Table 168: Absolute Maximum Ratings*

| Symbol | Parameter and Pins | Minimum | Maximum | Units |
|---|---|---|---|---|
| – | Supply voltage: PLLDVDD, PLLAVDD, PLLAVDD2,SAVDD, DVDD | GND–0.3 | 1.50 | V |
| – | Supply voltage: OVDD2, XTALVDD | GND–0.3 | 2.75 | V |
| – | Supply voltage: OVDD | GND–0.3 | 3.63 | V |
| $I_I$ | Input current | – | ±10 | mA |
| $T_{STG}$ | Storage temperature | –40 | +125 | °C |
| $V_{ESD}$ | Electrostatic discharge | – | 1000 | V |
| – | Input voltage: digital input pins | GND–0.3 | 3.63 | V |

**Note**: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

## Recommended Operating Conditions

*Table 169: Recommended Operating Conditions*

| Symbol | Parameter | Pins | Minimum | Maximum | Units |
|---|---|---|---|---|---|
| VDD | Supply voltage | PLLDVDD, PLLAVDD, PLLAVDD2,SAVDD, DVDD | 1.14 | 1.26 | V |
| | | OVDD2, XTALVDD | 2.38 | 2.63 | V |
| | | OVDD (RGMII mode) | 2.38 | 2.63 | V |
| | | OVDD (GMII/RvMII mode) | 3.14 | 3.47 | V |
| $V_{IH}$ | High-level input voltage | All digital inputs | 2.0 | – | V |
| $V_{IL}$ | Low-level input voltage | All digital inputs | – | 0.8 | V |
| $T_A$ | Ambient operating temperature | | 0 | 70 | °C |

# Electrical Characteristics

*Table 170: Electrical Characteristics*

| Symbol | Parameter | Pins | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{DD}$* | Maximum supply current | 1.2V Power rail | – | 0.718 | 0.725 | 0.812 | Amps |
| | | 2.5V Power rail | – | 0.005 | 0.010 | 0.012 | Amps |
| | | OVDD (2.5V) | – | 0.023 | 0.026 | 0.028 | Amps |
| | | OVDD (3.3V) | – | 0.023 | 0.026 | 0.028<br>IMP port | Amps |
| $V_{OH}$ | High-level output voltage | Digital output pins | $I_{OH}$ = –8 mA | 2.1 | – | – | V |
| $V_{OL}$ | Low-level output voltage | Digital output pins | $I_{OL}$ = +8 mA | – | – | 0.5 | V |
| $V_{OP}$ | Transmitter output peak-to-peak differential voltage | Serdes output pins | Programmable | 150 | 500 | 1000 | mV |
| $V_{IH}$ | High-level input voltage | Digital input pins | – | 1.7 | – | – | V |
| | | XTALI<br>Does not include Digital Pins Pulldown (DPM) | – | 1.7 | – | – | V |
| $V_{IH}$ | High-level input voltage | Digital Pins Pulldown (DPD) | – | 2.0 | – | – | V |
| $V_{IL}$ | Low-level input voltage | Digital input pins | – | –0.3 | – | 0.7 | V |
| | | XTALI | – | –0.3 | – | 0.8 | V |
| $V_{ID}$ | Peak-to-peak differential input voltage | Serdes Input Pins | AC coupled input signal, DC level biased in receiver | 100 | – | 2000 | mV |
| $I_I$ | Input current | Digital inputs w/ pullup resistors | $V_I$ = OVDD2 | – | – | +100 | µA |
| | | Digital inputs w/ pullup resistors | $V_I$ = GND | – | – | –200 | µA |
| | | Digital inputs w/ pulldown resistors | $V_I$ = OVDD2 | – | – | +200 | µA |
| | | Digital inputs w/ pulldown resistors | $V_I$ = GND | – | – | –10 | µA |
| | | All other digital inputs | GND ≤ $V_I$ ≤ OVDD2 | – | – | ±100 | µA |
| $I_{OZ}$ | High-impedance output current | All three-state outputs | GND ≤ $V_O$ ≤ OVDD2 | – | – | ±10 | µA |
| | | All open-drain outputs | $V_O$ = OVDD2 | – | – | ±10 | µA |

***Table 170: Electrical Characteristics (Cont.)***

| Symbol | Parameter | Pins | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $R_{IN}$ | Receiver input impedance | Serdes input pins | Differential, integrated on-chip | 80 | 100 | 120 | Ω |
| $R_O$ | Transmitter output impedance | Serdes output pins | Differential | 80 | 100 | 120 | Ω |

# Section 9: Timing Characteristics

## Reset and Clock Timing

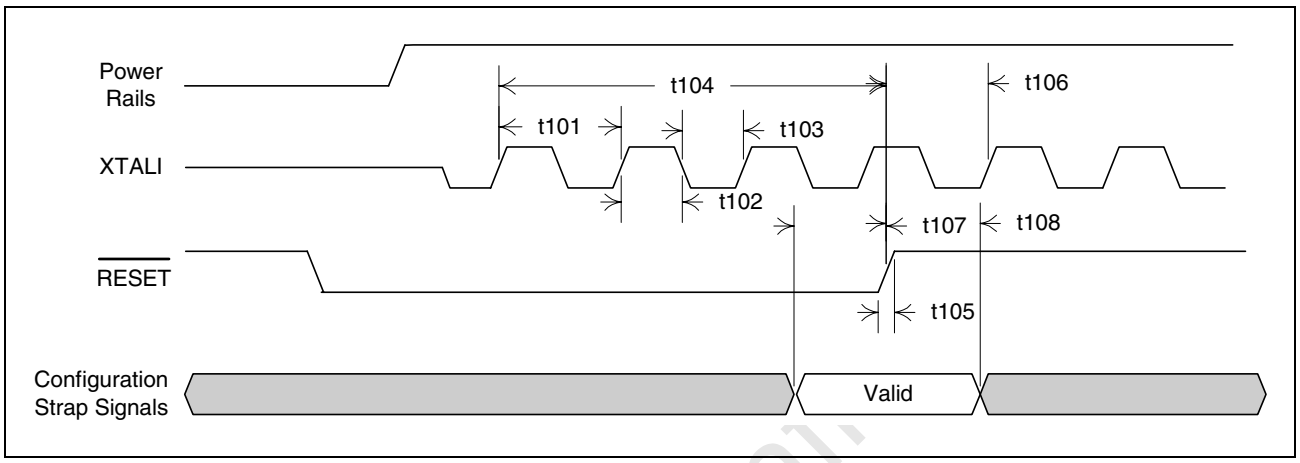


**Figure 31: Reset and Clock Timing**

***Table 171: Reset and Clock Timing***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* |
|---|---|---|---|---|
| XTALI period | t101 | 39.998 ns | 40 ns | 40.002 ns |
| XTALI high time | t102 | 18 ns | – | 22 ns |
| XTALI low time | t103 | 18 ns | – | 22 ns |
| $\overline{\text{RESET}}$ low pulse duration | t104 | 400 ns | 50 ms | – |
| $\overline{\text{RESET}}$ rise time | t105 | – | – | – |
| Configuration valid setup to $\overline{\text{RESET}}$ rising | t107 | 100 ns | – | – |
| Configuration valid hold from $\overline{\text{RESET}}$ rising | t108 | – | – | 0 ns |

# Serial Interface Timing

The following specifies timing information regarding the Serial Interface.

## Serial Interface Output Timing

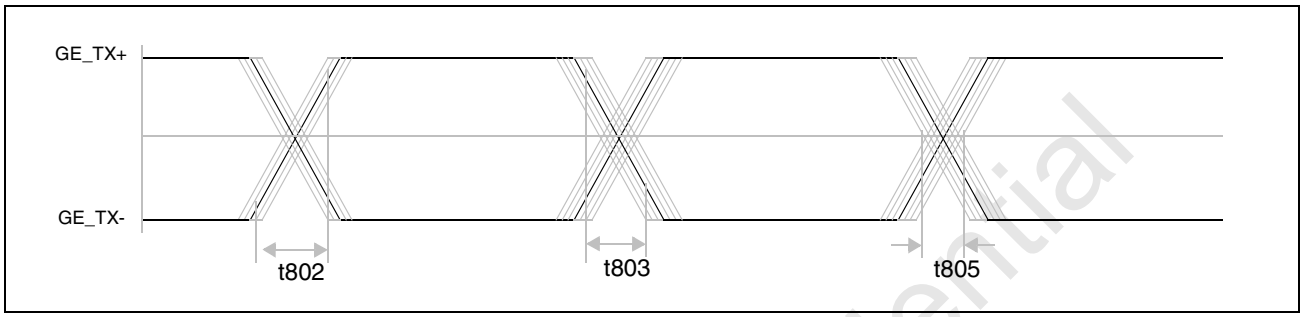


**Figure 32: Serial Interface Output Timing**

***Table 172: Serial Interface Output Timing***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| SGTX Signaling Speed | t801 | — | 1.25 | — | GBd |
| SGTX Rise Time (20%-80%) | t802 | 100 | — | 200 | ps |
| SGTX Fall Time (20%- 80%) | t803 | 100 | — | 200 | ps |
| SGTX Output Differential Skew (SGTX+ vs.SGTX-) | t804 | — | — | 20 | ps |
| SGTX Total Jitter | t805 | — | — | 192 | ps |

## Serial Interface Input Timing

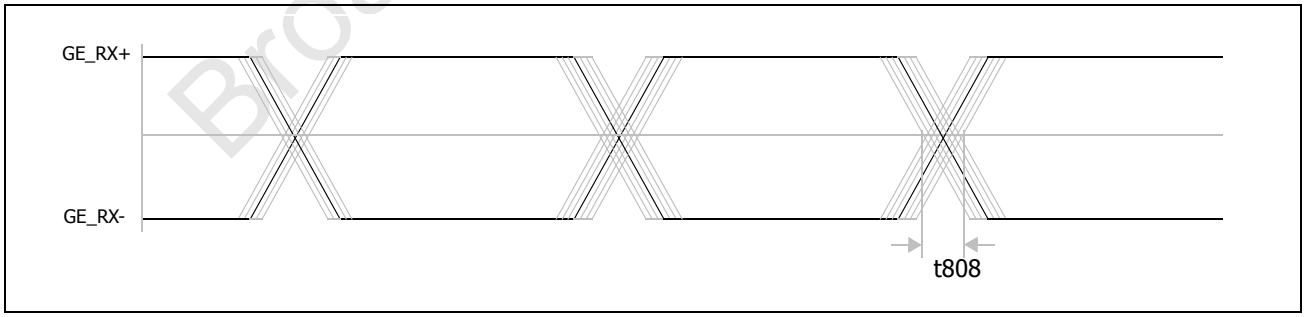


**Figure 33: Serial Interface Input Timing**

*Table 173: Serial Interface Input Timing*

| Description | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| SGRX Signaling Speed | t806 | — | 1.25 | — | GBd |
| SGRX Input Differential Skew (SGRX+ vs.SGRX-) | t807 | — | — | 40 | ps |
| SGRX Jitter (pk-pk) | t808 | — | — | 480 | ps |
| SGRX Differential Input (pk-pk) | t809 | 0.1 | — | 2.0 | V |

# Reverse MII (RvMII) Timing

The following specifies timing information regarding the IMP interface pins when configured in Reverse MII mode.

## Reverse MII Output Timing

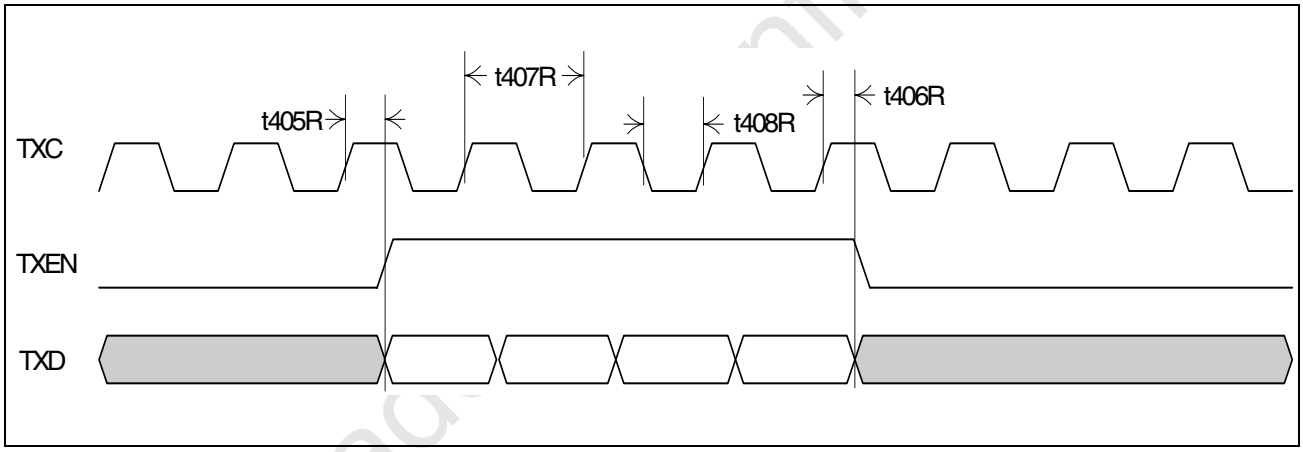


**Figure 34: RvMII Mode Output Timing**

*Table 174: RvMII Mode Output Timing*

| Parameter | Description | Minimum | Typical | Maximum |
|---|---|---|---|---|
| t405R | TXC high to TXEN, TXD, TXER valid | – | – | 29 ns |
| t406R | TXC high to TXEN, TXD, TXER invalid | 11 ns | – | – |
| t407R | TXC clock period | – | 40 ns | – |
| t408R | TXC high/low time | 14 ns | – | 26 ns |

# Reverse MII Input Timing

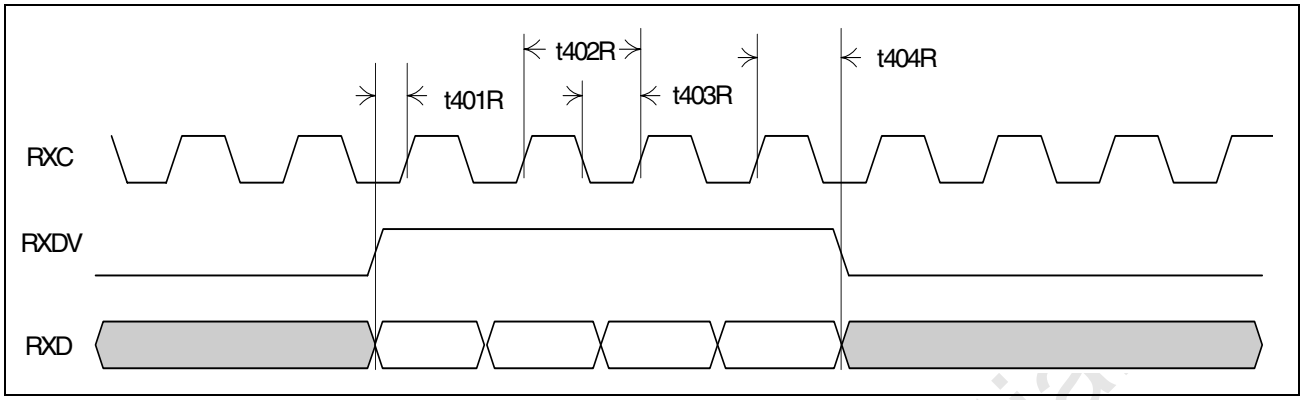


**Figure 35: RvMII Mode Input Timing**

***Table 175: RvMII Mode Input Timing***

| *Parameter* | *Description* | *Minimum* | *Typical* | *Maximum* |
|---|---|---|---|---|
| t401R | RXDV, RXD, RXER, to RXC rising setup time | 15 ns | – | – |
| t402R | RXC clock period (100BASE-TX mode only) | – | 40 ns | – |
| t403R | RXC high/low time (100BASE-TX mode only) | 14 ns | – | 26 ns |
| t404R | RXDV, RXD, RXER, to RXC rising hold time | 0 ns | – | – |

# RGMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in RGMII mode.

## RGMII Output Timing (Normal Mode)

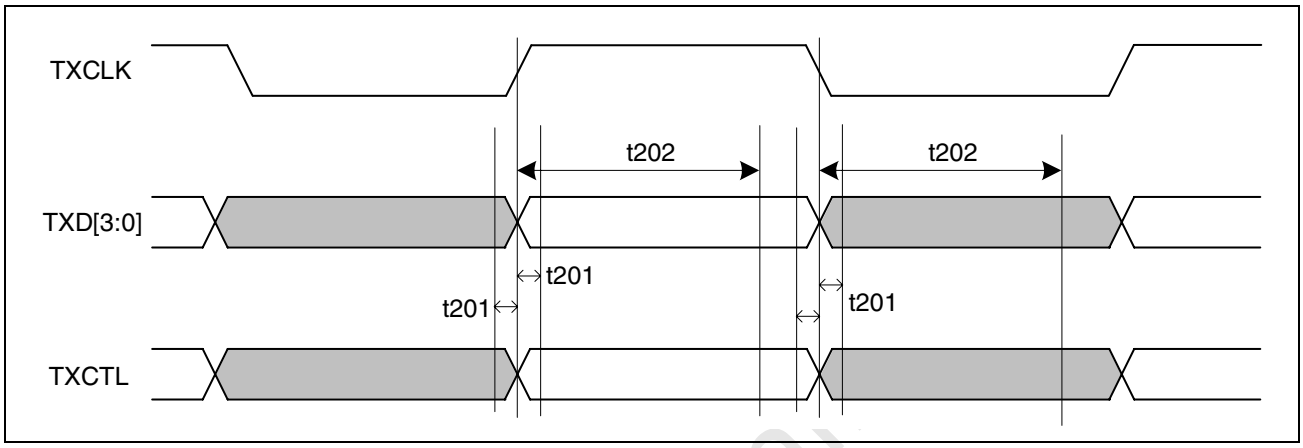


**Figure 36: RGMII Output Timing (Normal Mode)**

***Table 176: RGMII Output Timing (Normal Mode)***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| TXCLK clock period (1000M mode) | – | 7.2 | 8 | 8.8 | ns |
| TXCLK clock period (100M mode) | – | 32 | 40 | 48 | ns |
| TXCLK clock period (10M mode) | – | 320 | 400 | 480 | ns |
| Data valid to clock transition: Available setup time at the output source | t201 | –500 (1000M) | – | +500 (1000M) | ps |
| Clock transition to data valid: Available hold time at the output source | t202 | 1.2 | – | – | ns |

**Note:** The output timing in 10/100M operation is always as specified in the delayed mode.

# RGMII Output Timing (Delayed Mode)

RGMII Output Timing defaults to the delayed mode when the TXC_DELAY pin is pulled high at power-on reset.

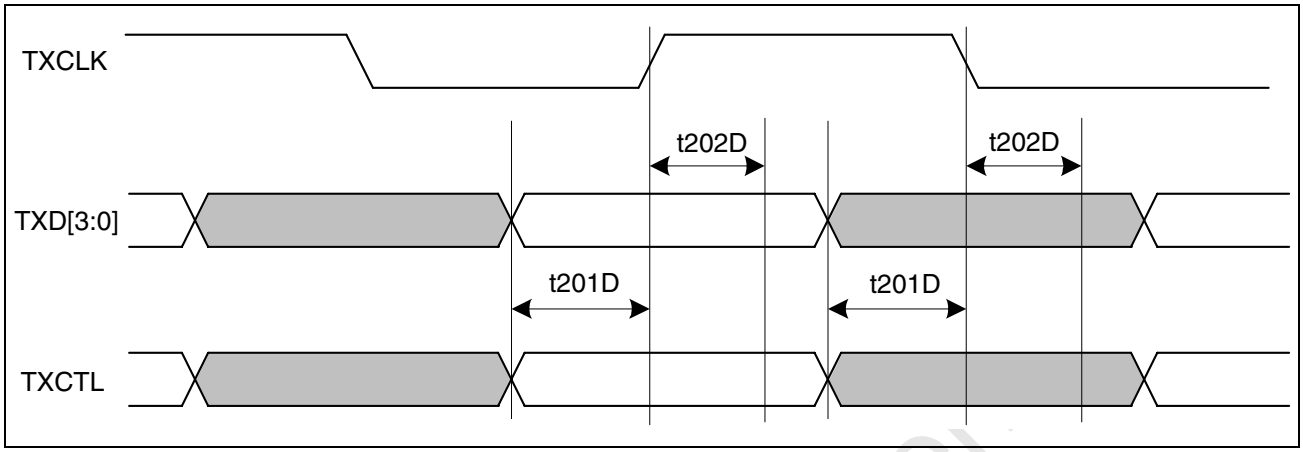


**Figure 37: RGMII Output Timing (Delayed Mode)**

***Table 177: RGMII Output Timing (Delayed Mode)***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| TXCLK clock period (1000M mode) | – | 7.2 | 8 | 8.8 | ns |
| TXCLK clock period (100M mode) | – | 32 | 40 | 48 | ns |
| TXCLK clock period (10M mode) | – | 320 | 400 | 480 | ns |
| Data valid to clock transition: Available setup time at the output source (delayed mode) | t201D | 1.2 (all speeds) | – | – | ns |
| Clock transition to data valid: Available hold time at the output source (delayed mode) | t202D | 1.2 | – | – | ns |

# RGMII Input Timing (Normal Mode)

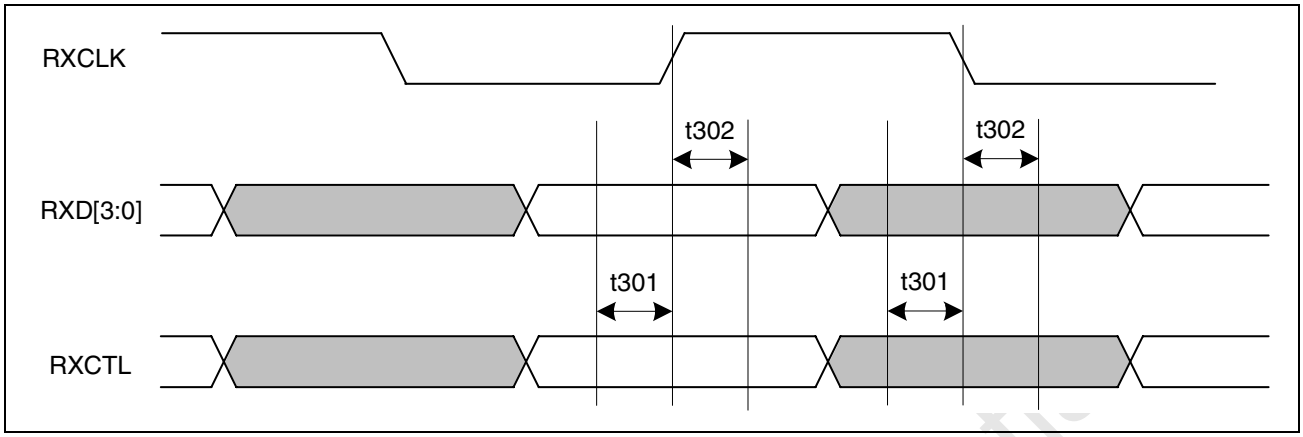


**Figure 38: RGMII Input Timing (Normal Mode)**

***Table 178: RGMII Input Timing (Normal Mode)***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| RXCLK clock period (1000M mode) | – | 7.2 | 8 | 8.8 | ns |
| RXCLK clock period (100M mode) | – | 36 | 40 | 44 | ns |
| RXCLK clock period (10M mode) | – | 360 | 400 | 440 | ns |
| Input setup time | t301 | 1.0 (all speeds) | – | – | ns |
| Input hold time | t302 | 1.0 (all speeds) | – | – | ns |
| Required data window at the input | t301+t302 | 2.0 | – | – | ns |

# RGMII Input Timing (Delayed Mode)

RGMII Input Timing defaults to the delayed mode when the RXC_DELAY pin is pulled high at power-on reset.

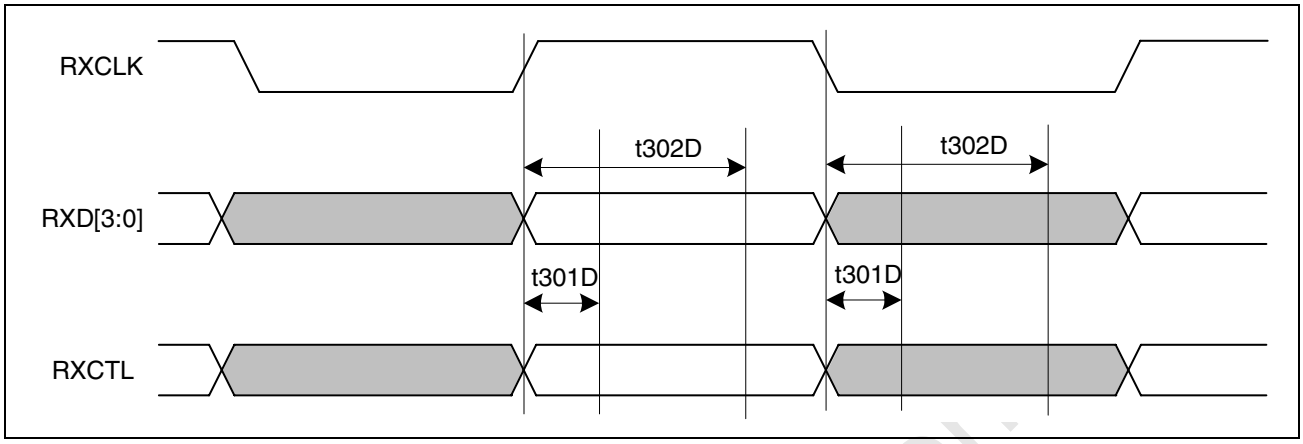


**Figure 39: RGMII Input Timing (Delayed Mode)**

***Table 179: RGMII Input Timing (Delayed Mode)***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| RXCLK clock period (1000M mode) | – | 7.2 | 8 | 8.8 | ns |
| RXCLK clock period (100M mode) | – | 36 | 40 | 44 | ns |
| RXCLK clock period (10M mode) | – | 360 | 400 | 440 | ns |
| Input setup time (delayed mode) | t301D | –1.0 (1000M) | – | – | ns |
| | | –5.0 (10/100M) | – | – | ns |
| Input hold time (delayed mode) | t302D | 3.0 (1000M) | – | – | ns |
| | | 7.0 (10/100M) | – | – | ns |
| Required data window at the input | t301D+t302D | 2.0 | – | – | ns |

# GMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in GMII mode.

## GMII Interface Output Timing

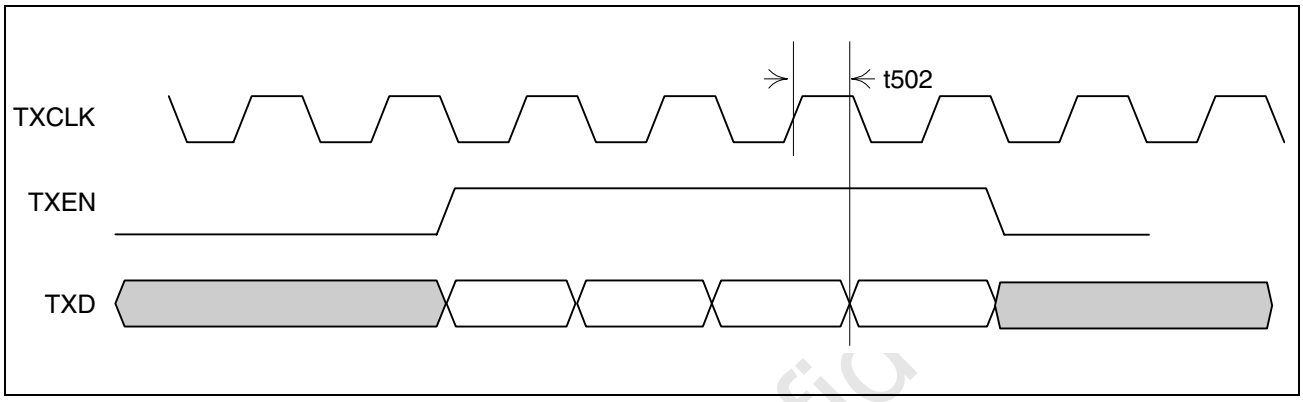


**Figure 40: GMII Output Timing**

***Table 180: GMII Output Timing***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| TXCLK clock period (1000M mode) | – | – | 8 | – | ns |
| TXCLK clock period (100M mode) | – | – | 40 | – | ns |
| TXCLK clock period (10M mode) | – | – | 400 | – | ns |
| Output delay from TXCLK rising | t502 | 0.5 | – | 5.5 | ns |

# GMII Interface Input Timing

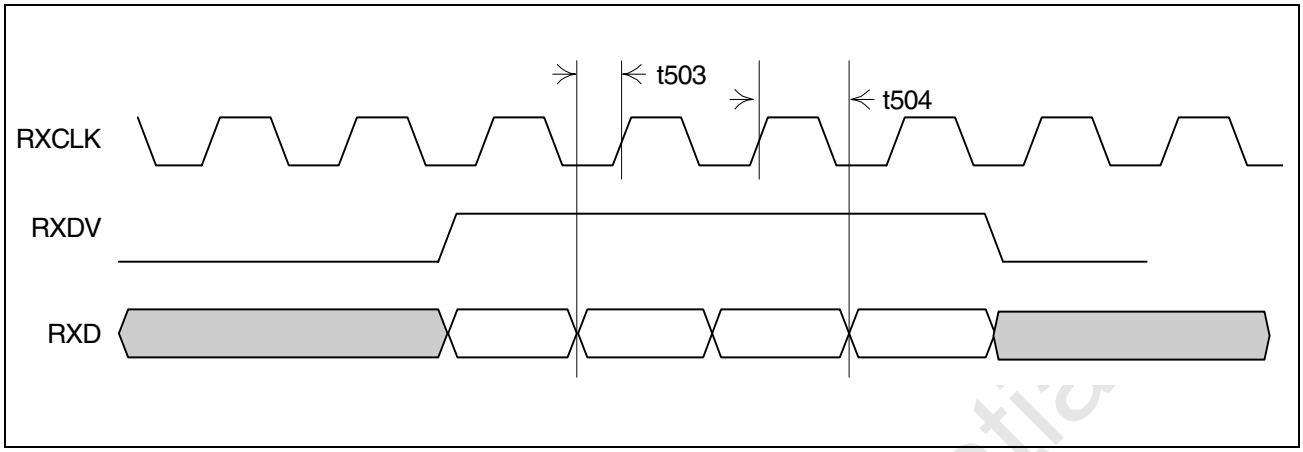


**Figure 41: GMII Input Timing**

***Table 181: GMII Input Timing***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| RXCLK clock period (1000M mode) | – | – | 8 | – | ns |
| RXCLK clock period (100M mode) | – | – | 40 | – | ns |
| RXCLK clock period (10M mode) | – | – | 400 | – | ns |
| Input setup time | t503 | 2.0 | – | – | ns |
| Input hold time | t504 | 0.0 | – | – | ns |

# MDC/MDIO Timing

The following specifies timing information regarding the MDC/MDIO interface pins.

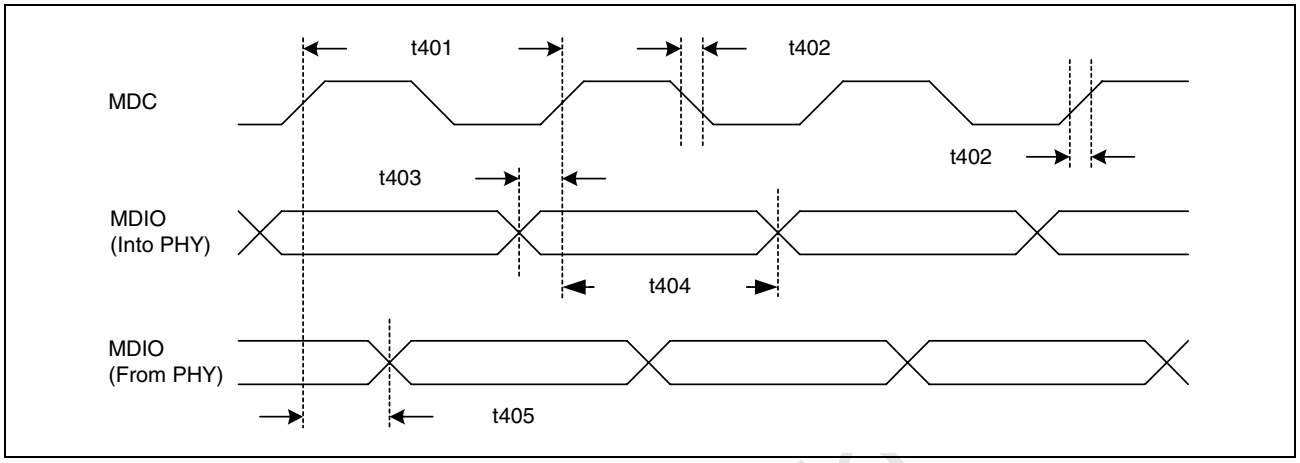


**Figure 42: MDC/MDIO Timing (Slave Mode)**

***Table 182: MDC/MDIO Timing (Slave Mode)***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| MDC cycle time | t401 | 80 | – | – | ns |
| MDC high/low | – | 30 | – | – | ns |
| MDC rise/fall time | t402 | – | – | 10 | ns |
| MDIO input setup time to MDC rising | t403 | 7.5 | – | – | ns |
| MDIO input hold time from MDC rising | t404 | 7.5 | – | – | ns |
| MDIO output delay from MDC rising | t405 | 0 | – | 45 | ns |

***Table 183: MDC/MDIO Timing (Master Mode)***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| MDC cycle time | t401 | 80 | – | – | ns |
| MDC high/low | – | 30 | – | – | ns |
| MDC rise/fall time | t402 | – | – | 10 | ns |
| MDIO input setup time to MDC rising | t403 | 20 | – | – | ns |
| MDIO input hold time from MDC rising | t404 | 0 | – | – | ns |
| MDIO output delay from MDC rising | t405 | 15 | – | 65 | ns |

# Serial LED Interface Timing

The following specifies timing information regarding the LED interface pins.

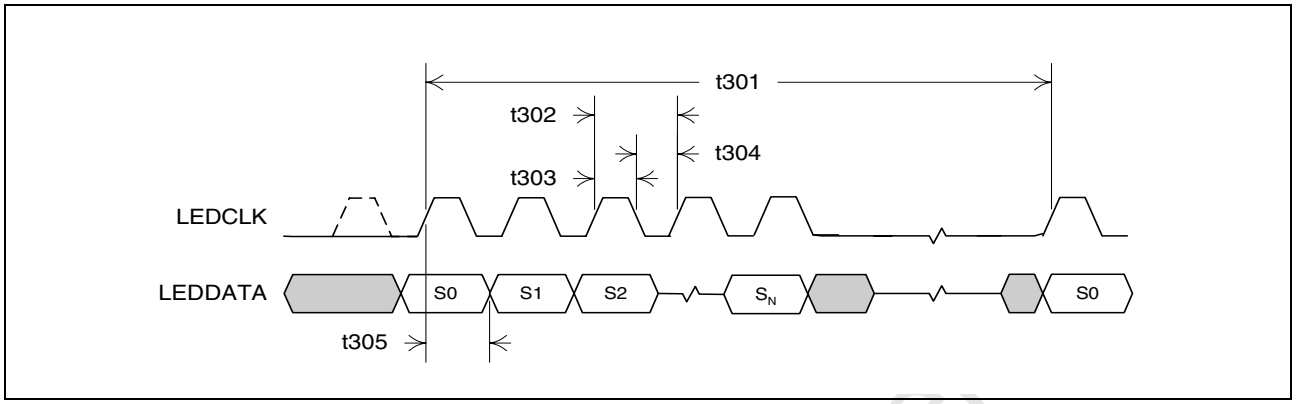


**Figure 43: Serial LED Interface Timing**

***Table 184: Serial LED Interface Timing***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* | *Unit* |
|---|---|---|---|---|---|
| LED update cycle period | t301 | – | 42 | – | ms |
| LEDCLK period | t302 | – | 640 | – | ns |
| LEDCLK high-pulse width | t303 | 310 | – | 330 | ns |
| LEDCLK low-pulse width | t304 | 310 | – | 330 | ns |
| LEDCLK to LEDDATA output time | t305 | 270 | – | 340 | ns |

# SPI Timing

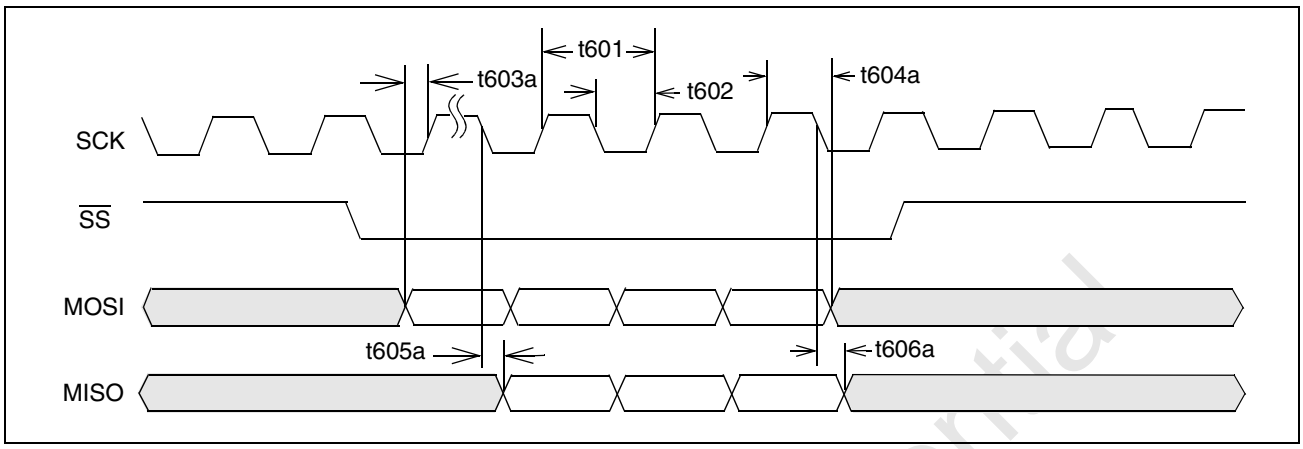


**Figure 44: SPI Timing, $\overline{SS}$ Asserted During SCK High**

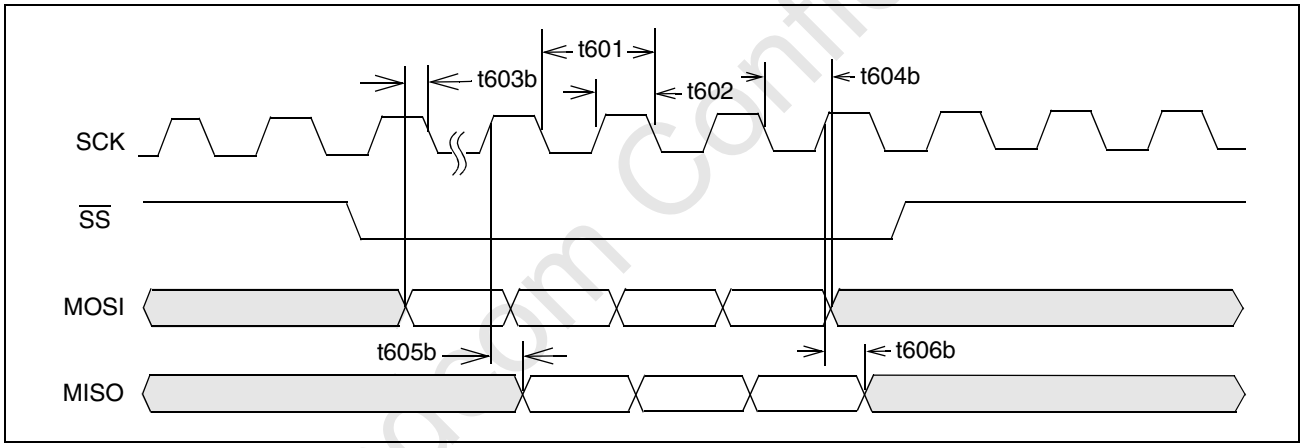


**Figure 45: SPI Timing, $\overline{SS}$ Asserted During SCK Low**

***Table 185: SPI Timing***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* |
|---|---|---|---|---|
| SCK clock period | t601 | – | 500 ns | – |
| SCK high/low time | t602 | 200 ns | – | 300 ns |
| MOSI to SCK setup time | t603a, t603b | 5 ns | – | – |
| MOSI to SCK hold time | t604a, t604b | 12 ns | – | – |
| SCK to MISO valid | t605a, t605b | – | – | 25 ns |
| SCK to MISO invalid | t606a, t606b | 0 ns | – | – |

**Note:** The BCM5387 behaves only as a slave device. $\overline{SS}$ is asynchronous. If $\overline{SS}$ is asserted during SCK high, then the BCM5387 samples data on the rising edge of SCK and references the falling edge to output data. Otherwise, the BCM5387 samples data on the falling edge and outputs data on the rising edge of SCK.

# EEPROM Timing

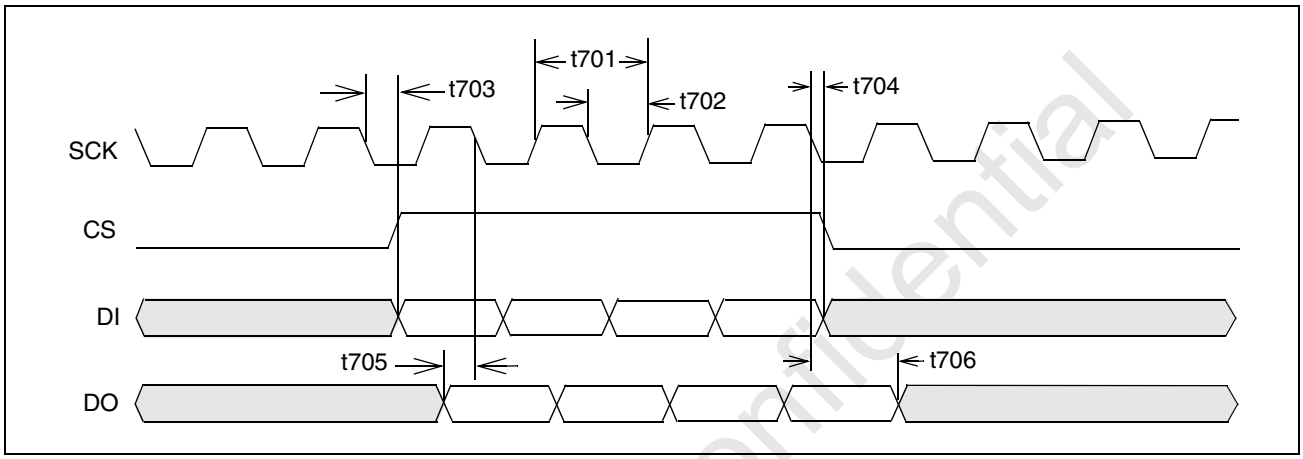


**Figure 46: EEPROM Timing**

***Table 186: EEPROM Timing***

| *Description* | *Parameter* | *Minimum* | *Typical* | *Maximum* |
|---|---|---|---|---|
| SCK clock frequency | t701 | – | 100 KHz | – |
| SCK high/low time | t702 | – | 5 us | – |
| SCK low to CS, DI valid | t703 | – | – | 500 ns |
| SCK low to CS, DI invalid | t704 | 500 ns | – | – |
| DO to SCK falling setup time | t705 | 200 ns | – | – |
| DO to SCK falling hold time | t706 | 200 ns | – | – |

# Section 10: Thermal Characteristics

***Table 187: Thermal Characteristics***

| *Airflow* | *Measured at 0m/s* |
|---|---|
| $Theta_{JA}$ (°C/W) | 25.38 |
| $Theta_{JB}$ (°C/W) | 10.41 |
| $Theta_{JC}$ (°C/W) | 9.45 |
| Maximum junction temperature $T_{JA}$ (°C) | 125 |

# Section 11: Mechanical Information

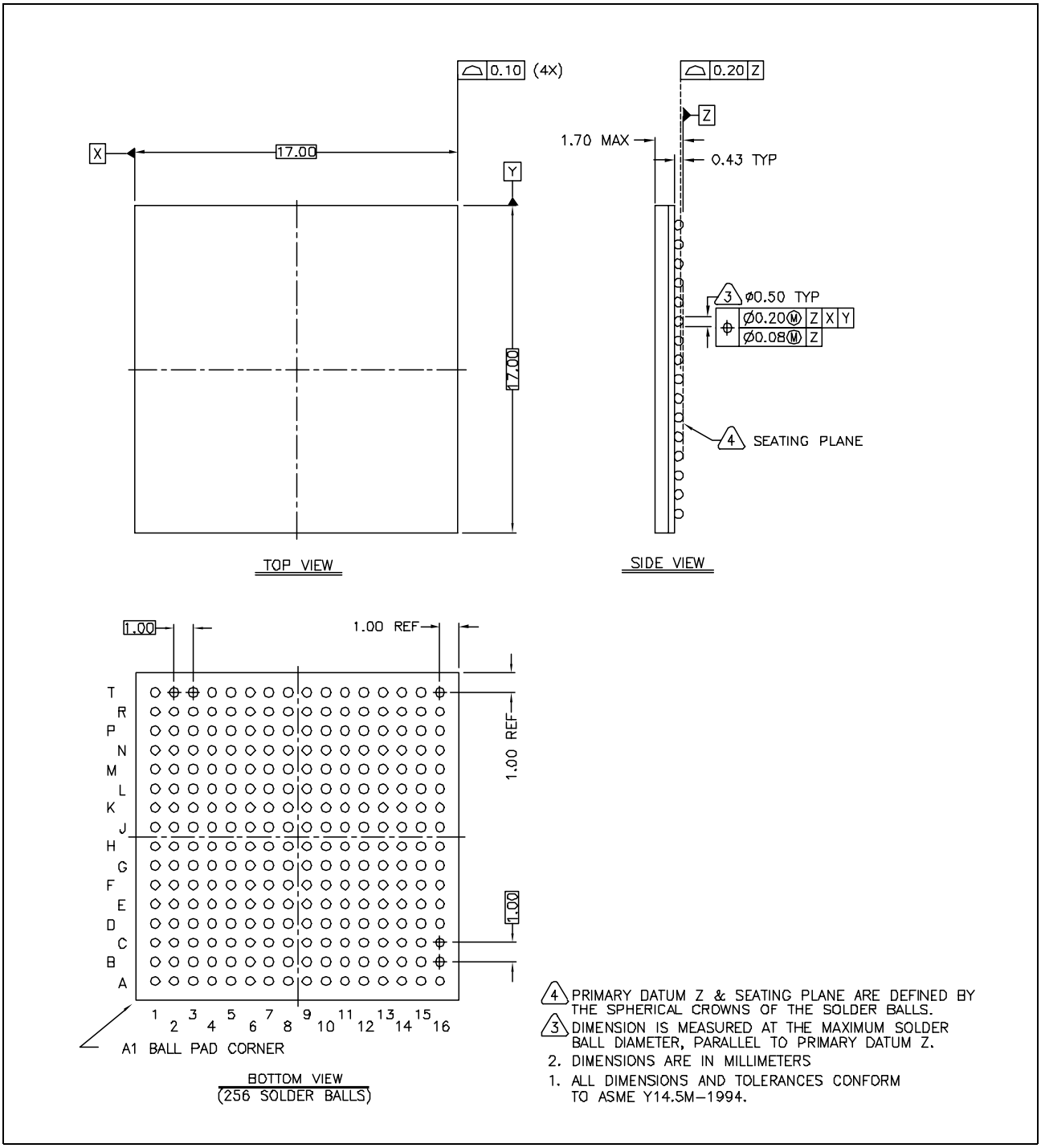


**Figure 47: 256-FBGA Package Outline Drawing**

# Section 12: Ordering Information

| *Part Number* | *Package* | *Ambient Temperature* |
|---|---|---|
| BCM5387KFB(G) | 256-FBGA | 0°C to 70°C |
| BCM5387IFB(G) | 256-FBGA | –40°C to 85°C |

**Note:** (G) represents the lead-free package option.

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