Data Sheet

BCM5396

Single-Chip 16-Port SerDes Gigabit Switch

The BCM5396 is a 16-port Gigabit Ethernet (GbE) switch integrated with 16 1.25G SerDes/SGMII port interfaces for connecting to external Gigabit PHYs or fiber modules. The BCM5396 provides the lowest-power and cost GbE functionality to the desktop switching solution or WebSmart application.

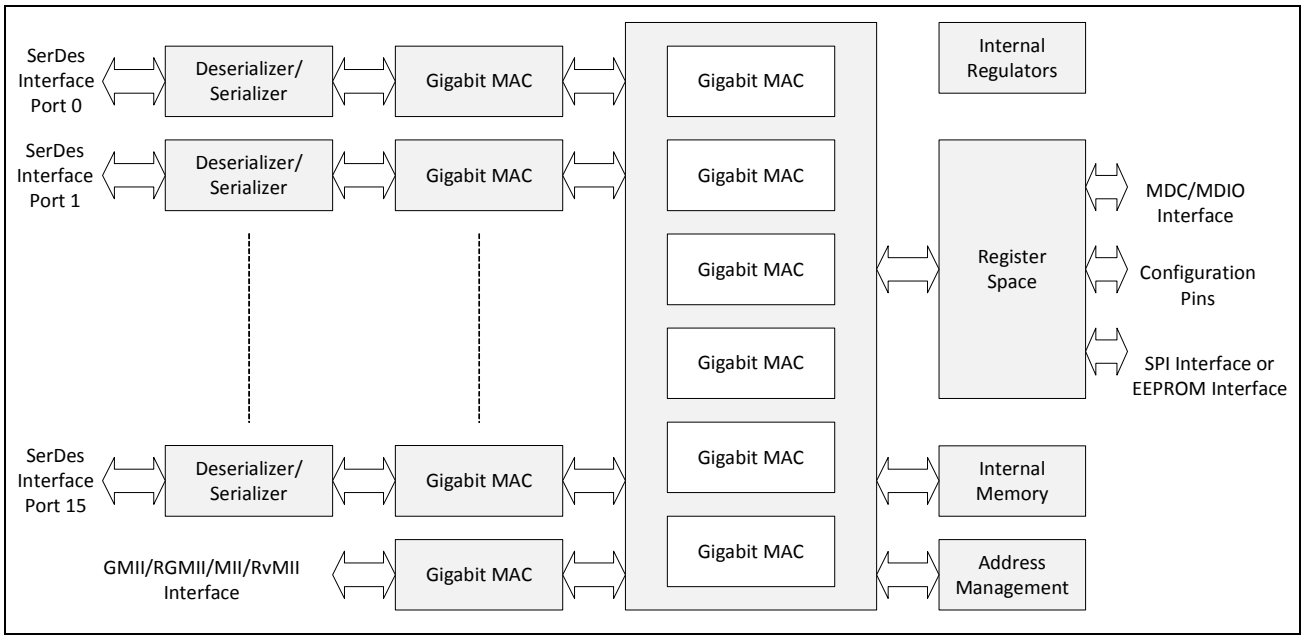
The BCM5396 is a highly integrated solution, combining all of the functions of a high-speed switch system, including packet buffer, Media Access Controllers (MACs), address management, and a non-blocking switch controller into a single monolithic 0.13 µm CMOS device. The BCM5396 complies with the IEEE 802.3, 802.3u, 802.3ab, and 802.3x specifications, including the MAC control PAUSE frame and auto-negotiation subsections, providing compatibility with all industry-standard Ethernet, Fast Ethernet, and GbE devices.

The BCM5396 device provides integrated 1.25G SerDes, reducing board footprint requirements. The 16 ports have SGMII interfaces for connecting with external GbE transceivers.

- 16-port 10/100/1000 Mbps integrated switch controller via 1.25G SerDes/SGMII/fiber
- Embedded 256 KB on-chip packet buffer
- One 10/100/1000 Mbps In-band Management Port (IMP) with GMII/RGMII/RvMII/MII interface for PHY-less connection to a CPU/management entity (for management purposes only)
- Integrated address management
- Supports up to 4K MAC addresses
- Supports jumbo frames up to 9728 bytes.
- Supports EEPROM for low-cost chip configuration
- Integrated Motorola SPI-compatible interface
- Supports port mirroring
- Port-based VLAN and 4K IEEE 802.1Q tag VLAN
- Port-, DiffServ-, MAC-, and IEEE 802.1p-based QoS for four queues
- Supports Spanning Tree, Rapid Spanning Tree, and Multiple Spanning Tree protocols (802.1D/1s/1w)
- Supports IEEE Standard 802.1X port security
- Supports pseudo-PHY MDIO access
- MAC-based trunking with link fail-over
- Ethernet-in-the-last-mile (EFM) support: OAM and P
- Low-power (2.2W total) 1.2V core/2.5V (SGMII I/O)/3.3V (GMII/MII/RvMII) and 2.5V RGMII operation with 3.3V I/O tolerance
- 256-pin FBGA package

5396-DS116-R

Figure 1: Functional Block Diagram



Revision History

Revision	*Date*	*Change Description*
5396-DS116-R	06/20/16	**Updated:** • "Register Access Through Pseudo-PHY Interface" on page 66 • "MDC/MDIO Interface Register Programming" on page 71 • "Port 16 (IMP) State Override Register (Page 00h: Address 70h)" on page 98 • Table 93: "Internal SerDes Registers Page Descriptions 10h–1Fh," on page 127 • Table 94: "Internal SerDes Registers Page 10h–1Fh," on page 127 • Table 176: "MDC[0]/MDIO[0] Timing," on page 188
5396-DS115-R	11/17/14	**Updated:** • Figure 38: "256-Pin FBGA Package Outline Drawing," on page 199
5396-DS114-R	10/04/13	**Added:** • "Ethertype Based QoS" on page 30 **Updated:** • Figure 2: "Priority Packet Mapping Flow," on page 28 • Table 1: "Frame Priority Decision Tree Summary," on page 31 • "Jumbo Frame Support" on page 34 • Table 18: "Pseudo-PHY MII Register Definitions," on page 73 • "Serial LED Interface" on page 75 • Table 46: "External PHY Scan Control Register (Page 00h: Address 86h)," on page 107 • Table 228: "Serial LED Interface Timing," on page 214
5396-DS113-R	02/07/12	**Updated:** • Table 139: "Internal SerDes Registers Page Descriptions 10h–1Fh," on page 145. • Table 140: "Internal SerDes Registers Page 10h–1Fh," on page 145. • Table 192: "New Priority Map Register (Pages 34h: Address 0C–0Fh)," on page 185.
5396-DS112-R	06/10/10	**Updated:** • Table 144: "Auto-Negotiation Link Partner Ability (Page 10h–1Fh: Address 0Ah–0Bh)," on page 153. • "PRBS Status Register (Page 10h ~ 1Fh: Address 32h ~ 33h)" on page 166.
5396-DS111-R	08/26/09	**Updated:** • Section 12: "Ordering Information," on page 175.
5396-DS110-R	02/25/08	**Updated:** • "Signal Descriptions" on page 54: BIST_CLRMEM_SEL and SKIP_MEMBIST descriptions. **Removed:** • References to behavior of management frames in unmanaged mode

Revision	*Date*	*Change Description*
5396-DS109-R	11/13/07	**Updated:** • "Management Frames" on page 24, and "Frame Management" on page 32: Corrected terminology relating to the in-band management port. • Table 59, "Management Mode Registers (Page 02h)," on page 81: Changed definition of bits 7:6. **Added:** • "In-Band Management Port" on page 33: Added note. • Table 23, "Signal Descriptions," on page 53 and "Pin Assignments" on page 58: Added BIST_CLRMEM_SEL, SKIPMEMBIST, EN_EXT_CLK, and EXT_CLK signals to all signal/pin tables and figures.
5396-DS108-R	06/25/07	**Updated:** • "In-Band Management Port" on page 33. • Table 28, "10/100/1000 Port Control Register (Page 00h: Address 00h–0Fh)," on page 69 • Table 29, "IMP Port Control Register (Page 00h: Address 10h)," on page 69. • Table 66, "Global Management Configuration Register (Page 02h: Address 00h)," on page 86. • Table 229, "Thermal Properties, With External Heat Sink, 23 mm. ´ 23 mm. ´ 15 mm. Blade Fin," on page 180. **Removed:** • Memory Test Control Register (Page 00h: Address E0h) from page 75.
5396-DS107-R	07/12/06	**Updated:** • Figure 39, "256-Pin FBGA Package Outline Drawing," on page 181.
5396-DS106-R	05/24/06	**Added:** • Table 154, "BER/CRC Error Counter Register (Page 10h ~ 1Fh: Address 2Eh ~ 2Fh)," on page 128. • Table 155, "PRBS Control Register (Page 10h ~ 1Fh: Address 30h ~ 31h)," on page 128. • Table 156, "PRBS Control Register (Page 10h ~ 1Fh: Address 32h ~ 33h)," on page 128. • Table 157, "Pattern Generator Control Register (Page 10h ~ 1Fh: Address 34h ~ 35h)," on page 129. • Table 158, "Pattern Generator Control Register (Page 10h ~ 1Fh: Address 36h ~ 37h)," on page 130. • Table 159, "Pattern Generator Control Register (Page 10h ~ 1Fh: Address 36h ~ 37h)," on page 130. • Table 160, "Force Transmit 1 Register (Page 10h ~ 1Fh: Address 3Ah ~ 3Bh)," on page 130. • Table 161, "Block Address (Pages 10h–1Fh: Address 3Eh ~ 3Fh)," on page 131.

Revision	*Date*	*Change Description*
5396-DS105-R	04/19/06	**Updated:** • Features list on front cover. • “LED Interfaces” on page 50. • Table 23, “Signal Descriptions,” on page 53. • Table 24, “Pin Assignment (Listed by Pin Number),” on page 58. • Table 25, “Pin Assignment (Listed by Signal Name),” on page 60. • Figure 21, “Pins Top View,” on page 62. • Table 27, “Control Registers (Page 00h),” on page 67. • LED A, B, C, and D registers to Reserved in Table 27, “Control Registers (Page 00h),” on page 67. • Table 65, “Strap Value Register (Page 01h: Address 70h–73h),” on page 85. • Table 94, “ARL Search Result Register 0 (Page 05h: Address 3Bh–3Eh),” on page 98. • Table 95, “ARL Search MAC/VID Result Register 1 (Page 05h: Address 40h–47h),” on page 98. • Table 231, “Ordering Information,” on page 182. **Removed:** • LED A, B, C, and D register descriptions from section “Control Registers” on page 67.
5396-DS104-R	11/10/05	**Added:** • I-temp package ordering information to Table 223, “Ordering Information”.
5396-DS103-R	09/21/05	**Updated:** • The minimum, typical, and maximum for the 2.5V power rail pin in Table 208, “Electrical Characteristics”.
5396-DS102-R	09/16/05	**Updated:** • The minimum, typical, maximum, and units for the 2.5V power rail pin in Table 208, “Electrical Characteristics”. **Added:** • 3.3V power rail (IMP port) pin for IDD symbol in Table 208, “Electrical Characteristics”8.

Revision	*Date*	*Change Description*
5396-DS101-R	09/13/05	**Updated:** • Figure 16, “Serial EEPROM Connection,” on page 42. • That the AUTO_POLL_DIS pin is pulled low, not high, during power-on/ reset in “MDC/MDIO Interface” on page 44. • Figure 17, “MDC/MDIO Interface,” on page 44. • *When the switch is master-sourcing* to *When the switch is slave-driven* in “MDC/MDIO Interface Register Programming” on page 49. • In Table 23, “Signal Descriptions,” on page 53.: – Description for HW_FWDG_EN. – Type for EXTCLK. • Pages 50h–60h to Reserved in Table 26, “Global Page Register Map,” on page 64. • The Description in Table 95, “ARL Search Control Register (Page 05h: Address 30h),” on page 98. • The Default in Table 169, “Queue N Weight Register (Page 30h: Address 81h–84h),” on page 132. • Table 208, “Electrical Characteristics,” on page 158. **Added:** • Page 00 Addr 24H~25H Bit[10:8] to Table 19, “Serial LED Mode Matrix,” on page 50. **Removed:** • From Table 7, “Behavior for Reserved Multicast Addresses,” on page 19: – 01-80-C2-00-00-01 – 01-80-C2-00-00-10
5396-DS100-R	04/15/05	Initial release.

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About This Document

Purpose and Audience

This document provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM5396. This document is for designers interested in integrating the BCM5396 switch into their hardware designs and for others who need specific data about the physical characteristics and operation of the BCM5396 switch.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

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In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

Section 1: Introduction

Overview

The BCM5396 is a single-chip, 16-port switch device with a 17th port dedicated to the CPU interface.

- It is a 16-port non-blocking 10/100/1000 Mbps switch controller with a SerDes/SGMII interface for connection to an external 10/100/1000 Ethernet transceiver or to the SerDes interface of a 1000 Mbps full-duplex fiber module.
- All 16 SerDes ports have SGMII interface support.
- The 17th GbE port supports a Smart/WebSmart switch.
- For WebSmart/managed applications, the 17th port supports GMII/RGMII/MII/RvMII for CPU connection.
- It contains an integrated Motorola SPI-compatible interface for register access.
- Supports Ethernet-in-the-First-Mile (EFM) for OAM and P.
- Integrates high-performance 256 KB packet buffer memory.

The GMACs support full-duplex and half-duplex operations for 10 Mbps and 100 Mbps, but they support full-duplex operations at 1000 Mbps only. Flow control is supported in the half-duplex mode with backpressure. In full-duplex mode, IEEE Standard 802.3x frame-based flow control is supported. The GMACs are IEEE Standard 802.3-compliant and support maximum frame sizes of 9728 bytes.

Data Sheet Information

The following notational conventions are used in this document:

- Signal names are shown in uppercase letters (such as DATA).
- A bar over a signal name indicates that it is active low (such as $\overline{SS}$).
- In register and signal descriptions, [n:m] indicates a range from bit n to bit m (such as [7:0] indicates bits 7 through 0, inclusive).
- The use of R, RSVD, or Reserved indicates that a bit or field is reserved by Broadcom for future use. Typically, R is used for individual bits, and RSVD or Reserved is used for fields.
- Numerical modifiers such as K or M follow traditional usage (such as 1 KB means 1,024 bytes, 100 Mbps [referring to fast Ethernet speed] means 100,000,000 bps, and 133 MHz means 133,000,000 Hz).

Section 2: Features and Operation

Overview

The BCM5396 includes the following features:

See the pages indicated for more details about these features.

Quality of Service

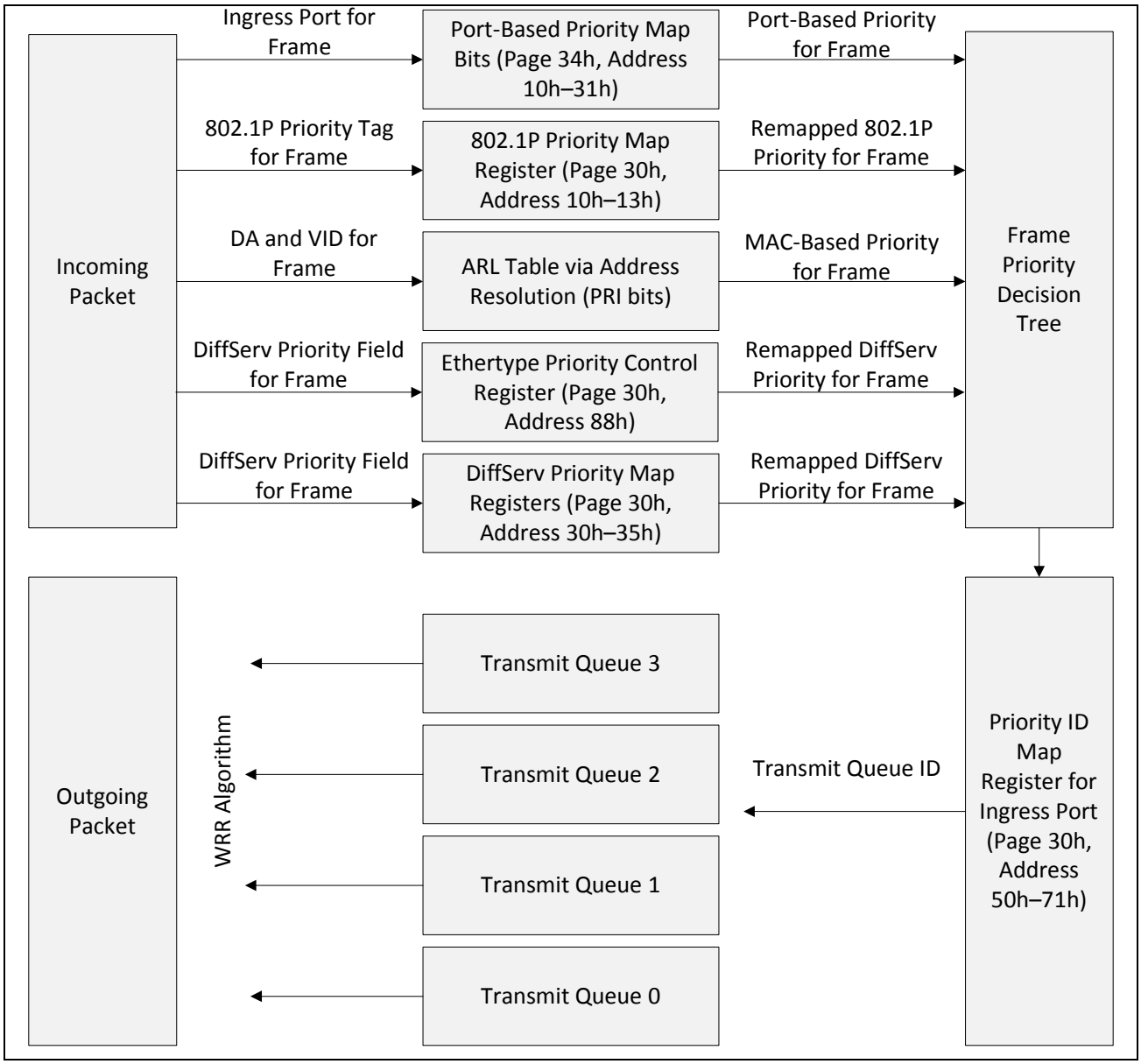
The Quality of Service (QoS) feature provides up to four internal queues per port to support four different traffic priorities. These priorities can be programmed in such a way that high-priority traffic experiences less delay in the switch under congested conditions than does low-priority traffic. This can be important in minimizing latency for delay-sensitive traffic. The BCM5396 can assign the packet to one of the four egress transmit queues, according to information in:

- "Port-Based QoS" on page 26 (Ingress Port ID)
- IEEE Standard 802.1P QoS
- MAC-Based QoS
- DiffServ QoS
- Ethertype Based QoS
- Frame Priority Decision Tree

Use Table 1 on page 28 to determine which priority system is used, based on four programmable register bits detailed in the table. This priority is then assigned to one of the four priority queues on a port-by-port basis.

Figure 2 shows a flow diagram of the priority mapping. The QoS mechanism operates at full wire speed.

Figure 2: Priority Packet Mapping Flow



Egress Transmit Queues

Each egress port can support up to four transmit queues as programmed in the "QoS TX Control Register (Page 30h: Address 80h)" on page 152. Each incoming frame is assigned to an egress transmit queue depending on its assigned priority. Each egress transmit queue is a list specifying an order for packet transmission. The corresponding egress port will transmit packets from each of the queues according to a programmable algorithm, with the higher priority queues being given greater access than the lower priority queues, with Queue 0 being the lowest priority queue.

The BCM5396 uses a Weighted Round Robin (WRR) algorithm to schedule each transmit queue. The weights for each queue can be programmed via the "Queue N (0–3) Weight Register (Page 30h: Address 81h–84h)" on page 152. The BCM5396 also supports a High Queue Preempt (HQP) feature, enabled via the "QoS TX Control Register (Page 30h: Address 80h)" on page 152, which works in conjunction with the WRR algorithm. When enabled, the highest priority queue empties first, then the lower priority queues use the WRR algorithm to schedule their transmission.

Port-Based QoS

Port-based QoS can be activated by either asserting the QoS_EN strap pin (for pin details, refer to Table 23: "Signal Descriptions," on page 77) or by programming the "QoS Global Control Register(Page 30h: Address 00h)" on page 146.

The priority of the ingress port is determined by the PORT_QOS_PRI, bits [15:13] of the "Port N (0–16) Default 802.1Q Tag Register (Page 34h: Address 10h–31h)" on page 162. The value of these bits determines the port-based priority assigned to each frame arriving at the given ingress port. The port-based priority is assigned to the priority ID bits depending on the result of the Table 1: "Frame Priority Decision Tree Summary," on page 28. Each priority ID is mapped to one of the egress transmit queues based on the ingress port via the "QoS RX Port N (0–16) Control Register(Page 30h: Address 50h–71h)" on page 151.

If the QoS_EN strap pin referred to in "QoS Global Control Register(Page 30h: Address 00h)" on page 146 is pulled high during power-on/reset, ports[7:0] are assigned the highest queue by default, and ports[15:8] are assigned the lowest queue.

If the port-based QoS is disabled, the port-based priority for all traffic for the given ingress port will default to 0. For more information about the egress transmit queues, refer to "Egress Transmit Queues" on page 26.

IEEE Standard 802.1P QoS

IEEE Standard 802.1P QoS is enabled on a port-by-port basis via the 802_1P_EN bit in the "QoS 1P Enable Register (Page 30h: Address 04h–07h)" on page 147.

When using the IEEE Standard 802.1P priority mechanism, the packet is examined for the presence of a valid IEEE Standard 802.1P priority tag. If the tag is present, the packet is assigned a remapped IEEE Standard 802.1P priority based on the mapping in “802.1P/1Q Priority Map Register (Page 30h: Address 10h–13h)” on page 147. If the tag is not present or IEEE Standard 802.1P operation is not enabled, a MAC-based priority is assigned to the packet. The IEEE Standard 802.1P/MAC-based priority is assigned to the priority ID bits depending on the result of the Table 1: “Frame Priority Decision Tree Summary,” on page 28. The priority ID is mapped to one of the egress transmit queues based on the ingress port via the “QoS RX Port N (0–16) Control Register(Page 30h: Address 50h–71h)” on page 151. For more information about the egress transmit queues, refer to “Egress Transmit Queues” on page 26.

MAC-Based QoS

MAC-based QoS is enabled when the IEEE Standard 802.1P QoS is disabled via the QoS_EN_802_1P bit in the “QoS 1P Enable Register (Page 30h: Address 04h–07h)” on page 147.

When using MAC-based QoS, the destination address and VLAN ID are used to index the ARL table as described in “Data Sheet Information” on page 23. The matching ARL entry contains a 3-bit PRI field as shown in Table 4: “Address Table Entry for Unicast Address,” on page 39. These bits set the MAC-based priority for the frame. The MAC-based priority is assigned to the priority ID bits depending on the result in Table 4. The priority ID for the frame is mapped to one of the egress transmit queues based on the ingress port via the “QoS RX Port N (0–16) Control Register(Page 30h: Address 50h–71h)” on page 151. The PRI bits for a learned ARL entry default to priority 0. To change the default, an ARL entry is written to the ARL table as described in the “Writing an ARL Entry” on page 43. For more information about the egress transmit queues, refer to “Egress Transmit Queues” on page 26.

DiffServ QoS

DiffServ QoS is enabled on a port-by-port basis via the “QoS DiffServ Enable Register (Page 30h: Address 08h–0Bh)” on page 147. When using the DiffServ priority mechanism, the packet is classified based on the DSCP field in the IP Header. If the tag is present, the packet is assigned a remapped DiffServ priority based on the “DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)” on page 148 through the “DiffServ Priority Map 3 Register(Page 30h: Address 42h–47h)” on page 150. If the tag is not present or DiffServ is not enabled, a remapped DiffServ priority is not available, and the DiffServ priority will default to 000. The DiffServ priority is assigned to the priority ID bits depending on the result of the Table 1. Each priority ID is mapped to one of the egress transmit queues based on the ingress port via the “QoS RX Port N (0–16) Control Register(Page 30h: Address 50h–71h)” on page 151. For more information, refer to “Egress Transmit Queues” on page 26.

Ethertype Based QoS

Ethertype Based QoS can be enabled via the EtherType Pri bit in the Ethertype Priority Control Register (Page 30h : Address 88h).

The Ethertype based QoS has the highest priority QoS type. The user can designate the output queue via PRI_ETHERTYPE_QUEUE in the Ethertype Priority Control Register along with the actual Ethertype that the user is basing the QoS on.

Frame Priority Decision Tree

The frame priority decision tree determines which of the priority systems is used to determine the priority ID bits for a given frame. As summarized above, the priority ID bits for a frame can be determined according to the ingress port-based priority, IEEE Standard 802.1p priority, MAC-based priority, or DiffServ priority information. The decision as to which priority system to use is based on the Port_QoS_En bit and the QoS_Layer_Sel bits of the "QoS Global Control Register(Page 30h: Address 00h)" on page 146. Table 1 on page 28 summarizes how these programmable bits affect the derived priority. The DiffServ and IEEE Standard 802.1P QoS priorities are available only if the respective QoS is enabled and the received packet has the appropriate tagging.

Table 1: Frame Priority Decision Tree Summary

Port_QoS_En	*QoS_Layer_Sel*	*Value of Priority ID Bits*
0	00	Remapped 802.1P QoS if available; otherwise, MAC-based QoS.
0	01	Remapped DiffServ QoS if available; otherwise, priority ID = 000.
0	10	Remapped DiffServ QoS if available; otherwise, remapped 802.1P QoS if available; otherwise, MAC-based QoS.
0	11	The highest available priority of the following: remapped 802.1P QoS, remapped DiffServ QoS, or MAC-based QoS.
1	00	Port-based QoS.
1	01	Port-based QoS.
1	10	Port-based QoS.
1	11	The highest available priority of the following: Ethertype-Based QoS, Port-based QoS, remapped 802.1P QoS, remapped DiffServ QoS, or MAC-based QoS.

Note: Ethertype Based QoS is the highest priority base if enabled.

Port-Based VLAN

The port-based VLAN (Virtual LAN) feature partitions the switching ports into virtual private domains designated on a per port basis. Data switching outside of the port's private domain is not allowed. The BCM5396 provides flexible VLAN configuration for each ingress (receiving) port.

The port-based VLAN feature works as a filter, filtering out traffic destined to non-private domain ports. The private domain ports are selected for each ingress port via the "Port VLAN Control Register (Page 31h: Address 00h–43h)" on page 154. For each received packet, the ARL resolves the DA and obtains a forwarding vector, a list of ports to which the frame shall be forwarded. The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the non-private domain ports. The frame is forwarded only to those that meet the ARL table criteria and the port-based VLAN criteria.

IEEE Standard 802.1Q VLAN

The BCM5396 supports IEEE Standard 802.1Q VLAN and up to approximately 4096 VLAN table entries that reside in the internal memory (the entire memory capacity). Once the VLAN table is programmed and maintained by the microcontroller, the BCM5396 autonomously handles all operations of the protocol. These actions include the stripping or adding of the IEEE Standard 802.1Q tag depending on the requirements of the individual transmitting port. BCM5396 also performs all the necessary VLAN lookups in addition to MAC L2 lookups.

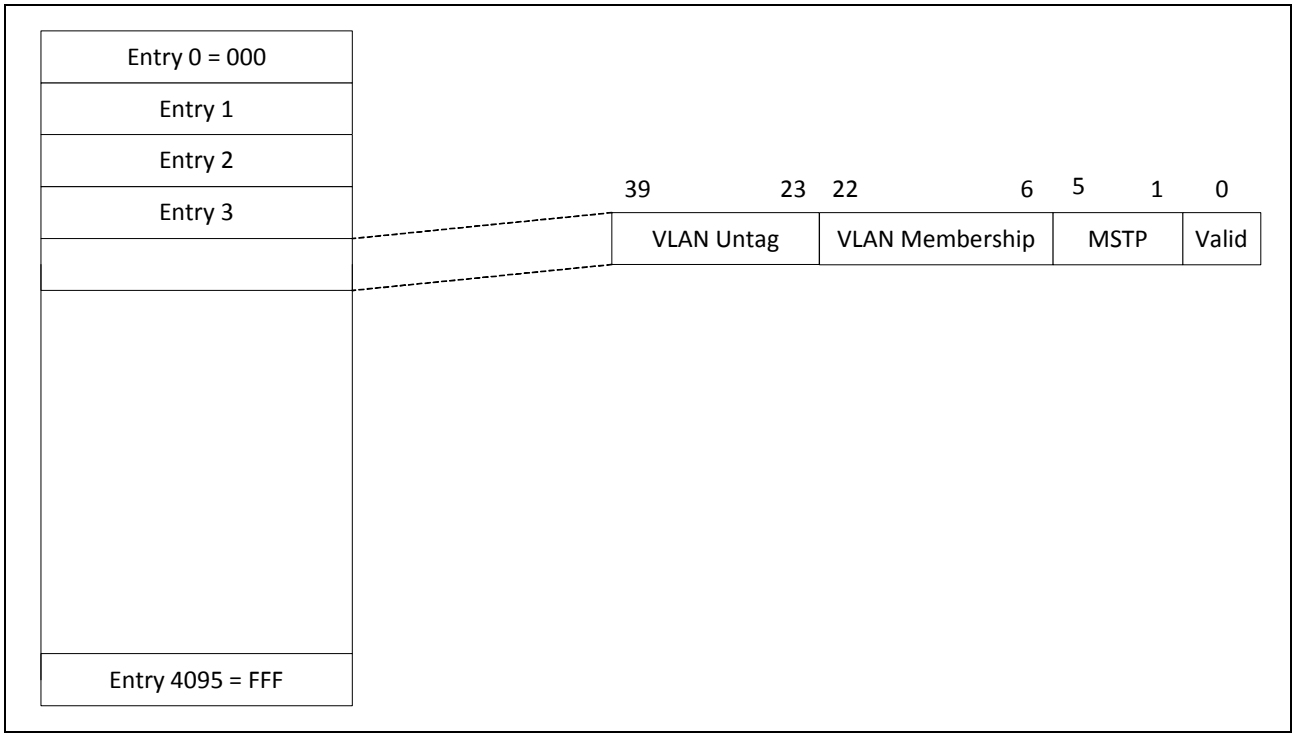
VLAN Table Organization

Each VLAN table entry, also referred to as a VID or VLAN ID, consists of a valid bit, untag map, and forward map.

- The valid bit designates whether the VID is valid.
- The untag map controls whether the egress packet is tagged or untagged.
- The forward map defines the membership within a VLAN domain.

The untag map and forward map include bit-wise representation of all the ports.

Figure 3: VLAN Table Organization



Programming the VLAN Table

The IEEE Standard 802.1Q VLAN feature can be enabled by writing to the EN_1QVLAN bit in the "Global Control 0 Register (Page 34h: Address 00h)" on page 158. The default priority and VID can be assigned to each port in the "Port N (0–16) Default 802.1Q Tag Register (Page 34h: Address 10h–31h)" on page 162. These priorities and VIDs are necessary when tagging a previously untagged frame. The hashing algorithm uses either [VID, MAC] or [MAC] for the ARL index key, depending on the VLAN_LEARN_MODE (this applies only to hashing and should not be confused with VLAN learning) bit in the Global Control 0 Register (Page 34h: Address 00h). If both the VID and MAC address are used, a single MAC address is able to be a member of multiple VLANs simultaneously.

Write the VLAN table using the following steps:

1. Use the "VLAN Table Entry Register (Page 05h: Address 63h–6Ah)" on page 123 to define which ports are part of the VLAN group and which ports should be untagged. The Valid bit should be set to 1.
2. Use the "VLAN Table Address Index Register (Page 05h: Address 61h–62h)" on page 122 to define the VLAN ID of the VLAN group.

Note: 000h and FFFh are not valid VID numbers.

3. Set bit 0 of the "VLAN Table Read/Write Control Register (Page 05h: Address 60h)" on page 122 to 0, indicating a write operation.
4. Set bit 7 of the "VLAN Table Read/Write Control Register (Page 05h: Address 60h)" on page 122 to 1, starting the write operation. This bit returns to 0 when the write is complete.

Read the VLAN table using the following steps:

1. Use the "VLAN Table Address Index Register (Page 05h: Address 61h–62h)" on page 122 to determine from which VLAN group to read the data.
2. Set bit 0 of the "VLAN Table Read/Write Control Register (Page 05h: Address 60h)" on page 122 to 1, to indicate a read operation.
3. Set bit 7 of the "VLAN Table Read/Write Control Register (Page 05h: Address 60h)" on page 122 to 1, to start the read operation. This bit returns to 0 when the read is complete.
4. Read the "VLAN Table Read/Write Control Register (Page 05h: Address 60h)" on page 122 to obtain the VLAN table entry information.

Jumbo Frame Support

The Jumbo Frame support requirements are:

- Definition of over size packets:
  - The packets above 1518 bytes for untagged packets are considered as over size packets.
  - The packets above 1522 bytes for tagged packets are considered as over size packets.
- When Jumbo Frame support is off:
  - The packets above 1536 bytes are considered as bad packets and dropped.
  - The number 1536 is rather an arbitrary number from the design team.
- When the Jumbo Frame feature is on:
  - Packets up to 9724(untagged) bytes will be forwarded.
  - Packets up to 9728(tagged) bytes will be forwarded.
  - User can define the good jumbo packet size in Jumbo MIB Good frame Max size register.
  - This value only applies to the MIB counter, not the actual operation of drop/accept.
  - There is no register that defines the acceptable jumbo frame size other than the 9728 byte size.

The BCM5396 can receive and transmit frames of extended length on ports linked at gigabit speed. Referred to as jumbo frames, these packets may be longer than 1518 bytes (when untagged), but shorter than 9728 bytes. This feature can be enabled on individual ports by writing to the “Jumbo Frame Port Mask Register (Page 40h: Address 01h–04h)” on page 163. Jumbo packets can only be received or forwarded to 1000BASE-T linked ports that are jumbo frame enabled. Jumbo packets consume larger blocks of buffer memory. Add the PHY jumbo enable bit if necessary. Up to 38 buffer memory pages are required for storing the longest allowed jumbo frame. While there is no physical limitation to the number of ports that can be jumbo enabled, it is recommended that no more than two be enabled simultaneously to ensure system performance. There is no performance penalty for enabling additional jumbo ports, beyond the potential strain on memory resources that can occur due to accumulated jumbo packets at multiple ports.

Port Trunking/Aggregation

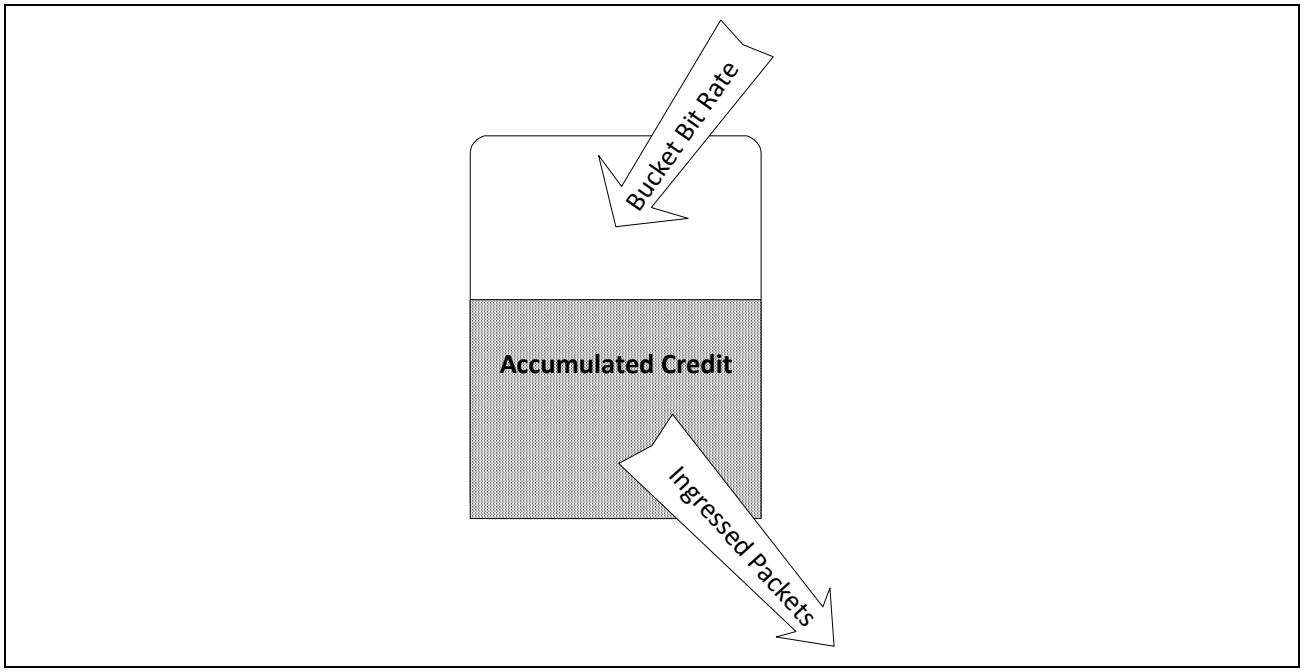
The BCM5396 supports MAC-based trunking. The trunking feature allows more than one port to be grouped together as a single link connection between two switch devices. This increases the effective bandwidth through a link and provides redundancy. The BCM5396 allows up to four trunk groups, with each trunk group consisting of two to eight physical link ports. There is no restriction in membership in any trunk group (such as sequential ordering of link ports), as illustrated in the trunk group vector of the Trunking Group register (see “Trunking Group Register (Page 32h: Address 90h–9Fh)” on page 157). All link ports within a trunk group must be of the same speed. The trunk ports cannot overlap with different groups. By performing a dynamic hashing algorithm on the MAC address, each packet destined for the trunk is forwarded to one of the valid ports within the trunk group. This method has several key advantages. By dynamically performing this function, the traffic patterns can be more balanced across the ports within a trunk. In addition, the MAC-based algorithm provides dynamic failover. If a port within a trunking group fails, the other ports within the trunk automatically assume all traffic designated for the trunk. It allows for a seamless, automatic redundancy scheme. This hashing function can be performed on either the DA, SA, or DA/SA, depending on the trunk hash selector bit of the MAC Trunking Control register (see “MAC Trunking Control Register (Page 32h: Address 01h)” on page 156).

Broadcast Storm Suppression/Rate Control

Forwarding traffic consumes switch resources that can negatively impact the forwarding of other traffic. The rate-based broadcast storm suppression mechanism is used to protect regular traffic from an overabundance of broadcast or multicast traffic. This feature monitors the rate of ingressed traffic of programmable packet types. If the rates of these packet types exceed the programmable maximum rate, the packets are dropped, or flow control is activated. To enable broadcast storm suppression, the feature can be activated in the "Broadcast Storm Suppression Registers" on page 164.

The broadcast storm mechanism works on a credit-based rate system that figuratively uses a bucket to track the bandwidth of each port (refer to Figure 4). Credit is continually added to the bucket at a programmable bucket bit rate. Credit is decremented from the bucket whenever one of the programmable packet types is ingressed at the port. If no packets are ingressed for a considerable length of time, the bucket credit continues to increase up to a programmable maximum bucket size. If a heavy burst of traffic is suddenly ingressed at the port, the bucket credit is drained. When the bucket empties, incoming traffic is constrained to the bucket bit rate—the rate at which credit is added to the bucket. At this point, excess packets are either dropped or deterred via flow control depending on the suppression drop mode also in the global "Suppression Control Register (Page 41h: Address 00h–03h)" on page 165.

Figure 4: Bucket Flow



Two-Bucket System

For added flexibility, the BCM5396 employs two buckets to track the rate of ingressed packets. Each of the two buckets, Bucket 0 and Bucket 1, can be programmed to monitor different packet types via the Suppression Packet Types Mask of the "Suppression Control Register (Page 41h: Address 00h–03h)" on page 165. For example, Bucket 0 could monitor broadcast packets, while Bucket 1 monitors multicast packets. Multiple packet types can be monitored by each bucket, and a packet type can be monitored by both buckets.

The rates of each bucket can be programmed individually (refer to "Bucket Bit Rate"). For example, the broadcast packets of Bucket 0 could have a maximum of 3 Mbps, whereas the multicast packets of Bucket 1 could be allowed up to 80 Mbps. The size of each bucket can be programmed via the "Port N (0–15) Receive Rate Control Register (Page 41h: Address 10h–4Fh)" on page 166. This determines the maximum credit that can accumulate in each bucket. The Rate Count and Bucket Size can be programmed individually for each port, providing another level of flexibility. The Suppression Control Register (Page 41h: Address 00h–03h) can be enabled or disabled on a per port basis via the Port N (0–15) Receive Rate Control Register (Page 41h: Address 10h–4Fh). This system allows the user to control dual packet type rates on a per port basis.

Bucket Bit Rate

The relative ingress rates of each bucket can be programmed via the rate count value of the Port N (0–15) Receive Rate Control Register (Page 41h: Address 10h–4Fh) on a per port basis. Each port will have a programmable rate count value for Bucket 0 and Bucket 1. Additionally, the bit rate mode is programmed via the Suppression Control Register (Page 41h: Address 00h–03h) on a chip basis. If this bit is set to 1, the packet rate is to be automatically scaled according to the port link speed. Ports operating at 1000 Mbps would be allotted a 100x higher ingress rate than ports linked at 10 Mbps. Together, the rate count value and the bit rate mode determine the bucket bit rate, which is a reflection of how quickly data can be ingressed (Kbps) at the given port for a given bucket. The rate count values are specified in Table 2. Values outside these ranges are not valid entries.

Table 2: Bucket Bit Rate

Rate Count (RC)	*Bit Rate Mode*	*Link Speed*	*Bucket Bit Rate Equation (Kbps)*	*Approximate Computed Bucket Bit Rate Values (as a function of RC)*
1–28	0	Any	= (RC x 8 x 1024) / 125	64 KB, 128 KB, 192 KB, ... , 1.792 MB
29–127	0	Any	= (RC – 27) x 1024	2 MB, 3 MB, 4 MB, ... , 100 MB
128–240	0	Any	= (RC – 115) x 1024 x 8	104 MB, 112 MB, 120 MB, ... , 1000 MB
1–125	1	10 Mbps	= (RC x 8 x 1024) / 100	0.08 MB, 0.16 MB, 0.24 MB, ... 10 MB
1–125	1	100 Mbps	= (RC x 8 x 1024) / 10	0.8 MB, 1.6 MB, 2.4 MB, ... , 100 MB
1–125	1	1000 Mbps	= RC x 8 x 1024	8 MB, 16 MB, 24 MB, ... 1000 MB

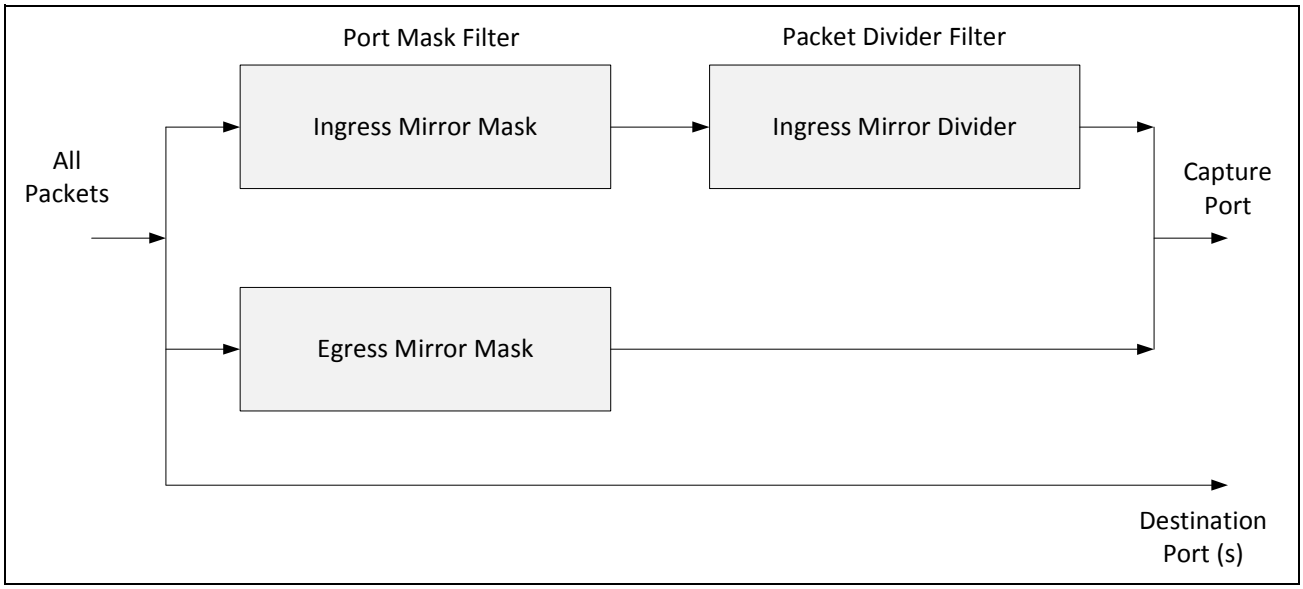
Port Mirroring

The BCM5396 supports port mirroring, allowing ingress and/or egress traffic to be monitored by a single port defined as the mirror capture port. The BCM5396 can be configured to mirror the ingress traffic and/or egress traffic of any other port(s). Mirroring multiple ports is possible but can create congestion at the mirror capture port. Several filters are used to decrease congestion.

Enabling Port Mirroring

Port Mirroring is enabled by setting the MIRROR_ENABLE bit in the "Mirror Capture Control Register (Page 02h: Address 10h–11h)" on page 109.

Figure 5: Mirror Filter Flow



Capture Port

The capture port is capable of monitoring other specified ports. Frames transmitted and received at the other ports are forwarded to the capture port according to the "Mirror Filtering Rules" on page 35. The capture port is specified by the Mirror Capture Control Register (Page 02h: Address 10h–11h).

Mirror Filtering Rules

Mirror Filtering Rules consist of a set of two filter operations, "Port Mask Filter"and "Packet Divider Filter", that are applied to traffic ingressed and/or egressed at a switch port. They are programmed using the following registers:

- Ingress Mirror Rules are programmed using two registers:
  - "Ingress Mirror Control Register (Page 02h: Address 12h–15h)" on page 110
  - "Ingress Mirror Divider (Page 02h: Address 16h–17h)" on page 110
- Egress Mirror Rules are programmed using:
  - "Egress Mirror Control Register (Page 02h: Address 1Ch–1Fh)" on page 110

Port Mask Filter

The IN_MIRROR_MASK bits in the "Ingress Mirror Control Register (Page 02h: Address 12h–15h)" on page 110 define the receive ports that are monitored. The OUT_MIRROR_MASK bits in the "Egress Mirror Control Register (Page 02h: Address 1Ch–1Fh)" on page 110 define the transmit ports that are monitored.

Any number of ingress/egress ports can be programmed to be mirrored, but bandwidth restrictions on the mirror capture port must be adhered to so as not to cause congestion or packet loss.

Packet Divider Filter

The IN_DIV_EN bit in the "Ingress Mirror Control Register (Page 02h: Address 12h–15h)" on page 110 allows further statistical sampling to be performed. When IN_DIV_EN = 1, the receive frames passing the initial filter are divided by the value IN_MIRROR_DIV, which is a 10-bit value stored in the "Ingress Mirror Divider (Page 02h: Address 16h–17h)" on page 110. Only one out of every *n* frames is forwarded to the mirror capture port, where n is the number specified in the IN_MIRROR_DIV bits.

Note: When multiple ingress ports have been enabled in the IN_MIRROR_MASK, the cumulative total packet count received from all ingress ports is divided by the value of IN_MIRROR_DIV to deliver the n^{th} receive frame to the mirror capture port.

IGMP Snooping

The BCM5396 supports Layer 2 IGMP snooping. When IGMP is enabled, the BCM5396 forwards IGMP frames to the frame management port. The external management entity programs the multicast membership information into the ARL table.

IP Layer IGMP Snooping

IP layer IGMP snooping is enabled by setting bit[3] of the “Global Management Configuration Register” on page 108. When asserted, IGMP IP layer snooping is enabled. A frame with value of 2 in the IP header protocol field, and not an IGMP query, is forwarded to the CPU port. The management CPU can then determine from the IGMP control packets which port should participate in the multigroup session by programming the multicast address in the ARL table or the Multicast Address 1/2 registers and the Multiport Vector 1/2 registers.

IEEE Standard 802.1x Port-Based Security

IEEE Standard 802.1x is a port-based authentication protocol. If a user port (supplicant) wants to get service from another port (authenticator), it must be approved by the authenticator. Usually, the authenticator passes an authentication protocol (EAP) to an authentication server containing all the security information.

EAP (Extensive Authentication Protocol) is a higher-layer protocol used for authentication purposes. For Layer 2 ports to participate in the EAP protocol more efficiently, IEEE Standard 802.1x created another Layer 2 protocol called EAPOL (EAP over LAN). With EAPOL, L2 can initiate or stop authentication functions by itself.

Thus, if a port needs service from another port, it needs to be authenticated by that port. EAPOL is the protocol used by the authentication process.

The BCM5396 device supports IEEE Standard 802.1x. By receiving and extracting special frames, management can control whether the ingress and egress ports should forward packets. Special frames include a BPDU frame (MAC_DA = 01:80:C2:00:00:00) or user-defined address, an EAPOL frame (MAC_DA = 01:80:C2:00:00:03, and MAC_DA 01:80:C2:00:00:00–01:80:C2:00:00:0F excluding MAC_DA = 01:80C2:00:00:01).

When the BCM5396 is in management mode, it will forward an EAPOL frame with MAC_DA = 01:80:C2:00:00:03 to the management entity, which can send it to the authentication server. Eventually, the management entity knows if this client (identified by its MAC SA) is qualified or not. If it is not qualified, the management entity will instruct the switch to drop the frame.

If only the clients qualified by the authentication process are to be supported, the management entity needs to create static entries in the ARL table, causing all non-IEEE Standard 802.1x special frames to be dropped. A client MAC address is added to the ARL table by the management entity only when it has passed the authentication process. By so doing, the switch will only forward qualified clients. For unqualified clients, only IEEE Standard 802.1x special frames can be forwarded to the management entity.

Address Management

The BCM5396 Address Resolution Logic contains the following features:

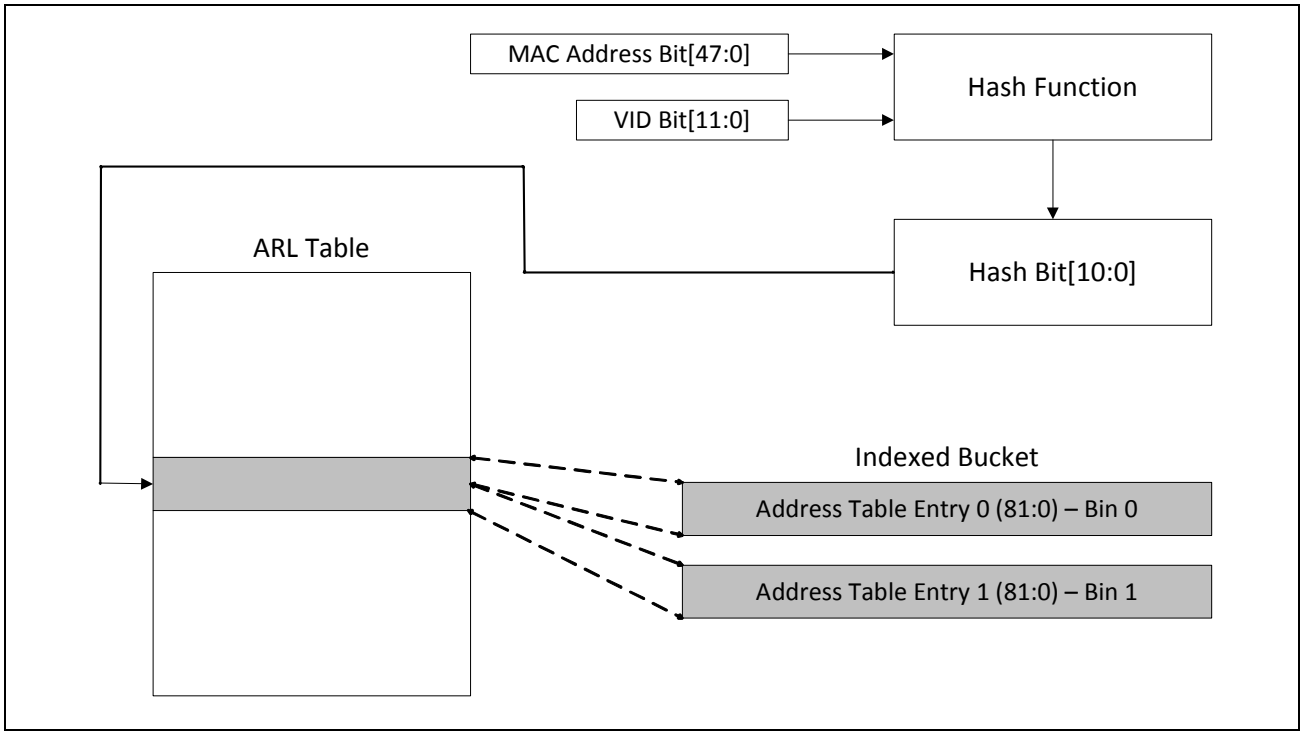
- Two-bins-per-bucket address table configuration
- Hashing of the MAC/VID address to generate the address table pointer

The address management unit of the BCM5396 provides wire speed learning and recognition functions. The address table supports 4096 unicast/multicast addresses using on-chip memory.

Address Table Organization

The MAC addresses are stored in embedded SRAM. Each bucket contains two entries (or bins). The address table has 2048 buckets with two entries in each bucket. This allows up to two different MAC addresses with the same hashed index bits to be mapped into the address table simultaneously.

Figure 6: Address Table Organization



The index to the address table is computed using a hash algorithm based on the MAC address.

Note: If EN_1QVLAN in "Global Control 0 Register" and VLAN_LEARN_MODE are set to 1 in the "Global Control 0 Register (Page 34h: Address 00h)" on page 158, both the MAC address and the VLAN ID (VID) are used to compute the hashed index. See "IEEE Standard 802.1Q VLAN" on page 29.

The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16-bit CRC hash value. Bits 10:0 of the hash are used as an index to the approximately 2000 buckets of the address table.

The CRC-CCITT polynomial is:

Hashing can be disabled by setting HASH_DISABLE bit to 1 in the "Global ARL Configuration Register (Page 04h: Address 00h)" on page 112. When hashing is disabled, the BCM5396 device uses a direct addressing method via the MAC address.

Address Learning

Information is gathered from received unicast packets, and *learned* or stored for the future purpose of forwarding frames addressed to the receiving port. During the receive process, the frame information (such as the Source Address [SA] and VID) is saved until completion of the packet. An entry is created in the ARL table memory if the following conditions are met:

- The packet is received without error.
- The packet is of legal length.
- The packet has a unicast SA.
- If using IEEE Standard 802.1Q VLAN, the packet is from an SA that belongs to the indicated VLAN domain.
- The packet does not have a reserved multicast destination address. The EN_RES_MUL_LEARN bit of the "Reserved Multicast Control Register (Page 00h: Address 50h)" on page 96 can disable this condition.
- There is free space available in memory to which the hashed index points.

When unicast packets are dynamically learned, the VALID bit is set, the AGE bit is set, and the STATIC bit is cleared in the entry. See Table 4: "Address Table Entry for Unicast Address," on page 39 for a description of a unicast ARL entry.

Multicast addresses are not learned into the ARL table, but must be written via one of the "Programming Interfaces" on page 58. See "Writing an ARL Entry" on page 43 and Table 6: "Address Table Entry for Multicast ARL Address," on page 41, for more information.

Address Resolution and Frame Forwarding

Received packets are forwarded based on the information learned or written into the ARL table. Address resolution is the process of locating this information and assigning a forwarding destination to the packet. The Destination Address (DA) and VID of the received packet is used to calculate a hashed index to the ARL table. The hashed index key is used by the address resolution function to locate a matching ARL entry. The frame is assigned a destination based on the forward field (PORTID or IPMC0) of the ARL entry. If the address resolution function fails to return a matching ARL entry, the packet is flooded to all appropriate ports. The following two sections describe the specifics of address resolution and frame forwarding for "Unicast Addresses" and "Multicast Addresses" on page 40.

Unicast Addresses

A frame containing a unicast destination address is assigned a forwarding field corresponding to a single port. The unicast address resolution algorithm is listed as follows:

- If the MPORT_ADDR_EN bit is set in "Global ARL Configuration Register (Page 04h: Address 00h)" on page 112 and the DA matches one of the addresses programmed in the "Multiport Address 1 Register (Page 04h: Address 10h–15h)" on page 113 or the "Multiport Address 2 Register (Page 04h: Address 20h–25h)" on page 114, the packet is forwarded to the corresponding port map contained in the "Multiport Vector 1 Register (Page 04h: Address 16h–19h)" on page 113 or the "Multiport Vector 2 Register (Page 04h: Address 26h–29h)" on page 114. See "Using the Multiport Addresses" on page 42 for more information.
- The lower 11 bits of the hashed index key are used as a pointer into the address table memory, and both entries in the bucket are retrieved. The address resolution logic processes the two entries in parallel.
- If the valid indicator is set and the address stored at one of the locations matches the index key of the packet received, the forwarding field port ID is assigned to the destination port of the packet.
- If the destination port matches the source port, the packet is not forwarded.
- If the address resolution function fails to return a matching valid ARL entry and the Unicast_Drop_En bit of the "New Control Register (Page 00h: Address 3Bh)" on page 95 is set, the frame is forwarded according to the port map in the "Unicast Lookup Failed Forward Map Register (Page 00h: Addr 54h–57h)" on page 97.
- Otherwise, the packet is flooded to all appropriate ports.

If the EN_1QVLAN and VLAN_LEARN_MODE are set to 1 in the "Global Control 0 Register (Page 34h: Address 00h)" on page 158, the VID is used in conjunction with the DA to index the ARL table. See Table 3 for definitions of the unicast index key and assigned forwarding field. The forwarding field for a unicast packet is the port ID contained in the matching ARL entry. See Table 4 for a description of a unicast ARL entry.

Table 3: Unicast Forward Field Definitions

EN_1QVLAN	*VLAN_LRN_MODE*	*Index Key*	*Forwarding Field*
1	1	DA and VID	Port ID
1	0	DA	Port ID
0	X	DA	Port ID

Table 4: Address Table Entry for Unicast Address

Field	*Description*
VID	VLAN ID associated with the MAC address.
VALID	• 1 = Entry is valid. • 0 = Entry is empty.
STATIC	• 1 = Entry is static, will not be aged out, and is written and updated by software. • 0 = Entry is dynamically learned and aged.
AGE	• 1 = Entry has been accessed or learned since last aging process. • 0 = Entry has not been accessed since last aging process.
PRI	MAC-based priority (only valid for static entries). See "Quality of Service" on page 24 for more information.
Reserved	–
PORTID	Port Identifier. The port associated with the MAC address.
MAC ADDRESS	48-bit MAC address.

Note: The fields described in Table 4 can be written via the "ARL MAC/VID Entry 0 Register (Page 05h: Address 10h–17h)" on page 116 and "ARL FWD Entry 0 Register (Page 05h: Address 18h–1Bh)" on page 116. Similarly, the same applies for entry 1 in "ARL MAC/VID Entry 1 Register (Page 05h: Address 20h–27h)" on page 117 and "ARL FWD Entry 1 Register (Page 05h: Address 28h–2Bh)" on page 118.

Multicast Addresses

A frame containing a multicast destination address is assigned a forwarding field corresponding to multiple ports specified in a port map. If the IP_MULTICAST bit is set in the "New Control Register (Page 00h: Address 3Bh)" on page 95, the multicast frame is assigned a forwarding field corresponding to a multicast port map from the matching ARL entry. If no matching ARL entry is found, the packet is flooded to all appropriate ports.

The multicast address resolution algorithm is listed as follows:

- If the DA matches one of the globally assigned reserved addresses between 01-80-C2-00-00-00 and 01-80-C2-00-00-2F, the packet is handled as described in Table 7: "Behavior for Reserved Multicast Addresses," on page 42.
- If the MPORT_ADDR_EN bit is set in "Global ARL Configuration Register (Page 04h: Address 00h)" on page 112 and the DA matches one of the addresses programmed in the "Multiport Address 1 Register (Page 04h: Address 10h–15h)" on page 113 or the "Multiport Address 2 Register (Page 04h: Address 20h–25h)" on page 114, the packet is forwarded to the corresponding port map contained in the "Multiport Vector 1 Register (Page 04h: Address 16h–19h)" on page 113 or the "Multiport Vector 2 Register (Page 04h: Address 26h–29h)" on page 114. See "Using the Multiport Addresses" on page 42 for more information.
- Otherwise, the lower 11 bits of the hashed index key are used as a pointer into the ARL table memory, and both entries in the bucket are retrieved. The address resolution logic processes the two entries in parallel.
- If the valid indicator is set and the address stored at one of the entry locations matches the index key of the packet received, the forwarding field port map is assigned to the destination port of the packet.
- If the address resolution function fails to return a matching valid ARL entry and the MCST_DLF_FWD bit of the "New Control Register (Page 00h: Address 3Bh)" on page 95 is set, the frame is forwarded according to the port map in the Unicast Lookup Failed Forward Map Register (Page 00h: Addr 54h–57h).
- Otherwise, all other multicast and broadcast packets are flooded to all appropriate ports.

If the EN_1QVLAN and VLAN_LEARN_MODE are set to 1 in the "Global Control 0 Register (Page 34h: Address 00h)" on page 158, the VID is used in conjunction with the DA to index the ARL table. See Table 5 for definitions of the multicast index key and assigned forwarding field. The forwarding field for a multicast packet is the port map contained in the matching ARL entry. See Table 6 for a description of a multicast ARL entry. See "Accessing the ARL Table Entries" on page 43 for more information.

Table 5: Multicast Forward Field Definitions

EN_1QVLAN	*IP_MULTICAST*	*Index Key*	*Forwarding Field*
1	0	DA and VID	Port ID
0	0	DA	Port ID
1	1	DA and VID	IPMC0
0	1	DA	IPMC0

Table 6: Address Table Entry for Multicast ARL Address

Field	*Description*
VID	VLAN ID associated with the MAC address.
VALID	• 1 = Entry is valid. • 0 = Entry is empty.
AGE	The age bit is ignored for static ARL table entries.
PRI	MAC-based priority (only valid for static entries). See "Quality of Service" on page 24 for more information.
Reserved	–
IPMC0[16:0]	Multicast forwarding mask. The field is a per port vector. Bits correspond to ports [16:0], respectively. • 1 = Forwarding enable. • 0 = Forwarding disable.
MAC ADDRESS	48-bit MAC address.

Note: The fields described in Table 6 can be written via the "ARL MAC/VID Entry 0 Register (Page 05h: Address 10h–17h)" on page 116 and "ARL FWD Entry 0 Register (Page 05h: Address 18h–1Bh)" on page 116. Similarly, the same applies for entry 1 in "ARL MAC/VID Entry 1 Register (Page 05h: Address 20h–27h)" on page 117 and "ARL FWD Entry 1 Register (Page 05h: Address 28h–2Bh)" on page 118.

Reserved Multicast

Table 7 summarizes the actions taken for specific reserved multicast addresses. Packets identified with these destination addresses are handled uniquely since they are designed for special functions. Bits[4:0] of the "Reserved Multicast Control Register (Page 00h: Address 50h)" on page 96 program groups of these addresses to be dropped or forwarded. Writing to these bits can change the default action summarized in Table 7.

Table 7: Behavior for Reserved Multicast Addresses

MAC Address	*Function*	*IEEE Standard 802.1 Specified Action*	*Action (Managed Mode)*
01-80-C2-00-00-00	Bridge group address	Drop frame	Forward to IMP port
01-80-C2-00-00-02	Reserved	Drop frame	Forward to IMP port only
01-80-C2-00-00-03	IEEE Standard 802.1x port-based network access control	Drop frame	Forward to IMP port only
01-80-C2-00-00-04–01-80-C2-00-00-0F	Reserved	Drop frame	Forward to IMP port only
01-80-C2-00-00-11–01-80-C2-00-00-1F	Reserved	Forward frame	Forward to all ports except IMP port
01-80-C2-00-00-20	GMRP address	Forward frame	Forward to all ports except IMP port
01-80-C2-00-00-21	GVRP address	Forward frame	Forward to all ports except IMP port
01-80-C2-00-00-22–01-80-C2-00-00-2F	Reserved	Forward frame	Forward to all ports except IMP port

Using the Multiport Addresses

As a backup to the ARL table, the "Multiport Address 1 Register (Page 04h: Address 10h–15h)" on page 113 and "Multiport Address 2 Register (Page 04h: Address 20h–25h)" on page 114 can be used. Packets with a corresponding DA are forwarded to the port map contained in the "Multiport Vector 1 Register (Page 04h: Address 16h–19h)" on page 113 or the "Multiport Vector 2 Register (Page 04h: Address 26h–29h)" on page 114. These registers must be enabled via the MPORT_ADDR_EN bit in the "Global ARL Configuration Register (Page 04h: Address 00h)" on page 112. While the name suggests that these registers are used only for multicasting, they can be used for multicast or unicast addresses, and the forwarding map can include one or more ports.

Static Address Entries

The BCM5396 supports static ARL table entries that are created and updated via one of the "Programming Interfaces" on page 58. These entries can contain either unicast or multicast destinations. The entries are created by writing the entry location via the Table 75: "ARL/VLAN Access Registers (Page 05h)," on page 114, and setting the STATIC bit. The AGE bit is ignored. Static entries are not automatically learned MAC addresses or port associations. They are not aged out by the automatic internal aging process. See "Writing an ARL Entry" on page 43 for details.

Accessing the ARL Table Entries

ARL table entries are accessed by one of two mechanisms. The first mechanism uses the ARL Read/Write Control, which allows an address entry location to be read, modified, or written based on the value of a known MAC address. The second mechanism searches the ARL table sequentially, returning all valid entries.

Reading an ARL Entry

The steps for reading an ARL entry:

1. Set the MAC address in the "MAC Address Index Register (Page 05h: Address 02h–07h)" on page 115.
2. Set the VLAN ID in the "VLAN ID Index Register (Page 05h: Address 08h–09h)" on page 116. This is necessary only if the VID is used in the index key.
3. Set the ARL_R/W bit to 1 in the "ARL Read/Write Control Register (Page 05h: Address 00h)" on page 115.

- Set the START/DONE bit to 1 in the "ARL Read/Write Control Register (Page 05h: Address 00h)" on page 115. This initiates the read operation.

The MAC address and VLAN ID are used to calculate the hashed index to the ARL table. The matching ARL bucket is read. The contents of entry 0 are stored in the "ARL MAC/VID Entry 0 Register (Page 05h: Address 10h–17h)" on page 116 and "ARL FWD Entry 0 Register (Page 05h: Address 18h–1Bh)" on page 116. The contents of entry 1 are stored in the "ARL MAC/VID Entry 1 Register (Page 05h: Address 20h–27h)" on page 117 and the "ARL FWD Entry 1 Register (Page 05h: Address 28h–2Bh)" on page 118.

Entries that do not have the VALID bit set should be ignored. The contents of the MAC/VID registers must be compared against the known MAC address and VID. Entries that do not match may be a valid entry, but are not a valid match for the index key. All other read entries are considered valid ARL entries.

Writing an ARL Entry

The steps for writing an ARL entry:

1. Follow the steps above to read the ARL entry matching the MAC address and VID that is written to the table.
2. Keep the values of the "MAC Address Index Register (Page 05h: Address 02h–07h)" on page 115, the "VLAN ID Index Register (Page 05h: Address 08h–09h)" on page 116, the "ARL MAC/VID Entry 0 Register (Page 05h: Address 10h–17h)" on page 116, the "ARL FWD Entry 0 Register (Page 05h: Address 18h–1Bh)" on page 116, the "ARL MAC/VID Entry 1 Register (Page 05h: Address 20h–27h)" on page 117, and the "ARL FWD Entry 1 Register (Page 05h: Address 28h–2Bh)" on page 118.
3. Determine which ARL entry (0 or 1) is to be written, based on the existing values of the VALID bit and MAC/VID bits.
4. Modify the "ARL FWD Entry 0 Register (Page 05h: Address 18h–1Bh)" on page 116 or the "ARL FWD Entry 1 Register (Page 05h: Address 28h–2Bh)" on page 118 as necessary. Set the STATIC bit so that the entry is not aged out.
5. Set the ARL_R/W bit to 0 in the "ARL Read/Write Control Register (Page 05h: Address 00h)" on page 115.
6. Set the START/DONE bit to 1 in the "ARL Read/Write Control Register (Page 05h: Address 00h)". This initiates the write operation.

The MAC address and VID are used to calculate the hashed index to the ARL table. Both entry 0 and entry 1 are written to the matching ARL bucket.

An ARL table can also be accessed using Memory Access register (Page 08h). This requires software to do the hashing on MACDA and / VLAN ID and places the results in the table.

Searching the ARL Table

The second way to access the ARL table is through the ARL search control. The entire ARL table is searched sequentially, revealing each valid ARL entry. Setting the START/DONE bit in the "ARL Search Control Register (Page 05h: Address 30h)" on page 119 begins the search from the top of the ARL table. This bit is cleared when the search is complete. During the ARL search, the ARL_SR_VALID bit indicates when a found valid 76-bit entry is available in the "ARL Search MAC/VID Result Register 0 (Page 05h: Address 33h–3Ah)" on page 120 and the "ARL Search Result Register 0 (Page 05h: Address 3Bh–3Eh)" on page 120, and in the "ARL Search MAC/VID Result Register 1 (Page 05h: Address 40h–47h)" on page 121 and the "ARL Search Result Register 1 (Page 05h: Address 48h–4Bh)" on page 121. When the host reads the contents of this register, the search process automatically continues to seek the next valid entry in the address table. Invalid address entries are skipped, providing the host with an efficient way of searching the entire address table.

The ARL search and ARL read/write operations execute in parallel with other register accesses. This allows the host processor to start a read, write or search process, and then read/write other registers, returning periodically to see if the operation has completed.

Address Aging

The aging process periodically removes dynamically learned addresses from the ARL table. When an ARL entry is learned or referenced, the AGE bit is set to 1. The aging process scans the ARL table at regular intervals, aging out entries not accessed during the previous one to two aging intervals. The aging interval is programmable via the AGE_TIME bits in the "Aging Time Control (Page 02h: Address 0Ch–0Fh)" on page 109. Aging is disabled by setting the AGE_TIME bits to 0.

Entries that are written and updated via one of the "Programming Interfaces" on page 58 should have the STATIC bit set. Thus, they are not affected by the aging process.

For each entry in the ARL table, the aging process performs the following:

- If the VALID bit is not set, then it does nothing.
- If the VALID bit is set and the STATIC is set, then it does nothing.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is set, then it clears the AGE bit. This keeps the entry in the table, but it marks the entry in such a way that it is removed if it is not accessed before the subsequent Aging scan.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is reset; then it resets the VALID bit. This effectively deletes the entry from the ARL table. The entry has been aged out.

Fast Aging to Support Rapid Spanning Tree Protocol

The rapid spanning tree protocol allows a backup port to replace a failed port in a very short time (in the millisecond range). In order to support this protocol, the switch needs to be able to age out all entries belonging to the failed port. Using "Fast Aging Control Register (Page 00h: Address 88h)" on page 100, when FAST_AGE_START/DONE is set to 1 (default = 0), the switch ages out entries that match both the "Fast Aging Port Register (Page 00h: Address 89h)" on page 101 and the "Fast Aging VID Register (Page 00h: Address 8Ah–8Bh)" on page 101. Once aging is complete, the switch resets the bit to logic 0.

When AGE_OUT_ALL_PORTS in "Fast Aging Port Register (Page 00h: Address 89h)"bit[7] is set to logic 1, it indicates that all ports are aged out (must also match VID). On the other hand, bits[3:0] PORT_ID indicate a selected entry to be aged out of the ARL table (must also match VID).

Fast VID aging is achieved via the "Fast Aging VID Register (Page 00h: Address 8Ah–8Bh)". When bit[15] is set, the VID is aged out (must also match the PORT_ID). Bits[11:0] specify the VID to be aged out (must also match PORT_ID).

Note that when bit[0] EN_FAST_AGE_STATIC in "Fast Aging Control Register (Page 00h: Address 88h)"is set to logic 1, fast aging will age out both static and dynamic entries. When set to the default value of logic 0, only dynamic entries are aged out.

Bridge Management

To support Bridge Management, the BCM5396 provides the following:

- IEEE Standard 802.1D spanning tree protocol and rapid reconfiguration of spanning tree
- IEEE Standard 802.1s multiple spanning trees. See "IEEE Standard 802.1s Multiple Spanning Tree Registers" on page 169
- Bridge management state register access through the CPU interface
- Bridge Protocol Data Unit (BPDU) frame forwarding through the CPU interface or the MII interface

Spanning Tree Port State

The BCM5396 device supports the spanning tree protocol by providing the spanning tree state in the "10/100/1000 Port N Control Register [0:15](Page 00h: Address 00h–0Fh)" on page 93 for each of the 17 ports. Each Port Control Register (PCR) contains three bits dedicated to STP state (STP_STATE[2:0]), as well as additional bits to control the operation of the MAC port.

In the unmanaged compatible mode of the operation (SW_FWDG_MODE = Unmanaged), the default state of the STP_STATE[2:0] bits is all 0s, and no spanning tree state is maintained. Write operations to the spanning tree state bits are ignored. Frames are forwarded based only on their DA. Known unicast address frames are forwarded to their single-defined destination port, and unknown unicast as well as all multicast/broadcast addressed frames are flooded to all ports, with the exception of the management port, providing SW_FWDG_EN = 1. BPDU frames are one of the IEEE Standard 802.1 reserved multicast addresses that the unmanaged mode floods. For a complete description of the forwarding behavior of the unmanaged address resolution logic, refer to Table 7: "Behavior for Reserved Multicast Addresses," on page 42.

In the BCM5396 mode of operation (SW_FEWDG_MODE = managed), 17 ports are considered *network ports* and can have STP port state associated with them, these being the 16 integrated 10/100/1000bps ports and the MII port.

The BCM5396 reacts to the STP state bits as written by the management CPU, as follows (provided SW_FWDG_EN = 1):

Disable

In this state, all frames received by the port are discarded. The port does not forward any transmit frames queued by either BCM5396 receive network ports or frames cast by the management entity using IMP. Addresses are not learned by ports in the Disabled state. This is the default state that the BCM5396 powers up in when SW_FWDG_MODE = Managed.

Blocking

In this state, the MAC port forwards received BPDUs to the designated Management port (IMP). All other frames received by the port are discarded, and the addresses are not learned. The port does not forward any transmit frames queued by other receive network ports.

Listening

In this state, the MAC port forwards received BPDUs to the designated In-band Management port (IMP). All other frames received by the port are discarded and the addresses are not learned. The port does not forward any transmit frames queued by other received network ports, but transmits frames cast by the management entity using IMP, as expected (such as BPDUs). Note that the learning and listening states of all the BCM5396 ports are identical. The external management processor running the STP algorithm must distinguish between these two states using the STP algorithm, but it is able to store the learning and listening state information into the BCM5396 for consistency.

Learning

In this state, the MAC port forwards received BPDUs to the management port, transmits BPDUs sent into the management port, and does not learn incoming frames' MAC addresses. All other frames received by the port are discarded.

Forwarding

In this state, the MAC port forwards received BPDUs to the management port, transmits BPDUs sent into the management port, forwards all other frames, and learns all incoming frames' MAC addresses.

Table 8: Spanning Tree State

Spanning Tree State	*Receive BPDU*	*Transmit BPDU*	*Normal Frame*	*Address Learning*	*STP_State*
No spanning tree or spanning tree disable	Treated as multicast frame	Flood to all ports	Forward	Learn	11 + global flag

Table 8: Spanning Tree State

Spanning Tree State	*Receive BPDU*	*Transmit BPDU*	*Normal Frame*	*Address Learning*	*STP_State*
Disable state	Disabled	Disabled	Do not forward	Do not learn	00
Blocking state	Forward to management	Disabled	Do not forward	Do not learn	01
Listening state	Forward to management	Enabled	Do not forward	Do not learn	10
Learning state	Forward to management	Enabled	Do not forward	Do not learn	10
Forwarding state	Forward to management	Enabled	Forward	Learn	11

Management Frames

Management frames received by the BCM5396 are forwarded to the bridge management entity (an external CPU or microcontroller) through the IMP (in-band management port).

The following frames are forwarded to the bridge management entity in the BCM5396 mode:

- **BPDU Frame:** BPDUs are identified by the bridge group address (01:80:C2:00:00:00) in the destination address field of a frame. The STP_STATE bits in the “10/100/1000 Port N Control Register [0:15](Page 00h: Address 00h–0Fh)” on page 93 must be configured to permit BPDU reception on a particular port. A BPDU received on such a port is forwarded with the Port ID of the receiving port to the port configured in the FRM_MNGT_PORT field of the “Global Management Configuration Register” on page 108.
- **Reserved Multicast Addressed Frames:** Frames with IEEE Standard 802.1-administered reserved multicast addresses (between 01:80:C2:00:00:02 and 01:80:C2:00:00:0F) in their DA field are forwarded only to the management port with a header which includes the Port ID of the port from which the frame was received. Frames with all LANs bridge management group address (01:80:C2:00:00:10) as the DA are forwarded to all ports, with the management port again receiving the header information to identify the Port ID from which the frame was received.
- **Directed Management Agent Frames:** Packets with the DA equal to one of the MAC addresses associated with the management port.These addresses are generally entered as static addresses by the management port.
- **Mirrored Frames:** Ingress or egress port frames that have been assigned to be mirrored to the management port.

To transmit a frame from the management port, the management agent is responsible for encapsulating the actual management frame which is transmitted in its entirety within an additional header and FCS field. The resolution rules for transmitted management frames are as follows:

- a. If the header OPCODE (refer to Table 11 on page 57) indicates the frame has a normal unicast or multicast address, the frame is forwarded according to the address table resolution. Frames with broadcast addresses or multicast addresses not found in the address table are flooded to all ports.
- b. If the header OPCODE (refer to Table 11 on page 57) indicates the frame is an egress directed frame, the frame is forwarded to the Port ID identified in the header.
- c. If the header OPCODE, shown in Table 11 on page 57, indicates that the frame is a multicast egress directed frame, the frame is forwarded to multiple ports identified in the header.

Multiple Spanning Tree Protocol (IEEE Standard 802.1s)

The Multiple Spanning Tree Protocol (MSTP) which uses the Rapid Spanning Tree protocol (RSTP) to provide rapid convergence, enables VLANs to be grouped into a spanning-tree instance, provides for multiple forwarding paths for data traffic, and enables load balancing. The most common initial deployment of MSTP and RSTP is in the backbone and distributed layers of a Layer 2 switched network. This deployment provides the highly available network required in a service-provider environment. Both RSTP and MSTP improve the operation of the spanning tree while maintaining backward compatibility with equipment that is based on the (original) IEEE Standard 802.1D spanning tree. The BCM5396 can support up to 32 spanning trees.

The multiple spanning table index is stored in the VLAN table. A total of 32 indexes are supported. Setting En_802_1s “Multiple Spanning Tree Control Register (Page 43h: Address 00h)” on page 170, bit[2] to logic 1 enables 802.1s support. Thus, spanning tree status is fetched from the multiple spanning tree table in the VLAN table.

Section 3: System Functional Blocks

Overview

The BCM5396 includes the following features:

- Media Access Controller
- Integrated High-Performance Memory
- Switch Controller

See the page numbers listed for more detail.

Media Access Controller

The BCM5396 contains seventeen 10/100/1000 GMACs. The MAC automatically selects the appropriate speed, CSMA/CD or full-duplex, based on the PHY auto-negotiation result. In FDX mode, IEEE Standard 802.3x PAUSE-frame-based flow control is also determined through auto-negotiation. The MAC is IEEE Standard 802.3, 802.3u, and 802.3x compliant.

Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than 1518 bytes (when untagged) or 9728 bytes for jumbo enabled ports

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded.

Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and interpacket gap enforcement.

In 10/100 half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the IEEE Standard 802.3 requirements for frame deferral. Following deferral, the transmitter adds eight bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the 16th consecutive collision, the backoff algorithm starts over at the initial state, the collision counter is reset, and attempts to transmit the current frame continue. Following a late collision, the frame is aborted and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame and the 96 bit-times of IPG have been observed.

Flow Control

The BCM5396 implements an intelligent flow control algorithm to minimize the system impact resulting from traffic congestion. Buffer memory allocation is adaptive to the status of each port's speed and duplex mode, providing an optimal balance between flow management and per port memory depth. The BCM5396 initiates flow control in response to buffer memory conditions on a per port basis.

The MACs are capable of flow control in both full- and half-duplex modes.

10/100 Mbps Half-Duplex Mode

In 10/100 Mbps half-duplex mode, the MAC back pressures a receiving port by transmitting a 96-bit time jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow control state.

10/100/1000 Mbps Full-Duplex Mode

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow control frames are recognized and, when properly received, set the flow control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control, the transmit controller transmits a MAC control PAUSE frame with the pause time set to maximum. When the condition that caused the flow control state is no longer present, a second MAC control PAUSE frame is sent with the pause time field set to 0.

Integrated High-Performance Memory

The BCM5396 supports 256 MB of high-performance SRAM for storing packet data, the ARL table, the VLAN table, the TX queues and descriptors. This eliminates the need for external memory, allowing for implementation of extremely low-cost systems.

The internal RAM controller efficiently executes memory transfers and achieves non-blocking performance for stand-alone 16-port applications.

Switch Controller

The core of the BCM5396 device is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration, and transmit descriptor queueing.

Buffer Management

The frame buffer memory is divided into pages, units of data consisting of 256 bytes each. Each packet received may be allocated more than one page. For example, six pages are required to store a 1522-byte frame. Frame data is stored in the buffer memory as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. This list tracks the transmission of the packet. After successful packet transmission, the buffer memory is released to the free buffer pool.

Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, the VLAN lookup, learning and aging functions, egress descriptor update, and output port queue managers. These processes are arbitrated to provide fair access to the memory and minimize latency of critical processes to provide a fully non-blocking solution.

Transmit Output Port Queues

Frames are maintained in the egress port using a linked list. Two levels of linked lists are used to maintain one output queue (refer to Figure 7 on page 52). The first level is the TXQ linked list, and the second level is the buffer tag linked list. The TXQ linked list is used to maintain frame priority order for each port. For each frame, the buffer tag linked list is used to maintain the order of the buffer pages corresponding to each frame.

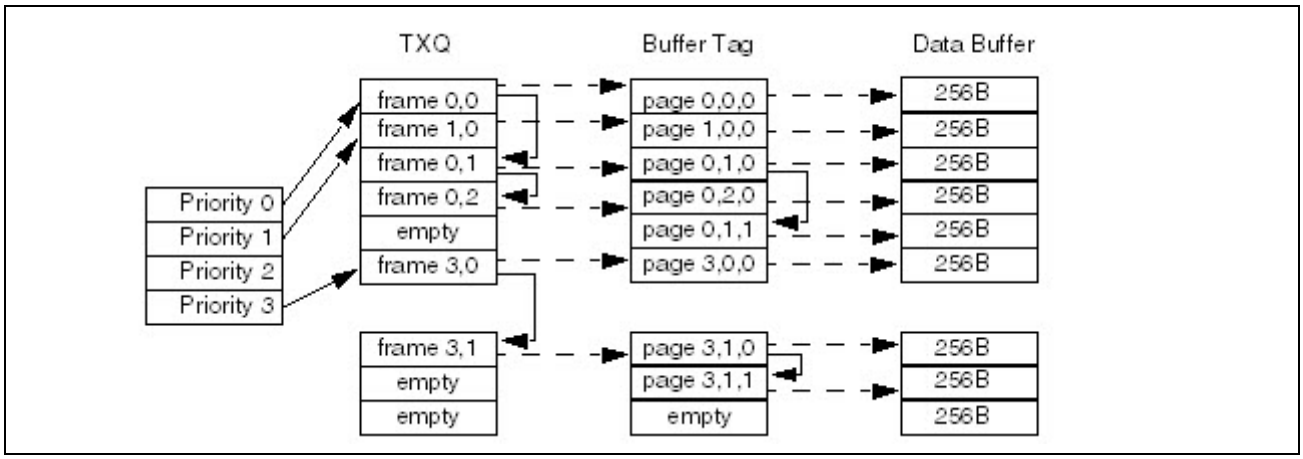
Each egress port supports up to four transmit queues for servicing Quality of Service (QoS). All four transmit queues share the 512 entries of the TXQ table. The TXQ table is maintained as linked list, and each node in the TXQ uses one entry in the TXQ table. The TXQ size for each priority can be programmed to up to 512 entries.

When QoS function has been turned off, the switch controller maintains one output queue for each egress port. The TXQ table is maintained in a per port individual internal memory.

- Each node in the queue represents a pointer which points to a frame buffer tag.
- Each buffer tag includes frame information and a pointer to the next buffer tag.
- Each buffer tag has an associated page allocated in the frame buffer.

For a packet with a frame size larger than 256 bytes, multiple buffer tags are required. A 9728-byte jumbo frame, for instance, requires 38 buffer tags to handle the frame.

Figure 7: TXQ and Buffer Tag Structure



Section 4: System Interfaces

Overview

The BCM5396 includes the following interfaces:

- Serial Interface
- Frame Management
- Programming Interfaces
- MDC/MDIO Interface
- LED Interfaces

These interfaces are discussed in more detail on the pages listed above.

Serial Interface

Each LVDS-compatible serial port can be configured in SGMII or SerDes mode.

SGMII Mode

The SGMII interface transmits serial data differentially at 1.25 Gbaud via the TXDN and TXDP pins and receives serial data differentially via the RXDN and RXDP pins. Transmit data timing is recovered from the incoming data signal, and the attached link partner does the same. The SGMII interface pins are shared with the SerDes interface pins.

The data signals operate at 1.25 Gbaud. Each of these signals is realized as a differential pair because of the speed of operation, providing signal integrity while minimizing system noise. The SGMII signals use LVDS voltage levels. Both the data and clock signals are DC-balanced; therefore, implementations that meet the AC parameters but fail to meet the DC parameters can be AC-coupled.

The 1.25 Gbaud transfer rate of the SGMII is greater than required for the BCM5396 transceiver operating at 10 Mbps or 100 Mbps. When these situations occur, the BCM5396 elongates the frame by replicating each frame byte 10 times for 100 Mbps and 100 times for 10 Mbps. This frame elongation takes place above the IEEE Standard 802.3z PCS layer, making the start frame delimiter appear only once per frame.

When the device operates at 10 Mbps or 100 Mbps, the SGMII differential pair replicates the data 100 and 10 times, respectively.

SerDes Mode

The SerDes interface operates via 1000BASE-X and complies with IEEE Standard 802.3, Clauses 36 and 37. The interface shares differential data pins with the SGMII interface. The BCM5396 SerDes can be used in various applications listed as follows:

- The SerDes interface can be connected to SerDes fiber modules creating switched fiber ports.
- The SerDes interface and be connected to a SerDes-to-Copper PHY creating switched copper ports.
- The SerDes interface can be connected to a SerDes MAC or switch for a SerDes Switch-to-Switch application.

The SerDes auto-negotiation is similar to the SGMII except for the link timer. Table 9 summarizes the differences between the two interfaces.The differential pair runs at 1.25 Gbps. The data is 8b/10b encoded, and the decoded data throughput is 1 Gbps.

Table 9: SGMII and SerDes Auto-Negotiation

	Link Timer	*Remote Fault*	*PAUSE Frame*	*Speed Bit*	*Link Status*	*Duplex Bit*
SGMII	1.6 ms	Not supported	Not supported	Supported	Supported	Supported
SerDes	10 ms	Supported	Supported	Not supported (always 1000BASE-X)	Not supported	Supported

SerDes/SGMII Auto-Negotiation

It is necessary to pass control information to the link partner when establishing a link. The link partner receives and decodes the sent control information and also begins auto-negotiation. The link partner acknowledges the update of the link status and visa versa. Upon receiving proper acknowledgement, the BCM5396 completes auto-negotiation and returns to normal data mode. The included control information for SerDes and SGMII is compared in Table 9.

Note: When SGMII/SerDes of one BCM5396 connects to another BCM5396:

It is required to turn off SGMII/SerDes auto-dectect function (set SerDes/SGMII Control 1 register bit[4]=0,SerDes/SGMII Control 1 register bit[0]=0 for SGMII mode), and force one BCM5396 into SGMII master(set SerDes/SGMII Control 1 register bit[5]=1), the other BCM5396 into SGMII slave (SerDes/SGMII Control 1 register bit[5]=0). Or force both into SerDes mode (set SerDes/SGMII Control 1 register bit[4]=0,SerDes/SGMII Control 1 register bit[0]=1 for SerDes/Fiber mode)

The reason: If SGMII/SerDes auto-dectect is enabled on both sides, each side is trying to switch between SGMII and SerDes mode. Sometimes they can not reach the same mode, hence they can not link up.

Frame Management

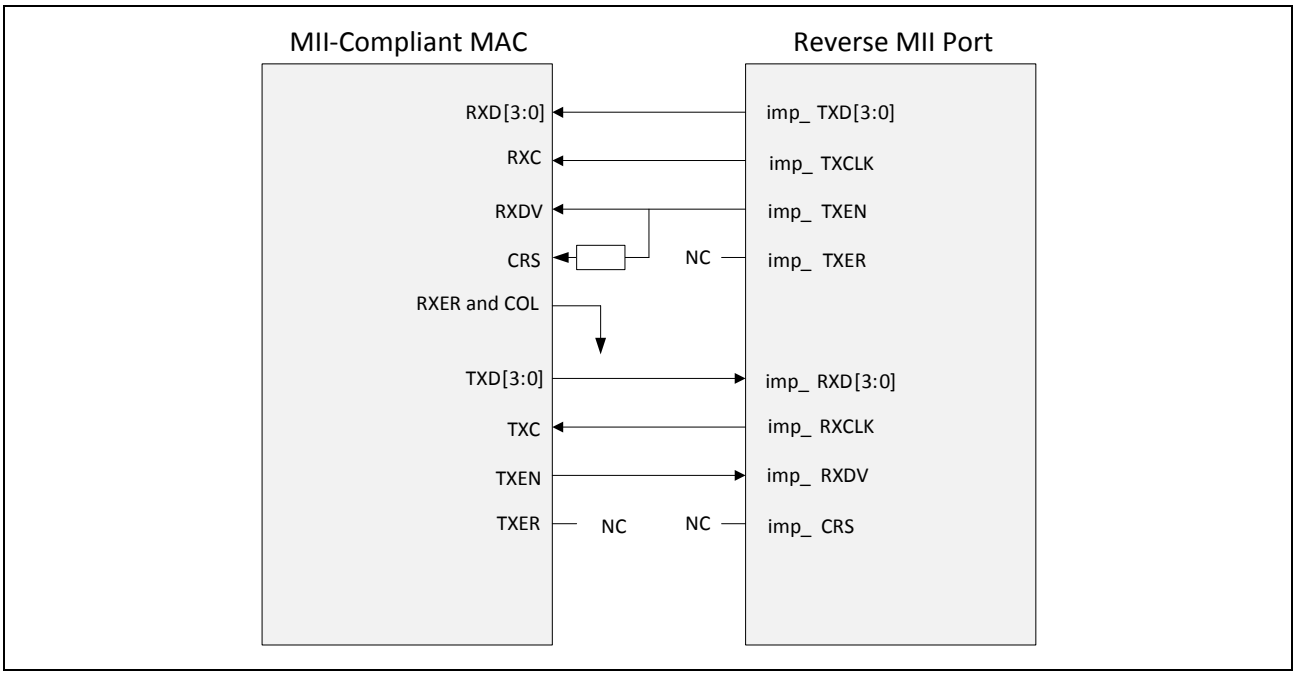
The BCM5396 provides a dedicated in-band managemnet port (IMP) that works in conjunction with the frame management block to receive forwarded management frames directed to the switch. An external CPU connects via the IMP interface to process the forwarded frames and respond appropriately.

The frame management block is configured via the FRM_MNGT_PORT bits of the “Global Management Configuration Register” on page 108 to work with the MII interface creating an IMP.

Reverse MII Port

The media-independent interface (MII) serves as a digital data interface between the BCM5396 and an external 10/100 Mbps management entity. Reverse MII (RvMII) notation reflects the MII port interfacing to a MAC-based external agent. The RvMII contains all the signals required to transmit and receive data at 10 Mbps for both full-duplex and half-duplex operation. Figure 8 on page 55 shows the RvMII connection information.

Figure 8: RvMII Port Connections



GMII Port

The Gigabit Media Independent Interface (GMII) serves as a digital data interface between the BCM5396 and an external gigabit management entity. Transmit and receive data is clocked on the rising edge of the clocks. The GMII transmits and receives synchronously via the TXD[3:0] and RXD[3:0] data signals.

RGMII Port

The Reduced Gigabit Media Independent Interface (RGMII) serves as a digital data interface between the BCM5396 and an external gigabit management entity. Transmit and receive data is clocked on the rising and falling edges of the clocks. This reduces the number of data signals crossing the MAC interface without affecting the data transmission rate. The RGMII transmits and receives data synchronously via the TXD[3:0] and RXD[3:0] data signals.

In-Band Management Port

The MII port is designated as the management port, and it is referred to as the in-band management Port (IMP). The IMP can be used as a full-duplex 10/100/1000 Mbps port.This can be used to forward extensive management information to the external management agent such as BPDU, mirrored frames, or frames addressed to other static address entries that have been identified to be of special interest to the management system.

Note: The MII port is a dedicated management port and cannot be put in a regular data port mode. Packet traffic in and out of this port always has the Broadcom tag attach to it.

Unicast, multicast and broadcast traffic is forwarded to the IMP based on the state of the RX_UCST_EN, RX_MCST_EN and RX_BCST_EN bits of the “IMP Port (Port 16) Control Register (Page 00h: Address 10h)” on page 93. If these bits are cleared, no frame data is forwarded to the frame management port (with the exception of frames meeting the criteria for “Port Mirroring” on page 34).

The BCM5396 device will intrusively tag frames destined to the management entity to allow the identity of the originating ingress port of a frame to be retained. Additional header information is inserted into the original frame between the original SA field and type/length fields. The tag includes the BRCM type (8874h) field and the BRCM tag field. A recalculated FCS is appended to the resultant frame before the frame is forwarded. The management frame format is defined in Table 10.

Table 10: Transmit/Receive Frame Format Over Management Port

Destination Address	Source Address	BRCM Type	BRCM Tag (32 bits)	Original Type/Length	Frame Data	Original FCS	Recalculated FCS

Similarly, the host system must insert the BRCM type/length and tag fields into the frames it wishes to send into the management port to be routed to specified egress ports. The OPCODE within the tag field determines how the frame is handled and allows frames to be forwarded using the normal address lookup or via a PortID designation within the tag.

The BRCM tag and BRCM type/length fields are transmitted with the convention of highest significant octet first followed by next lowest significant octet, etc., and with the least significant bit of each octet transmitted out from the MAC first. So, for the BRCM type/length field in Table 10, the most significant octet would be transmitted first (bits 24:31), with bit 24 being the first bit transmitted.

Table 12 on page 57 shows the format of the BRCM tag field for RX from the CPU, and Table 13 on page 58 shows the format of the BRCM TAG TX to the CPU. The OPCODE field slightly modifies the use and validity of some fields in the tag. Table 11 on page 57 defines the supported OPCODEs, and identifies each of the other fields in the BRCM tag in detail.

The MII port can be connected directly to a MAC device with an MII.

The MII can be selected as the management port using the FRM_MNGT_PORT field of the “Global Management Configuration Register” on page 108.

When management mode is enabled in "Switch Mode Register (Page 00h: Address 20h)" on page 94, the MII port is assigned as the IMP port. All frames sent into or out of the IMP port needs a 4-byte Broadcom tag as specified in Table 12 on page 57 and Table 13 on page 58.

Table 11: OPCODE Field in BRCM Tag for Management Port Frame

OpCodes	Name	Description
0 0 0	Unicast/multicast	Normal unicast and multicast frames are forwarded using the address table lookup of the DA contained in the frame.
	Broadcast	Broadcast frames sent by the host management system into IMP port are forwarded based on the broadcast rule that is in effect.
0 0 1	Reserved	Reserved
0 1 0	Egress directed	An egress directed frame is sent by the host management system into the IMP port and is forwarded to the egress port specified in the destination port ID fields in the BRCM tag.
0 1 1	Multicast egress directed	A multicast egress directed frame is sent by the host management system into the IMP port and is forwarded to multiple egress ports specified in the dest port vector field.
1 x x	Reserved	Reserved

Table 12: IMP Broadcom TAG RX from CPU

TAG[31:29]	TAG[28:27]	TAG[26:5]	TAG[4:0]
OPCODE = Unicast (000)	NA	NA	NA
OPCODE = Single Egress Directed (010)	NA	NA	DST_PORTid[4:0]
OPCODE = Multicast Egress Directed (011)	TAG[28:17] = NA	Fwdmap [16:0] = TAG[16:0]	

OPCODE = 000:If a frame is unicast/multicast, then it is checked by ARL. If a frame is broadcast, it follows the broadcast rule. Basically, this OPCODE treats the frame like a normal network port.

OPCODE = 001: Reserved

OPCODE = 010: Single egress direct frame. Frame is forwarded to single destination port based on TAG[4:0].

OPCODE = 011:Multiple egress direct frame: Frame forward map is copied from TAG[16:0].

** By setting TAG[16] = 1, CPU scan loopback frame to itself.

OPCODE = 1xx:Reserved:

*** For reserved OPCODE, IMP (MII) port shall drop that frame.

When a packet is sent from the CPU to the IMP port, a minimum of 74 bytes is required. This includes the Broadcom Type (2 bytes), Broadcom Tag (4 bytes), minimum Ethernet frame size (64 bytes including CRC) and 4-byte Outer CRC. The Broadcom Tag and type fields along with the outer CRC would be stripped by the Switch and the minimum 64-byte Ethernet frame would be forwarded accordingly.

There is only one format for all frames from IMP to CPU. It covers all multicast, unicast, and broadcast frames. Frame byte count and source port ID will always be carried in TAG as shown in Table 13.

Table 13: IMP Broadcom TAG TX to CPU

TAG[31:29]	*TAG[28:15]*	*TAG[14:5]*	*TAG[4:0]*
OPCODE = 000	FM_byte_cnt[13:0]	NA	SRC Portid[4:0]

Programming Interfaces

The BCM5396 can be programmed via the SPI Interface or the EEPROM Interface. The interfaces share a common pin set that is configured via the CPU_EEPROM_SEL strap pin. The "SPI Interface" on page 58 provides access for a general-purpose microcontroller, allowing read and write access to the internal BCM5396 register space. It is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol. Alternatively, the "EEPROM Interface" on page 64 can be connected to an external EEPROM for writing register values upon power-up initialization.

The internal address space of the BCM5396 device is broken into a number of pages. Each page groups a logical set of registers associated with a specific function, for example, Page 00h: Control Registers, Page 01h: , Page 05h: , etc. Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is utilized.

All pages have reserved registers from addresses F0h–FFh, and all pages behave identically over this space. Address FFh is the Page Register accessible from any page. Writing a new binary value to these bits changes the currently accessible page. Address FEh is the SPI Status Register, and addresses F0h–F7h are the SPI Data I/O Register. These registers are used for writing and reading data to the register space.

Explanation follows for using the serial interface with an SPI-compatible CPU (SPI interface) or an EEPROM (EEPROM interface). Either mode can be selected with the strap pin, CPU_EEPROM_SEL. Both modes have access to the same register space.

SPI Interface

The BCM5396 can be controlled over a serial interface that is compatible with a subset of the Motorola Synchronous Serial Peripheral Interface (SPI) bus. The microcontroller interface consists of four signals: serial clock (SCK), slave select ($\overline{SS}$), master-in/slave-out (MISO) and master-out/slave-in (MOSI). The BCM5396 always operates as an SPI slave device, it never initiates a transfer on the SPI and only responds to the read/write requests issued from a master device.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM5396. This protocol establishes the definition of the first two bytes issued by the master to the BCM5396 slave during an SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

The SPI mode supports two different access mechanisms, normal SPI and fast SPI, determined by the content of the command byte. Figure 9 shows the normal SPI command byte, and Figure 10 shows the fast SPI command byte. These two mechanisms should not be mixed in an implementation; the CPU should always initiate transfers consistently with only one of the two mechanisms.

0	1	1	MODE = 0	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 9: Normal SPI Command Byte

Byte Offset (MSB)	Byte Offset	Byte Offset (LSB)	MODE = 1	CHIP ID 2 (MSB)	CHIP ID 1	CHIP ID 0 (LSB)	Read/Write (0/1)

Figure 10: Fast SPI Command Byte

The MODE bit (bit 4) of the command byte determines the meaning of bits 7:5. If bit 4 is a 0, it is a normal SPI command byte, and bits 7:5 should be defined as 011b. If bit 4 is a 1, bits 7:5 indicate a fast SPI command byte and the byte offset into the register that the BCM5396 starts to read from (byte offsets are not supported for write operations).

In both command bytes, bits[3:1] indicate the CHIP ID to be accessed. Because the BCM5396 operates as a single-chip system, the CHIP ID is 000. Note that the $\overline{SS}$ signal must also be active for any BCM5396 device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = Read, 1 = Write) and determines the transmission direction of the data.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page. This address is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/received, allowing a contiguous block data from a register to be stored/read in a single transmission.

When the fast SPI command byte mode is used, the actual start location of a read operation can be modified by the offset contained in bits 7:5 of the command byte. Reading/writing data from/to separate registers, even if those registers are contiguous in the current page, must be performed by supplying a new command byte and register address for each register, with the address as defined in the appropriate page register map.

Noncontiguous blocks are also stored/read through the use of multiple transmissions, which allow a new command byte and register base address to be specified. The $\overline{SS}$ signal must remain low for the entire read or write transaction, as shown in Figure 11 on page 60 and Figure 12 on page 60, with the transaction terminated by the deassertion of the $\overline{SS}$ line by the master.

Figure 11: SPI Serial Interface Write Operation

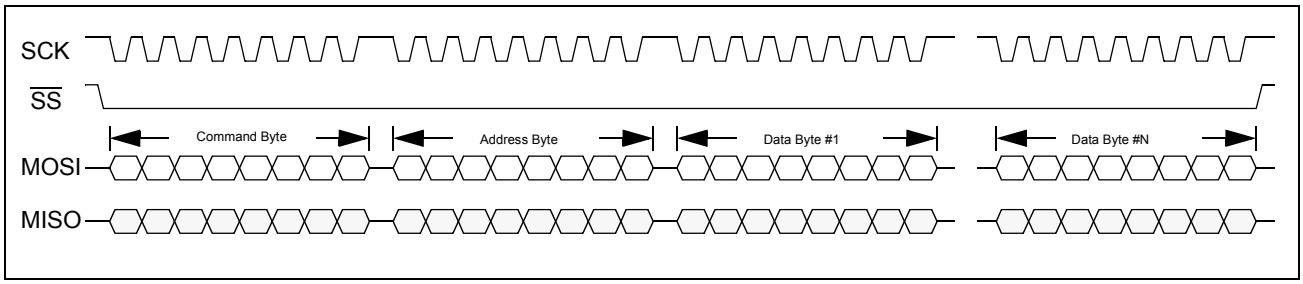
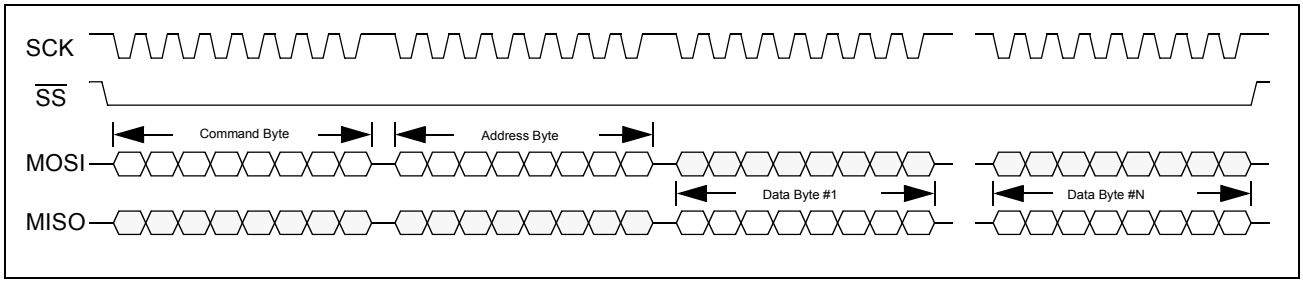


Figure 12: SPI Serial Interface Read Operation



The Serial interface supports operation up to 2 MHz in SPI mode. A maximum of four devices can be cascaded/addressed.

Normal SPI Mode

Normal SPI mode allows single-byte read and multi byte string write operations, with the CPU polling to monitor progress. Read operations are performed using the "SPI Status Register" on page 175 and "SPI Data I/O Register" on page 175. All read operations are of the form:

```
<CMD, CHIP ID, R><REG ADDR>
```

where the first byte is the command byte with the appropriate CHIP ID and read bits set, and the second byte is the register address.

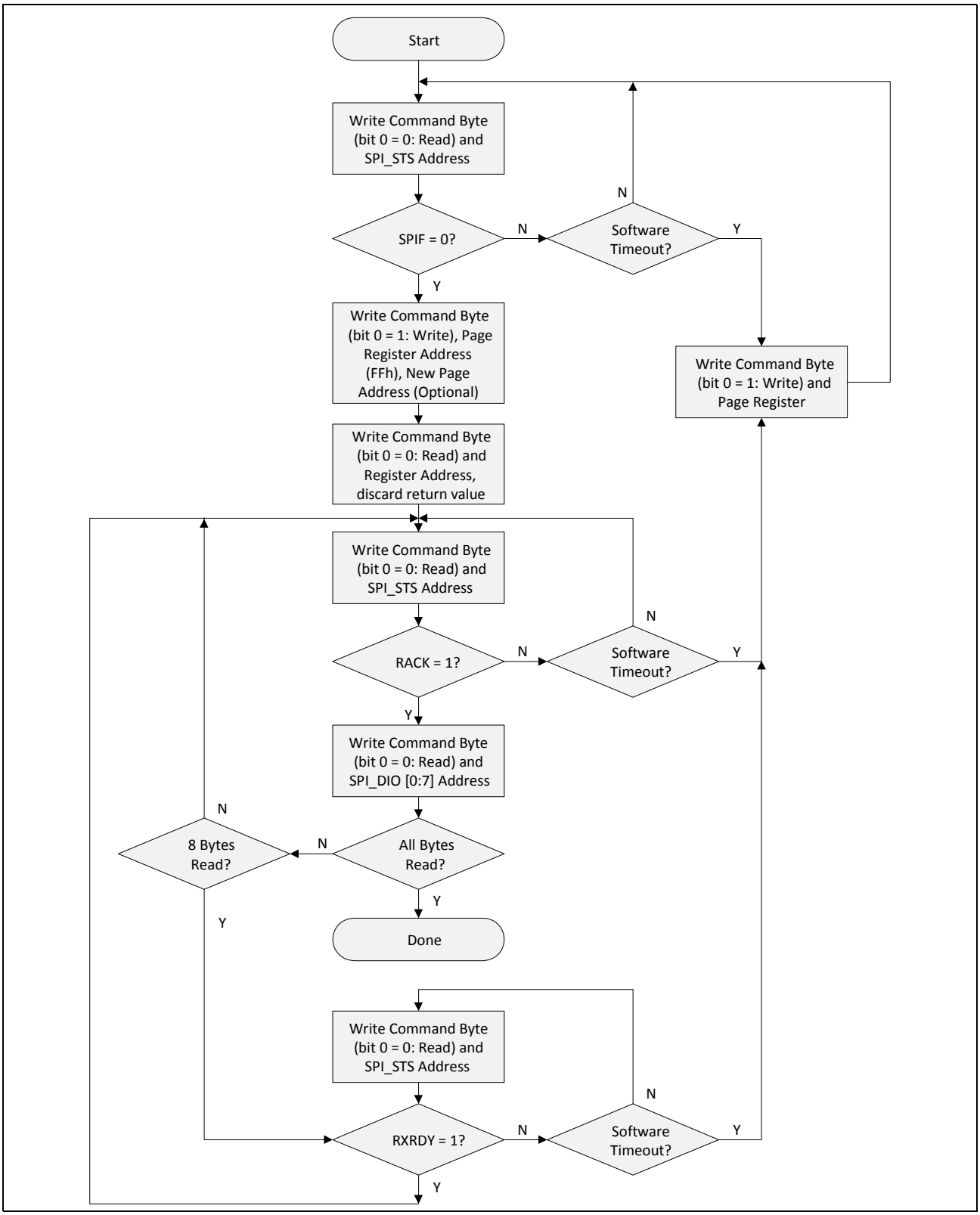
All write operations are of the form:

```
<CMD, CHIP ID, W><REG ADDR><DATA0>...<DATAn>
```

where the first byte is the command byte with the appropriate CHIP ID and write bits set, the second byte is the register address, and the remaining bytes are the exact number of data bytes appropriate for the selected register. Failure to provide the correct number of data bytes means the register write operation does not occur.

A simple flow chart for the read process is shown in Figure 13 on page 61.

Figure 13: Normal SPI Mode Read Flow Chart



To read a register, first the "Page Register" on page 175 is written (<CMD, CHIP ID, W><REG ADDR = FFh><DATA = NEW PAGE>). It is only necessary to write the page register when moving to a new page. Once in the correct page, a read operation is performed on the appropriate register (<CMD, CHIP ID, R><REG ADDR>). Once the "SPI Status Register" on page 175 indicates that the data is available (RACK = 1), the data can be read. Data is read from the "SPI Data I/O Register" on page 175, located at F0h–F7h on every page (so no page swap is necessary to read the data on any page). A read operation can access any or all of the bytes on a specific register, including the ability to start at any offset.

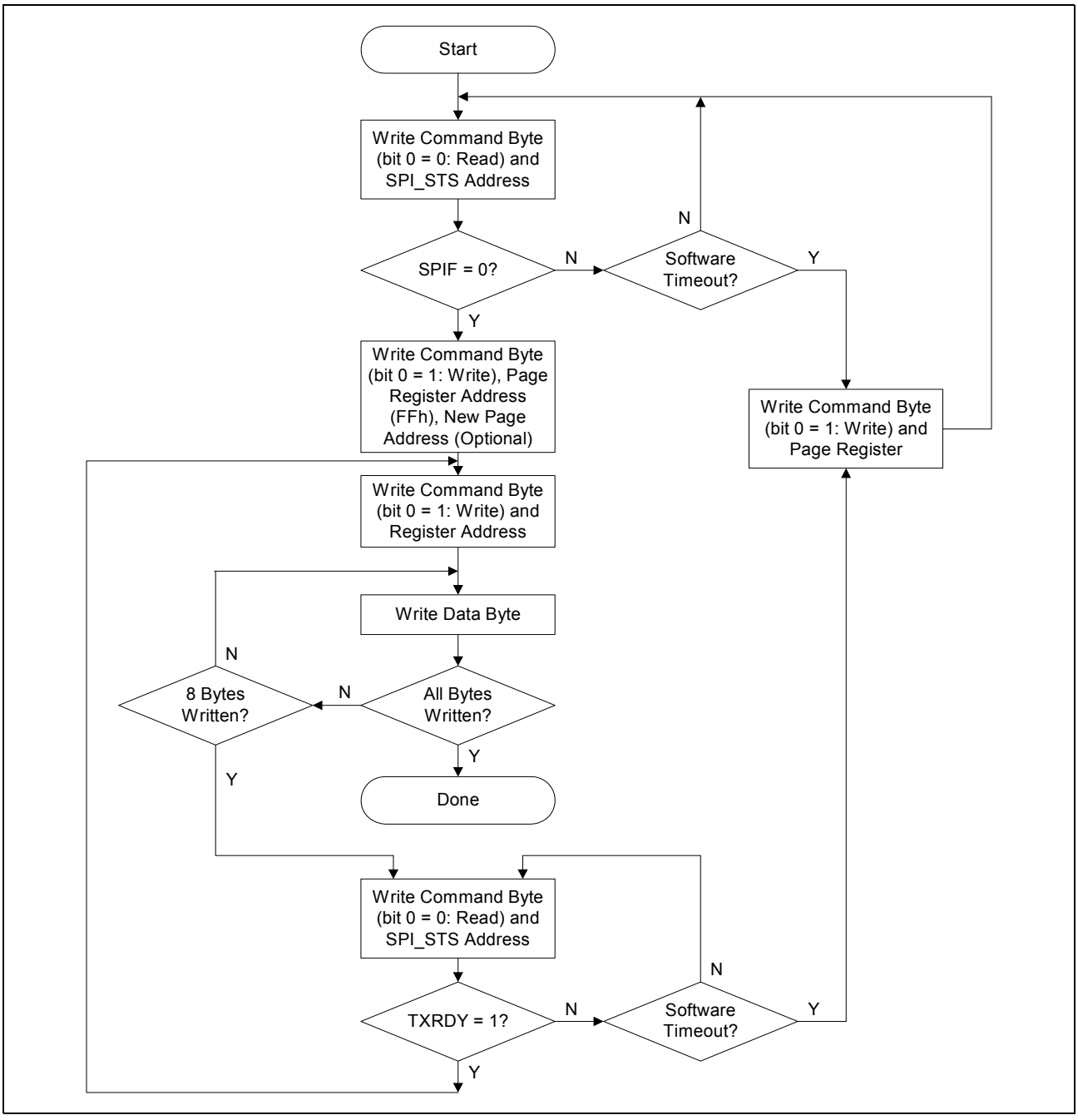
Example: Reading [0] from SPI Data I/O Register reads the least significant byte of the register, and successive reads to SPI Data I/O Register[0] read the remaining bytes. However, reading the first byte from SPI Data I/O Register[2] reads the third byte of the register, and successive reads to SPI Data I/O Register[2] read the remaining bytes of the register up to the most significant byte of the register. It is not necessary to read all bytes of registers, only the bytes of interest. The SPI master can then move on to perform another read or write operation.

A flowchart for the write process is shown in Figure 14 on page 63. To write a register, the Page Register is written to, if necessary, (<CMD, CHIP ID, W><REG ADDR = FFh><DATA = NEW PAGE>), then data is written to the selected register (<CMD, CHIP ID, W><REG ADDR><DATA0>...<DATAn>), where DATA0 is the least significant byte of the register, and DATAn is the most significant byte of the register, and the exact number of bytes is present as defined by the register width. No byte offset is provided for write operations, and all bytes must be present to activate the write process internal to the BCM5396.

The following simple rules apply to the normal SPI mode:

- A write to the Page Register at any time causes the SPI state machine to reset.
- A read operation can access any number of bytes at any offset using the SPI Data I/O Registers.
- A write operation must write the exact number of bytes to the register being accessed.
- The RXRDY/TXRDY flags in SPI Status Register must be checked after each 8-byte string has been read/written to ensure the next string is ready and can be accepted (since the largest internal register is 8 bytes, this restriction only applies to reading and writing frames via the SPI).

Figure 14: Normal SPI Mode Write Flow Chart



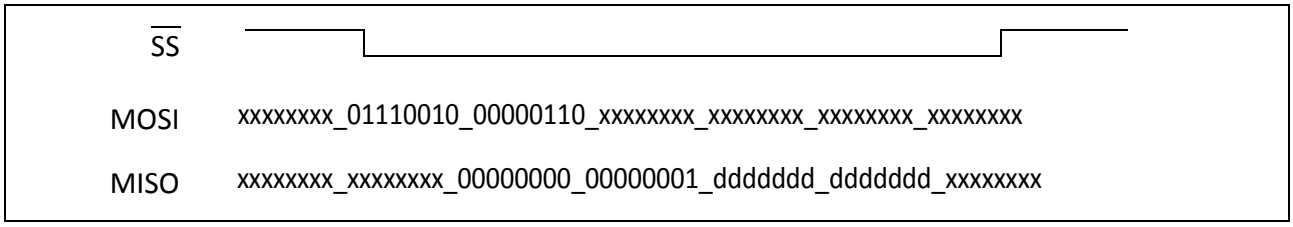
Fast SPI Mode

Fast SPI mode makes use of the fact that the SPI port is inherently full-duplex and provides an explicit acknowledge on read cycles to eliminate the polling of the SPI_STS register for RACK polling. Fast SPI mode requires the MODE bit in the command byte to be set as indicated in Figure 10 on page 59. Like normal SPI mode, fast SPI mode also supports byte offsets for read operations.

Read operations do not access the SPI Data I/O Register. Instead, status and data are output on the MISO line by the BCM5396. Once the page register and the register within that page have been set, the master reads the MISO line state. The BCM5396 immediately puts out a byte string which indicates the state of the RACK bit in bit 0. Once bit 0 is sampled high, the next byte is the least significant byte of the read data, and successive bytes follow. Byte offset of the register is provided by using bits 7:5 of the command byte to index from byte 0 (000) to byte 7 (111) as the first byte to be presented on MISO.

Example: If command byte [7:0] = 011_1_001_0 that indicates a read offset of 3 (4th byte) in the register to be accessed (register 6 in this example). The RACK status bit is provided on the MISO line (00000001) when the read data (dddddddd) is to follow on the MISO line. An example of the timing is shown in Figure 15.

Figure 15: Timing Example



Write operations are identical in fast and normal SPI mode.

EEPROM Interface

The BCM5396 can be connected via the serial interface to a low-cost external serial EEPROM, enabling it to download register programming instructions during power-on initialization. For each programming instruction fetched from the EEPROM, the instruction executes immediately and affects the register file.

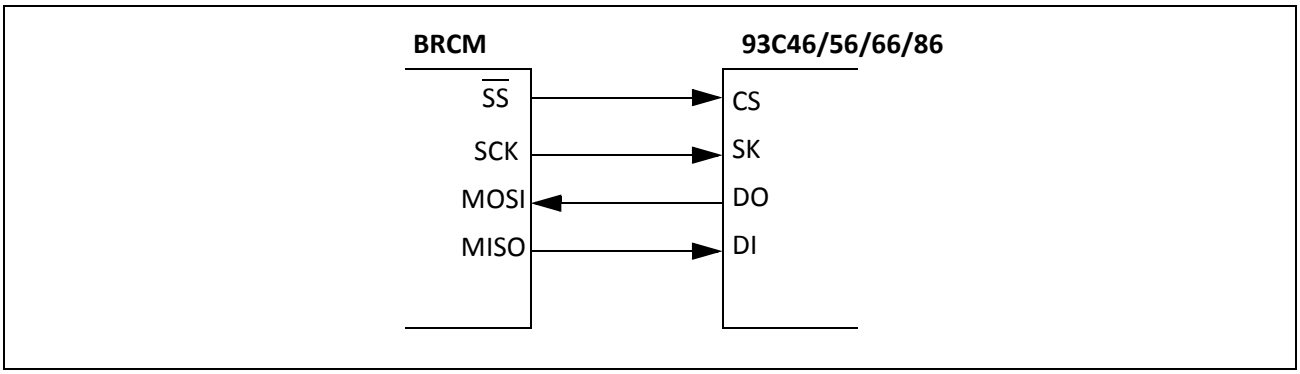
During the chip initialization phase, the data is sequentially read-in from the EEPROM after the internal memory has been cleared. The first data read-in is the HEADER and matches a predefined magic code. In the case where the HEADER data does not match the instruction fetch, the process stops, and the EEPROM controller treats it as if no EEPROM exists. If the magic code matches, the fetch instruction process continues until it reaches the instruction length defined in the HEADER.

Due to the different access cycles of different capacity EEPROMs, the strap pins EEPROM_EXT[1:0] are used to support the various EEPROM devices according to Table 14.

Table 14: EEPROM_EXT[1:0] Settings

EEPROM_EXT[1:0]	*EEPROM*
00	93C46
01	93C56
10	93C66
11	93C86

Figure 16: Serial EEPROM Connection



EEPROM Format

The EEPROM should be configured to x16 word format. The header contains a key and length information as in Table 15. The actual data stored in EEPROM is byte-swapped as shown in Table 16.

- Upper 5 bits are magic code 15h, which indicates that valid data follows.
- Bit 10 is for speed indication. A 0 means normal speed. A 1 indicates speedup. The default is 0.
- Lower 10 bits indicate the total length of all entries. For example:
  - 93C46 up to 64 words
  - 93C56 up to 128 words
  - 93C66 up to 256 words
  - 93C86 up to 1024 words

Table 15: EEPROM Header Format

15:11	*10*	*9:0*
Magic code, 15h	Speed	Total Entry Number 93C46: 0—63 93C56: 0–127 93C66: 0–255 93C86: 0–1023

Table 16: EEPROM Contents

7:0	*15:11*	*10*	*9:8*
Total entry number	Magic code, 15h	Speed	Total entry number

After chip initialization, the header is read from the EEPROM and used to compare to the predefined magic code. When the fetched data does not match the predefined magic code, the EEPROM instruction fetch process is stopped. If the magic code is matched, fetching of instructions continues until the instruction length is as defined by the total entry number in the header, as listed in Table 15.

The EEPROM Port shares pins with the SPI port. Either the SPI port or the EEPROM can be selected by using the strap pin, CPU_EEPROM_SEL. The register space for the EEPROM port is the same as for the SPI port.

Ask your local Broadcom FAE for EEPROM Programming Guide for more details on EEPROM data format.

MDC/MDIO Interface

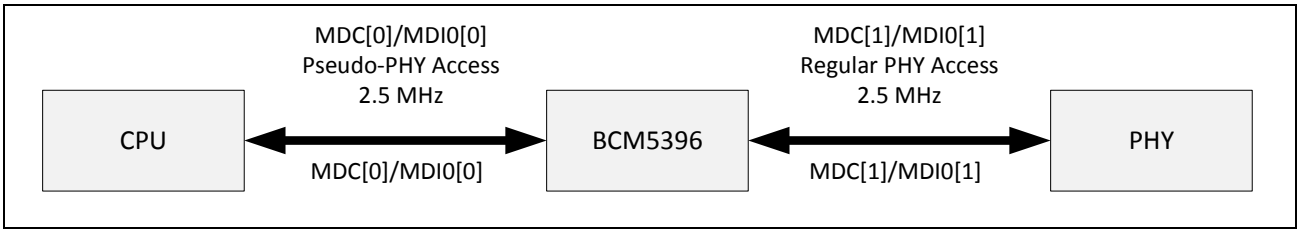
The BCM5396 has an MDC/MDIO interface to read/write the register information of the external PHYs. Each of the external PHYs can be connected to the MDC[1] and MDIO[1] pins of the BCM5396. The BCM5396 can automatically poll the register set of the external PHY if the AUTO_POLL_DIS pin is pulled low during power-on/reset.

Each serial port external PHY of the BCM5396 is assigned a unique PHY address. The address by default is set to ascending or descending order, based on the internal register setting (Page 00h: Addr 86h). Each external PHY checks that the PHY address of the initiated command matches that of its own before executing the command. The MDC[1]/MDIO[1] interface is not used for an external device to poll the register set of the internal PHY ports.

Note: The MDC[1]/MDI0[1] interface on BCM5396 is master and used to poll the register set of an external PHY.

The BCM5396 has a default chip ID of 00. This chip ID cannot be modified.

Figure 17: MDC/MDIO Interface



Register Access Through Pseudo-PHY Interface

All the BCM5396 registers can be accessed through the MDC[0] and MDIO[0] interface from the CPU. The MDC[0]/MDIO[0] interface is slave on BCM5396 and is connected to the internal SPI interface of the switch. The switch register and internal SerDes PHY register is organized into pages, each of which contains a certain set of registers. To access the switch register, both the page number and the register address need to be specified.

The switch and internal SerDes PHY registers are accessed through a pseudo-PHY (PHY Address = 0x1E), which is not used by any of the physical PHYs on the BCM5396 MDC[0]/MDIO[0] path. The algorithm for read access to the switch registers is shown in Figure 18 on page 68. The algorithm for write access to it is shown in Figure 19 on page 69. The pseudo-PHY MDC[0]/MDIO[0] interface has an address space of 32, as shown in Figure 20 on page 70. The first 16 registers are reserved by IEEE. Only addresses 16–31 can be used to access. The MDC[0]/MDIO[0] registers used to access are defined in Table 17 on page 71. The register page number, register address, and access type are determined by registers 16 and 17. The data read from a register or written to a register is stored in registers 0x24 to 0x27 (64 bits total).

Note: The internal SerDes PHY registers are also accessed through the Pseudo-PHY (PHY Address = 0x1E) on MDC[0]/MDIO[0] bus, like other switch registers. The internal SerDes PHY registers can NOT be accessed by MDC[0]/MDIO[0] directly.

Figure 18: Read Access to Switch via Pseudo-PHY (PHY ADD = 1_1110) MDC[0]/MDIO[0] Path

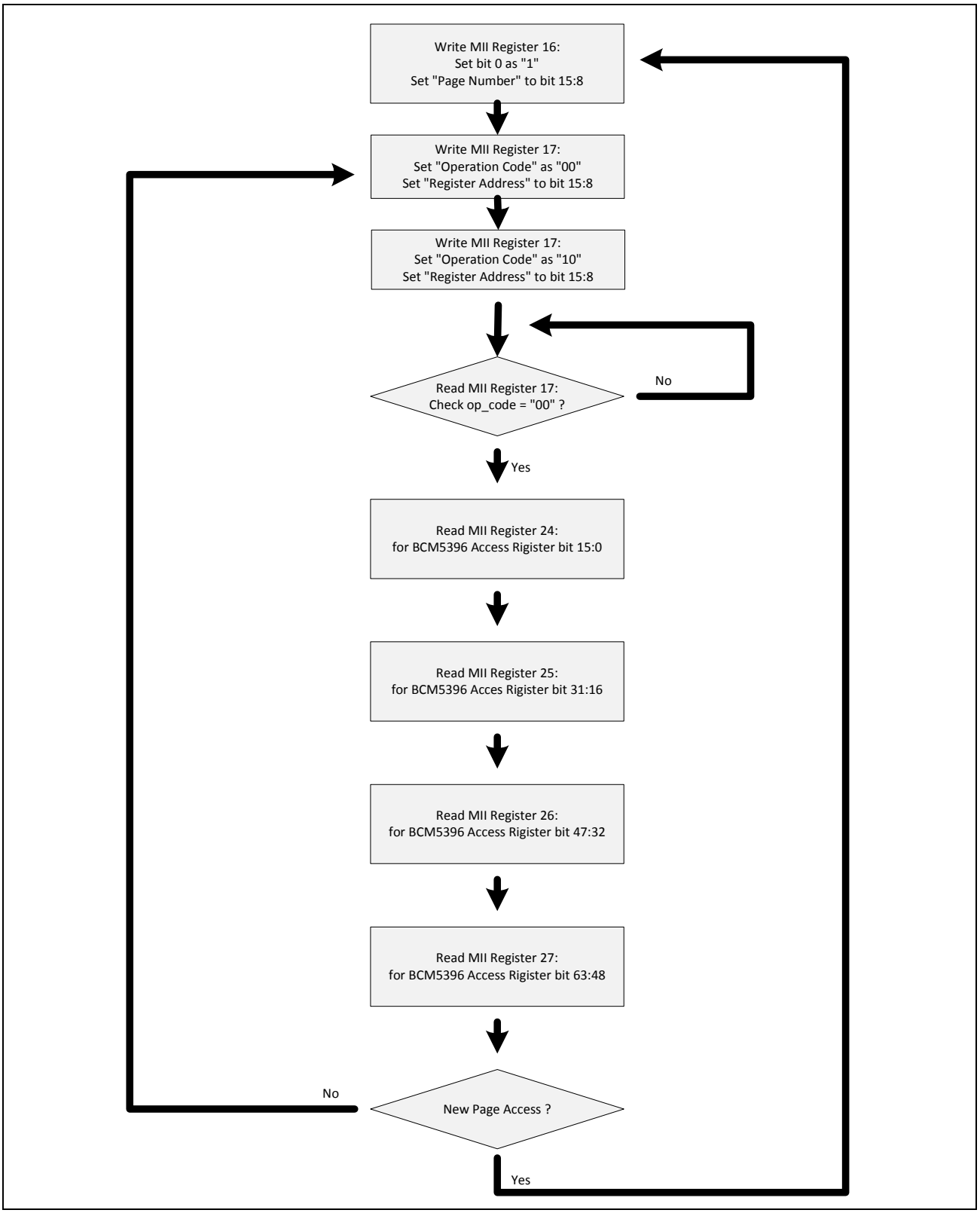


Figure 19: Write Access to Switch via Pseudo-PHY (PHY ADD = 1_1110) MDC[0]/MDIO[0] Path

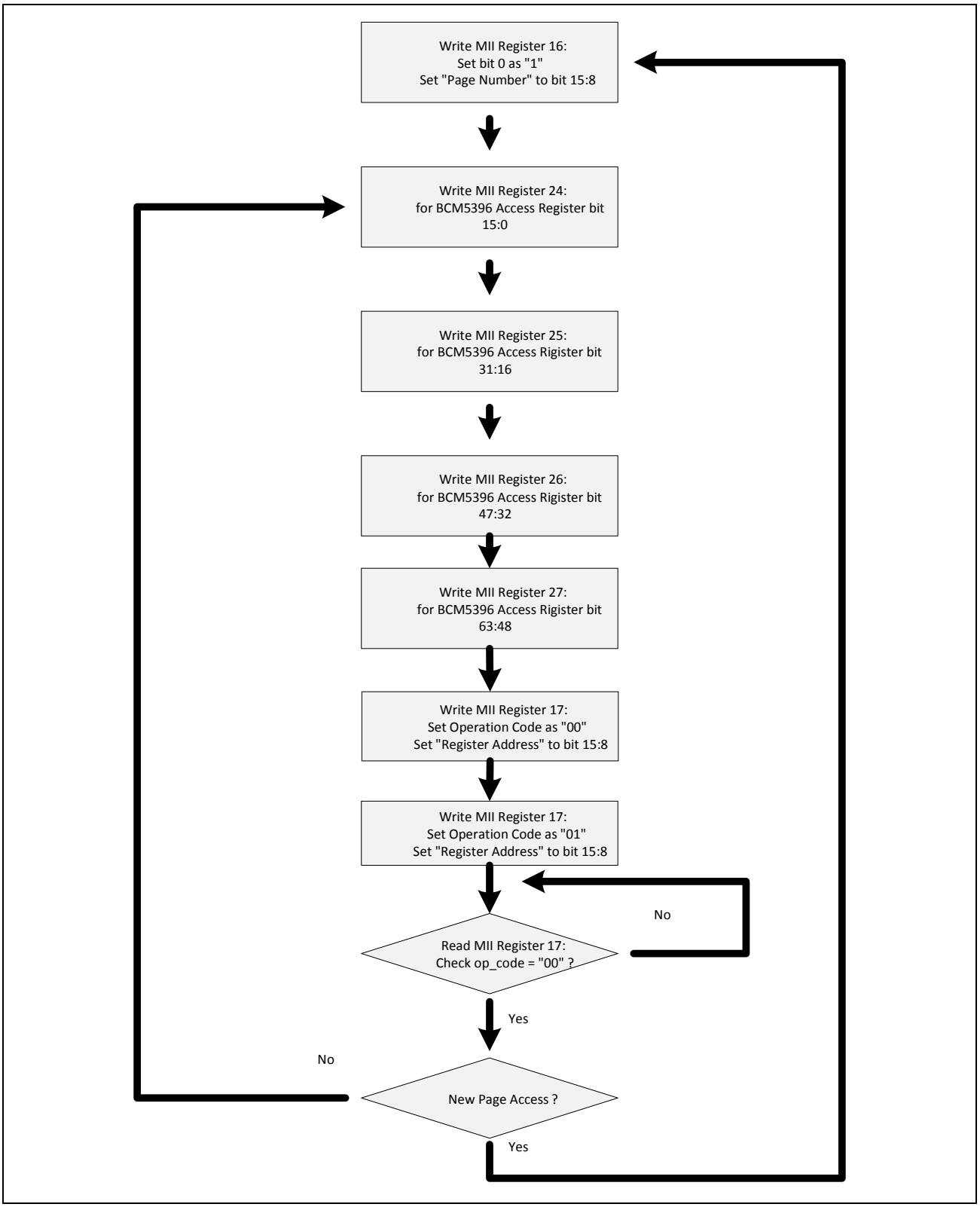


Figure 20: Pseudo-PHY MII Register Map

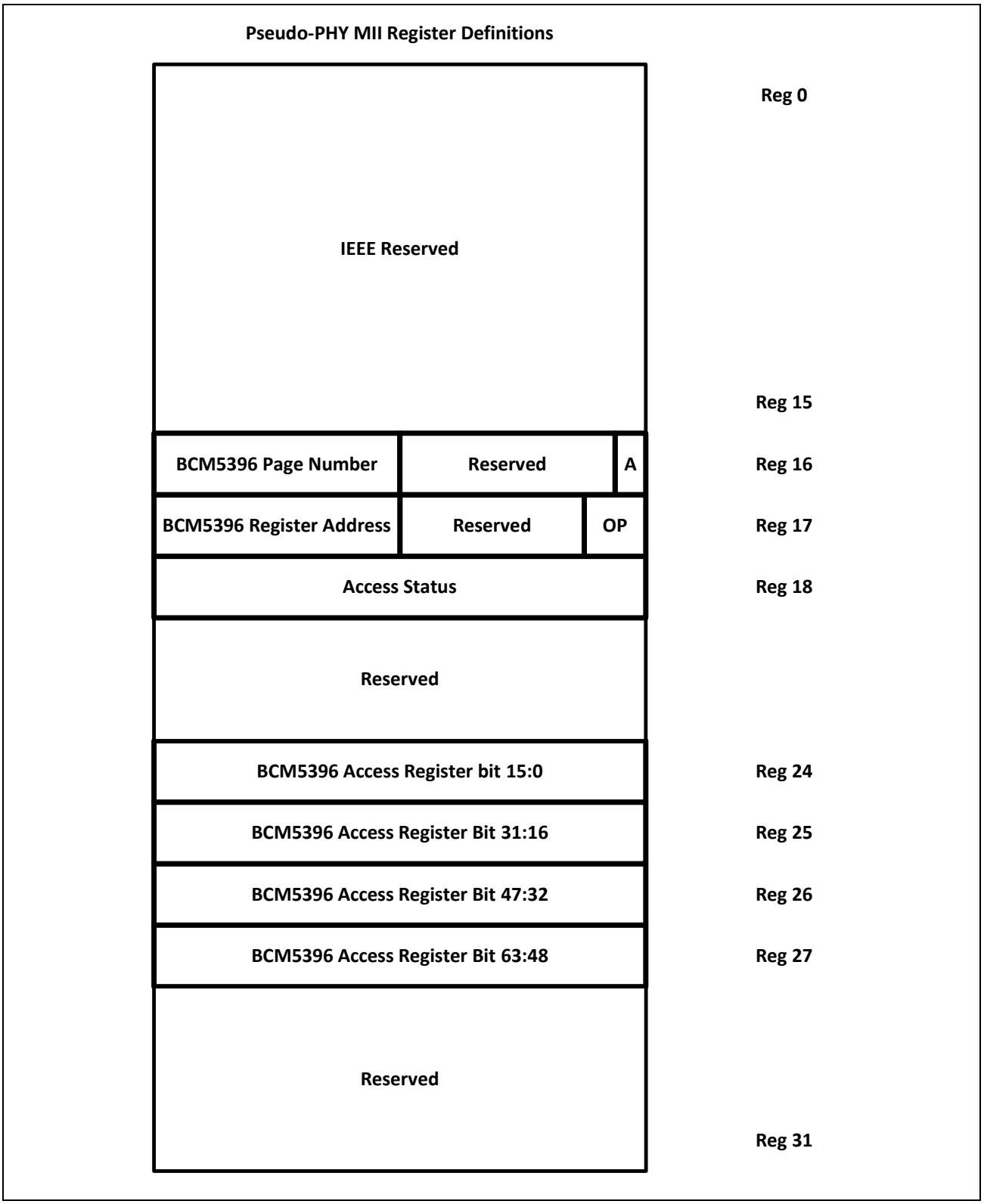


Table 17: Pseudo-PHY MII Register Definitions

Bits	R/W	Description
Register 16 (0x10)—Switch Register Set Access Control Register		
15:8	R/W	Switch page number
7:1	Reserved	Reserved
0	R/W	Switch register set MDC[0}/MDIO[0] access enable
Register 17 (0x11)—Switch Register Set Read/Write Access Control Register		
15:8	R/W	Switch register address.
7:2	Reserved	Reserved
1:0	RW/SC	Opcode: 00 = No operation 01 = Write operation 10 = Read operation 11 = Reserved
Register 18 (0x12)—Switch Register Access Status Register		
15:2	Reserved	Reserved
1	RO/LH	Operation error. This bit is set to show operation error when opcode is 11.
0	RO/LH	Prohibit access (for page number = 8'h1X, which are PHY MII registers).
Register 24 (0x18)—Switch Register Access		
15:0	R/W	Switch Access register bits [15:0].
Register 25 (0x19)—Switch Register Access		
31:16	R/W	Switch Access register bits [31:16].
Register 26 (0x1A)—Switch Register Access		
47:32	R/W	Switch Access register bits [47:32].
Register 27 (0x1B)—Switch Register Access		
63:48	R/W	Switch Access register bits [63:48].
Register 28–31 (0x1C–0x1F)—Reserved		

MDC/MDIO Interface Register Programming

The BCM5396 is fully compliant with the MII clause of the IEEE Standard 802.3u Ethernet specification. There are two pins of MDC and two pins of MDIO. When the switch is slave-driven by the 2.5 MHz MDC[0], the serial input/output data signal is an MDIO[0] slave for pseudo-MDIO switch read/write register access.

When the external PHY registers are serially written to or read from, the BCM5396 sources MDC[1] clock and BCM5396 MDC[1]/MDIO[1] is the MDIO master. Serial bidirectional data transmitted via the respective MDIO pin is synchronized with the respective MDC clock.

The MDIO bits are latched on the rising edge of the MDC clock. MDC may be stopped between frames provided no timing requirements are violated. MDC must be active during each valid bit of every frame, including all preamble, instruction, address data, and at least one idle bit. Each MII read or write instruction is initiated by the BCM5396 and contains the following:

- **Preamble (PRE)**. To signal the beginning of an MII instruction after reset, at least 32 consecutive one bits must be written to the MDIO pin. A preamble of 32 one bits is required only for the first read or write following reset. A preamble of fewer than 32 one bits causes the remainder of the instruction to be ignored.
- **Start of Frame (ST).** A 01 pattern indicates that the start of the instruction follows.
- **Operation Code (OP)**. A read instruction is indicated by 10, while a write instruction is indicated by 01.
- **PHY Address (PHYAD)**. A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
- **Register Address (REGAD)**. A 5-bit register address follows, with the MSB transmitted first.
- **Turnaround (TA).** The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent by the BCM5396 chip during these two bit times. When a read operation is being performed, the MDIO pin of the BCM5396 must be put in a high-impedance state during these bit times. The external PHY drives the MDIO pin to 0 during the second bit time.
- **Data.** The last 16 bits of the Instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first by the BCM5396. During a read operation, the data bits are driven by the external PHY with the MSB transmitted first.

Table 18 summarizes the complete management frame format.

Table 18: MII Management Frame Format

Operation	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*Data*	*Direction*
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ	Z ... Z	Driven to PHY
						Z0	D ... D	Driven by PHY
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Driven to PHY

See Section 9: “Timing Characteristics,” on page 179 for more information regarding the timing requirements.

Example: To put a PHY with address 00001 into loopback mode, issue the following write MII instruction:

1111 1111 1111 1111 1111 1111 1111 1111 0101 00001 00000 10 0100 0000 0000 0000

To determine if a PHY is in the link pass state, issue the following read MII instruction:

1111 1111 1111 1111 1111 1111 1111 1111 0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ

The external PHY drives the MDIO line during the last 17 bit times. If the link status is good, the third bit from the end (bit 2) is 1.

Note:

1. TA1 bit will be low when the MDC[0]/MDIO[0] reads BCM5396, that is one clock cycle ahead to be low compared to IEEE Clause 22 standard. TA1 and TA0 bits are both 0 when reading BCM5396.
2. The last respond data bit (bit[0]) cycle on MDIO[0] from BCM5396 is shorter that other previous data bits when the MDC[0]/MDIO[0] master reads BCM5396. But the setup and hold time of the last respond data bit still can meet the MDC[0]/MDIO[0] master timing requirement.

LED Interfaces

The BCM5396 provides visibility per port of link status, port speed, duplex mode, combined transmit and receive activity, and collision. The Serial LED Interface is supplied to drive the status to the LEDs as outlined in "LED Control Register (Page 00h: Address 24h–25h)" on page 95.

During power-on and reset, the serial interface shifts a continuous low value for 1.34 seconds.

Serial LED Interface

A two-pin serial interface, LEDDATA and LEDCLK, provides data and clock to enable external shift registers to capture the LED status indications from the BCM5396 for each port. The status encapsulated within the shift sequence is configured by the LEDMODE[2:0] configuration signals. The configuration signals select both the number of status bits per port and the status type of each bit.

LEDCLK is generated by dividing the 25 MHz input clock by 8, providing a 320 ns clock period. The LEDDATA outputs are generated on the falling edge of the LEDCLK, and they have adequate setup and hold time to be clocked externally on the rising edge of LEDCLK.

The first two bits in the sequence are RESVD and LEDERR. Next follows an 8-bit load status word. The following shift sequence is sequential per port status words:

1. Each port status word contains up to 2 to 5 bits, depending on mode selection, for the designated status.
2. Port 0 status word is shifted out first, followed by port 1 and then the remaining serial ports.
3. The shift sequence is repeated every 42 ms.

Table 19: Serial LED Mode Matrix

LEDMODE[2:0]	***Port N (N = 0–15) Starting from Port 0***						
Page 00 Addr 24H~25H Bit[10:8]	***stat0[1:0]***	***stat1[7:0]***	***stat2***	***stat3***	***stat4***	***stat5***	***stat6***
000	RESVD LEDERR	LOAD	LNK/ACT	DUPLEX	SPEED100	SPEED1000	–
001	RESVD LEDERR	LOAD	LNK/ACT/SPD	DUPLEX	–	–	–
010	RESVD LEDERR	LOAD	LNK	ACT	SPEED100	SPEED1000	DUPLEX
011	RESVD LEDERR	LOAD	LNKG/ACTF	LNKF/ ACTG	DPX/COL	–	–
100	RESVD LEDERR	LOAD	LNK/ACT	DUPLEX	SPEED100	SPEED1000	COLSN
101	RESVD LEDERR	LOAD	LNK/ACT/SPD	DUPLEX	COLSN	–	–
110	RESVD LEDERR	LOAD	DUPLEX	COLSN	–	–	–

Table 19: Serial LED Mode Matrix (Cont.)

LEDMODE[2:0]	Port N (N = 0–15) Starting from Port 0						
Page 00 Addr 24H~25H Bit[10:8]	stat0[1:0]	stat1[7:0]	stat2	stat3	stat4	stat5	stat6
111	RESVD LEDERR	LOAD	LNK/ACT	DPX/COL	SPEED1000	SPEED100	–

Table 20: Serial LED Status Types

Name	Description
LEDERR	Error indication. Internal memory fails self-test during power-on reset. Low if failure occurs.
LOAD	Bandwidth utilization indicator. 8-bit binary value indicating the percentage of total switch bandwidth utilized over a 42 ms interval for packet data.
LNK	Link indicator. Low when link is established. High when link is off.
LNK/ACT	Link and activity indicator. Low when link is established. Blinking at 12 Hz when link is up and port is transmitting and receiving.
LNK/ACT/SPD	Link, activity, and speed indicator. Low when link is up. Blinks at 3 Hz when port is transmitting or receiving in 10 Mbps mode. Blinks at 6 Hz when port is transmitting or receiving in 100 Mbps mode. Blinks at 12 Hz when in 1000 Mbps mode.
LNKG/ACTF	1 Gbps link, 10/100 Mbps activity indicator. Low when 1000 Mbps link is up. Blinks at 12 Hz when there is activity in 10 Mbps/100 Mbps mode. High in all other cases.
LNKF/ACTG	10/100 Mbps link, 1 Gbps activity indicator. Low when 10 Mbps/100 Mbps link is up. Blinks at 12 Hz when there is activity in 1000 Mbps mode. High in all other cases.
DUPLEX	Duplex mode indicator. High for half-duplex or no link, and low for full-duplex and link.
DPX/COL	Duplex and collision indicator. Blinking when collision is detected. Low for full-duplex and link.
ACT	Activity indicator. Low for 42 ms when transmit or receive activity is detected during previous 42 ms interval. High during no activity or no link.
COLSN	Collision indicator. Low for 42 ms when collision is detected during the previous 42 ms interval. High in the absence of collisions or no link.
SPEED100	100M speed indicator. Low for 100 Mbps link; otherwise, high.
SPEED1000	1000M speed indicator. Low for link at 1000 Mbps, high for all other conditions.

The load meter LEDs provide a bar-graph indication of the percentage of total available bandwidth of the switch utilized by packet data over a periodic interval of 42 ms. The bar graph scale is shown in Table 21.

Table 21: Load Meter LED Decode

Load[7:0]	Number of LEDs ON	Bandwidth (%)
00000000	8	100% (all LEDs on)
10000000	7	>50.0%
11000000	6	25.0-50.0%
11100000	5	12.5-25.0%
11110000	4	6.25-12.5%

Table 21: Load Meter LED Decode (Cont.)

Load[7:0]	*Number of LEDs ON*	*Bandwidth (%)*
11111000	3	3.13-6.25%
11111100	2	1.56-3.13%
11111110	1	0.78-1.56%
11111111	0	< 0.78% (all LEDs off)

Section 5: Hardware Signal Definitions

I/O Signal Types

The following conventions are used to identify the I/O types in Table 23: “Signal Descriptions,” on page 77. The I/O pin type is useful in referencing the DC pin characteristics contained in “Electrical Characteristics” on page 177.

Table 22: I/O Signal Type Definitions

Abbreviation	*Description*
$\overline{\ }$	Active-low signal, indicated by overbar
3T	3.3V-tolerant
A	Analog pin type
B	Bias pin type
CS	Continuously sampled
D	Digital pin type
DNC	Do not connect
G	SGMII pin type
GND	Ground
I	Input
I/O	Bidirectional
I_{PU}	Input with internal pull-up
O_{3S}	Three-state output
OD	Open drain
O_{DO}	Open-drain output
OT	Tri-stateable signal
O	Output
PD	Internal pull-down
SOR	Sample on reset
PWR	Power pin supply
PU	Internal pull-up
XT	Crystal pin type

Signal Descriptions

Table 23: Signal Descriptions

Signal Name	Type	Description
Serial Interface		
RXDN[1:16] RXDP[1:16] TXDN[1:16] TXDP[1:16]	I/O_A	**Serial Transmit/Receive pairs.** Differential Serial input and output data pairs.
Clock/Reset		
$\overline{\text{RESETB}}$	I_{PU}, CS, D, ST, 3T	**Hardware Reset Input.** Active-low Schmitt-triggered input. Resets the BCM5396.
XTALI[1:0] XTALO[1:0]	I_{XT} O_{XT}	**25 MHz Crystal Oscillator Input/Output.** A continuous 25 MHz reference clock must be supplied to the BCM5396 by connecting a 25 MHz crystal between these two pins or by driving XTALI with an external 25 MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTALO unconnected. The maximum XTALI input voltage is 3.0V.
IMP Interface		
Imp_GTXCLK (If IMP port not used, may be left floating)	O	**IMP GMII Transmit Clock.** This clock is driven to synchronize the transmit data in GMII mode. **RGMII Transmit Clock.** This clock is driven to synchronize the transmit data in RGMII mode. 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. In RGMII mode, both edges of the clock are used to align with TXD[3:0].
Imp_TXCLK (If IMP port not used, may be left floating)	I O	**IMP MII Transmit Clock.** Synchronizes the TXD[3:0] in MII mode. In 100 Mbps mode, this output is 25 MHz. In 10 Mbps mode this output is 2.5 MHz. **RvMII Receive Clock.** Synchronizes the TXD[3:0] in RvMII mode and connects to the MAC/management entity RXC. In 100 Mbps mode, this output is 25 MHz. In 10 Mbps mode this output is 2.5 MHz.
Imp_TXD[7:0]	O	**IMP GMII Transmit Data Output (First Nibble).** Data bits TXD[7:0] are clocked on the rising edge of GTXCLK. **RGMII Transmit Data Output.** For 1000 Mbps operation, data bits TXD[3:0] are clocked on the rising edge of GTXCLK, and data bits TXD[7:4] are clocked on the falling edge of GTXCLK. For 10 Mbps and 100 Mbps operation, data bits TXD[3:0] are clocked on the rising edge of GTXCLK. **MII Transmit Data Output**. Clocked on the rising edge of TXCLK supplied by MAC/management entity. **RvMII Receive Data Output**. Clocked on the rising edge of TXCLK and connected to the RXD pins of the external MAC/management entity.

Table 23: Signal Descriptions (Cont.)

Signal Name	Type	Description
Imp_TXEN	O	**IMP GMII/MII Transmit Enable.** Active-high. TXEN indicates the data on the TXD pins is encoded and transmitted. **RGMII Transmit Control.** On the rising edge of TXCLK, TXEN indicates that a transmit frame is in progress, and the data present on the TXD[3:0] output pins is valid. On the falling edge of TXCLK, TXEN is a derivative of GMII mode TXEN and TXER signals. **RvMII Receive Data Valid.** Active high. Connected to RXDV pin of MAC/management entity. Indicates that a receive frame is in progress, and the data present on the TXD[3:0] output pins is valid.
Imp_TXER	O	**IMP GMII/MII Transmit Error.** Active-high. Asserting TXER when TXEN is high indicates an transmission error. TXER is also used to indicate carrier extension when operating in Half-duplex mode.
Imp_RXCLK	I	**IMP GMII Receive Clock.** 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. **RGMII Receive Clock.** 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. Data bits RXD[3:0] are clocked in on the rising edge of the RXCLK, and data bits RXD[7:4] are clocked in on the falling edge of the RXCLK. **MII Receive Clock.** 25 MHz for 100 Mbps operation, and 2.5 MHz for 10-Mbps operation.
	O	**RvMII Transmit Clock.** Synchronizes the RXD[3:0] in RvMII mode and connects to the MAC/management entity TXC. 25 MHz for 100 Mbps mode, and 2.5 MHz for 10 Mbps mode.
Imp_RXD[7:0]	I	**IMP GMII Receive Data Input (First Nibble).** Data bits RXD[7:0] are clocked on the rising edge of RXCLK. **RGMII Receive Data Input.** For 1000 Mbps operation, data bits RXD[3:0] are clocked-in on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mbps and 100 Mbps modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK. **MII Receive Data Input.** Data bits RXD[3:0] are clocked on the rising edge of RXCLK. **RvMII Transmit Data Input.** Clocked on the rising edge of RXCLK and connected to the TXD pins of the external MAC/management entity.
Imp_RXDV	I	**GMII/MII Receive Data Valid.** Active high. RXDV indicates that a receive frame is in progress, and the data present on the RXD output pins is valid. **RGMII Receive Data Valid.** Functional equivalent of GMII RXDV on the rising edge of RXCLK and functional equivalent of a logical derivative of GMII RXDV and RXER on falling edge of RXCLK. **RvMII Transmit Enable.** Active-high. Indicates the data on the RXD[3:0] pins is encoded and transmitted. Connects to the TXEN of the external MAC/management entity.
Imp_RXER	I	**GMII/MII Receive Error.** Indicates an error during the receive frame.

Table 23: Signal Descriptions (Cont.)

Signal Name	Type	Description
MDC/MDIO Interface		
MDIO[0]	I/O_{PU}	**Management Data I/O.** This serial input/output data signal is an MDIO slave for pseudo MDIO switch read/write register access. See "MDC/MDIO Interface" on page 66 for more information.
MDC[0]	I/O_{PU}	**Management Data Clock.** This is a 2.5 MHz clock and the switch is slave. Accesses internal MII registers and BCM5396 registers. It is also called "Pseudo_PHY"
MDIO[1]	I/O_{PU}	**Management Data I/O.** This serial input/output data signal is an MDIO master for external PHY Scan in the normal mode. It is a slave in SerDes test mode.
MDC[1]	I/O_{PU}	**Management Data Clock.** This is a 2.5 MHz clock and the switch is master. Access external MII registers by using CPU SPI Master. It is also dedicated for PHY_SCAN logic to constantly scan external PHY status, when strap pin Auto_Poll_Disable is set to 0. It is also called Hardware Polling.
LED Interface		
LEDCLK	O_{PD}	**LED Shift Clock.** This clock is periodically active to enable LEDDATA to shift into external registers.
LEDDATA	O_{PD}	**Serial LED Data Output.** Serial LED data for all ports is shifted out when LEDCLK is active. LEDMODE[2:0] pins set the serial data content. See "LED Interfaces" on page 73 for a functional description of this signal.
Programming Interfaces		
SCK	I_{PD}, 3T	**SPI Serial Clock.** Clock input to the BCM5396 SPI Interface supplied by the SPI master. Supports up to 2 MHz. Enabled if CPU_EEPROM_SEL is high during power-on reset.
	O_{PD}	**EEPROM Serial Clock.** Clock output to an external EEPROM device. Enabled if CPU_EEPROM_SEL is low during power-on reset. See "Programming Interfaces" on page 58 for more information.
$\overline{SS}$/CS	I_{PU}, 3T	**SPI Slave Select.** Active low signal which enables a SPI Interface Read or Write operation. Enabled if CPU_EEPROM_SEL is high during power-on reset.
	O_{PU}	**EEPROM Chip Select.** Active high control signal that enables a read operation from an external EEPROM device. Enabled if CPU_EEPROM_SEL is low during power-on reset. See "Programming Interfaces" on page 58 for more information.
MOSI/DI	I_{PU}, 3T	**SPI Master-Out/Slave-In.** Input signal which receives control and address information for the SPI Interface, as well as serial data during Write operations. Enabled if CPU_EEPROM_SEL is high during power-on reset.
	O_{PU}	**EEPROM Data In.** Serial data input to an external EEPROM device. Enabled if CPU_EEPROM_SEL is low during power-on reset. See "Programming Interfaces" on page 58 for more information.

Table 23: Signal Descriptions (Cont.)

Signal Name	Type	Description
MISO/DO	O_{PU} PU	**SPI Master-In/Slave-Out.** Output signal which transmits serial data during a SPI Interface Read operation. Enabled if CPU_EEPROM_SEL is high during power-on reset.
	I_{PU}	**EEPROM Data Out.** Serial data output to an external EEPROM device. Enabled if CPU_EEPROM_SEL is low during power-on reset. See "Programming Interfaces" on page 58 for more information.
Configuration Pins		
AUTO_POLL_DIS	$I_{PD, SOR}$	Automatic PHY Polling Disable. • 0 = Enable external PHY polling. • 1 = Disable external PHY polling. See "MDC/MDIO Interface" on page 66 for more information.
MEM_CLK_FREQ[1:0]	$I_{PD,}$ SOR	System Clock Selection. Determines rate of system clock. Both pins should be low for normal operation. 00 = 156.3 MHz (Normal Operation) 01 = 125.0 MHz 10 = 138.9 MHz
CPU_EEPROM_SEL	$I_{PU,}$ SOR	CPU or EEPROM Interface Selection. CPU_EEPROM_SEL = 0: Enable EEPROM Interface. CPU_EEPROM_SEL = 1: Enable SPI Interface. See "Programming Interfaces" on page 58 for more information.
ENFDXFLOW	$I_{PU,}$ SOR	**Enable Automatic Full-Duplex Flow Control.** In combination with the results of auto-negotiation, sets the flow control mode. See "Flow Control" on page 50 for more information.
ENHDXFLOW	$I_{PU,}$ SOR	**Enable Automatic Backpressure.** When this pin is pulled high, it enables half-duplex backpressure flow control when a port is configured to half-duplex. See "Flow Control" on page 50 for more information.
EEPROM_EXT[1:0]	$I_{PD,}$ SOR	Extended EEPROM Interface Selection. EEPROM_EXT[1:0] = 00: Supports 93C46 EEPROM EEPROM_EXT[1:0] = 01: Supports 93C56 EEPROM EEPROM_EXT[1:0] = 10: Supports 93C66 EEPROM EEPROM_EXT[1:0] = 11: Supports 93C86 EEPROM See "EEPROM Interface" on page 64 for more information.
$\overline{\text{HW\_FWDG\_EN}}$	$I_{PU,}$ SOR	**Forwarding Enable.** Active high. If this pin is pulled low at power-up, frame forwarding is disabled. In an unmanaged design, this pin should be pulled high.
$\overline{\text{IMP\_MODE[1:0]}}$	$I_{PD,}$ SOR	**IMP Port Mode.** Sets the mode of the IMP port based on the value of the pins at power-on reset. If not used, tie to VSS. 00: RvMII mode 01: MII mode 10: GMII mode 11: RGMII mode

Table 23: Signal Descriptions (Cont.)

Signal Name	Type	Description
QoS_EN	I_{PD}, SOR	QoS Enable. QoS_EN = 0: Disable QoS function. QoS_EN = 1: Enable QoS function. See "Quality of Service" on page 24 for more information.
QoS_FC_OFF	I_{PU}, SOR	QoS Flow Control Disable. 0 = Enable flow control when QoS is enabled. 1 = Disable flow control when QoS is enabled.
RXC_DELAY	I_{PD}, SOR	**RXCLK Clock Timing Delay.** Active high. This pin enables the RXCLK-to-data sampling timing delay for IMP/RGMII interface *only*. Pin T03: VDD for IMP RGMII 2 ns delay enabled. VSS for IMP RGMII 2 ns delay disabled.
TXC_DELAY	I_{PD}, SOR	**TXC Clock Timing Delay.** Active high. This pin enables the TXC-to-Data timing delay for IMP/RGMII interface *only*. Pin T03: VDD for IMP RGMII 2 ns delay enabled. VSS for IMP RGMII 2 ns delay disabled.
Imp_VOLT_SEL	I_{PD}, SOR	**IMP Port Voltage Select.** Determines the voltage input/output levels of the IMP interface when configured to GMII/RvMII/MII modes. 0 = 3.3V. 1 = 2.5V. When configured to RGMII mode, the IMP port voltage levels are fixed at 2.5V.
BIST_CLRMEM_SEL	I_{PU}, SOR	**Memory Clear Bit. Active Low.** This signal is designed to work in conjunction with the SKIP_MEMBIST signal. • If BIST_CLRMEM_SEL is low, SKIP_MEMBIST becomes a "don't care" bit and the device will run BIST after power up. The control memory will be cleared after BIST is run. • If BIST_CLRMEM_SEL is high and SKIP_MEMBIST is low, the device will NOT run BIST after power up, but control memory will still be cleared after power up. BIST_CLRMEM_SEL and SKIP_MEMBIST only work in these two states; other states are undefined.
SKIP_MEMBIST	I_{PD}, SOR	Skip Memory BIST option during power-up initialization. This signal is designed to work in conjunction with BIST_CLRMEM_SEL. See the "BIST_CLRMEM_SEL" description for more details.
EN_EXT_CLK	Ipd	**Enable External Clock input. Active high.** This signal is used to enable an external clock source to be fed into the device. The external clock source is to be used only for the testing purposes. It is recommended to pull down the signal to prevent from any external noise from getting in.
EXT_CLK	No pull	**External Clock input.** Active high. This is an input pin for an external clock signal. It is recommended to be pulled down.

Table 23: Signal Descriptions (Cont.)

Signal Name	*Type*	*Description*
Power		
PLLAVDD1	PWR	Phase Locked Loop Analog VDD 1.
PLLAVDD2	PWR	Phase Locked Loop Analog VDD 2. +1.2V for SerDes.
PLLDVDD3	PWR	Phase Locked Loop Digital VDD 3. +1.2V
PLLDVDD4		Phase Locked Loop Digital VDD 4. +1.2V
TXVDD	PWR	SerDes Transmit VDD +1.2V.
VDDC	PWR	Core Voltage 1.2V.
VDDO25	PWR	All other I/O pins expect IMP.
VDDO33	PWR	2.5V for RGMII and 3.3V for GMII/MII/RvMII (IMP Port).
VDDP	PWR	VDDP (2.5)
XTALVDD1	PWR	XTAL VDD 1. +2.5V.
XTALVDD2		XTAL VDD 2. +2.5V.
AVSS	PWR	Analog VSS
PLLAVSS1	PWR	Phase Locked Loop Analog VSS1
PLLAVSS2	PWR	Phase Locked Loop Analog VSS2
PLLAVSS3	PWR	Phase Locked Loop Analog VSS3
VSS	PWR	Digital VSS

Section 6: Pin Assignments

Table 24: Pin Assignment (Listed by Pin Number)

Pin	Signal Name
A01	AVSS
A02	TXVDD
A03	RXDN[1]
A04	RXDP[1]
A05	VDDP
A06	imp_TXD2
A07	imp_TXD6
A08	imp_TXCLK
A09	imp_RXD1
A10	imp_RXD4
A11	imp_RXD7
A12	imp_RXER
A13	RXDP[16]
A14	RXDN[16]
A15	TXVDD
A16	AVSS
B01	TXDN[1]
B02	TXDP[1]
B03	AVSS
B04	TXVDD
B05	VSS
B06	imp_TXD1
B07	imp_TXD5
B08	VSS
B09	VDDO33
B10	imp_RXD6
B11	VSS
B12	VDDO33
B13	TXVDD
B14	AVSS
B15	TXDN[16]
B16	TXDP[16]
C01	AVSS
C02	TXVDD
C03	RXDN[2]
C04	RXDP[2]
C05	imp_TXER
C06	imp_TXD3
C07	imp_TXD7
C08	imp_RXD0
C09	imp_RXD3
C10	imp_RXD5
C11	imp_RXDV
C12	VSS
C13	RXDN[15]
C14	RXDP[15]
C15	TXVDD
C16	AVSS
D01	TXDN[2]
D02	TXDP[2]
D03	AVSS
D04	PLLAVSS3
D05	imp_TXEN
D06	imp_TXD0
D07	imp_TXD4
D08	imp_GTXCLK
D09	imp_RXCLK
D10	imp_RXD2
D11	VSS
D12	VDDC
D13	TXVDD
D14	AVSS
D15	TXDN[15]
D16	TXDP[15]
E01	AVSS
E02	TXVDD
E03	RXDN[3]
E04	RXDP[3]
E05	PLLDVDD4
E06	VDDC
E07	VDDO33
E08	VDDC
E09	VDDO33
E10	VDDC
E11	VDDO33
E12	AVSS
E13	RXDP[14]
E14	RXDN[14]
E15	TXVDD
E16	AVSS
F01	TXDP[3]
F02	TXDN[3]
F03	AVSS
F04	TXVDD
F05	PLLDVDD3
F06	VSS
F07	VSS
F08	VSS
F09	VSS
F10	VSS
F11	VSS
F12	AVSS
F13	TXVDD
F14	AVSS
F15	TXDP[14]
F16	TXDN[14]
G01	XTALVDD1
G02	VSS
G03	RXDP[4]
G04	RXDN[4]
G05	AVSS
G06	VSS
G07	VSS
G08	VSS
G09	VSS
G10	VSS
G11	VSS
G12	AVSS
G13	RXDP[13]
G14	RXDN[13]
G15	VSS
G16	XTALVDD2
H01	TXDP[4]
H02	TXDN[4]
H03	PLLAVSS1
H04	PLLAVDD1
H05	AVSS
H06	VSS
H07	VSS
H08	VSS
H09	VSS
H10	VSS
H11	VSS
H12	AVSS
H13	PLLAVSS2
H14	PLLAVDD2
H15	TXDP[13]
H16	TXDN[13]
J01	XTALI0
J02	XTALO0
J03	RXDN[5]
J04	RXDP[5]
J05	AVSS
J06	VSS
J07	VSS
J08	VSS
J09	VSS
J10	VSS
J11	VSS
J12	AVSS
J13	RXDN[12]
J14	RXDP[12]
J15	XTALO1
J16	XTALI1
K01	TXDP[5]
K02	TXDN[5]
K03	AVSS
K04	TXVDD
K05	VSS
K06	VSS
K07	VSS
K08	VSS
K09	VSS
K10	VSS
K11	VSS
K12	VSS
K13	TXVDD
K14	AVSS
K15	TXDP[12]

Pin	Signal Name
K16	TXDN[12]
L01	AVSS
L02	TXVDD
L03	RXDP[6]
L04	RXDN[6]
L05	VDDC
L06	VSS
L07	VSS
L08	VSS
L09	VSS
L10	VSS
L11	VSS
L12	VDDC
L13	RXDN[11]
L14	RXDP[11]
L15	TXVDD
L16	AVSS
M01	TXDP[6]
M02	TXDN[6]
M03	AVSS
M04	TXVDD
M05	VDDC
M06	VDDC
M07	VDDO25
M08	VDDC
M09	VDDO25
M10	VDDO25
M11	VDDC
M12	VDDC
M13	TXVDD
M14	AVSS
M15	TXDP[11]
M16	TXDN[11]
N01	AVSS
N02	TXVDD
N03	RXDN[7]
N04	RXDP[7]
N05	ENFDXFLOW
N06	VSS
N07	CPU_EEPROM_SEL
N08	MEM_CLK_FREQ0
N09	VSS
N10	MDIO1
N11	MDC0
N12	VSS
N13	RXDP[10]
N14	RXDN[10]
N15	TXVDD
N16	AVSS
P01	TXDP[7]
P02	TXDN[7]
P03	AVSS
P04	VDDO25
P05	ENHDXFLOW
P06	EN_EXT_CLK[a]
P07	EEPROM_EXT1
P08	EEPROM_EXT0
P09	imp_MODE0
P10	MDIO0
P11	SCK
P12	VSS
P13	VSS
P14	VSS
P15	TXDP[10]
P16	TXDN[10]
R01	AVSS
R02	imp_VOLT_SEL
R03	RXDP[8]
R04	RXDN[8]
R05	HW_FWDG_EN
R06	AUTO_POLL_DIS
R07	EXT_CLK[a]
R08	MEM_CLK_FREQ1
R09	MDC1
R10	LEDDATA
R11	MISO/DO
R12	imp_MODE1
R13	RXDN[9]
R14	RXDP[9]
R15	TXVDD
R16	AVSS
T01	TXDP[8]
T02	TXDN[8]
T03	TXC_DELAY
T04	RXC_DELAY
T05	QoS_FC_OFF
T06	QoS_EN
T07	BIST_CLRMEM_SEL[a]
T08	SKIP_MEMBIST
T09	VSS
T10	LEDCLK
T11	MOSI/DI
T12	$\overline{SS}$/CS
T13	VSS
T14	RESETB
T15	TXDP[9]
T16	TXDN[9]

a. External pulldown recommended.

Table 25: Pin Assignment (Listed by Signal Name)

Signal Name	Pin
AUTO_POLL_DIS	R06
AVSS	A01
AVSS	A16
AVSS	B03
AVSS	B14
AVSS	C01
AVSS	C16
AVSS	D03
AVSS	D14
AVSS	E01
AVSS	E12
AVSS	E16
AVSS	F03
AVSS	F12
AVSS	F14
AVSS	G05
AVSS	G12
AVSS	H05
AVSS	H12
AVSS	J05
AVSS	J12
AVSS	K03
AVSS	K14
AVSS	L01
AVSS	L16
AVSS	M03
AVSS	M14
AVSS	N01
AVSS	N16
AVSS	P03
AVSS	R01
AVSS	R16
MEM_CLK_FREQ0	N08
MEM_CLK_FREQ1	R08
CPU_EEPROM_SEL	N07
EEPROM_EXT0	P08
EEPROM_EXT1	P07
ENFDXFLOW	N05
ENHDXFLOW	P05
HW_FWDG_EN	R05
imp_GTXCLK	D08
imp_MODE0	P09
imp_MODE1	R12
imp_RXCLK	D09
imp_RXD0	C08
imp_RXD1	A09
imp_RXD2	D10
imp_RXD3	C09
imp_RXD4	A10
imp_RXD5	C10
imp_RXD6	B10
imp_RXD7	A11
imp_RXDV	C11
imp_RXER	A12
imp_TXCLK	A08
imp_TXD0	D06
imp_TXD1	B06
imp_TXD2	A06
imp_TXD3	C06
imp_TXD4	D07
imp_TXD5	B07
imp_TXD6	A07
imp_TXD7	C07
imp_TXEN	D05
imp_TXER	C05
imp_VOLT_SEL	R02
LEDCLK	T10
LEDDATA	R10
MDC0	N11
MDC1	R09
MDIO0	P10
MDIO1	N10
MISO/DO	R11
MOSI/DI	T11
PLLAVDD1	H04
PLLAVDD2	H14
PLLAVSS1	H03
PLLAVSS2	H13
PLLAVSS3	D04
PLLDVDD3	F05
PLLDVDD4	E05
QoS_EN	T06
QoS_FC_OFF	T05
RESETB	T14
RXC_DELAY	T04
RXDN[1]	A03
RXDN[10]	N14
RXDN[11]	L13
RXDN[12]	J13
RXDN[13]	G14
RXDN[14]	E14
RXDN[15]	C13
RXDN[16]	A14
RXDN[2]	C03
RXDN[3]	E03
RXDN[4]	G04
RXDN[5]	J03
RXDN[6]	L04
RXDN[7]	N03
RXDN[8]	R04
RXDN[9]	R13
RXDP[1]	A04
RXDP[10]	N13
RXDP[11]	L14
RXDP[12]	J14
RXDP[13]	G13
RXDP[14]	E13
RXDP[15]	C14
RXDP[16]	A13
RXDP[2]	C04
RXDP[3]	E04
RXDP[4]	G03
RXDP[5]	J04
RXDP[6]	L03
RXDP[7]	N04
RXDP[8]	R03
RXDP[9]	R14
SCK	P11
$\overline{SS}$/CS	T12
TXC_DELAY	T03
TXDN[1]	B01
TXDN[10]	P16
TXDN[11]	M16
TXDN[12]	K16
TXDN[13]	H16
TXDN[14]	F16
TXDN[15]	D15
TXDN[16]	B15
TXDN[2]	D01
TXDN[3]	F02
TXDN[4]	H02
TXDN[5]	K02
TXDN[6]	M02
TXDN[7]	P02
TXDN[8]	T02
TXDN[9]	T16
TXDP[1]	B02
TXDP[10]	P15
TXDP[11]	M15
TXDP[12]	K15
TXDP[13]	H15
TXDP[14]	F15
TXDP[15]	D16
TXDP[16]	B16
TXDP[2]	D02
TXDP[3]	F01
TXDP[4]	H01
TXDP[5]	K01
TXDP[6]	M01
TXDP[7]	P01
TXDP[8]	T01
TXDP[9]	T15
TXVDD	A02
TXVDD	A15
TXVDD	B04
TXVDD	B13
TXVDD	C02
TXVDD	C15
TXVDD	D13
TXVDD	E02
TXVDD	E15
TXVDD	F04
TXVDD	F13
TXVDD	K04
TXVDD	K13
TXVDD	L02
TXVDD	L15
TXVDD	M04
TXVDD	M13
TXVDD	N02
TXVDD	N15
TXVDD	R15
VDDC	D12
VDDC	E06
VDDC	E08
VDDC	E10
VDDC	L05
VDDC	L12
VDDC	M05
VDDC	M06
VDDC	M08
VDDC	M11
VDDC	M12

Signal Name	Pin
VDDO25	P04
VDDO25	M07
VDDO25	M09
VDDO25	M10
BIST_CLRMEM_SEL[a]	T07
VDDO33	B09
VDDO33	B12
VDDO33	E07
VDDO33	E09
VDDO33	E11
VDDP	A05
VSS	B05
VSS	B08
VSS	B11
VSS	C12
VSS	D11
VSS	F06
VSS	F07
VSS	F08
VSS	F09
VSS	F10
VSS	F11
VSS	G02
VSS	G06
VSS	G07
VSS	G08
VSS	G09
VSS	G10
VSS	G11
VSS	G15
VSS	H06
VSS	H07
VSS	H08
VSS	H09
VSS	H10
VSS	H11
VSS	J06
VSS	J07
VSS	J08
VSS	J09
VSS	J10
VSS	J11
VSS	K05
VSS	K06
VSS	K07
VSS	K08

Signal Name	Pin
VSS	K09
VSS	K10
VSS	K11
VSS	K12
VSS	L06
VSS	L07
VSS	L08
VSS	L09
VSS	L10
VSS	L11
VSS	N06
VSS	N09
VSS	N12
EN_EXT_CLK[a]	P06
VSS	P12
VSS	P13
VSS	P14
EXT_CLK[a]	R07
SKIP_MEMBIST	T08
VSS	T09
VSS	T13
XTALI0	J01
XTALI1	J16
XTALO0	J02
XTALO1	J15
XTALVDD1	G01
XTALVDD2	G16

a. External pulldown recommended.

Figure 21: Pins Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVSS	TXVDD	RXDN[1]	RXDP[1]	VDDP	imp_TXD2	imp_TXD6	imp_TXCLK	imp_RXD1	imp_RXD4	imp_RXD7	imp_RXER	RXDP[16]	RXDN]
B	TXDN[1]	TXDP[1]	AVSS	TXVDD	VSS	imp_TXD1	imp_TXD5	VSS	VDDO33	imp_RXD6	VSS	VDDO33	TXVDD	AVS
C	AVSS	TXVDD	RXDN[2]	RXDP[2]	imp_TXER	imp_TXD3	imp_TXD7	imp_RXD0	imp_RXD3	imp_RXD5	imp_RXDV	VSS	RXDN[15]	RXDP
D	TXDN[2]	TXDP[2]	AVSS	PLLAVSS3	imp_TXEN	imp_TXD0	imp_TXD4	imp_GTXCLK	imp_RXCLK	imp_RXD2	VSS	VDDC	TXVDD	AVS
E	AVSS	TXVDD	RXDN[3]	RXDP[3]	PLLDVDD4	VDDC	VDDO33	VDDC	VDDO33	VDDC	VDDO33	AVSS	RXDP[14]	RXDN]
F	TXDP[3]	TXDN[3]	AVSS	TXVDD	PLLDVDD3	VSS	VSS	VSS	VSS	VSS	VSS	AVSS	TXVDD	AVS
G	XTALVDD1	VSS	RXDP[4]	RXDN[4]	AVSS	VSS	VSS	VSS	VSS	VSS	VSS	AVSS	RXDP[13]	RXDN]
H	TXDP[4]	TXDN[4]	PLLAVSS1	PLLAVDD1	AVSS	VSS	VSS	VSS	VSS	VSS	VSS	AVSS	PLLAVSS2	PLLA2
J	XTALI1	XTALO1	RXDN[5]	RXDP[5]	AVSS	VSS	VSS	VSS	VSS	VSS	VSS	AVSS	RXDN[12]	RXDP
K	TXDP[5]	TXDN[5]	AVSS	TXVDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TXVDD	AVS
L	AVSS	TXVDD	RXDP[6]	RXDN[6]	VDDC	VSS	VSS	VSS	VSS	VSS	VSS	VDDC	RXDN[11]	RXDP
M	TXDP[6]	TXDN[6]	AVSS	TXVDD	VDDC	VDDC	VDDO25	VDDC	VDDO25	VDDO25	VDDC	VDDC	TXVDD	AVS
N	AVSS	TXVDD	RXDN[7]	RXDP[7]	ENFDXFLOW	VSS	CPU_EEPROM_S	MEM_CLK_	VSS	MDIO1	MDC0	VSS	RXDP[10]	RXDN]
P	TXDP[7]	TXDN[7]	AVSS	VDDO25	ENHDXFLOW	EN_EXT_CLK	EEPROM_	EEPROM_EXT0	imp_MODE0	MDIO0	SCK	VSS	VSS	VS
R	AVSS	imp_VOLT_	RXDP[8]	RXDN[8]	HW_FWDG_EN	AUTO_POLL_DIS	EXT_CLK	MEM_CLK_	MDC1	LEDDATA	MISO/DO	imp_MODE1	RXDN[9]	RXDI
T	TXDP[8]	TXDN[8]	TXC_DELAY	RXC_DELAY	QoS_FC_OFF	QoS_EN	BIST_CLRMEM_S	SKIP_MEMBIS	VSS	LEDCLK	MOSI/DI	$\overline{SS}$/CS	VSS	RESE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

Section 7: Register Definitions

Register Definition

The BCM5396 registers set can be accessed through the In-band Management Port (IMP) and Serial Peripheral Interface (SPI). The register space is organized into pages, each containing a certain set of registers. The following table lists the pages defined in the BCM5396. Note that in addition to access via the SPI, the per port MII registers are still accessible via the MDC[0]/MDIO[0] path of the external MII, compatible with the BCM5318 device mode.

To access a page, the page register (0xFFh) is written with the page value. The registers contained in the page can then be accessed by their address.

Table 26: Global Page Register Map

Page	*Description*
00h	Control registers
01h	Status registers
02h	Management Mode registers
03h	Reserved
04h	ARL Control registers
05h	ARL Access registers
06h	Reserved
07h	Reserved
08h	Reserved
09h	Reserved
0Ah	Flow Control
0Bh–0Fh	Reserved
10h	Port 0 Integrated SerDes registers (10/100/1000 Port 0)
11h	Port 1 Integrated SerDes registers (10/100/1000 Port 1)
12h	Port 2 Integrated SerDes registers (10/100/1000 Port 2)
13h	Port 3 Integrated SerDes registers (10/100/1000 Port 3)
14h	Port 4 Integrated SerDes registers (10/100/1000 Port 4)
15h	Port 5 Integrated SerDes registers (10/100/1000 Port 5)
16h	Port 6 Integrated SerDes registers (10/100/1000 Port 6)
17h	Port 7 Integrated SerDes registers (10/100/1000 Port 7)
18h	Port 8 Integrated SerDes registers (10/100/1000 Port 8)
19h	Port 9 Integrated SerDes registers (10/100/1000 Port 9)
1Ah	Port 10 Integrated SerDes registers (10/100/1000 Port 10)
1Bh	Port 11 Integrated SerDes registers (10/100/1000 Port 11)
1Ch	Port 12 Integrated SerDes registers (10/100/1000 Port 12)

Table 26: Global Page Register Map (Cont.)

Page	*Description*
1Dh	Port 13 Integrated SerDes registers (10/100/1000 Port 13)
1Eh	Port 14 Integrated SerDes registers (10/100/1000 Port 14)
1Fh	Port 15 Integrated SerDes registers (10/100/1000 Port 15)
20h–2Fh	Reserved
30h	QoS registers
31h	VLAN registers
32h	Trunking registers
34h	IEEE Standard 802.1Q VLAN registers
35h–3Fh	Reserved
40h	Jumbo registers
41h	Broadcast Storm Suppression registers
42h	Reserved
43h	IEEE Standard 802.1s Multiple Spanning Tree registers
44h–4Fh	Reserved
50h	Reserved
51h	Reserved
52h	Reserved
53h	Reserved
54h	Reserved
55h	Reserved
56h	Reserved
57h	Reserved
58h	Reserved
59h	Reserved
5Ah	Reserved
5Bh	Reserved
5Ch	Reserved
5Dh	Reserved
5Eh	Reserved
5Fh	Reserved
60h	Reserved
61h–7Fh	Reserved
80h	Port 0 External PHY registers (10/100/1000 Port 0)
81h	Port 1 External PHY registers (10/100/1000 Port 1)
82h	Port 2 External PHY registers (10/100/1000 Port 2)
83h	Port 3 External PHY registers (10/100/1000 Port 3)
84h	Port 4 External PHY registers (10/100/1000 Port 4)
85h	Port 5 External PHY registers (10/100/1000 Port 5)
86h	Port 6 External PHY registers (10/100/1000 Port 6)

Table 26: Global Page Register Map (Cont.)

Page	*Description*
87h	Port 7 External PHY registers (10/100/1000 Port 7)
88h	Port 8 External PHY registers (10/100/1000 Port 8)
89h	Port 9 External PHY registers (10/100/1000 Port 9)
8Ah	Port 10 External PHY registers (10/100/1000 Port 10)
8Bh	Port 11 External PHY registers (10/100/1000 Port 11)
8Ch	Port 12 External PHY registers (10/100/1000 Port 12)
8Dh	Port 13 External PHY registers (10/100/1000 Port 13)
8Eh	Port 14 External PHY registers (10/100/1000 Port 14)
8Fh	Port 15 External PHY registers (10/100/1000 Port 15)
90h–EFh	Reserved
F0h	SPI Data I/O 0
F1h	SPI Data I/O 1
F2h	SPI Data I/O 2
F3h	SPI Data I/O 3
F4h	SPI Data I/O 4
F5h	SPI Data I/O 5
F6h	SPI Data I/O 6
F7h	SPI Data I/O 7
F8h–FDh	Reserved
FEh	SPI Status register
FFh	Page register

Control Registers

Table 27: Control Registers (Page 00h)

Address	*Bits*	*Register Name*
00h	8	10/100/1000 Port Control register 0
01h	8	10/100/1000 Port Control register 1
02h	8	10/100/1000 Port Control register 2
03h	8	10/100/1000 Port Control register 3
04h	8	10/100/1000 Port Control register 4
05h	8	10/100/1000 Port Control register 5
06h	8	10/100/1000 Port Control register 6
07h	8	10/100/1000 Port Control register 7
08h	8	10/100/1000 Port Control register 8
09h	8	10/100/1000 Port Control register 9
0Ah	8	10/100/1000 Port Control register 10
0Bh	8	10/100/1000 Port Control register 11
0Ch	8	10/100/1000 Port Control register 12
0Dh	8	10/100/1000 Port Control register 13
0Eh	8	10/100/1000 Port Control register 14
0Fh	8	10/100/1000 Port Control register 15
10h	8	IMP Port (Port 16) Control register
11h–1Fh		Reserved
20h	8	Switch Mode register
21h–23h		Reserved
24h–25h	16	LED Control register
28h–2Bh	32	Reserved
2Ch–2Fh	32	Reserved
30h–33h	32	Reserved
34h–37h	32	Reserved
3Bh	8	New Control register
3Ch–4Fh		Reserved
50	8	Reserved—Multicast Control register
51h	8	Load Meter Update Rate Control register
52h	8	TXq Flush Mode register
54h–57h	32	Reserved
58h–5Bh	32	Multicast Lookup Failed Forward Map register
5Ch–5Fh		Reserved
60h	8	Port 0 Port State Override register
61h	8	Port 1 Port State Override register
62h	8	Port 2 Port State Override register

Table 27: Control Registers (Page 00h) (Cont.)

Address	Bits	Register Name
63h	8	Port 3 Port State Override register
64h	8	Port 4 Port State Override register
65h	8	Port 5 Port State Override register
66h	8	Port 6 Port State Override register
67h	8	Port 7 Port State Override register
68h	8	Port 8 Port State Override register
69h	8	Port 9 Port State Override register
6Ah	8	Port 10 Port State Override register
6Bh	8	Port 11 Port State Override register
6Ch	8	Port 12 Port State Override register
6Dh	8	Port 13 Port State Override register
6Eh	8	Port 14 Port State Override register
6Fh	8	Port 15 Port State Override register
70h	8	Port 16 (IMP) Port State Override register
71h–76h		Reserved
77h	8	IEEE Standard 802.1x Control register 1
78h–7Bh	32	IEEE Standard 802.1x Control register 2
7Ch–7Fh		Reserved
80h–83h	32	SD Default register
84h–85h	16	SD_SEL_EARLY register
86h	8	External PHY Scan Control register
87h		Reserved
88h	8	Fast Aging Control register
89h	8	Fast Aging Port register
8Ah–8Bh	16	Fast Aging VID register
8Ch–8Dh	16	Reserved
8Eh–8Fh		Reserved
90h	8	Pause Frame Detection Control register
91h–9Fh		Reserved
A0h	8	RGMII Control register
A1h	8	Reserved
A2h	8	Reserved
A3h–DFh		Reserved
E1h–FEh		Reserved
FFh	8	Page register

10/100/1000 Port N Control Register [0:15](Page 00h: Address 00h–0Fh)

Table 28: 10/100/1000 Port Control Register (Page 00h: Address 00h–0Fh)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	CPU writes the current computed states of its spanning tree algorithm for this port. 000 = No spanning tree (unmanaged mode) 001 = Disabled state (default for managed mode) 010 = Blocking state 011 = Listening state 100 = Learning state 101 = Forwarding state 110–111= Reserved	Controlled by HW_FWDG_EN strap option
4:2	Reserved	RO	Reserved	0
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level. (The internal TXQ Flush Mode Control Register (page 00h, address 52h), must also be set to 0x02 to disable the transmit function.)	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level.	0

IMP Port (Port 16) Control Register (Page 00h: Address 10h)

Table 29: IMP Port Control Register (Page 00h: Address 10h)

Bit	Name	R/W	Description	Default
7:5	STP_STATE[2:0]	R/W	Spanning tree protocol state. CPU writes the current computed states of its spanning tree algorithm for this port. 000 = No spanning tree (unmanaged mode) 001 = Disabled state 010 = Blocking state 011 = Listening state 100 = Learning state 101 = Forwarding state 110–111 = Reserved Ignored when SW_FWDG_MODE = unmanaged.	Controlled by HW_ FWDG_ EN strap option
4	RX_UCST_EN	R/W	Receive unicast enable. Enables the receipt of unicast frames on the IMP, when the IMP is configured as the frame management port, and the frame is flooded due to no matching address table entry. When cleared, unicast frames that meet the mirror ingress/ egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as a frame management port.	0

Table 29: IMP Port Control Register (Page 00h: Address 10h) (Cont.)

Bit	Name	R/W	Description	Default
3	RX_MCST_EN	R/W	Receive multicast enable. Enables the receipt of multicast frames on the IMP, when the IMP is configured as the frame management port and the frame is flooded due to no matching address table entry. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as a frame management port.	0
2	RX_BCST_EN	R/W	Receive broadcast enable. Enables the receipt of broadcast frames on the IMP, when the IMP is configured as the frame management port. When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as a frame management port.	0
1	TX_DISABLE	R/W	Disables the transmit function of the port at the MAC level. (The internal TXQ Flush Mode Control Register (page 0h, address 52h) must also be set to 0x02 to disable the transmit function.)	0
0	RX_DISABLE	R/W	Disables the receive function of the port at the MAC level.	0

Switch Mode Register (Page 00h: Address 20h)

Table 30: Switch Mode Register (Page 00h: Address 20h)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved	0
4	NOBLKCD	R/W	Do not block carrier-detected signal. 0: Block CD. 1: Not to block; txport always defers to CRS.	0
3	Fast TX Descriptor Return	R/W	Controls which algorithm is used to release packets when a link goes down.	0
2	RTRY_LMT_DIS	R/W	Retry Limit Disable. When set, disables the Retry limit on all MAC ports (10/100BASE-T and MII ports). Causes a MAC port in half-duplex operation, to continue to retry the same packet regardless of the number of collision attempts.	$\overline{1}$

Table 30: Switch Mode Register (Page 00h: Address 20h)

Bit	Name	R/W	Description	Default
1	SW_FWDG_EN	R/W	Software Forwarding Enable. SW_FWDG_EN = 1: Frame forwarding is enabled. SW_FWDG_EN = 0: Frame forwarding is disabled. Read from HW_FWDG_EN pin on power-on. Can be overwritten subsequently. For managed switch implementations (BCM5396 mode), the switch should be configured to disable forwarding on power-on to allow the processor to configure the internal address table and other parameters, before frame forwarding is enabled.	HW_FWDG_EN strap pin
0	SW_FWDG_MODE	R/W	Software Forwarding Mode. Strapped from the inverse of the HW_FWDG_EN pin at power-on. Can be overwritten subsequently. 0 = Unmanaged mode. 1 = Managed mode. The ARL treats Reserved Multicast addresses differently dependent on this selection. Refer to Table 5 on page 41 for a precise definition.	Inverse of HW_FWDG_EN strap pin

LED Control Register (Page 00h: Address 24h–25h)

Table 31: LED A Register (Page 00h: Address 24h–25h)

Bit	Name	R/W	Description	Default
15:11	Reserved	R/W	Reserved	0
10:8	LED Mode	R/W	Mode control for LED output sequence	‘b111
7:0	Flash rate	R/W	LED flash rate	‘h20

New Control Register (Page 00h: Address 3Bh)

Table 32: New Control Register (Page 00h: Address 3Bh)

Bit	Name	R/W	Description	Default
7	MCST_DLF_FWD	R/W	0 = Flood multicast packet if ARL table lookup fails. 1 = Forward multicast packets according to Table 5: “Multicast Forward Field Definitions,” on page 41 if ARL table lookup fails.	0
6	UNICAST_DROP_EN	R/W	0 = Flood unicast packet if ARL table lookup fails. 1 = Forward unicast packets according to Table 3: “Unicast Forward Field Definitions,” on page 39 if ARL table lookup fails.	0
5:1	Reserved	R/W	Spare registers	0
0	IP_MULTICAST	R/W	0 = Disable 4K IP multicast address scheme. 1 = Enable 4K IP multicast address scheme.	1

Reserved Multicast Control Register (Page 00h: Address 50h)

Table 33: Reserved Multicast Register (Page 00h: Address 50h)

Bit	Name	R/W	Description	Default
7	EN_RES_MUL_LEARN	R/W	Bit[7]: en_reserved_McastDA_learn. 0: Do not learn (default) 1: Learn	0
6:5	Reserved	R/W	Reserved	0
4	EN_MUL_4	R/W	Bit[3]: 01:80:C2:00:00:20 – 01:80:C2:00:00:2F. 0: Forward (default) 1: Drop	0
3	EN_MUL_3	R/W	Bit[2]: 01:80:C2:00:00:11 – 01:80:C2:00:00:1F. 0: Forward (default) 1: Drop	0
2	EN_MUL_2	R/W	Bit[2]: 01-80-C2-00-00-10. 0: Forward (default) 1: Drop	0
1	EN_MUL_1	R/W	Bit[1]: 01:80:C2:00:00:02 – 01:80:C2:00:00:0F. 0: Forward 1: Drop (default)	1
0	EN_MUL_0	R/W	Bit[0]:01-80-C2-00-00-00 0: Forward (default) 1: Drop	0

Load Meter Update Rate Control Register (Page 00h: Address 51h)

Table 34: Load Meter Update Rate Control Register (Page 00h: Address 51h)

Bit	Name	R/W	Description	Default
7:4	Reserved	RO	Reserved	0
3:0	Stat_Stop_Cnt	R/W	Statistic Update Rate Counter 0: 40 ms 1: 80 ms 2: 120 ms 3: 160 ms Up to 320 ms	3h

Unicast Lookup Failed Forward Map Register (Page 00h: Addr 54h–57h)

Table 35: Unicast Lookup Failed Forward Map Register (Page 00h: 54h–57h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	UNI_LOOKUP_FAIL_FWD_MAP	R/W	Unicast Lookup Failed Forward Map. When unicast lookup fails, drop is enabled (Page 00, Offset 3Bh) and lookup failure happens. ARL forwards the frame according to this register setting.	0

Multicast Lookup Failed Forward Map Register (Page 00h: Address 58h–5Bh)

Table 36: Multicast Lookup Failed Forward Map Register (Page 00h: Address 58h–5Bh)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	MUL_LOOKUP_FAIL_FORWARD_ MAP	R/W	Multicast Lookup Failed Forward Map. When multipath lookup fails, drop is enabled (page 00, Offset 3Bh) and lookup failure happens. ARL forwards the frame according to this register setting.	0

Port *N* State Override Register[0:15] (Page 00h: Address 60h–6Fh)

Table 37: Port N State Override Register (Page 00h: Address 60–6Fh)

Bit	Name	R/W	Description	Default
7	Software Override	R/W	CPU set software override bit to 1 to make bits [5:0] affected. PHY scan register is overridden.	0
6	Reserved	R/W	Reserved	0
5	TX Flow Control Enable	R/W	Software TX flow control enable	0
4	RX Flow Control Enable	R/W	Software RX flow control enable	0
3:2	Speed	R/W	Software port speed setting: 2’b00: 10M 2’b01: 100M 2’b10: 1000M	2’b10
1	Duplex Mode	R/W	Software duplex mode setting: 0: Half-duplex 1: Full-duplex	1
0	Link State	R/W	0: Link down 1: Link up	1

Port 16 (IMP) State Override Register (Page 00h: Address 70h)

Table 38: Port 16 (IMP) State Override Register (Page 00h: Address 70h)

Bit	Name	R/W	Description	Default
7	Software Override	R/W	CPU set software override bit to 1 to make bits [5:0] affected. PHY scan register is overridden.	0
6	EN_IMP_RX_PAUSE_NOTAG	R/W	This is used when MII port is configured as management. 0 = RXMAC detect PAUSE frame with BRCM tag. 1 = RXMAC detect standard PAUSE frame (No BRCM tag).	0
5	TX Flow Control Enable	R/W	Software TX flow control enable	0
4	RX Flow Control Enable	R/W	Software RX flow control enable	0
3:2	Speed	R/W	Software port speed setting: 2'b00: 10M 2'b01: 100M 2'b10: 1000M	2'b10
1	Duplex Mode	R/W	Software duplex mode setting: 0: Half-duplex 1: Full-duplex	1
0	Link State	R/W	0: Link Down 1: Link Up	1

Note: When the BCM5396 IMP port connects to CPU GMAC/MAC, since there is no auto-negotiation between GMAC/MAC,users need to set Port 16 (IMP) State Override Register to force the IMP port link up, set the speed, duplex mode and flow control you want. For example, set the register to value 0x8B to force the IMP port link up at 1000M duplex.

802.1X Control Register 1 (Page 00h: Address 77h)

Table 39: 802.1X Control Register 1 (Page 00h: Address 77h)

Bit	Name	R/W	Description	Default
7:1	Reserved	RO	Reserved	0
0	MODE_802_1X	R/W	0: Drop frames if MAC_SA misses, and frames are not IEEE Standard 802.1x special frames. 1: Drop frames if frames are not IEEE Standard 802.1x special frames.	0

802.1X Control Register 2 (Page 00h: Address 78h–7Bh)

Table 40: 802.1X Control Register 2 (Page 00h: Address 78h–7Bh)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	PORT_BLOCK	R/W	Individual bit to enable each port's security function	0

SD_DEFAULT Register (Page 00h: Address 80h–83h)

Table 41: SerDes Default Values Register (Page 00h: Address 80h–83h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	15'b0
16:0	SerDes default	R/W	SerDes IP used this default to set up its internal registers. bits[16:15]: pause_def[1:0] = 2'b00 bit[14]: adv_hdx_def = 1 bit[13]: adv_fdx_def = 1 bit[12]: tbi_def = 0 bit[11]: fiber_def = 0 bit[10]: clk125_disable_def = 1 bits[9:8]: fifo_elasticity_def[1:0] = 2'b00 bit[7]: freqlock_tx_def = 0 bit[6]: autodet_def = 1 bit[5]: parallel_detect_def = 1 bit[4]: ext_phy_crs_def = 0 bit[3]: invert_ext_phy_crs_def = 0 bit[2]: sd_enable_def = 0 bit[1]: invert_sd_def = 0 bit[0]: disable_tx_crs_def = 0	17'h6460

SD_SEL_EARLY Register (Page 00h: Address 84h–85h)

Table 42: SerDes Select Early Version of CRS and COL Register (Page 00h: Address 84h–85h)

Bit	Name	R/W	Description	Default
15:0	Reserved	R/W	0: Select regular version of CRS and COL 1: Select early version of CRS and COL. SerDes must use external PHY CRS to generate early version of CRS and COL.	16'b0

EXTERNAL_PHY_SCAN_CONTROL Register

Table 43: External PHY Scan Control Register (Page 00h: Address 86h)

Bit	Name	R/W	Description	Default
7	EXTERNAL_PHY _SCAN_ENABLE	R/W	Writing 1 to this bit allows the port to scan the attached external PHY. Writing 0 to this bit disables this operation. Default is set to the inversion of the AUTO_POLL pin strap value. 0: Disable internal FSM to scan external PHY status 1: Enable	~AUTO_POLL _DIS
6	Reserved	RO	Reserved	1'b0
5	External PHY Address Increment	R/W	0: Decrement PHY_ID of PHY0 = PHY[0] PHY[n] = (PHY[0] – n)%32 1: Increment PHY_ID of PHY0 = PHY[0] PHY[n] = (PHY[0] + n)%32 ***Example:*** Increment case PHY[0] = 5, PHY[12] = (PHY[0]+12)%32) = 5'd17 ***Example:*** Decrement case PHY[0] = 5, PHY[12] = (PHY[0] – 12)%32 (5-12)%32 = 5'h19	1'b1
4:0	External PHY base address	R/W	PHY_ID of external PHY 0, PHY[0]	5'b0

Note: The external PHY addressing scheme MUST be in sequence relative to the switch port. For example, if using a quad PHY to connect to all 16 switch ports, PHY 1 must be addressed from 1 ~ 4, PHY 2 = 5 ~ 8, PHY 3 = 9 ~ 12, and
PHY 4 = 13 ~ 16 (assuming an ascending order).

Fast Aging Control Register (Page 00h: Address 88h)

Table 44: Fast Aging Control Register (Page 00h: Address 88h)

Bit	Name	R/W	Description	Default
7	FAST_AGE_START/DONE	R/W (SC)	Write 1 to start the fast aging process, aging out entries that match both FAST AGING PORT and FAST AGING VID registers, as well as the EN_FAST_AGE_STATIC bit. After the fast aging is done, this bit is cleared to 0.	0
6:1	Reserved	RO	Reserved	0
0	EN_FAST_AGE_STATIC	R/W	0: Fast aging ages out only dynamic entries. 1: Fast aging ages out both static and dynamic entries.	0

Fast Aging Port Register (Page 00h: Address 89h)

Table 45: Fast Aging Port Register (Page 00h: Address 89h)

Bit	Name	R/W	Description	Default
7	AGE_OUT_ALL_PORTS	R/W	0: The Port field indicates the port to be aged out. 1: All ports shall be aged out (must match VID also).	0
6:4	Reserved	RO	Reserved	0
3:0	PORT_ID	R/W	The port to be aged out of ARL (must match VID also).	0

Fast Aging VID Register (Page 00h: Address 8Ah–8Bh)

Table 46: Fast Aging VID Register (Page 00h: Address 138d–139d, 8Ah–8Bh)

Bit	Name	R/W	Description	Default
15	AGE_OUT_ALL_VIDS	R/W	0: The VID field indicates the VLAN ID to be aged out. 1: All VIDs shall be aged out (must match PORT_ID also).	0
14:12	Reserved	RO	Reserved	0
11:0	VID	R/W	The VID to be aged out of ARL (must match PORT_ID also).	0

Pause Frame Detection Control Register (Page 00h: Address 90h)

Table 47: Pause Frame Detection Control Register (Page 00h: Address 90h)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Reserved	0
1	PAUSE_IGNORE_ ETHERTYPE	R/W	PAUSE_IGNORE_ETHERTYPE. 0: Check EtherType field on pause frame detection. 1: Ignore EtherType field on pause frame detection.	0
0	PAUSE_IGNORE_DA	R/W	PAUSE_IGNORE_DA. 0: Check DA field on pause frame detection. 1: Ignore DA field on pause frame detection.	0

Status Registers

Table 48: Status Registers (Page 01h)

Address	Bits	Register Name
00h–03h	32	Link Status Summary register
04h–07h	32	Link Status Change register
08h–0Fh	64	Port Speed Summary register
10h–13h	32	Duplex Status Summary register
14h–17h	32	TX PAUSE Status Summary register
18h–1Bh	32	RX PAUSE Status Summary register
1Ch–1Fh	–	Reserved
20h	8	Port 0 PHY Status register
21h	8	Port 1 PHY Status register
22h	8	Port 2 PHY Status register
23h	8	Port 3 PHY Status register
24h	8	Port 4 PHY Status register
25h	8	Port 5 PHY Status register
26h	8	Port 6 PHY Status register
27h	8	Port 7 PHY Status register
28h	8	Port 8 PHY Status register
29h	8	Port 9 PHY Status register
2Ah	8	Port 10 PHY Status register
2Bh	8	Port 11 PHY Status register
2Ch	8	Port 12 PHY Status register
2Dh	8	Port 13 PHY Status register
2Eh	8	Port 14 PHY Status register
2Fh	8	Port 15 PHY Status register
30h–3F	–	Reserved
40h	16	SerDes Signal Detection Status register
41h–45h	–	Reserved
46h	8	Reserved
47h–6Fh	–	Reserved
70h–73h	32	Strap Value register
74h–FEh	–	Reserved
FFh	8	Page register

Link Status Summary (Page 01h: Address 00h–03h)

Table 49: Link Status Summary Register (Page 01h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	LINK_STATUS[16:0]	RO	Link status. 17-bit field indicating the link status for each 10/100/1000BASE-T port, (Bits 0–15 = 10/100/1000BASE-T ports, bit 16 = GMII port.) 0 = Link fail. 1 = Link pass.	0

Link Status Change (Page 01h: Address 04h–07h)

Table 50: Link Status Change Register (Page 01h: Address 04h–07h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	LINK_STATUS[16:0]	RO	Link status change. 17-bit field indicating that the link status for an individual 10/100/1000BASE-T port, had changed since the last read operation (Bits 0–15 = 10/100/1000BASE-T ports, bit 16 = IMP/GMII) Upon change of link status, a bit remains set until cleared by a read operation. 0 = Link status constant. 1 = Link status change.	0

Port Speed Summary (Page 01h: Address 08h–0Fh)

Table 51: Port Speed Summary Register (Page 01h: Address 08h–0Fh)

Bit	Name	R/W	Description	Default
63:34	Reserved	RO	Reserved	0
33:0	PORT_SPEED[33:0]	RO	Port speed. 34-bit field indicating the operating speed for each 10/100/1000BASE-T port, the GMII port (Bits 0 – 15 = 10/100/1000BASE-T ports, bit 16 = GMII Port). Bits 15:0 = Port 15 – Port 0 (Bits [1:0] for Port 0, and Bits [31:30] for Port 15) 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps	0

Duplex Status Summary (Page 01h: Address 10h–13h)

Table 52: Duplex Status Summary Register (Page 01h: Address 10h–13h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	DUPLEX_STATE[16:0]	RO	Duplex State. 17-bit field indicating the half/full-duplex state for each 10/100/1000BASE-T port, the MII port (Bits 0 - 16 = 10/100/1000BASE-T ports, bit 17= GMII Port). 0 = Half-duplex. 1 = Full-duplex.	0

TX Pause Status Summary (Page 01h: Address 14h–17h)

Table 53: TX PAUSE Status Summary Register (Page 01h: Address 14h–17h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	TXPAUSE_STATE[16:0]	RO	TX PAUSE State. 17-bit field indicating the PAUSE state for each 10/100/1000BASE-T port, the GMII port (Bits 0 – 15 = 10/100/1000BASE-T ports, bit 16 = GMII Port). Bits 16–0 = Port 16 – Port 0 Transmit Pause Capability: 0 = Disabled. 1 = Enabled.	0

Note: TX Pause Status Summary register is only valid for full-duplex mode.

RX Pause Status Summary (Page 01h: Address 18h–1Bh)

Table 54: RX PAUSE Status Summary Register (Page 01h: Address 18h–1Bh)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	RX PAUSE_STATE[16:0]	RO	RX PAUSE State. 16-bit field indicating the PAUSE state for each 10/100/1000BASE-T port, the GMII port (Bits 0 – 15 = 10/100/1000BASE-T ports, Bit 16 = GMII Port). Bits 16–0 = Port 16 – Port 0 receive pause capability: 0 = Disabled. 1 = Enabled.	0

Note: RX Pause Status Summary register is only valid for full-duplex mode.

Port *N* PHY Status Register[0:15] (Page 01h: Address 20h–2Fh)

Table 55: Port N PHY Status Register (Page 01h: Address 20–2Fh)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0
6	PHY Scan Error	RO	PHY scan error indication.	0
5	TX Flow Control Status	RO	Software TX flow control enable.	0
4	RX Flow Control Enable	RO	Software RX flow control enable.	0
3:2	Speed	RO	Software port speed setting: 2'b00: 10M 2'b01: 100M 2'b10: 1000M	0
1	Duplex Mode	RO	Software duplex mode setting: 0: Half-duplex 1: Full-duplex	0
0	Link State	RO	0: Link down 1: Link up	0

SerDes Signal Detect Status Register (Page 01h: Address 40h)

Table 56: SerDes Signal Detect Status Register (Page 01h: Address 40h)

Bit	Name	R/W	Description	Default
15:0	SerDes Signal Detect Status	RO	SerDes signal detect status for Port0–15 in fiber mode.	0

BIST Status Register (Page 01h, Address 46h)

Table 57: BIST Status Register (Page 01h, Address 46h)

Bit	Name	R/W	Description	Default
7:2	Reserved	RO	Write 0x00, ignore when read.	0
1	MEM_ERR	RC	Internal packet buffer memory error. When this bit =1, it indicates the packet buffer memory failed the internal self-test during initialization/power up.	0
0	Reserved	RC	–	0

Strap Value Register (Page 01h: Address 70h–73h)

Table 58: Strap Value Register (Page 01h: Address 70h–73h)

Bit	Name	R/W	Description	Default
31:21	Reserved	RO	Reserved	0
20:0	STRAP_VALUE_VECTOR	RO	Display Strap Pin Value: Bit 20 = RXC_DELAY Bit 19 = TXC_DELAY Bit 18 = imp_VOLT_SEL Bit 17 = HW_FWDG_EN Bit 16 = Reserved Bit 15 = ENHDXFLOW Bit 14 = ENFDXFLOW Bit 13 = Reserved Bit 12 = QoS_EN Bit 11 = QoS_FC_OFF Bits 10:9 = MEM_CLOCK_FREQ[1:0] Bits 8:7 = EEPROM_TYPE[1:0] Bit 6 = CPU_EEPROM_SEL Bit 5 = Reserved Bit 4 = Reserved Bits 3:2 = imp_MODE[1:0] Bit 1 = AUTO_POLL_DIS Bit 0 = Reserved	

Management Mode Registers

Table 59: Management Mode Registers (Page 02h)

Address	Bits	Register Name
00h	8	Global Management Configuration
01h–03h	–	Reserved
04h–0Bh	64	Reserved
0Ch–0Fh	32	Aging Time Control
10h–11h	16	Mirror Capture Control
12h–15h	32	Ingress Mirror Control
16h–17h	16	Ingress Mirror Divider
18h–1Bh	48	Reserved
1Ch–1Fh	32	Egress Mirror Control
20h–21h	16	Reserved
22h–25h	–	Reserved
26h–2Fh	–	Reserved
30h	8	MODEL ID register
31h–3Fh	–	Reserved
40h	8	Revision ID register
41h–FEh	–	Reserved
FFh	8	Page register

Global Management Configuration Register

Table 60: Global Management Configuration Register (Page 02h: Address 00h)

Bit	Name	R/W	Description	Default
7:6	FRM_MNGT_PORT	R/W	Frame Management Port. Defines the physical port used to report management frames directed to the switch: 00 = Reserved; BCM5396 has a dedicated management port, and this port cannot be configured as a regular data port. 01 = Reserved 10 = Enable IMP Port 11 = Reserved	00
5:4	Reserved	R/W	Reserved	00
3	IGMP_IP_EN	R/W	IGMP IP layer Snooping Enable. When asserted, IGMP IP layer snooping is enabled. As incoming frame has value 2 in the IP header protocol field, it will be forwarded to CPU port.	0
2	Reserved	R/W	Reserved	0

Table 60: Global Management Configuration Register (Page 02h: Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
1	RX_BPDU_EN	R/W	Receive BPDU Enable. Enables all ports to receive BPDUs and forward to the defined physical management port. Management CPU must set this bit to globally allow BPDUs to be received.	0
0	Reserved	R/W	Reserved.	0

Aging Time Control (Page 02h: Address 0Ch–0Fh)

Table 61: Aging Time Control Register (Page 02h: Address 0Ch–0Fh)

Bit	Name	R/W	Description	Default
31:20	Reserved	RO	Reserved	0
19:0	AGE_TIME	R/W	Specifies the aging time in seconds for dynamically learned address. Maximum age time is 1,048,575 sec. Note that while IEEE Standard 802.1D specifies a range of values of 10–1,000,000 sec., this register does not enforce this range. Setting the AGE_TIME to zero disables the aging process.	300 (decimal)

Mirror Capture Control Register (Page 02h: Address 10h–11h)

Table 62: Mirror Capture Control Register (Page 02h: Address 10h–11h)

Bit	Name	R/W	Description	Default
15	MIRROR_ENABLE	R/W	Global enable/disable for all mirroring on this chip. When reset, mirroring is disabled. When set, mirroring is enabled according to the ingress and egress control rules to the port designated by the MIRROR_CAPTURE_PORT. 0 = Disable. 1 = Enable.	0
14	BLK_NOT_MIR	R/W	When Enabled, all traffic to Mirror_Capture_Port will be blocked except mirror traffic. 0 = Disable. 1 = Enable.	0
13:5	Reserved	RO	Reserved	0
4:0	MIRROR_CAPTURE_PORT_ID	R/W	Mirror Capture Port ID. Port ID identifies the single unique port designated as the port to which all ingress and/or egress traffic is mirrored on this chip/system.	0

Ingress Mirror Control Register (Page 02h: Address 12h–15h)

Table 63: Ingress Mirror Control Register (Page 02h: Address 12h–15h)

Bit	Name	R/W	Description	Default
31:30	Reserved	R/W	Reserved	0
29	IN_DIV_EN	R/W	Ingress Divider Enable. Mirror every n^{th} received frame (n = IN_MIRROR_DIV) that has passed through the IN_MIRROR_MASK.	0
28:17	Reserved	R/W	Reserved	0
16:0	IN_MIRROR_MASK [16:0]	R/W	Ingress Mirror Port Mask. 17-bit mask which selectively allows any port with its corresponding bit set to be mirrored to the port identified by the MIRROR_CAPTURE_PORT_ID value. Note that while multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT_ID. Bits 0–16 = Port 0–16.	0

Ingress Mirror Divider (Page 02h: Address 16h–17h)

Table 64: Ingress Mirror Divider Register (Page 02h: Address 16h–17h)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Reserved	0
9:0	IN_MIRROR_DIV	R/W	Ingress Mirror Divider. Receive frames that have passed the IN_MIRROR_MASK rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT_ID. When the IN_DIV_EN bit in the Ingress Mirror Control register is set, frames that pass the IN_MIRROR_MASK rule are further divided by the value loaded into this register, so that only one in n frames (where n = IN_MIRROR_DIV) is mirrored.	0

Egress Mirror Control Register (Page 02h: Address 1Ch–1Fh)

Table 65: Egress Mirror Control Register (Page 02h: Address 1Ch–1Fh)

Bit	Name	R/W	Description	Default
31:17	Reserved	R/W	Reserved	0

Table 65: Egress Mirror Control Register (Page 02h: Address 1Ch–1Fh) (Cont.)

Bit	Name	R/W	Description	Default
16:0	OUT_MIRROR_MASK	R/W	Egress Mirror Port Mask. 17-bit mask which selectively allows any port with its corresponding bit set, to be mirrored to the port identified by the MIRROR_CAPTURE_PORT_ID value. Note that while multiple bits in a device may be set, severe congestion and/or frame loss may occur if excessive bandwidth from the mirrored port(s) is directed to the MIRROR_CAPTURE_PORT_ID. Bits 0–16 = Port0–16.	0

Model ID (Page 02h: Address 30h)

Table 66: Model ID Register (Page 02h: Address 30h)

Bit	Name	R/W	Description	Default
7:0	Model ID	RO	Chip Model ID	8’d96

Revision ID (Page 02h: Address 40h)

Table 67: Revision ID Register (Page 02h: Address 40h)

Bit	Name	R/W	Description	Default
7:0	Revision ID	RO	Chip Revision ID	0

ARL Control Registers

Table 68: ARL Control Registers (Page 04h)

Address	Bits	Register Name
00h	8	Global ARL Configuration
01h–03h	–	Reserved
04h–09h	48	BPDU Multicast Address (default: 01-80-C2-00-00-00)
0Ah–0Fh	–	Reserved
10h–15h	48	Multiport Address 1
16h–19h	32	Multiport Vector 1
1Ah–1Fh	–	Reserved
20h–25h	48	Multiport Address 2
26h–29h	32	Multiport Vector 2
2Ah–43h	–	Reserved
44h–FEh	–	Reserved
FFh	8	Page Register

Global ARL Configuration Register (Page 04h: Address 00h)

Table 69: Global ARL Configuration Register (Page 04h: Address 00h)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved	0
4	MPORT_ADDR_EN	R/W	Multiport Address Enable. When set by the host, enables the Multiport Address 1 and 2 registers, and their associated Multiport Vector 1 and 2 registers. This enables these registers in the ARL search. Note that if only one multiport address is required, the host should write both multiport address/ vector entries to the same value.	0
3:1	Reserved	R/W	Reserved	0
2	AGE_ACCELERATE	R/W	Engineering Testing only. Not to release to customers.	0
1	Reserved	R/W	Reserved	0
0	HASH_DISABLE	R/W	Disable the hash function for the ARL in such a way that entries are directly mapped to the table. The hash function is enabled as the default for the BCM5396 ARL, but can be disabled by setting this bit.	0

BPDU Multicast Address Register (Page 04h: Address 04h–09h)

Table 70: BPDU Multicast Address Register (Page 04h: Address 04h–09h)

Bit	Name	R/W	Description	Default
47:0	BPDU_MC_ADDR	R/W	BPDU Multicast Address 1. Defaults to the IEEE Standard 802.1-defined reserved multicast address for the Bridge Group Address. Programming to an alternate value allows support of proprietary protocols in place of the normal Spanning Tree Protocol. Frames with a matching DA to this address will be forwarded to the designated management port (IMP or SMP).	01-80-C2-00-00-00h

Multiport Address 1 Register (Page 04h: Address 10h–15h)

Table 71: Multiport Address 1 Register (Page 04h: Address 10h–15h)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR_1	R/W	Multiport Address 1. Allows a frame with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 1 register. Must be enabled using the MPORT_ADDR_EN bit in the Global ARL Configuration register.	00-00-00-00-00-00h

Multiport Vector 1 Register (Page 04h: Address 16h–19h)

Table 72: Multiport Vector 1 Register (Page 04h: Address 16h–19h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	MPORT_VCTR_1 [16:0]	R/W	Multiport Vector 1. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 1 register will be forwarded to each port with a bit set in the Multiport Vector 1 bit map. Bits 0–16: Port 0–16.	0

Multiport Address 2 Register (Page 04h: Address 20h–25h)

Table 73: Multiport Address 2 Register (Page 04h: Address 20h–25h)

Bit	Name	R/W	Description	Default
47:0	MPORT_ADDR_2	R/W	Multiport Address 2. Allows a frame with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector 2 register. Must be enabled using the MPORT_ADDR_EN bit in the Global ARL Configuration register.	00-00-00-00-00-00h

Multiport Vector 2 Register (Page 04h: Address 26h–29h)

Table 74: Multiport Vector 2 Register (Page 04h: Address 26h–29h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	MPORT_VCTR_2 [16:0]	R/W	Multiport Vector 2. A bit mask corresponding to the physical ports on the chip. A frame with a DA matching the content of the Multiport Address 2 register will be forwarded to each port with a bit set in the Multiport Vector 2 bit map. Bits 0–16: Port 0–16.	0

ARL/VLAN Table Access Registers

Table 75: ARL/VLAN Access Registers (Page 05h)

Address	Bits	Register Name
00h	8	ARL Read/Write Control
01h–0Fh	–	Reserved
02h–07h	48	MAC Address Index
08h–09h	12	VLAN ID Index
0Ah–0Fh	–	Reserved
10h–17h	64	ARL MAC/VID Entry 0
18h–1Bh	32	ARL FWD Entry 0
1Ch–1Fh	–	Reserved
20h–27h	64	ARL MAC/VID Entry 1
28h–2Bh	32	ARL FWD Entry 1
2Ch–2Fh	–	Reserved
30h	8	ARL Search Control
31h–32h	16	ARL Search Address
33h–3Ah	64	ARL Search MAC/VID Result 0

Table 75: ARL/VLAN Access Registers (Page 05h) (Cont.)

Address	Bits	Register Name
3Bh–3Eh	32	ARL Search Result 0
3Fh	8	Reserved
40h–47h	64	ARL Search MAC/VID Result 1
48h–4Bh	32	ARL Search Result 1
4Ch–5Fh	–	Reserved
60h	8	VLAN/TABLE Read/Write Control
61h–62h	16	VLAN TABLE Address Index
63h–6Ah	64	VLAN TABLE Entry
6Bh–FEh	–	Reserved
FFh	8	Page Register

ARL Read/Write Control Register (Page 05h: Address 00h)

Table 76: ARL Read/Write Control Register (Page 05h: Address 00h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/Done Command. Write as 1 to initiate a read or write command, after first loading the MAC_ADDR_INDX register with the MAC address for which the ARL entry is to be read or written. The BCM5396 resets the bit to indicate a read/write operation is complete and data from the bin entry is available in ARL Entry 0/1. Note that both ARL Entry 0/1 are always read from or written to by the BCM5396 when accessing the address table locations in memory.	0
6:1	Reserved	RO	Reserved	0
0	ARL_R/W	R/W	ARL Read/Write: 1 = Read 0 = Write	0

MAC Address Index Register (Page 05h: Address 02h–07h)

Table 77: MAC Address Index Register (Page 05h: Address 02h–07h)

Bit	Name	R/W	Description	Default
47:0	MAC_ADDR_INDX	R/W	MAC Address Index. The MAC address for which status is to be read or written. By writing the 48-bit SA or DA address and initiating a read command, the complete ARL bin location (two entries deep) is returned in the ARL Entry 0/1 locations. Both entries are 64 bits wide. Initiating a write command will write the contents of ARL Entry 0/1 to the specified bin location (2 entries deep) and will overwrite the current contents of the bin, regardless of the status of the Valid bit(s) in each entry.	00-00-00-00-00-00h

VLAN ID Index Register (Page 05h: Address 08h–09h)

Table 78: VID Index Register (Page 05h: Address 08h–09h)

Bit	Name	R/W	Description	Default
11:0	VID_INDX	R/W	VID Index. The MAC address for which status is to be read or written. By writing the 48-bit SA or DA address into the MAC address index and the 12-bit VID Index register if IEEE Standard 802.1Q is enabled, and initiating a read command, the complete ARL bin location (2 entries deep) returns in the ARL Entry 0/1 locations and VID Entry0/1. Both ARL entries are 64 bits wide. Both VID entries are 12 bits wide. Initiating a write command writes the contents of ARL Entry 0/1 and VID Entry 0/1 to the specified bin location (2 entries deep) and overwrites the current contents of the bin, regardless of the status of the Valid bit(s) in each entry.	12'h0

ARL MAC/VID Entry 0 Register (Page 05h: Address 10h–17h)

Table 79: ARL MAC/VID Entry 0 Register (Page 05h: Address 10h–17h)

Bit	Name	R/W	Description	Default
63:60	Reserved	RO	Reserved	0
59:48	VID0	R/W	VID0. The VID0 register is used to write the VID field of the ARL table or to read the VID field of the ARL table entry. ARL FWD Entry 0 Register and MAC/VID Entry 0 Register compose a complete entry in ARL Table while IEEE Standard 802.1Q is enabled.	0
47:0	MACADDR0	R/W	MAC Address.	0

ARL FWD Entry 0 Register (Page 05h: Address 18h–1Bh)

Table 80: ARL FWD Entry 0 Register (Page 05h: Address 18h–1Bh)

Bit	Name	R/W	Description	Default
31:22	Reserved	RO	Reserved	0
21:11	If(MACADDR[47] ==1) FWD_PRT_MAP[16:6]	R/W	Multicast Group Forward Portmap. Bits 22:11 = Portmap[16:6].	0

10:6	PORTID
	If(MACADDR[47]==0)
	PORT number[4:0]
	
	If(MACADDR[47] ==1)
	FWD_PRT_MAP[5:1]
		R/W	Port Identification.
			The port number which identifies where the station with unique MACADDR is connected.
			Forward Port Map
			
			Multicast Group Forward Portmap
			Bits 10:6 = Portmap[5:1].
				0

Table 80: ARL FWD Entry 0 Register (Page 05h: Address 18h–1Bh) (Cont.)

Bit	Name	R/W	Description	Default
5	STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry. If (MACADDR[47]==1) This is Portmap[0].	0
4	AGE	R/W	Age. Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
3	VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
2:0	PRIORITY	R/W	Priority bit for MAC-based QoS.	0

ARL MAC/VID Entry 1 Register (Page 05h: Address 20h–27h)

Table 81: ARL MAC/VID Entry 1 Register (Page 05h: Address 20h–27h)

Bit	Name	R/W	Description	Default
63:60	Reserved	RO	Reserved	0
59:48	VID1	R/W	VID1. The VID1 register is used to write the VID field of the ARL table or to read the VID field of the ARL table entry. ARL Entry 1 register and VID Entry 1 register compose a complete entry in ARL table while IEEE Standard 802.1Q is enabled.	0
47:0	MACADDR1	R/W	MAC Address.	0

ARL FWD Entry 1 Register (Page 05h: Address 28h–2Bh)

Table 82: ARL FWD Entry 1 Register (Page 05h: Address 28h–2Bh)

Bit	Name	R/W	Description	Default
31:22	Reserved	RO	Reserved	0
21:11	If (MACADDR[47] ==1) FWD_PRT_MAP[16:6]	R/W	Multicast Group Forward Portmap. Bits 22:11 = Portmap[16:6].	0

10:6	PORTID
	If (MACADDR[47]==0)
	PORT number[4:0]
	
	If (MACADDR[47] ==1)
	FWD_PRT_MAP[5:1]
		R/W	Port Identification.
			The port number which identifies where the station with unique MACADDR is connected.
			
			Forward Port Map
			Multicast Group Forward Portmap
			Bits 10:6 = Portmap[5:1].
				0

5	STATIC	R/W	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry. If (MACADDR[47]==1), this is portmap[0].	0
4	AGE	R/W	Age. Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
3	VALID	R/W	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
2:0	PRIORITY	R/W	Priority bit for MAC-based QoS.	0

ARL Search Control Register (Page 05h: Address 30h)

Table 83: ARL Search Control Register (Page 05h: Address 30h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/Done. Write a 1 to initiate a sequential search of the ARL entries, returning each entry that is currently occupied (Valid = 1 and AGE = 0) in the ARL Search Result register. Reading the ARL Search Result Register causes the ARL search to continue. The BCM5396 will clear this bit to indicate the entire ARL entry database has been searched.	0
6:1	Reserved	RO	Reserved	0
0	ARL_SR_VALID	RC	ARL Search Result Valid. Set by the BCM5396 to indicate that an ARL entry is available in the ARL Search Result register. Reset by a host read to the ARL Search Result register, which will cause the ARL search process to continue through the ARL entries until the next entry is found with a Valid bit set. This bit should not be reset by a host read to the ARL Search VID Result register. The correct process for reading an ARL entry after having searched a valid one is as follows: Read ARL Search VID Result register => Read ARL Search Result register Entry 1. Read ARL Search VID Result register => Read ARL Search Result register Entry 0. Entry 1 is missed if Entry 0 is read first, because reading Entry 0 causes the resetting of all entries.	0

ARL Search Address Register (Page 05h: Address 31h–32h)

Table 84: ARL Search Address Register (Page 05h: Address 31h–32h)

Bit	Name	R/W	Description	Default
15	ARL_ADDR_VALID	R/W (SC)	ARL Address Valid. Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry currently being accessed. Intended for factory test/diagnostic use only.	0
14:0	ARL_ADDR	R/W	ARL Address. 15-bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location and is intended for factory test/diagnostic use only.	0

ARL Search MAC/VID Result Register 0 (Page 05h: Address 33h–3Ah)

Table 85: ARL Search MAC/VID Result Register 0 (Page 05h: Address 33h–3Ah)

Bit	Name	R/W	Description	Default
63:60	Reserved	RO	Reserved	0
59:48	ARL_SEARCH_VID_RESULT	RO	ARL Search VID Result. The ARL Search VID Result registers keep the VID field in Valid ARL Entry indicated by ARL Search Function.	0
47:0	ARL_SEARCH_MACADDR	RO	ARL Search MAC Address result	0

ARL Search Result Register 0 (Page 05h: Address 3Bh–3Eh)

Table 86: ARL Search Result Register 0 (Page 05h: Address 3Bh–3Eh)

Bit	Name	R/W	Description	Default
31:22	Reserved	RO	Reserved	0
21:11	If (MACADDR[47] ==1) FWD_PRT_MAP[16:6]	R/W	Multicast Group Forward Portmap Bits 22:11 = Portmap[16:5]	0

10:6	PORTID
	If(MACADDR[47]==0)
	PORT number[4:0]
	
	If(MACADDR[47] ==1)
	FWD_PRT_MAP[5:1]
		R/W	Port Identification.
			The port number which identifies where the station with unique MACADDR is connected.
			
			Forward Port Map
			Multicast Group Forward Portmap
			Bits 10:6 = Portmap[5:1].
				0

5	STATIC	RO	Static. Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry. If(MACADDR[47] ==1), this bit is portmap[0].	0
4	AGE	RO	Age. Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0

Table 86: ARL Search Result Register 0 (Page 05h: Address 3Bh–3Eh) (Cont.)

Bit	Name	R/W	Description	Default
3	VALID	RO	Valid. Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
2:0	PRIORITY	RO	Priority bit for MAC-based QoS.	0

ARL Search MAC/VID Result Register 1 (Page 05h: Address 40h–47h)

Table 87: ARL Search MAC/VID Result Register 1 (Page 05h: Address 40h–47h)

Bit	Name	R/W	Description	Default
63:60	Reserved	RO	Reserved	0
59:48	ARL_SEARCH_VID_RESULT	RO	ARL Search VID Result. The ARL Search VID Result registers keep the VID field in Valid ARL Entry indicated by ARL Search function.	0
47:0	ARL_SEARCH_MACADDR	RO	MAC Address.	0

ARL Search Result Register 1 (Page 05h: Address 48h–4Bh)

Table 88: ARL Search Result Register 1 (Page 05h: Address 48h–4Bh)

Bit	Name	R/W	Description	Default
31:23	Reserved	RO	Reserved	0
21:11	If(MACADDR[47] ==1) FWD_PRT_MAP[16:6]	R/W	Multicast Group Forward Portmap Bits 22:11 = Portmap[16:5]	0

10:6	PORTID
	If(MACADDR[47]==0)
	PORT number[4:0]
	
	If(MACADDR[47] ==1)
	FWD_PRT_MAP[5:1]
		R/W	Port Identification
			The port number which identifies where the station with unique MACADDR is connected.
			
			Forward Port Map
			Multicast Group Forward Portmap
			Bits 10:6 = Portmap[5:1]
				0

5	STATIC	RO	Static Set to indicate that the entry is controlled by the external management processor, and automatic learning and aging of the entry will not take place. When cleared, the internal learning and aging process will control the validity of the entry. If(MACADDR[47] ==1), this bit is portmap[0]	0

Table 88: ARL Search Result Register 1 (Page 05h: Address 48h–4Bh) (Cont.)

Bit	Name	R/W	Description	Default
4	AGE	RO	Age Set to indicate that an address entry has been learned or accessed. Reset by the internal aging algorithm. If the internal aging process detects a Valid entry has remained unused for the period set by the AGE_TIME, and the entry has not been marked as Static, the entry will have the Valid bit cleared. The Age bit is ignored if the entry has been marked as Static.	0
3	VALID	RO	Valid Set to indicate that a valid MAC address is stored in the MACADDR field, and that the entry has not aged out or been freed by the management processor. Reset when an entry is empty, the address has been aged out by the internal aging process, or the external management processor has invalidated the entry. Automatic learning will take place if an address location is not valid and has not been marked as static.	0
2:0	PRIORITY	RO	Priority bit for MAC-based QoS	0

VLAN Table Read/Write Control Register (Page 05h: Address 60h)

Table 89: VLAN Table Read/Write Control Register (Page 05h: Address 60h)

Bit	Name	R/W	Description	Default
7	START/DONE	R/W (SC)	Start/Done Command Write as 1 to initiate a read or write command, after first loading the VTBL Address Index register with the VLAN ID for which the VTBL entry is to be read or written. The BCM5396 resets the bit to indicate a write operation completed, or a read operation is complete and data from the bin entry is available in VTBL Entry.	0
6:1	Reserved	RO	Reserved	0
0	VTBL_R/W	R/W	VTBL Read/Write 1 = Read. 0 = Write.	0

VLAN Table Address Index Register (Page 05h: Address 61h–62h)

Table 90: VLAN Table Address Index Register (Page 05h: Address 61h–62h)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	Reserved	0
11:0	VTBL_ADDR_INDEX	R/W	VLAN Table Address Index The VLAN Table Address Index Register is used to access VLAN Table Entry.	0

VLAN Table Entry Register (Page 05h: Address 63h–6Ah)

Table 91: VLAN Table Entry Register (Page 05h: Address 63h–6Ah)

Bit	Name	R/W	Description	Default
63:40	Reserved	RO	Reserved	0
39:23	UNTAG_MAP	R/W	Untag Port Map The VLAN-tagged Frame forward to the destination ports corresponding bits set in the Map will be untagged. Bits16:0: Port 16:0 (Bit16: IMP Port)	0
22:6	FWD_MAP	R/W	Forward Port Map The VLAN-tagged Frame is allowed to be forwarded to the destination ports corresponding bits set in the Map Bits16:0: Port 16:0 (Bit16: IMP Port)	0
5:1	SPT	R/W	Spanning tree Index	0
0	VALID	R/W	VALID Set to indicate that a valid VID entry is stored in the VLAN table.	0

Reserved Registers

Table 92: Flow Control Registers (Page 0Ah)

Address	Bits	Register Name
00h–0Fh	128	Reserved
10h–11h	16	Reserved
12h–1Fh	112	Reserved
20h–21h	16	Reserved
22h–23h	16	Reserved
24h–25h	16	Reserved
26h–27h	16	Reserved
28h–29h	16	Reserved
2Ah–2Bh	16	Reserved
2Ch–2Dh	16	Reserved
2Eh–2Fh	16	Reserved
30h–31h	16	Reserved
32h–33h	16	Reserved
34h–35h	16	Reserved
36h–37h	16	Reserved
38h–39h	16	Reserved
3Ah–3Bh	16	Reserved

Table 92: Flow Control Registers (Page 0Ah) (Cont.)

Address	Bits	Register Name
3Ch–3Dh	16	Reserved
3Eh–3Fh	16	Reserved
40h–41h	16	Reserved
42h–43h	16	Reserved
44h–45h	16	Reserved
46h–47h	16	Reserved
48h–49h	16	Reserved
4Ah–4Bh	16	Reserved
4Ch–4Dh	16	Reserved
4Eh–4Fh	16	Reserved
50h–57h	64	Reserved
58h–59h	16	Reserved
5Ah–5Bh	16	Reserved
5Ch–5Dh	16	Reserved
5Eh–5Fh	16	Reserved
60h–61h	16	Reserved
62h–63h	16	Reserved
64h–65h	16	Reserved
66h–67h	16	Reserved
68h–6Fh	64	Reserved
70h–71h	16	Reserved
72h–73h	16	Reserved
74h–75h	16	Reserved
76h–77h	16	Reserved
78h–79h	16	Reserved
7Ah–7Fh	48	Reserved
80h–81h	16	Reserved
82h–8Fh	112	Reserved
90h–91h	16	Reserved
92h–93h	16	Reserved
94h–95h	16	Reserved
96h–97h	16	Reserved
98h–99h	16	Reserved
9Ah–9Bh	16	Reserved
9Ch–9Dh	16	Reserved
9Eh–9Fh	16	Reserved

Reserved (Page 0Ah: Register 00h–01h)

Reserved (Page 0Ah: Register 10h–11h)

Reserved (Page 0Ah: Register 20h–27h)

Reserved (Page 0Ah: Register 28h–2Fh)

Reserved (Page 0Ah: Register 30h–37h)

Reserved (Page 0Ah: Register 38h–3Fh)

Reserved (Page 0Ah: Register 40h–47h)

Reserved (Page 0Ah: Register 48h–4Fh)

Reserved (Page 0Ah: Register 56h–57h)

Reserved (Page 0Ah: Register 58h–59h)

Reserved (Page 0Ah: Register 5Ah–5Bh)

Reserved (Page 0Ah: Register 5Ch–5Dh)

Reserved (Page 0Ah: Register 60h–67h)

Reserved (Page 0Ah: Register 70h–77h)

Reserved (Page 0Ah: Register 78–79h)

Reserved (Page 0Ah: Register 80h–81h)

Reserved (Page 0Ah: Register 90h–91h)

Reserved (Page 0Ah: Register 92h–93h)

Reserved (Page 0Ah: Register 94h–95h)

Reserved (Page 0Ah: Register 96h–97h)

Reserved (Page 0Ah: Register 98h–99h)

Reserved (Page 0Ah: Register 9Ah–9Bh)

Reserved (Page 0Ah: Register 9Ch–9Dh)

Reserved (Page 0Ah: Register 9Eh–9Fh)

Internal SerDes Registers (Port 0–15): Page 10h–1fh

Table 93: Internal SerDes Registers Page Descriptions 10h–1Fh

Access Through SPI	*Description*
Page Number (Hex)	*Port Number*
10h	Port 0
11h	Port 1
12h	Port 2
13h	Port 3
14h	Port 4
15h	Port 5
16h	Port 6
17h	Port 7
18h	Port 8
19h	Port 9
1Ah	Port 10
1Bh	Port 11
1Ch	Port 12
1Dh	Port 13
1Eh	Port 14
1Fh	Port 15

Table 94: Internal SerDes Registers Page 10h–1Fh

Address (Through SPI Interface)	*Block Number*	*Bits*	*Description*
00h–01h	0	16	MII Control Register (Page 10h ~ 1F: Addr 00h ~ 01h)
02h–03h	0	16	MII Status Register (Page 10h ~ 1Fh: Addr 02h ~ 03h)
04h–07h	0	–	Reserved
08h–09	0	16	Auto-Negotiation Advertisement Register (Page 10h ~ 1Fh: Addr 08h ~ 09h)
0Ah–0Bh	0	16	Auto-Negotiation Link Partner Ability Register (Page 10h ~ 1Fh: Addr 0Ah ~ 0Bh)
0Ch–0Dh	0	16	Auto-Negotiation Expansion Register (Page 10h ~ 1Fh: Addr 0Ch ~ 0Dh)
0Eh–1Dh	0	–	Reserved
1Eh–1Fh	0	16	Extended Status Register (Page 10h ~ 1Fh: Addr 1Eh ~ 1Fh)

Table 94: Internal SerDes Registers Page 10h–1Fh (Cont.)

Address (Through SPI Interface)	Block Number	Bits	Description
20h–21h	0	16	* SerDes/SGMII Control 1 Register in Block 0 * Analog Transmit Register in Block 1 (Page 10h ~ 1Fh: Addr 20h ~ 21h)
22h–23h	0	16	SerDes/SGMII Control 2 Register in Block 0 (Page 10h ~ 1Fh: Addr 22h ~ 23h)
24h–25h	0	16	SerDes/SGMII Control 3 Register in Block 0 (Page 10h ~ 1Fh: Addr 24h ~ 25h)
26h–27h	0	16	Reserved
28h–29h	0	16	SerDes/SGMII Status 1 Register (Page 10h ~ 1Fh: Addr 28h ~ 29h)
2Ah–2Bh	0	16	SerDes/SGMII Status 2 Register (Page 10h ~ 1Fh: Addr 2Ah ~ 2Bh)
2Ch–2Dh	0	16	SerDes/SGMII Status 3 Register (Page 10h ~ 1Fh: Addr 2Ch ~ 2Dh)
2Eh–2Fh	0	16	BER/CRC Error Counter Register (Page 10h ~ 1Fh: Addr 2Eh ~ 2Fh)
30h ~ 31h	0	16	PRBS Control Register (Page 10h ~ 1Fh: Addr 30h ~ 31h)
32h ~ 33H	0	16	PRBS Status Register (Page 10h ~ 1Fh: Addr 32h ~ 33h)
34h ~ 35h	0	16	Pattern Generator Control Register (Page 10h ~ 1Fh: Addr 34h ~ 35h)
36h ~ 37h	0	16	Pattern Generator Status Register (Page 10h ~ 1Fh: Addr 36h ~ 37h)
3Ah ~ 3Bh	0	16	Force Transmit 1 Register (Page 10h ~ 1Fh: Addr 3Ah ~ 3Bh)
3Ch ~ 3Dh	0	16	Force Transmit 1 Register (Page 10h ~ 1Fh: Addr 3Ch ~ 3Dh)
3Eh ~ 3Fh	1	16	Block Address Number (Page 10h ~ 1Fh: Addr 3Eh ~ 3Fh)

Note: When Block 1 is select via Page 10h ~ 1Fh: Addr 3Eh ~ 3Fh, Address spaces 22h ~ 2Dh are Reserved.

MII Control Register (Page 10h–1Fh: Address 00h–01h)

Table 95: MII Control (Page 10h–1Fh: Address 00h–01h)

Bit	Name	R/W	Description	Default
15	RST_SW	R/W	PHY reset. 0 = Normal operation. 1 = PHY reset.	0
14	LOOPBACK	R/W	Loopback enable. 0 = Normal operation. 1 = Loopback enable.	0

Table 95: MII Control (Page 10h–1Fh: Address 00h–01h) (Cont.)

Bit	Name	R/W	Description	Default
13	Speed Select (LSB)	R/W	Speed Select Bits [6, 13]. 1X = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps Only used in SGMII Mode. Ignored when in SerDes Mode.	0
12	AN_EN	R/W	Auto-negotiation Enable (AN). 0 = Disable. 1 = Enable AN.	1
11	PWRDN	R/W	Power-down will disable the port conserving power consumption. MDC/MDIO and SPI access is still available. 0 = Normal operation. 1 = Low power mode enable.	0
10	Reserved	RO	Reserved. Write 0, ignore read.	0
9	RESTART_AN	R/W	Restart AN. 0 = Normal operation. 1 = Restart the AN process.	0
8	Duplex	R/W	Full-duplex. 0 = Half-duplex 1 = Full-duplex	1
7	COL_TEST_EN	R/W	Collision test enable. 0 = Normal operation. 1 = Collision test mode enable.	0
6	Speed Select (MSB)	R/W	Speed Select Bits [6, 13]. 1X = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps Only used in SGMII Mode. Ignored when in SerDes Mode.	1
5:0	Reserved	RO	Reserved. Write 0, ignore read.	0x00

MII Status Register (Page 10h–1Fh: Address 02h–03h)

Table 96: MII Status (Page 10h–1Fh: Address 02h–03h)

Bit	Name	R/W	Description	Default
15	100BASE_T4	RO	0 = Not capable. 1 = 100BASE-T4 capable.	0
14	100BASEX_FDX	RO	0 = Not capable. 1 = 100BASE-X full-duplex capable.	0
13	100BASEX_HDX	RO	0 = Not capable. 1 = 100BASE-X half-duplex capable.	0

Table 96: MII Status (Page 10h–1Fh: Address 02h–03h) (Cont.)

Bit	Name	R/W	Description	Default
12	10BASET_FDX	RO	0 = Not capable. 1 = 10BASE-T full-duplex capable.	0
11	10BASET_HDX	RO	0 = Not capable. 1 = 10BASE-T half-duplex capable.	0
10	100BASET2_FDX	RO	0 = Not capable. 1 = 100BASE-T2 full-duplex capable.	0
9	100BASET2_HDX	RO	0 = Not capable 1 = 100BASE-T2 half-duplex capable.	0
8	EXT_STATUS	RO	0 = No extended status. 1 = Extended status in register 0x0F.	1
7	Reserved	RO	Reserved. Write 0, ignore read.	0
6	MF_PREAMBLE_SUPPRESSION	RO	0 = PHY does not accept management frames with preamble suppressed. 1 = PHY accepts management frames with preamble suppressed.	1
5	AN_COMPLT	RO	Auto negotiation complete. 0 = Not done. 1 = AN complete.	0
4	RF	RO	Remote fault. 0 = No fault detected. 1 = Remote fault detected.	0
3	AN_ABILITY	RO	Auto negotiation ability. 0 = Not capable of AN. 1 = AN capable.	1
2	LINK_STATUS	RO	Link status. 0 = Link fail. 1 = Good link.	0
1	JABBER_DETECT	RO	Jabber detect. 0 = Not detected. 1 = Jabber detected.	0
0	EXT_CAPABILITY	RO	Extended capability. 0 = Supports basic register set only. 1 = Extended register capabilities supported.	1

Auto-Negotiation Advertisement (Page 10h–1Fh: Address 08h–09h)

Table 97: Auto-Negotiation Advertisement (Page 10h–1Fh: Address 08h–09h)

Bit	Name	R/W	Description	Default
15	NEXT_PG	RO	Next page. 1 = Next page ability supported 0 = Next page ability not supported	0
14	Reserved	RO	Reserved, write as 0, ignore read.	0
13:12	RF	R/W	Remote fault: 00 = No fault 01 = Link failure 10 = Offline 11 = An error	00
11:9	Reserved	RO	Reserved, write as 0, ignore read.	00
8:7	PAUSE	R/W	Pause 00 = No pause 01 = Symmetric pause 10 = Asymmetric pause towards link partner 11 = Both symmetric and asymmetric pause towards local device	11
6	HDX Capable	R/W	Half-duplex 0 = Do not advertise half-duplex 1 = Advertise half-duplex	1
5	FDX Capable	R/W	Full-duplex 0 = Do not advertise full-duplex 1 = Advertise full-duplex	1
4:0	Reserved	RO	Reserved, write as 0, ignore read.	00

Auto-Negotiation Link Partner Ability (Page 10h–1Fh: Address 0Ah–0Bh)

Table 98: Auto-Negotiation Link Partner Ability (Page 10h–1Fh: Address 0Ah–0Bh)

Bit	Name	R/W	Description	Default
15	Next Page/Link	RO	When link partner configured to SerDes mode (bit[0] = 0): 1 = Link partner is next page capable 0 = Link partner is not next page capable When link partner configured to SGMII mode (bit[0] = 1): 1 = Link 0 = No link	0
14	ACK	RO	Reserved, write as 0, ignore read.	0

Table 98: Auto-Negotiation Link Partner Ability (Page 10h–1Fh: Address 0Ah–0Bh) (Cont.)

Bit	Name	R/W	Description	Default
13:12	Remote Fault/ Duplex	RO	When link partner configured to SerDes mode (bit[0] = 0), these bits indicate advertised remote fault setting of link partner: 00 = No fault 01 = Link failure 10 = Offline 11 = AN error When link partner configured to SGMII mode bit[0] = 1), these bits indicate advertised duplex of link partner: x1 = Full-duplex x0 = Half-duplex	0x0
11:10	Speed	RO	When link partner configured to SerDes mode (bit[0] = 0), these bits are reserved When link partner configured to SGMII mode (bit[0] = 1), indicates advertised link speed of link partner: 1x = 1000M 01 = 100M 00 = 10M	0x0
9	Reserved	RO	Reserved, write as 0, ignore read.	00
8:7	Pause Capable	RO	When link partner configured to SerDes mode (bit[0] = 0), indicates link partner pause capabilities: 00 = No pause 01 = Symmetrical pause 10 = Asymmetrical pause towards link partner 11 = Both symmetric and asymmetric pause towards local device When link partner configured to SGMII mode (bit[0] = 1), these bits are Reserved.	0x0
6	HDX Capable	RO	When link partner configured to SerDes mode (bit[0] = 0), indicates link partner pause capabilities: 0 = Not half-duplex capable 1 = Half-duplex capable When link partner configured to SGMII mode (bit[0] = 1), these bits reserved	0
5	FDX (for SerDes only)	RO	When link partner configured to SerDes mode (bit[0] = 0), indicates link partner pause capabilities: 0 = Not full-duplex capable 1 = Full-duplex capable When link partner configured to SGMII mode (bit[0] = 1), these bits reserved	0
4:1	Reserved	RO	Reserved, write as 0, ignore read.	0x0
0	SGMII	RO	SGMII mode. 0 = Fiber mode 1 = SGMII mode	0

Auto-Negotiation Expansion (Page 10h–1Fh: Address 0Ch–0Dh)

Table 99: Auto-Negotiation Expansion (Page 10h–1Fh: Address 0Ch–0Dh)

Bit	Name	R/W	Description	Default
15:3	Reserved	RO	Reserved, write as 0, ignore read.	0x0000
2	NP_ABILITY	RO	Next page ability. 0 = Local device is not next page enabled. 1 = Local device is next page enabled.	0
1	PG_REC	RO	Page received. 0 = New link code word is not received. 1 = New link code word is received.	0
0	Reserved	RO	Reserved, write as 0, ignore read.	0

Extended Status Register (Page 10h–1Fh: Address 1Eh–1Fh)

Table 100: Extended Status (Page 10h–1Fh: Address 1Eh–1Fh)

Bit	Name	R/W	Description	Default
15	1000BASEX_FDX	RO	0 = Not capable 1 = 1000BASE-X full-duplex capable	1
14	1000BASEX_HDX	RO	0 = Not capable 1 = 1000BASE-X half-duplex capable	1
13	1000BASET_FDX	RO	0 = Not capable 1 = 1000BASE-T full-duplex capable	0
12	1000BASET_HDX	RO	0 = Not capable 1 = 1000BASE-T half-duplex capable	0
11:0	Reserved	RO	Reserved, write as 0, ignore read.	000

SerDes/SGMII Control 1 (Page 10h–1Fh: Address 20H ~ 21H, BLOCK 0)

Table 101: SerDes/SGMII Control1 (Page 10h–1Fh: Address 20h–21h, Block 0)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Reserved, write as 0, ignore read.	0
14	Reserved	R/W	Reserved	0
13	Global Write	R/W	MDC/MDIO commands addressed to PHYADD 00 will affect all ports that have the Global Write enabled. 0 = Normal operation 1 = Global Write Enabled	0

Table 101: SerDes/SGMII Control1 (Page 10h–1Fh: Address 20h–21h, Block 0) (Cont.)

Bit	Name	R/W	Description	Default
12	SERDES_TX_AMP_OVR	R/W	SerDes Tx Amplitude Override 1 = Allows the override of "Output_Voltage_Level" (Bits [15:12]) of Analog Transmit Register (Page 10h~1Fh: Address 20h~21h Block 1). 0 = Normal operation. Bit [14] of "Output_Voltage_Level" of Analog Transmit Register (Page 10h~1Fh: Address 20h~21h Block 1) is internally set based on SGMII or SerDes mode.	0
11	Counter Select	R/W	Error Counter Register Definition Configures the type of events counted in "BER/CRC Error Counter Register (Page 10h ~ 17h: Address 2Eh). 0 = Select CRC errors 1 = Select received packets	0
10	REMOTE_LPBK	R/W	Remote loopback operates in all available speeds. 0 = Normal operation. 1 = Enable remote loopback (operates in 10/100/1000 speed).	0
9	Reserved	RO	Reserved	0
8	CD_EN	R/W	0 = Disable comma detection 1 = Enable comma detection	1
7	CRC_DIS	R/W	0 = Enable CRC checker. 1 = Disable CRC checker by gating the clock to save power.	1
6	Reserved	R/W	Reserved	1
5	SGMII_MSTR	R/W	This bit configures the port to operate in Master mode (typical of PHY device) to allow testing link conditions between two Switch ports. 0 = Normal operation. 1 = SGMII mode operates in master PHY mode. If auto-negotiation is enabled, then the local device sends out the following auto-negotiation code word: [15] = 1 [14] = ack [13] = 0 [12] = Register 0, bit 8 [11] = Register 0, bit 6 [10] = Register 0, bit 13 [9:0] = 0000000001	0
4	AUTODET_EN	R/W	0 = Disable auto-detection (fiber or SGMII mode is set according to bit 0 of this register). 1 = Enable auto-detection (fiber and SGMII mode switches each time a auto-negotiation page is received with the wrong selector field in bit 0.)	1
3	Reserved	R/W	Reserved	0

Table 101: SerDes/SGMII Control1 (Page 10h–1Fh: Address 20h–21h, Block 0) (Cont.)

Bit	Name	R/W	Description	Default
2	Reserved	R/W	Reserved	0
1	TBI	R/W	0 = GMII interface. 1 = Ten-bit interface.	0
0	FIBER	R/W	0 = SGMII mode. 1 = Fiber SerDes mode.	0

Analog Transmit Register (Page 10H ~ 1FH: Address 20H ~ 21H BLOCK 1.)

refer to page 10h ~ 1fh: address 3e on how to select this register.

Table 102: Analog Transmit Register (Page 10h ~ 1Fh: Address 20h ~ 21h, Block 1)

Bit	Name	R/W	Description	Default
15:12	Output_Voltage_Level	R/W	This setting may need to be changed from the default value if the transmitter is required to drive long trace lengths. If Bit[12] of SerDes/SGMII Control 1 Register (Page 10h–1Fh: Address 20h~21h, Block 0) is set to 1, the bits control the output voltage level from 0 mV to 750 mV in 16 equal steps (before any loss or variations in resistance). This is approximate. The actual voltage swing can be found by measuring the device on the board. If Block 0, Register 20h, bit 12 is set to 0, then bit 14 is internally set based on SGMII or SerDes mode. Only bits 15, 13, and 12 can be programmed. All four bits determine transmit amplitude.	4'b1100
11:9	Reserved	–	Reserved	3'b100
8:6	Pre_Emphasis_Coeff	R/W	Allows eight possible combinations ranging from 0% to 50%. 0x7 is 50% and 0x0 is 0%. The granularity is roughly linear across the eight settings.	0h
5:0	Reserved	R/W	Reserved	6'b10-0000

SerDes/SGMII Control 2 (Page 10h–1Fh: Address 22h–23h)

Table 103: SerDes/SGMII Control 2 (Page 10h–1Fh: Address 22h–23h)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Reserved, write as 0, ignore read.	0
14	CLEAR_BER_CNTR	R/W SC	1 = Clear bit-error-rate counter "BER/CRC Error Counter Register (Page 10h ~ 17h: Address 2E)" bit[15:8]. 0 = Normal operation.	0
13	TRANSMIT_IDLE_JAM_SEQ_TEST	R/W	This bit activates a transmit idle test sequence for testing purposes. The 16-stage, 10-bit transmit test sequence is forced regardless of link conditions. Setting Force Transmit 1/2 in addition to this bit can modify the idle test sequence. "Force Transmit 1 Register (Page 10h ~ 17h: Address 3Ch)" bit[9:0] will override D16.2 for stage 6 (289h) 1 = Enable transmit idle test sequence 0 = Normal operation	0
12:8	Reserved	RO	Reserved, write as 0, ignore read.	0
7	Reserved	RO	Reserved, write as 0, ignore read.	0
6	Reserved	RO	Reserved, write as 0, ignore read.	0
5	FORCE_XMIT_DATA_ON_TXSIDE	R/W	1 = Allow packets to be transmitted regardless of the condition of the link or synchronization. 0 = Normal operation.	0

Table 103: SerDes/SGMII Control 2 (Page 10h–1Fh: Address 22h–23h) (Cont.)

Bit	Name	R/W	Description	Default
4	DIS_RF_SENSE	R/W	0 = Automatically detect remote faults and send remote fault status to link partner via auto-negotiation when fiber mode is selected. SGMII does not support remote faults. 1 = Disable automatic sensing of remote faults, such as auto-negotiation error.	0
3	Reserved	RO	Reserved.	0
2	Stable Link Filter	R/W	This bit forces the constant sync status for 10ms before establishing link. This prevents potential false-link events in SerDes applications not using auto-negotiation or the signal detect pin. 0 = Normal operation. 1 = Sync-status must be set for a solid 10 ms before a valid link is established when auto-negotiation is disabled.	0
1	DIS_FALSE_LINK	R/W	0 = Normal operation. 1 = Do not allow link to be established when auto-negotiation is disabled and receiving auto-negotiation code words. The link is only established in this case after idles are received. (This bit does not need to be set, if bit 0 is set.)	0
0	EN_PAR_DET	R/W	0 = Disable. 1 = Enable parallel detection. (This turns auto negotiation on and off as needed to properly link up with the link partner. The idles and auto-negotiation code words received from the link partner are used to make this decision.)	1

SerDes/SGMII Control 3 (Page 10h–1Fh: Address 24h–25h)

Table 104: SerDes/SGMII Control 3 (Page 10h–1Fh: Address 24h–25h)

Bit	Name	R/W	Description	Default
15	Reserved	RO	Reserved, write as 0, ignore read.	0
14	Reserved	RO	Reserved, write as 0, ignore read.	0
13	DIS_TX_CRS	R/W	0 = Normal operation. 1 = Disable generating CRS from transmitting in half-duplex mode. Only receiving generates CRS.	0
12:7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	1
5:3	Reserved	RO	Reserved	0
2:1	FIFO_ELAS_TX_RX	R/W	00 = Supports packets up to 5 KB. 01 = Supports packets up to 10 KB. 1X = Supports packets up to 13.5 KB.	01
0	Reserved	RO	Reserved.	0

Reserved (Page 10h–1Fh: Address 26h–27h)

SerDes/SGMII Status 1 (Page 10h–1Fh: Address 28h–29h)

Table 105: SerDes/SGMII Status 1 (Page 10h–1Fh: Address 28h–29h)

Bit	Name	R/W	Description	Default
15	TXFIFO_ERR	RO	0 = No transmit FIFO error detected since last read. 1 = Transmit FIFO error detected since last read.	0
14	RXFIFO_ERR	RO	0 = No receive FIFO error detected since last read. 1 = Receive FIFO error detected since last read.	0
13	FALSE_CRS	RO	0 = No false carrier detected since last read. 1 = False carrier detected since last read.	0
12	CRC_ERR	RO	0 = No CRC error detected since last read or detection is disabled via "SerDes/SGMII Control 1 Register (Page 10h ~ 1Fh: Address 20h)" bit[7]. 1 = CRC error detected since last read.	0
11	TX_ERR	RO	0 = No transmit error code detected since last read. 1 = Transmit error code detected since last read (rx_data_error state in PCS receive FSM).	0
10	RX_ERR	RO	0 = No receive error since last read. 1 = Receive error since last read (early_end state in PCS receive FSM).	0
9	CRS_EXT	RO	0 = No carrier extend error since last read. 1 = Carrier extend error since last read (extend_err in PCS receive FSM).	0
8	EARLY_END_EXT	RO	0 = No early end extension since last read. 1 = Early end extension since last read (early_end_ext in PCS receive FSM).	0
7	LINK_CHG	RO	0 = Link status has not changed since last read. 1 = Link status has changed since last read.	0
6	PAUSE_RES_RX	RO	0 = Disable pause receive. 1 = Enable pause receive.	0
5	PAUSE_RES_TX	RO	0 = Disable pause transmit. 1 = Enable pause transmit.	0
4:3	SPEED_STAT	RO	00 = 10 Mbps. 01 = 100 Mbps. 1X = 1000 Mbps.	0x0
2	DUPLEX_STAT	RO	0 = Half-duplex. 1 = Full-duplex.	0
1	LINK_STAT	RO	0 = Link is down. 1 = Link is up.	0
0	SGMII_MODE	RO	0 = SerDes mode (1000BASE-X). 1 = SGMII mode.	0

SerDes/SGMII Status 2 (Page 10h–1Fh: Address 2Ah–2Bh)

Table 106: SerDes/SGMII Status 2 (Page 10h–1Fh: Address 2Ah–2Bh)

Bit	Name	R/W	Description	Default
15	SGMII_MODE_CHG	RO	0 = SGMII/SerDes mode has not changed since last read (fixed in SGMII or SerDes mode). 1 = SGMII/SerDes mode has changed since last read (SGMII mode enabled or disabled). This bit is useful when the auto-detection is enabled in "SerDes/SGMII Control 1 Register (Page 10h ~ 1Fh: Address 20h bit[4])".	0
14	CONS_MISMATCH	RO	A consistency mismatch results from incompatibilities represented in the link code word of the local and remote link partners. SerDes or SGMII mode. 0 = Consistency mismatch has not been detected since last read. 1 = Consistency mismatch detected since last read.	0
13	AN_RES_ERR	RO	0 = Auto-negotiation error has not been detected since last read. 1 = Auto-negotiation error detected since last read.	0
12	SGMII_SEL_MIS	RO	A SGMII selector mismatch occurs when the auto-negotiation page received from the link partner has bit[0] = 0 while local device is in SGMII mode. 0 = SGMII selector mismatch not detected since last read. 1 = SGMII selector mismatch detected since last read.	0
11	SYNC_STAT_FAIL	RO	0 = Sync_status has not failed since last read. 1 = Sync_status has failed since last read (synchronization has been lost).	0
10	SYNC_STAT_OK	RO	0 = Sync_status ok has not been detected since last read. 1 = Sync_status ok detected since last read (synchronization has been achieved).	0
9	RUDI_C	RO	0 = Rudi_c has not been detected since last read. 1 = Rudi_c detected since last read.	0
8	RUDI_I	RO	0 = Rudi_i has not been detected since last read. 1 = Rudi_i detected since last read.	0
7	RUDI_INVALID	RO	0 = Rudi_invalid has not been detected since last read. 1 = Rudi_invalid detected since last read.	0
6	LINK_DN_SYNC_LOSS	RO	0 = Failure condition has not been detected since last read. 1 = A valid link went down due to a loss of synchronization for over 10 ms.	0
5	IDLE_DETECT	RO	0 = Idle detect state not entered since last read. 1 = Idle detect state in auto-negotiation FSM entered since last read.	0
4	CMPLT_ACK	RO	0 = Complete acknowledge state not entered since last read. 1 = Complete acknowledge state in auto-negotiation FSM entered since last read.	0

Table 106: SerDes/SGMII Status 2 (Page 10h–1Fh: Address 2Ah–2Bh) (Cont.)

Bit	Name	R/W	Description	Default
3	ACK_DETECT	RO	0 = Acknowledge detect state not entered since last read. 1 = Acknowledge detect state in auto-negotiation FSM entered since last read.	0
2	ABILITY_DETECT	RO	0 = Ability detect state not entered since last read. 1 = Ability detect state in auto-negotiation FSM entered since last read.	0
1	AN_DIS_LINK_OK	RO	0 = An_disable_link_ok not entered since last read. 1 = An_disable_link_ok state in auto-negotiation FSM entered since last read.	0
0	AN_EN_LINK_OK	RO	0 = An_enable state has not been entered since last read. 1 = An_enable state in auto-negotiation FSM entered since last read.	0

SerDes/SGMII Status 3 (Page 10h–1Fh: Address 2Ch–2Dh)

Table 107: SerDes/SGMII Status 3 (Page 10h–1Fh: Address 2Ch–2Dh)

Bit	Name	R/W	Description	Default
15:10	Reserved	RO	Reserved. Write as 0, ignore read.	0x0
9	Signal Detect Filter Output	RO	This bit represents the output of the Signal Detect filter, regardless of whether the filter is active or not. This status signal is still valid when "SerDes/SGMII Control 1 Register (Page 10h ~ 1Fh: Address 20h)" bit[14] = 1. Noise pulses less than 16 ns wide are still removed whenever the filter is disabled 0 = Output of signal detect is not set. 1 = Output of signal detect filter is set. This signal is used for the PCS synchronization. When the Signal Detect signal is disabled "SerDes/SGMII Control 1 Register (Page 10h ~ 17H: Address 20h)" bit[2] = 0, then the output of the filter is forced high.	0
8	Signal Detect Inversion Output	RO	This status signal is the signal detect result when "SerDes/SGMII Control 1 Register (Page 10h ~ 1Fh: Address 20h)" bit[3] = 0; Otherwise, it is the inversion of the signal detect. 0 = Output of signal detect is not set. 1 = Output of signal detect filter is set. This is the only valid Signal Detect status bit when the port is powered down from "MII Control Register (Page 10h ~ 1Fh: Address 00h)" bit[11].	0
7	SD_FILTER_CHG	RO	0 = Signal detect has not changed since last read. 1 = Signal detect has changed since last read. The signal detect change is based on a change in bit [9] of this register.	0
6	Reserved	RO	Reserved	0
5	Reserved	RO	Reserved	0

Table 107: SerDes/SGMII Status 3 (Page 10h–1Fh: Address 2Ch–2Dh) (Cont.)

Bit	Name	R/W	Description	Default
4	Reserved	RO	Reserved. Write as 0, ignore read.	0
3:0	Reserved	RO	Reserved. Write as 0, ignore read.	0x0

BER/CRC Error Counter Register (Page 10h ~ 1Fh: Address 2Eh ~ 2Fh)

Table 108: BER/CRC Error Counter Register (Page 10h ~ 1Fh: Address 2Eh ~ 2Fh)

Bit	Name	R/W	Description	Default
15:8	Bit Error Rate (BER) Counter	RO	Number if invalid code groups detect while sync_status = 1 Freezes at FFh Write "SerDes/SGMII Control 2 Register (Page 10h ~ 17h: Address 22h)" bit[14] = 1 in order to clear.	00h
7:0	CRC Error/ Receive Packet Counter	R/W CR	Number of CRC errors detected since last read. Freezes at FFh. When "SerDes/SGMII Control 1 Register (Page 10h ~ 17h: Address 20h)" bit[11] is set, the counter detects the number of received packets instead of CRC errors.	00h

PRBS Control Register (Page 10h ~ 1Fh: Address 30h ~ 31h)

Table 109: PRBS Control Register (Page 10h ~ 1Fh: Address 30h ~ 31h)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Write as 0, ignore on read.	00h
3:2	PRBS	R/W	11 = x(n) = 1 + x(28) + x(31) 10 = x(n) = 1 + x(18) + x(23) 01 = x(n) = 1 + x(14) + x(15) 00 = x(n) = 1 + x(6) + x(7)	00
1	Invert PRBS Order	R/W	1 = Invert polynomial sequence 0 = Normal operation	0
0	PRBS Enable	R/W	1 = Enable PRBS 0 = Disable PRBS	0

PRBS Status Register (Page 10h ~ 1Fh: Address 32h ~ 33h)

Table 110: PRBS Status Register (Page 10h ~ 1Fh: Address 32h ~ 33h)

Bit	Name	R/W	Description	Default
15:13	PRBS Error State	RO CR	Grey coded FSM: 100 = 1024 or more errors 101 = 512 ~ 1023 errors 111 = 256 ~ 511 errors 110 = 128 ~ 255 errors 010 = 64 ~ 127 errors 011 = 32 ~ 63 errors 001 = 1 ~ 31 errors 000 = No errors	000
12	PRBS Lost Lock	RO LH	1 = PRBS has lost lock since last read 0 = PRBS has not lost lock since last read	0
11	PRBS Locked	RO	1 = PRBS monitor is locked 0 = PRBS monitor is not locked	0
10:0	PRBS Errors	RO CR	Number of PRBS errors detected while locked. Freezes at 7FFh. ***Note:*** Counter is not synchronized to read status clock. The might increment while reading, causing inaccurate results. The PRBS should be disabled before reading the 11-bit error counter.	000h

Pattern Generator Control Register (Page 10H ~ 1Fh: Address 34h ~ 35h)

Table 111: Pattern Generator Control Register (Page 10h ~ 1Fh: Address 34h ~ 35h)

Bit	Name	R/W	Description	Default
15	Reserved	R/W	Write as 0, ignore on read.	0
14	TXER	R/W	1 = Set txer = 1 during CRC portion of packet 0 = Normal operation	0
13	Skip CRC	R/W	1 = Do not append 32-bit CRC to end of packet 0 = Normal operation	0
12	CRC Checker Enable	R/W	1 = Enable CRC Checker to detect CRC errors on packets of any size (1-byte or more) 0 = Normal operation (CRC checker only detects CRC errors on packets of at least 72-bytes)	0

Table 111: Pattern Generator Control Register (Page 10h ~ 1Fh: Address 34h ~ 35h) (Cont.)

Bit	Name	R/W	Description	Default
11:9	IPG Select	R/W	000 = Invalid 001 = IPG of 6-bytes 010 = IPG of 10-bytes 011 = IPG of 14-bytes 100 = IPG of 18-bytes 101 = IPG of 22-bytes 110 = IPG of 26-bytes 111 = IPG of 30-bytes	100
8:3	Packet Size	R/W	000000 = Invalid 000001 = 256-bytes 000010 = 512-bytes 000011 = 768-bytes 000100 = 1024-bytes … … 111111 = 16,128-bytes	000100
2	Single Pass Mode	R/W	1 = Only send 1 packet and stop 0 = Send packets while bit 1 of this register is set	0
1	Run Pattern Generator	R/W	1 = A rising edge on this bit while the pattern generator is in the idle state will start sending packets. If the single pass mode is set, then a single packet will be sent and the idle state will be entered. If the single pass mode is not set, then packets will be sent until this bit is cleared. At this point, the current packet will finish transmitting and then enter the idle state. ***Note:*** A valid link must be established prior to sending packets. 0 = Do not send packet	0
0	Select Pattern Generator Data	R/W	1 = Send idles or pattern generator data into transmit FIFO (Ignore MAC transmit data) 0 = Normal operation	0

Pattern Generator Control Register (Page 10H ~ 1Fh: Address 36h ~ 37h)

Table 112: Pattern Generator Control Register (Page 10h ~ 1Fh: Address 36h ~ 37h)

Bit	Name	R/W	Description	Default
15:4	Reserved	R/W	Write as 0, Ignore on read.	000h
3	Pattern Generator Active	RO	1 = Pattern generator is still sending packets 0 = Pattern generator is idle	0

Table 112: Pattern Generator Control Register (Page 10h ~ 1Fh: Address 36h ~ 37h)

Bit	Name	R/W	Description	Default
2:0	Pattern Generator FSM	RO	000 = Idle 001 = Transmit preamble 011 = Transmit SFD 010 = Transmit data 110 = Transmit CRC 100 = IPG 101 = IPG 2 (allows FSM to be grey-coded	000

Force Transmit 1 Register (Page 10h ~ 1Fh: Address 3Ah ~ 3Bh)

Table 113: Pattern Generator Control Register (Page 10h ~ 1Fh: Address 36h ~ 37h)

Bit	Name	R/W	Description	Default
15:11	Reserved	R/W	Write as 0, ignore on read.	00h
10	Force Transmit	R/W	This bit enables a test transmit mode of two alternating patterns. Additionally, can be used in conjunction with the Transmit Idle Test via "SerDes/SGMII Control 2 Register (Page 10h ~ 17h: Address 22h)" bit[13]. 1 = Provide alternating bit[9:0] from this register and "Force Transmit 2 Register (Page 10h ~ 17h: Address 3Ch)" bit[9:0] to SerDes analog register. 0 = Normal operation	0
9:0	Force Transmit Data 1	R/W	Value in this register will be provided to SerDes analog transmitter every other clock cycle when bit[10] is set.	17Ch

Force Transmit 2 Register (Page 10h ~ 1Fh: Address 3Ch ~ 3Dh)

Table 114: Force Transmit 1 Register (Page 10h ~ 1Fh: Address 3Ah ~ 3Bh)

Bit	Name	R/W	Description	Default
15:10	Reserved	R/W	Write as 0, ignore on read.	00h
9:0	Force Transmit Data 2	R/W	Value in this register will be provided to SerDes analog transmitter every other clock cycle when "Force Transmit 1 Register (Page 10h ~ 17h: Address 3Ah)" bit[10] is set.	

Block Address (Pages 10h–1Fh: Address 3Eh ~ 3Fh)

Table 115: Block Address (Pages 10h–1Fh: Address 3Eh ~ 3Fh)

Bit	Name	R/W	Description	Default
15:4	Reserved	RO	Reserved. Write 0, ignore read.	0x000

Table 115: Block Address (Pages 10h–1Fh: Address 3Eh ~ 3Fh)

Bit	Name	R/W	Description	Default
3:0	BLK_NO	R/W	Registers 00–0fh and 1fh do not use block addressing and are fixed. Block 0 and Block 1 selected via these bits. 0000 = Valid (block 0). 0001 = Valid (block 1). 0010–1111 = Reserved for future implementation.	0x0

QoS Registers

Table 116: QoS Registers (Page 30h)

Address	Bits	Description
00h	8	QoS Global Control Register
01h–02h	16	QoS Threshold Control Register
03h	–	Reserved
04h–07h	32	QoS 1P Enable Register
08h–0Bh	32	QoS DiffServ Enable Register
0Ch–0Fh	8	Reserved
10h–13h	32	IEEE Standard 802.1P Priority Map Register
14h–2Fh	32	Reserved
30h–35h	48	DiffServ Priority Map 0 Register
36h–3Bh	48	DiffServ Priority Map 1 Register
3Ch–41h	48	DiffServ Priority Map 2 Register
42h–47h	48	DiffServ Priority Map 3 Register
48h–4Fh	–	Reserved
50h–51h	16	QoS RX Port 0 Control Register
52h–53h	16	QoS RX Port 1 Control Register
54h–55h	16	QoS RX Port 2 Control Register
56h–57h	16	QoS RX Port 3 Control Register
58h–59h	16	QoS RX Port 4 Control Register
5Ah–5Bh	16	QoS RX Port 5 Control Register
5Ch–5Dh	16	QoS RX Port 6 Control Register
5Eh–5Fh	16	QoS RX Port 7 Control Register
60h–61h	16	QoS RX Port 8 Control Register
62h–63h	16	QoS RX Port 9 Control Register
64h–65h	16	QoS RX Port 10 Control Register
66h–67h	16	QoS RX Port 11 Control Register
68h–69h	16	QoS RX Port 12 Control Register
6Ah–6Bh	16	QoS RX Port 13 Control Register
6Ch–6Dh	16	QoS RX Port 14 Control Register

Table 116: QoS Registers (Page 30h) (Cont.)

Address	Bits	Description
6Eh–6Fh	16	QoS RX Port 15 Control Register
70h–71h	16	QoS RX Port 16 Control Register
72h–7Fh	–	Reserved
80h	8	QoS TX Control Register
81h	8	TX Queue 0 Weight Register
82h	8	TX Queue 1 Weight Register
83h	8	TX Queue 2 Weight Register
84h	8	TX Queue 3 Weight Register
85h–87h	–	Reserved
88h–8Bh	32	EtherType Priority Control Register
8Ch–9Fh	–	Reserved
A0h–A3h	32	Enable Traffic Priority Remap Control Register
A4h	8	Traffic Priority Remap Register
A2h–FEh	–	Reserved
FF	8	Page Register

QoS Global Control Register(Page 30h: Address 00h)

Table 117: QoS Global Control Register (Page 30h: Address 00h)

Bit	Name	R/W	Description	Default
7	Reserved	R/W	Reserved	0
6	Port Base QOS En	R/W	Port-Based QoS Enable. When set, priority of packet of individual port can be assigned by default priority bits in Default 802.1Q Tag Register (Page: 34h Address 10h–31h). If port-based QoS is enabled, it overrides all other priorities except the case of qos_layer_sel = 11.	Strap pin QOS_EN
5:4	Reserved	R/W	Reserved	0
3:2	QOS_LAYER_SEL	R/W	QoS IP Layer/MAC Layer Selection. 2’b00: Layer 2 QoS only. Select IEEE Standard 802.1p if enabled and the RX frame is tagged; otherwise, select MAC-based. 2’b01: IP QoS only. Select DiffServ if enabled; otherwise, priority = 0. 2’b10: If (IP), then IP QOS ELSE LAYER2 QOS. For IP frame, select DiffServ (0 if DiffServ is off); for L2 frames, select IEEE Standard 802.1p if enabled and tagged; otherwise, MAC-based. 2’b11: Max Priority of All QOS algorithm. Select max priority from port-based, DiffServ if enabled, IEEE Standard 802.1p if enabled.	0

Table 117: QoS Global Control Register (Page 30h: Address 00h)

Bit	Name	R/W	Description	Default
1:0	Reserved	R/W	Reserved	0

QoS Threshold Control Register (Page 30h: Address 01h–02h)

Table 118: QoS Threshold Control Register (Page 30h: Address 01h–02h)

Bit	Name	R/W	Description	Default
15:14	Reserved	R/W	Reserved	0
13	EN_AUTOSET_ QOSREG	R/W	Enable Auto Set QoS Threshold register. When QoS mode is changed, the threshold value will be reload automatically if EN_AUTOSET_QOSREG.	1
12:0	Reserved	RO	Reserved	0

QoS 1P Enable Register (Page 30h: Address 04h–07h)

Table 119: QoS 1P Enable Register (Page 30h: Address 04h–07h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	QOS_EN_802_1P	R/W	Enable IEEE Standard 802.1p priority for individual ports. Bits 16:0 = Port 16–Port 0.	0

QoS DiffServ Enable Register (Page 30h: Address 08h–0Bh)

Table 120: QoS DiffServ Enable Register (Page 30h: Address 08h–0Bh)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	QOS_EN_DIFFSERV	R/W	Enable DiffServ priority for individual ports. Bits 16:0 = Port 16–Port 0.	0

802.1P/1Q Priority Map Register (Page 30h: Address 10h–13h)

Table 121: 1P/1Q Priority Map Register (Page 30h: Address 10h–13h)

Bit	Name	R/W	Description	Default
31:24	Reserved	RO	Reserved	8’b0
23:21	802.1P Tag 111 Priority Map	R/W	802.1P Priority Tag field == 111 to Priority ID map Register	3’b0
20:18	802.1P Tag 110 Priority Map	R/W	802.1P Priority Tag field == 110 to Priority ID map Register	3’b0

Table 121: 1P/1Q Priority Map Register (Page 30h: Address 10h–13h) (Cont.)

Bit	Name	R/W	Description	Default
17:15	802.1P Tag 101 Priority Map	R/W	802.1P Priority Tag field == 101 to Priority ID map Register	3'b0
14:12	802.1P Tag 100 Priority Map	R/W	802.1P Priority Tag field == 100 to Priority ID map Register	3'b0
11:9	802.1P Tag 011 Priority Map	R/W	802.1P Priority Tag field == 011 to Priority ID map Register	3'b0
8:6	802.1P Tag 010 Priority Map	R/W	802.1P Priority Tag field == 010 to Priority ID map Register	3'b0
5:3	802.1P Tag 001 Priority Map	R/W	802.1P Priority Tag field == 001 to Priority ID map Register	3'b0
2:0	802.1P Tag 000 Priority Map	R/W	802.1P Priority Tag field == 000 to Priority ID map Register	3'b0

DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)

Table 122: DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)

Bit	Name	R/W	Description	Default
47:45	DiffServ DSCP 001111 Priority Map	R/W	DiffServ DSCP == 001111 to Priority ID map Register	3'b0
44:42	DiffServ DSCP 001110 Priority Map	R/W	DiffServ DSCP == 001110 to Priority ID map Register	3'b0
41:39	DiffServ DSCP 001101 Priority Map	R/W	DiffServ DSCP == 001101 to Priority ID map Register	3'b0
38:36	DiffServ DSCP 001100 Priority Map	R/W	DiffServ DSCP== 001100 to Priority ID map Register	3'b0
35:33	DiffServ DSCP 001011 Priority Map	R/W	DiffServ DSCP== 001011 to Priority ID map Register	3'b0
32:30	DiffServ DSCP 001010 Priority Map	R/W	DiffServ DSCP== 001010 to Priority ID map Register	3'b0
29:27	DiffServ DSCP 001001 Priority Map	R/W	DiffServ DSCP== 001001 to Priority ID map Register	3'b0
26:24	DiffServ DSCP 001000 Priority Map	R/W	DiffServ DSCP== 001000 to Priority ID map Register	3'b0
23:21	DiffServ DSCP 000111 Priority Map	R/W	DiffServ DSCP== 000111 to Priority ID map Register	3'b0
20:18	DiffServ DSCP 000110 Priority Map	R/W	DiffServ DSCP== 000110 to Priority ID map Register	3'b0
17:15	DiffServ DSCP 000101 Priority Map	R/W	DiffServ DSCP== 000101 to Priority ID map Register	3'b0
14:12	DiffServ DSCP 000100 Priority Map	R/W	DiffServ DSCP== 000100 to Priority ID map Register	3'b0
11:9	DiffServ DSCP 000011 Priority Map	R/W	DiffServ DSCP== 000011 to Priority ID map Register	3'b0

Table 122: DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h) (Cont.)

Bit	Name	R/W	Description	Default
8:6	DiffServ DSCP 000010 Priority Map	R/W	DiffServ DSCP== 000010 to Priority ID map Register	3'b0
5:3	DiffServ DSCP 000001 Priority Map	R/W	DiffServ DSCP== 000001 to Priority ID map Register	3'b0
2:0	DiffServ DSCP 000000 Priority Map	R/W	DiffServ DSCP== 000000 to Priority ID map Register	3'b0

DiffServ Priority Map 1 Register (Page 30h: Address 36h–3Bh)

Table 123: DiffServ Priority Map 1 Register (Page 30h: Address 36h–3Bh)

Bit	Name	R/W	Description	Default
47:45	DiffServ DSCP 011111 Priority Map	R/W	DiffServ DSCP== 011111 to Priority ID map Register	3'b0
44:42	DiffServ DSCP 011110 Priority Map	R/W	DiffServ DSCP== 011110 to Priority ID map Register	3'b0
41:39	DiffServ DSCP 011101 Priority Map	R/W	DiffServ DSCP== 011101 to Priority ID map Register	3'b0
38:36	DiffServ DSCP 011100 Priority Map	R/W	DiffServ DSCP== 011100 to Priority ID map Register	3'b0
35:33	DiffServ DSCP 011011 Priority Map	R/W	DiffServ DSCP== 011011 to Priority ID map Register	3'b0
32:30	DiffServ DSCP 011010 Priority Map	R/W	DiffServ DSCP== 011010 to Priority ID map Register	3'b0
29:27	DiffServ DSCP 011001 Priority Map	R/W	DiffServ DSCP== 011001 to Priority ID map Register	3'b0
26:24	DiffServ DSCP 011000 Priority Map	R/W	DiffServ DSCP== 011000 to Priority ID map Register	3'b0
23:21	DiffServ DSCP 010111 Priority Map	R/W	DiffServ DSCP== 010111 to Priority ID map Register	3'b0
20:18	DiffServ DSCP 010110 Priority Map	R/W	DiffServ DSCP== 010110 to Priority ID map Register	3'b0
17:15	DiffServ DSCP 010101 Priority Map	R/W	DiffServ DSCP== 010101 to Priority ID map Register	3'b0
14:12	DiffServ DSCP 010100 Priority Map	R/W	DiffServ DSCP== 010100 to Priority ID map Register	3'b0
11:9	DiffServ DSCP 010011 Priority Map	R/W	DiffServ DSCP== 010011 to Priority ID map Register	3'b0
8:6	DiffServ DSCP 010010 Priority Map	R/W	DiffServ DSCP== 010010 to Priority ID map Register	3'b0
5:3	DiffServ DSCP 010001 Priority Map	R/W	DiffServ DSCP== 010001 to Priority ID map Register	3'b0
2:0	DiffServ DSCP 010000 Priority Map	R/W	DiffServ DSCP== 010000 to Priority ID map Register	3'b0

DiffServ Priority Map 2 Register (Page 30h: Address 3Ch–41h)

Table 124: DiffServ Priority Map 2 Register (Page 30h: Address 3Ch–41h)

Bit	Name	R/W	Description	Default
47:45	DiffServ DSCP 101111 Priority Map	R/W	DiffServ DSCP== 101111 to Priority ID map Register	3'b0
44:42	DiffServ DSCP 101110 Priority Map	R/W	DiffServ DSCP== 101110 to Priority ID map Register	3'b0
41:39	DiffServ DSCP 101101 Priority Map	R/W	DiffServ DSCP== 101101 to Priority ID map Register	3'b0
38:36	DiffServ DSCP 101100 Priority Map	R/W	DiffServ DSCP== 101100 to Priority ID map Register	3'b0
35:33	DiffServ DSCP 101011 Priority Map	R/W	DiffServ DSCP== 101011 to Priority ID map Register	3'b0
32:30	DiffServ DSCP 101010 Priority Map	R/W	DiffServ DSCP== 101010 to Priority ID map Register	3'b0
29:27	DiffServ DSCP 101001 Priority Map	R/W	DiffServ DSCP== 101001 to Priority ID map Register	3'b0
26:24	DiffServ DSCP 101000 Priority Map	R/W	DiffServ DSCP== 101000 to Priority ID map Register	3'b0
23:21	DiffServ DSCP 100111 Priority Map	R/W	DiffServ DSCP== 100111 to Priority ID map Register	3'b0
20:18	DiffServ DSCP 100110 Priority Map	R/W	DiffServ DSCP== 100110 to Priority ID map Register	3'b0
17:15	DiffServ DSCP 100101 Priority Map	R/W	DiffServ DSCP== 100101 to Priority ID map Register	3'b0
14:12	DiffServ DSCP 100100 Priority Map	R/W	DiffServ DSCP== 100100 to Priority ID map Register	3'b0
11:9	DiffServ DSCP 100011 Priority Map	R/W	DiffServ DSCP== 100011 to Priority ID map Register	3'b0
8:6	DiffServ DSCP 100010 Priority Map	R/W	DiffServ DSCP== 100010 to Priority ID map Register	3'b0
5:3	DiffServ DSCP 100001 Priority Map	R/W	DiffServ DSCP== 100001 to Priority ID map Register	3'b0
2:0	DiffServ DSCP 100000 Priority Map	R/W	DiffServ DSCP== 100000 to Priority ID map Register	3'b0

DiffServ Priority Map 3 Register(Page 30h: Address 42h–47h)

Table 125: DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h)

Bit	Name	R/W	Description	Default
47:45	DiffServ DSCP 111111 Priority Map	R/W	DiffServ DSCP== 111111 to Priority ID map Register	3'b0
44:42	DiffServ DSCP 111110 Priority Map	R/W	DiffServ DSCP== 111110 to Priority ID map Register	3'b0

Table 125: DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h) (Cont.)

Bit	Name	R/W	Description	Default
41:39	DiffServ DSCP 111101 Priority Map	R/W	DiffServ DSCP== 111101 to Priority ID map Register	3'b0
38:36	DiffServ DSCP 111100 Priority Map	R/W	DiffServ DSCP== 111100 to Priority ID map Register	3'b0
35:33	DiffServ DSCP 111011 Priority Map	R/W	DiffServ DSCP== 111011 to Priority ID map Register	3'b0
32:30	DiffServ DSCP 111010 Priority Map	R/W	DiffServ DSCP== 111010 to Priority ID map Register	3'b0
29:27	DiffServ DSCP 111001 Priority Map	R/W	DiffServ DSCP== 111001 to Priority ID map Register	3'b0
26:24	DiffServ DSCP 111000 Priority Map	R/W	DiffServ DSCP== 111000 to Priority ID map Register	3'b0
23:21	DiffServ DSCP 110111 Priority Map	R/W	DiffServ DSCP== 110111 to Priority ID map Register	3'b0
20:18	DiffServ DSCP 110110 Priority Map	R/W	DiffServ DSCP== 110110 to Priority ID map Register	3'b0
17:15	DiffServ DSCP 110101 Priority Map	R/W	DiffServ DSCP== 110101 to Priority ID map Register	3'b0
14:12	DiffServ DSCP 110100 Priority Map	R/W	DiffServ DSCP== 110100 to Priority ID map Register	3'b0
11:9	DiffServ DSCP 110011 Priority Map	R/W	DiffServ DSCP== 110011 to Priority ID map Register	3'b0
8:6	DiffServ DSCP 110010 Priority Map	R/W	DiffServ DSCP== 110010 to Priority ID map Register	3'b0
5:3	DiffServ DSCP 110001 Priority Map	R/W	DiffServ DSCP== 110001 to Priority ID map Register	3'b0
2:0	DiffServ DSCP 110000 Priority Map	R/W	DiffServ DSCP== 110000 to Priority ID map Register	3'b0

QoS RX Port N (0–16) Control Register(Page 30h: Address 50h–71h)

Table 126: QoS Port Control N Register (Page 30h: Address 50h–71h)

Bit	Name	R/W	Description	Default
15:14	Pri_111_to_QID	R/W	Priority ID 111 mapped to TX Queue ID	if (N ==0~7 && strap qos_en) 2'b11 else 2'b00
13:12	Pri_110_to_QID	R/W	Priority ID 110 mapped to TX Queue ID	if (N ==0~7 && strap qos_en) 2'b11 else 2'b00
11:10	Pri_101_to_QID	R/W	Priority ID 101 mapped to TX Queue ID	if (N ==0~7 && strap qos_en) 2'b11 else 2'b00
9:8	Pri_100_to_QID	R/W	Priority ID 100 mapped to TX Queue ID	if (N ==0~7 && strap qos_en) 2'b11 else 2'b00
7:6	Pri_011_to_QID	R/W	Priority ID 011 mapped to TX Queue ID	if (N ==0~7 && strap qos_en) 2'b11 else 2'b00

Table 126: QoS Port Control N Register (Page 30h: Address 50h–71h) (Cont.)

Bit	Name	R/W	Description	Default
5:4	Pri_010_to_QID	R/W	Priority ID 010 mapped to TX Queue ID	if (N ==0~7 && strap qos_en) 2'b11 else 2'b00
3:2	Pri_001_to_QID	R/W	Priority ID 001 mapped to TX Queue ID	if (N ==0~7 && strap qos_en) 2'b11 else 2'b00
1:0	Pri_000_to_QID	R/W	Priority ID 000 mapped to TX Queue ID	if (N ==0~7 && strap qos_en) 2'b11 else 2'b00

QoS TX Control Register (Page 30h: Address 80h)

Table 127: QoS TX Control Register (Page 30h: Address 80h)

Bit	Name	R/W	Description	Default
7:5	Reserved	RO	Reserved	0
4	HQ_Preempt	R/W	High Queue Preempt. When enabled, the highest queue will be served first whenever it has a frame. If the highest queue is empty, it sends frames from the other lower queues in the weight round-robin fashion using the programmed weights.	0
3:2	QOS_MODE	R/W	QoS Mode. 2'b00: Single Queue (No QoS) 2'b01: Two Queues Mode 2'b10: Three Queues Mode 2'b11: Four Queues Mode The bits are used for Multiple Queue Flow Control Threshold Setting.	{qos_en_strap, qos_en_strap}
1:0	Reserved	R/W	Reserved	0

Queue N (0–3) Weight Register (Page 30h: Address 81h–84h)

Table 128: Queue N Weight Register (Page 30h: Address 81h–84h)

Bit	Name	R/W	Description	Default
7:0	Service Weight	R/W	Queue N Weight Register. Set to reserve the Service Weight of Queue N.	The default value = 1 (Q0) • 'd1 for Q0 • 'd2 for 1 (Q0) • 'd4 for Q2 • 'd8 for Q3

EtherType Priority Control Register (Page 30h: Address 88h–8Bh)

Table 129: EtherType Priority Control Register (Page 30h: Address 88h–8Bh)

Bit	Name	R/W	Description	Default
31:19	Reserved	RO	Reserved	0
18	EN_ETHERTYPE_PRI	R/W	Enable EtherType priority QoS function.	0
17:16	PRI_ETHERTYPE_QUEUE	R/W	Queue number for the EtherType priority packets.	0
15:0	PRI_ETHERTYPE	R/W	Priority EtherType register. The EtherType value for the priority packets. The packet with matched EtherType is forwarded to the queue specified in PRI_ETHERTYPE_QUEUE.	0

Enable Traffic Priority Remap Control Register (Page 30h: Address A0h–A3h)

Table 130: Enable Traffic Priority Remap Control Register (Page 30h: Address A0h–A3h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	EN_TRAFFIC_PRI_REMAP	R/W	Enable Traffic Priority Remap. Bits 16:0 = Port 16–Port 0. When Enabled, the Priority of Different traffic will remap according to Traffic Priority Remap Register [Page 30H, Offset A4H].	0

Traffic Priority Remap Register (Page 30h: Address A4h)

Table 131: Traffic Priority Remap Register (Page 30h: Address A4h)

Bit	Name	R/W	Description	Default
7:6	Multicast Remap Priority	R/W	Multicast Traffic Remap Priority Queue ID map. (Except Reserved Multicast frame.)	0
5:4	Unicast Remap Priority	R/W	Unicast Traffic Remap Priority Queue ID map.	0
3:2	DLF Remap Priority	R/W	Destination Lookup Failed Traffic Remap Priority Queue ID map.	0
1:0	Broadcast	R/W	BroadcastTraffic Remap Priority Queue ID map.	0

Port-Based VLAN Control Registers

Table 132: Page 31h Port-based VLAN Registers

Address	Bits	Description
00h–03h	32	Port 0 VLAN Register
04h–07h	32	Port 1 VLAN Register
08h–0Bh	32	Port 2 VLAN Register
0Ch–0Fh	32	Port 3 VLAN Register
10h–13h	32	Port 4 VLAN Register
14h–17h	32	Port 5 VLAN Register
18h–1Bh	32	Port 6 VLAN Register
1Ch–1Fh	32	Port 7 VLAN Register
20h–23h	32	Port 8 VLAN Register
24h–27h	32	Port 9 VLAN Register
28h–2Bh	32	Port 10 VLAN Register
2Ch–2Fh	32	Port 11 VLAN Register
30h–33h	32	Port 12 VLAN Register
34h–37h	32	Port 13 VLAN Register
38h–3Bh	32	Port 14 VLAN Register
3Ch–3Fh	32	Port 15 VLAN Register
40h–43h	32	Port 16 VLAN Register

Port VLAN Control Register (Page 31h: Address 00h–43h)

Table 133: Port VLAN Control Register (Pages: 31h, Address 0h–43h)

Blt	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	Forwarding Mask[16:0]	R/W	Per-bit per port VLAN forwarding vector. A bit mask corresponding to the physical ports on the chip. Set the corresponding bit to 1 to enable forwarding to the egress port. Set the corresponding bit to 0 inhibit the forwarding. Bits 0–16: Port 0–16	1FFFFh

Trunking Registers

Table 134: Trunking Registers (Page 32h)

Address	Bits	Description
01h	8	MAC Trunk Control Register

Table 134: Trunking Registers (Page 32h) (Cont.)

Address	Bits	Description
02h–0Fh	112	Reserved
10h–11h	16	Reserved
12h–13h	16	Reserved
14h–15h	16	Reserved
16h–17h	16	Reserved
18h–19h	16	Reserved
1Ah–1Bh	16	Reserved
1Ch–1Dh	16	Reserved
1Eh–1Fh	16	Reserved
20h–21h	16	Reserved
22h–23h	16	Reserved
24h–25h	16	Reserved
26h–27h	16	Reserved
28h–2Fh	64	Reserved
30h–31h	16	Reserved
32h–33h	16	Reserved
34h–35h	16	Reserved
36h–37h	16	Reserved
38h–39h	16	Reserved
3Ah–3Bh	16	Reserved
3Ch–3Dh	16	Reserved
3Eh–3Fh	16	Reserved
40h–41h	16	Reserved
42h–43h	16	Reserved
44h–45h	16	Reserved
46h–47h	16	Reserved
48h–4Fh	64	Reserved
50h–51h	16	Reserved
52h–53h	16	Reserved
54h–55h	16	Reserved
56h–57h	16	Reserved
58h–59h	16	Reserved
5Ah–5Bh	16	Reserved
5Ch–5Dh	16	Reserved
5Eh–5Fh	16	Reserved
60h–61h	16	Reserved
62h–63h	16	Reserved
64h–65h	16	Reserved
66h–67h	16	Reserved

Table 134: Trunking Registers (Page 32h) (Cont.)

Address	Bits	Description
68h–6Fh	64	Reserved
70h–71h	16	Reserved
72h–73h	16	Reserved
74h–75h	16	Reserved
76h–77h	16	Reserved
78h–79h	16	Reserved
7Ah–7Bh	16	Reserved
7Ch–7Dh	16	Reserved
7Eh–7Fh	16	Reserved
80h–81h	16	Reserved
82h–83h	16	Reserved
84h–85h	16	Reserved
86h–87h	16	Reserved
88h–8Fh	64	Reserved
90h–93h	32	Trunk Group 0 in chip0
94h–97h	32	Trunk Group 1 in chip0
98h–9Bh	32	Trunk Group 2 in chip0
9Ch–9Fh	32	Trunk Group 3 in chip0
A0–FEh	–	Reserved
FF	8	Page Register

MAC Trunking Control Register (Page 32h: Address 01h)

Table 135: MAC Trunk Control Register (Pages: 32h, Address 1h)

Bit	Name	R/W	Description	Default
7:4	Reserved	RW	Reserved	4’b0
3	Enable MAC-based trunking	RW	Enable MAC trunking. Up to four trunk groups are supported. A trunk group can support up to eight ports (Ports[15:0]). When more than 8 bit are set in the trunking group register, the low 8 bits are valid settings.	0
2	Reserved	RW	Reserved	0
1:0	MAC-based trunking hash index selection	RW	00: Use hash (DA ^ SA) to generate index (default = 0.) 01: Use hash (DA) to generate index. 10: Use hash (SA) to generate index.	0

Trunking Group Register (Page 32h: Address 90h–9Fh)

Table 136: Trunk Group Register [0:3] (Pages: 32h, Address 90h–9Fh)

Bit	Name	R/W	Description	Default
31:16	Reserved	RO	Reserved	0
15:0	TRNK_GRP	R/W	Per-bit per port TRUNK Group Vector in chip 0. A bit mask corresponding to the physical ports on the chip. For physical ports which belong to the same trunk, the corresponding bit should be set to 1 (minimum of two ports and maximum of eight ports per trunk). Bits 0–15 stand for Ports 0–15 in chip 0 as trunk port.	0

IEEE Standard 802.1Q VLAN Registers

Table 137: QoS Registers (Page 34h)

Address	Bits	Description
00h	8	Global Control 0 Register
01h	8	Global Control 1Register
02h	8	Global Control 2 Register
03h–06h	32	Global Control 3 Register
07h	8	Global Control 4 Register
08h	8	Global Control 5 Register
09h	8	Global Control 6 Register
09h–0Bh	–	Reserved
0Ch–0Fh	32	New Priority Map Register
10h–11h	16	Default IEEE Standard 802.1Q Tag Port 0
12h–13h	16	Default IEEE Standard 802.1Q Tag Port 1
14h–15h	16	Default IEEE Standard 802.1Q Tag Port 2
16h–17h	16	Default IEEE Standard 802.1Q Tag Port 3
18h–19h	16	Default IEEE Standard 802.1Q Tag Port 4
1Ah–1Bh	16	Default IEEE Standard 802.1Q Tag Port 5
1Ch–1Dh	16	Default IEEE Standard 802.1Q Tag Port 6
1Eh–1Fh	16	Default IEEE Standard 802.1Q Tag Port 7
20h–21h	16	Default IEEE Standard 802.1Q Tag Port 8
22h–23h	16	Default IEEE Standard 802.1Q Tag Port 9
24h–25h	16	Default IEEE Standard 802.1Q Tag Port 10
26h–27h	16	Default IEEE Standard 802.1Q Tag Port 11
28h–29h	16	Default IEEE Standard 802.1Q Tag Port 12
2Ah–2Bh	16	Default IEEE Standard 802.1Q Tag Port 13
2Ch–2Dh	16	Default IEEE Standard 802.1Q Tag Port 14
2Eh–2Fh	16	Default IEEE Standard 802.1Q Tag Port 15
30h–31h	16	Default IEEE Standard 802.1Q Tag Port 16

Global Control 0 Register (Page 34h: Address 00h)

Table 138: Global Control 0 Register (Pages 34h: Address 00h)

Bit	Name	R/W	Description	Default
7	EN_1QVLAN	RW	When set to 1, the IEEE Standard 802.1Q VLAN function will be enabled.	0

Table 138: Global Control 0 Register (Pages 34h: Address 00h) (Cont.)

Bit	Name	R/W	Description	Default
6:5	VLAN_LEARN_MODE	RW	00: SVL (Shared VLAN Learning Mode), MAC is used to hash to generate the index to ARL table. 11: IVL (Independent VLAN Learning Mode), MAC and VID are used to hash to generate the index to ARL table. 01: Illegal setting. 10: Illegal setting.	11
4	Reserved	RW	Reserved	0
3:2	1QFRAME_CNTL	RW	00: No change. 01: Change priority (4 bits). 10: Change VID (12 bits). 11: Change priority and VID (16 bits).	00
1:0	1PFRAME_CNTL	RW	00: Illegal setting. 01: Illegal setting. 10: Change VID (12 bits). 11: Change priority and VID (16 bits).	2h

Global Control 1 Register (Page 34h: Address 01h)

Table 139: Global Control 1 Register (Pages 34h: Address 01h)

Bit	Name	R/W	Description	Default
7	Reserved	RW	Reserved	0
6	Enable IPMC Bypass V Untagmap	RW	When asserted will not check the IPMC frame with V_UNTAGMAP.	0
5	Enable IPMC Bypass V Fwdmap	RW	When asserted will not check IPMC frame with V_FWDMAP.	0
4	Reserved	RW	Reserved	Must be 0
3	Enable RSV Mcast V Untagmap	RW	When asserted, reserved multicast frames (except GMRP and GVRP) are checked by V_UNTAGMAP.	0
2	Enable RSV Mcast V Fwdmap	RW	When asserted, reserved multicast frames (except GMRP and GVRP) are checked by V_FWDMAP.	0
1	Reserved	RW	Reserved	Must be 1
0	Enable Special Entry VLAN Check	RW	If a special entry MAC address is detected, bypass ARL checking. The register provides the forwarding map. 0: Bypass all VLAN checking (tagging, V_FWDMAP, V_UNTAGMAP). 1: Two special entries (group0 and group1) address frame follow two VLAN rules. (tagging, V_UNTAGMAP).	0

Global Control 2 Register (Page 34h: Address 02h)

Table 140: Global Control 2 Register (Pages 34h: Address 02h)

Bit	Name	R/W	Description	Default
7	Enable Remap Priority Field	RW	When asserted, the PRI_FIELD (3 bits) in the ingress frame (IEEE Standard 802.1Q frame or priority-tagged frame) will be remapped to a new value based on re_map_reg[23:0]. The CFI bit is preserved as original frame. When this feature is enabled, control0[1:0] has to be either 01 or 11, and control0[3:2] has to be either 01 or 11. The managed MII port does not support V_tagging, so it cannot support priority remapping.	0
6	EN_GMRP_GVRP_UNTAGMAP	RW	When set to 1, GMRP, GVRP will be checked by V_UNTAGMAP. This rule does not apply to the MII_manage port.	0
5	EN_GMRP_GVRP_V_FWDMAP	RW	When set to 1, GMRP, GVRP will be checked by V_FWDMAP. This rule does not apply to the MII_manage port.	0
4	Reserved	RO	Reserved	Must be 1
3:2	Reserved	RO	Reserved	0
1:0	Reserved	RO	Reserved	0

Global Control 3 Register (Page 34h: Address 03h)

Table 141: Global Control 3 Register (Pages 34h: Address 03h–06h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16:0	Enable Drop Non 1Q frame	RW	When enabled, any non_1Q frame is dropped by this port (ports 16–0, respectively).	0

Global Control 4 Register (Page 34h: Address 07h)

Table 142: Global Control 4 Register (Pages 34: Address 07h)

Bit	Name	R/W	Description	Default
7:6	ingress_VID_check	RW	00: forward ingress VID violation frame (destination port is not in v_fwdmap). But do not learn in ARL table. 01: Drop frame if frame has VID violation. 10: Do not check ingress VID violation. This rule does not apply to the MII_management port.	00

Table 142: Global Control 4 Register (Pages 34: Address 07h) (Cont.)

Bit	Name	R/W	Description	Default
5	EN_MANAGE_RECEIVE_GVRP	RW	When set to 1. management port (the port with the CPU) will be the destination port of the GVRP frame.	0
4	EN_MANAGE_RECEIVE_GMRP	RW	When set to 1, management port (the port with the CPU) will be the destination port of the GMRP frame.	0
3	Reserved	RO	Reserved	Must be 0
2:1	Reserved	RO	Reserved	0
0	Reserved	RO	Reserved	Must be 0

Global Control 5 Register (Page 34h: Address 08h)

Table 143: Global Control 5 Register (Pages 34h: Address 08h)

Bit	Name	R/W	Description	Default
7	Reserved	RO	Reserved	0
6	EN_PRESERV_NON_1Q_FRAME	R/W	EN_PRESERV_NON_1Q_FRAME: (default 0) When enabled, it preserves untagged frame as untagged frame at TX regardless of untag map in VLAN table, and preserves priority 802.1p-tagged frames as priority-tagged frames at TX if untag map in VLAN Table is 0, but otherwise untag priority tag.	0
5	EN_PRESERV_1P_TAG	R/W	EN_PRESERV_1P_TAG. To enable this, en_preserv_non_1q_frame must be also enabled.When enabled, it preserves priority 802.1p-tagged frames as priority-tagged frames at TX even if untag map in VLAN table is 1.	0
4	Reserved	RO	Reserved	0
3	DROP_VTABLE_MISS	RW	When set to 1, a frame with V_table miss will be dropped. When set to 0, a frame with V_table miss will be flooded.	0
2	Reserved	RW	Reserved	0
1	EN_MANAGE_RX_BYPASS_CRCCHK	RW	When set to 1, The management port (MII) with CPU on it will ignore any CRC (BRCM tag frame, or Ethernet frame). When set to 0: The management port will check both CRC. With this option, the CPU does not need to calculate CRC for BRCM frame.	0
0	Enable TX port CRC generation	RW	When en_1QVLAN =0 (default=0). 0: TXport will not regenerate CRC when en_1QVALN = 0. 1: TXport will regenerate CRC even when en_1QVLAN = 0.	0

New Priority Map Register (Page 34h: Address 0Ch-0Fh)

Table 144: New Priority Map Register (Pages 34h: Address 0C–0Fh)

Bit	Name	R/W	Description	Default
31:24	Reserved	RO	Reserved	0
23:0	RE_MAP_REG	RW	When: 1) Global Control 2 Register (Page 34h: Address 02h) bit [7]=1, and 2) Global Control 0 Register(Page 34h : Address 00h) bit [0] = 1 3) Global Control 0 Register(Page 34h : Address 00h) bit [2] = 1 remap the original frames's priority to the one in RE_MAP_REG[23:0]. The mapping rules are: OLD NEW ---------- 000 re_map_reg[2:0] 001 re_map_reg[5:3] 010 re_map_reg[8:6] 011 re_map_reg[11:9] 100 re_map_reg[14:12] 101 re_map_reg[17:15] 110 re_map_reg[20:18] 111 re_map_reg[23:21] If the incoming frame is a PRI_TAGGED frame or tagged frame, then its priority field will be remapped if the remapping feature is enabled. If the incoming frame is an untagged frame, then the priority in DEFAULT_TAG will be used as the new priority.	0

Port N (0–16) Default 802.1Q Tag Register (Page 34h: Address 10h–31h)

Table 145: Port N Default 802.1Q Tag Register (Pages 34h: Address 10h–31h)

Bit	Name	R/W	Description	Default
15:13	Pri	R/W	Default Priority Bit. When the incoming packet is a non priority-tagged frame or non-1Q frame, Default Priority Bit is used as the Priority bit for the port if VLAN_1Q enabled. When port-based QoS is enabled, these bits are the default priority for the ingress port.	0
12	CFI	R/W	Canonical Form Indicator (BCM5396 does not care about this bit).	0
11:0	VID	R/W	Default VLAN ID. When the incoming packet is a non-1Q-tagged frame or priority-tagged frame, the default VLAN ID will be used as the VID for the port if VLAN_1Q enabled.	0

Jumbo Frame Control Registers

Table 146: Jumbo Frame Control Registers (Page 40h)

Address	Bits	Description
01h–04h	32	Jumbo Frame Port Mask Register
05h–FEh	Reserved	Reserved
FFh	8	Page Register

Jumbo Frame Port Mask Register (Page 40h: Address 01h–04h)

Table 147: Jumbo Frame Port Mask Registers (Pages 40h: Address 01h–04h)

Bit	Name	R/W	Description	Default
31:18	Reserved	RO	Reserved	0
17	Reserved	R/W	Reserved	0
16:0	Jumbo Frame Port Mask	R/W	Jumbo frame port mask. Ports defined in the Jumbo Frame Port Mask Register can receive/transmit jumbo frames (frames larger than 1522 bytes and smaller than 9728 bytes). Bits 16:0 = Port 16–0 in chip 0. 0: Disable jumbo frame capability. 1: Enable jumbo frame capability. Jumbo frames can be delivered to these ports. Non-jumbo frames are not constrained by the register setting.	0

Broadcast Storm Suppression Registers

Table 148: Broadcast Storm Suppression Registers (Page 41h)

Address	*Bits*	*Description*
0h–03h	32	Suppression Control Register
04h–0Fh	–	Reserved
10h–13h	32	Port 0 Receive Rate Control Register
14h–17h	32	Port 1 Receive Rate Control Register
18h–1Bh	32	Port 2 Receive Rate Control Register
1Ch–1Fh	32	Port 3 Receive Rate Control Register
20h–23h	32	Port 4 Receive Rate Control Register
24h–27h	32	Port 5 Receive Rate Control Register
28h–2Bh	32	Port 6 Receive Rate Control Register
2Ch–2Fh	32	Port 7 Receive Rate Control Register
30h–33h	32	Port 8 Receive Rate Control Register
34h–37h	32	Port 9 Receive Rate Control Register
38h–3Bh	32	Port 10 Receive Rate Control Register
3Ch–3Fh	32	Port 11 Receive Rate Control Register
40h–43h	32	Port 12 Receive Rate Control Register
44h–47h	32	Port 13 Receive Rate Control Register
48h–4Bh	32	Port 14 Receive Rate Control Register
4Ch–4Fh	32	Port 15 Receive Rate Control Register
50h–7Fh	–	Reserved
80h–81h	16	Port 0 Suppressed Packet Drop Count Register
82h–83h	16	Port 1 Suppressed Packet Drop Count Register
84h–85h	16	Port 2 Suppressed Packet Drop Count Register
86h–87h	16	Port 3 Suppressed Packet Drop Count Register
88h–89h	16	Port 4 Suppressed Packet Drop Count Register
8Ah–8Bh	16	Port 5 Suppressed Packet Drop Count Register
8Ch–8Dh	16	Port 6 Suppressed Packet Drop Count Register
8Eh–8Fh	16	Port 7 Suppressed Packet Drop Count Register
90h–91h	16	Port 8 Suppressed Packet Drop Count Register
92h–93h	16	Port 9 Suppressed Packet Drop Count Register
94h–95h	16	Port 10 Suppressed Packet Drop Count Register
96h–97h	16	Port 11 Suppressed Packet Drop Count Register
98h–99h	16	Port 12 Suppressed Packet Drop Count Register
9Ah–9Bh	16	Port 13 Suppressed Packet Drop Count Register
9Ch–9Dh	16	Port 14 Suppressed Packet Drop Count Register
9Eh–9Fh	16	Port 15 Suppressed Packet Drop Count Register
C0h–FEh	–	Reserved

Table 148: Broadcast Storm Suppression Registers (Page 41h) (Cont.)

Address	Bits	Description
FFh	8	Page Register

Suppression Control Register (Page 41h: Address 00h–03h)

Table 149: Suppression Control Registers (Pages 41h: Address 00h–03h)

Bit	Name	R/W	Description	Default
31:17	Reserved	RO	Reserved	0
16	Rate Count IPG	R/W	Bit Rate Mode Selection: 0: RX Rate Excludes IPG. 1: RX Rate Includes IPG.	0
15	BUCK1_BRM_SEL	R/W	Bit Rate Mode Selection: 0: Absolute bit rate mode. Incoming bit rate is defined in the refresh count specified in the "Port N (0–15) Receive Rate Control Register (Page 41h: Address 10h–4Fh)" on page 166, as an absolute amount and with no reference to link speed. 1: Bit rate related to link speed mode. Incoming bit rate is defined in the refresh count specified in the "Port N (0–15) Receive Rate Control Register (Page 41h: Address 10h–4Fh)" as a function of link speed.	0
14	BUCK1_DRP_EN	R/W	Suppression Drop Mode Enabled: 0: The Pause Frame/Jamming Frame will be transmitted if the allowed bandwidth is exceeded for the types of packets indicated below in the Packet Type Mask. 1: Incoming packets will be dropped if the allowed bandwidth is exceeded for the types of packets indicated below in the Packet Type Mask.	0
13:8	BUCK1_PACKET_TYPE	R/W	Suppressed Packet Type Mask in Bucket 1. This bit mask determines the type of packets to be monitored by Bucket 1. 0 = Disable suppression for the corresponding packet type. 1 = Enable suppression for the corresponding packet type. The bits in this field are defined as follows: Bit 0: Unicast. Bit 1: Multicast (multicast and destination lookup success). Bit 2: Broadcast and length type <16'h0600. Bit 3: Broadcast and length type >=16'h0600. Bit 4: Reserved MAC address frame (01-80-C2-00-00-XX). Bit 5: Destination lookup failed.	0

Table 149: Suppression Control Registers (Pages 41h: Address 00h–03h) (Cont.)

Bit	Name	R/W	Description	Default
7	Bucket 0 BRM_SEL	R/W	Bit Rate Mode Selection: 0: Absolute Bit Rate mode. The Rate Count in the "Port N (0–15) Receive Rate Control Register (Page 41h: Address 10h–4Fh)" on page 166 represents the incoming bit rate as an absolute data rate. 1: Bit Rate Related to Link Speed mode. The Rate Count in the "Port N (0–15) Receive Rate Control Register (Page 41h: Address 10h–4Fh)" on page 166 represents the incoming bit rate normalized with respect to the Link Speed Mode.	0
6	BUCK0_DRP_EN	R/W	Suppression Drop Mode Enabled: 0: The Pause Frame/Jamming Frame will be transmitted if the allowed bandwidth is exceeded for the types of packets indicated below in the Packet Type Mask. 1: Incoming packets will be dropped if the allowed bandwidth is exceeded for the types of packets indicated below in the Packet Type Mask.	0
5:0	BUCK0_PACKET_TYPE	R/W	Suppressed Packet Type Mask in Bucket 0. This bit mask determines the type of packets to be monitored by Bucket 0. 0 = Disable suppression for the corresponding packet type. 1 = Enable suppression for the corresponding packet type. The bits in this field are: Bit 0: Unicast. Bit 1: Multicast (multicast and destination lookup success). Bit 2: Broadcast and length type <16'h0600. Bit 3: Broadcast and length type >=16'h0600. Bit 4: Reserved MAC address frame (01-80-C2-00-00-XX). Bit 5: Destination lookup failed.	0

Port N (0–15) Receive Rate Control Register (Page 41h: Address 10h–4Fh)

Table 150: Port N Receive Rate Control Registers (Pages 41h: Address 10h–4Fh)

Bit	Name	R/W	Description	Default
31:23	Reserved	RO	Reserved	0
22	RATE_CON_EN	R/W	Enable Rate Control of the Ingress Port. This bit enables the rate control function for an individual port. 1 = Enable 0 = Disable	0

Table 150: Port N Receive Rate Control Registers (Pages 41h: Address 10h–4Fh) (Cont.)

Bit	Name	R/W	Description	Default
21:19	BUCK1_SIZE	R/W	Bucket Size. Bucket Size will affect the burst traffic: 3'b000: 16 KB (valid 4 KB) 3'b001: 20 KB (valid 8 KB) 3'b010: 28 KB (valid 16 KB) 3'b011: 40 KB (valid 28 KB) 3'b100: 76 KB (valid 64 KB) 3'b101: 140 KB (valid 128 KB) 3'b110: 268 KB (valid 256 KB) 3'b111: 500 KB (valid 488 KB)	0
18:11	BUCK1_REFRESH_COUNT	R/W	Refresh Count. The refresh count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the refresh count and the bit rate mode of the "Suppression Control Register (Page 41h: Address 00h–03h)" on page 165 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the suppressed packet type mask in the Suppression Control Register. Refer to "Broadcast Storm Suppression Registers" on page 164 for more details. Values written to these bits must be with the ranges specified by Table 2: "Bucket Bit Rate," on page 33. Values outside these ranges are not valid.	'd000
10:8	BUCK0_SIZE	R/W	Bucket Size. These bits determine the maximum size of bucket 0. This is specified on a per port basis. Bucket size will affect the burst traffic. 3'b000: 16 KB (valid 4 KB) 3'b001: 20 KB (valid 8 KB) 3'b010: 28 KB (valid 16 KB) 3'b011: 40 KB (valid 28 KB) 3'b100: 76 KB (valid 64 KB) 3'b101: 140 KB (valid 128 KB) 3'b110: 268 KB (valid 256 KB) 3'b111: 500 KB (valid 488 KB)	0

Table 150: Port N Receive Rate Control Registers (Pages 41h: Address 10h–4Fh) (Cont.)

Bit	Name	R/W	Description	Default
7:0	BUCK0_REFRESH_COUNT	R/W	Rate Count. The Rate Count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the rate count and the bit rate mode of the "Suppression Control Register (Page 41h: Address 00h–03h)" on page 165 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the suppressed packet type mask in the Suppression Control Register. Refer to "Broadcast Storm Suppression Registers" on page 164 for more details.	0

Port N (0–15) Suppressed Packet Drop Count Register (Page 41h: Address 80h–9Fh)

Table 151: Port N Suppressed Packet Drop Counter Register (Pages 41h: Address 80h–9Fh)

Bit	Name	R/W	Description	Default
15:0	Packet Dropped Count	RC	Packet Dropped Count. Record the dropped packet count for suppression drop count or jumbo filtered count. Reset after the register has been read.	0

IEEE Standard 802.1s Multiple Spanning Tree Registers

Table 152: IEEE Standard 802.1s Multiple Spanning Tree Registers (Page 43h)

Address	*Bits*	*Description*
0h	8	MSPT (Multiple Spanning Trees) Control Register
01h–0Fh	–	Reserved
10h–15h	48	MST 0 Table Register
16h–1Bh	48	MST 1 Table Register
1Ch–21h	48	MST 2 Table Register
22h–27h	48	MST 3 Table Register
28h–2Dh	48	MST 4 Table Register
2Eh–33h	48	MST 5 Table Register
34h–39h	48	MST 6 Table Register
3Ah–3Fh	48	MST 7 Table Register
40h–45h	48	MST 8 Table Register
46h–4Bh	48	MST 9 Table Register
4Ch–51h	48	MST 10 Table Register
52h–57h	48	MST 11 Table Register
58h–5Dh	48	MST 12 Table Register
5Eh–63h	48	MST 13 Table Register
64h–69h	48	MST 14 Table Register
6Ah–6Fh	48	MST 15 Table Register
70h–75h	48	MST 16 Table Register
76h–7Bh	48	MST 17 Table Register
7Ch–81h	48	MST 18 Table Register
82h–87h	48	MST 19 Table Register
88h–8Dh	48	MST 20 Table Register
8Eh–93h	48	MST 21 Table Register
94h–99h	48	MST 22 Table Register
9Ah–9Fh	48	MST 23 Table Register
A0h–A5h	48	MST 24 Table Register
A6h–ABh	48	MST 25 Table Register
ACh–B1h	48	MST 26 Table Register
B2h–B7h	48	MST 27 Table Register
B8h–BDh	48	MST 28 Table Register
BEh–C3h	48	MST 29 Table Register
C4h–C9h	48	MST 30 Table Register
CAh–CFh	48	MST 31 Table Register
D0h–FEh	–	Reserved
FFh	8	Page Register

Multiple Spanning Tree Control Register (Page 43h: Address 00h)

Table 153: Multiple Spanning Tree Control Register (Pages 43h: Address 00h)

Bit	Name	R/W	Description	Default
7:3	Reserved	RO	Reserved	0
2	EN_802_1S	R/W	0: Only one SPANNING tree supported. (Original mode). 1: Support IEEE Standard 802.1s (Multiple Spanning tree). Spanning tree status is fetched from MSPT_table.	0
1:0	Reserved	RO	Reserved	0

Multiple Spanning Tree Table Register (Page 43h: Address 10h–CFh)

Each register is 48 bits. There are 32 registers total.

Table 154: MST Table Registers (Page 43h: Address 10h–CFh)

Bit	Name	R/W	Description	Default
33:32	SPT_STA_PORT16	R/W	Spanning Tree State for Port 16: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
31:30	SPT_STA_PORT15	R/W	Spanning Tree State for Port 15: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
29:28	SPT_STA_PORT14	R/W	Spanning Tree State for Port 14: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
27:26	SPT_STA_PORT13	R/W	Spanning Tree State for Port 13: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
25:24	SPT_STA_PORT12	R/W	Spanning Tree State for Port 12: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00

Table 154: MST Table Registers (Page 43h: Address 10h–CFh) (Cont.)

Bit	Name	R/W	Description	Default
23:22	SPT_STA_PORT11	R/W	Spanning Tree State for Port 11: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
21:20	SPT_STA_PORT10	R/W	Spanning Tree State for Port 10: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
19:18	SPT_STA_PORT9	R/W	Spanning Tree State for Port 9: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
17:16	SPT_STA_PORT8	R/W	Spanning Tree State for Port 8: 00: Disable state 01: standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
15:14	SPT_STA_PORT7	R/W	Spanning Tree State for Port 7: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
13:12	SPT_STA_PORT6	R/W	Spanning Tree State for Port 6: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
11:10	SPT_STA_PORT5	R/W	Spanning Tree State for Port 5: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
9:8	SPT_STA_PORT4	R/W	Spanning Tree State for Port 4: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00

Table 154: MST Table Registers (Page 43h: Address 10h–CFh) (Cont.)

Bit	Name	R/W	Description	Default
7:6	SPT_STA_PORT3	R/W	Spanning Tree State for Port 3: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
5:4	SPT_STA_PORT2	R/W	Spanning Tree State for Port 2: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
3:2	SPT_STA_PORT1	R/W	Spanning Tree State for Port 1: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00
1:0	SPT_STA_PORT0	R/W	Spanning Tree State for Port 0: 00: Disable state 01: Standby state (blocking) 10: Unstable state (listening/learning) 11: Normal state (forwarding or no spanning tree)	00

Page 80–8Fh: External PHY Registers (Serial Ports)

Note: Information on the External PHY Registers should be obtained from the external PHY data sheet. Data is obtained by polling the registers of the external PHY via the "MDC/MDIO Interface" on page 66. The actual values or meanings of these bits are controlled by the external PHY. The following table maps the external PHY register address to the BCM5396 offset address.

Table 155: External PHY Registers (Serial Ports) Page Summary

Page	Description
80h	Port 0
81h	Port 1
82h	Port 2
83h	Port 3
84h	Port 4
85h	Port 5
86h	Port 6
87h	Port 7

Table 155: External PHY Registers (Serial Ports) Page Summary (Cont.)

Page	Description
88h	Port 8
89h	Port 9
8Ah	Port 10
8Bh	Port 11
8Ch	Port 12
8Dh	Port 13
8Eh	Port 14
8Fh	Port 15

Table 156: External PHY Registers (Serial Ports) (Page 80h–87h)

External PHY Register Address	BCM5396 Offset Address	Bits	IEEE Register Name
00h	00h–01h	16	MII Control Register
01h	02h–03h	16	MII Status Register
02h–03h	04h–07h	32	PHY Identifier Register
04h	08h–09h	16	Auto-negotiation Advertisement Register
05h	0Ah–0Bh	16	Auto-negotiation Link Partner Ability Register
06h	0Ch–0Dh	16	Auto-negotiation Expansion Register
07h	0Eh–0Fh	16	Next Page Transmit Register
08h	10h–11h	16	Link Partner Received Next Page Register
09h	12h–13h	16	1000BASE-T Control Register
0Ah	14h–15h	16	1000BASE-T Status Register
0Bh	16h–17h	16	Reserved
0Ch	18h–19h	16	Reserved
0Dh	1Ah–1Bh	16	Reserved
0Eh	1Ch–1Dh	16	Reserved
0Fh	1Eh–1Fh	16	IEEE Extended Status Register
10h	20h–21h	16	Reserved
11h	22h–23h	16	Reserved
12h	24h–25h	16	Reserved
13h	26h–27h	16	Reserved
14h	28h–29h	16	Reserved
15h	2Ah–2Bh	16	Reserved
16h	2Ch–2Dh	16	Reserved
17h	2Eh–2Fh	16	Reserved
18h	30h–31h	16	Reserved
19h	32h–33h	16	Reserved
1Ah	34h–35h	16	Reserved

Table 156: External PHY Registers (Serial Ports) (Page 80h–87h) (Cont.)

External PHY Register Address	BCM5396 Offset Address	Bits	IEEE Register Name
1Bh	36h–37h	16	Reserved
1Ch	38h–39h	16	Reserved
1Dh	3Ah–3Bh	16	Reserved
1Eh	3Ch–3Dh	16	Reserved
1Fh	3Eh–3Fh	16	Reserved
–	51h–EFh	–	Reserved
–	F0h	8	"SPI Data I/O Register" on page 175, 0
–	F1h	8	"SPI Data I/O Register" on page 175, 1
–	F2h	8	"SPI Data I/O Register" on page 175, 2
–	F3h	8	"SPI Data I/O Register" on page 175, 3
–	F4h	8	"SPI Data I/O Register" on page 175, 4
–	F5h	8	"SPI Data I/O Register" on page 175, 5
–	F6h	8	"SPI Data I/O Register" on page 175, 6
–	F7h	8	"SPI Data I/O Register" on page 175, 7
–	F8h–FDh	–	Reserved
–	FEh	8	"SPI Status Register" on page 175
–	FFh	8	"Page Register" on page 175

Global Registers

Table 157: Global Registers (Maps to All Pages)

Address	Bits	Description
F0h	8	"SPI Data I/O Register" on page 175, Bit 0
F1h	8	"SPI Data I/O Register" on page 175, Bit 1
F2h	8	"SPI Data I/O Register" on page 175, Bit 2
F3h	8	"SPI Data I/O Register" on page 175, Bit 3
F4h	8	"SPI Data I/O Register" on page 175, Bit 4
F5h	8	"SPI Data I/O Register" on page 175, Bit 5
F6h	8	"SPI Data I/O Register" on page 175, Bit 6
F7h	8	"SPI Data I/O Register" on page 175, Bit 7
F8–FDh	–	Reserved
FEh	8	"SPI Status Register" on page 175
FFh	8	"Page Register" on page 175

SPI Data I/O Register

Table 158: SPI Data I/O Register (Maps to All Registers, Address F0–F7h)

Bit	Name	R/W	Description	Default
7:0	SPI Data I/O	R/W	SPI data bytes[7:0]	0

SPI Status Register

Table 159: SPI Status Register (Maps to All Registers, Address FEh)

Bit	Name	R/W	Description	Default
7	SPIF	RO	SPI Read/Write Complete Flag	0
6	Reserved	RO	Reserved	0
5	RACK	RO (SC)	SPI Read Data Ready Acknowledgement (Self-Clearing)	0
4:2	Reserved	RO	Reserved	0
1	RXRDY	RO	SMP RX Ready Flag—Should check every 8 bytes	0
0	TXRDY	RO	SMP TX Ready Flag—Should check every 8 bytes	0

Page Register

Table 160: Page Register (Maps to All Registers, Address FFh)

Bit	Name	R/W	Description	Default
7:0	PAGE_REG	R/W	Binary value determines the value of the accessed register page.	0

Section 8: Electrical Characteristics

Absolute Maximum Ratings

For details on each pin, refer to Table 23: “Signal Descriptions,” on page 77.

Table 161: Absolute Maximum Ratings

Symbol	Parameter and Pins	Minimum	Maximum	Units
–	Supply voltage: PLLDVDD, PLLAVDD, PLLAVDD2, SAVDD	VSS–0.3	1.50	V
–	Supply voltage: XTALVDD	VSS–0.3	2.75	V
I_I	Input current	–	±10	mA
T_{STG}	Storage temperature	-40	+125	°C
V_{ESD}	Electrostatic discharge	–	1000	V
–	Input voltage: digital input pins	VSS–0.3	3.63	V

Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

Recommended Operating Conditions

For details on each pin, refer to Table 23: “Signal Descriptions,” on page 77.

Table 162: Recommended Operating Conditions

Symbol	Parameter	Pins	Minimum	Maximum	Units
VDD	Supply voltage	PLLDVDD, PLLAVDD, PLLAVDD2, AVDD	1.14	1.26	V
		XTALVDD	2.38	2.63	V
V_{IH}	High-level input voltage	All digital inputs	2.0	–	V
V_{IL}	Low-level input voltage	All digital inputs	–	0.8	V
T_A	Ambient operating temperature		0	70	°C

Electrical Characteristics

For details on each pin, refer to Table 23 on page 77.

Table 163: Electrical Characteristics

Symbol	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Maximum supply current	1.2V power rail	–	1.51	1.608	1.706	Amps
		2.5V power rail	–	0.004	0.005	0.006	Amps
		3.3V power rail (IMP port)	–	0.014	0.015	0.017	Amps
V_{OH}	High-level output voltage	Digital output pins GMII (IMP) @ 3.3V VDD	I_{OH} = –8 mA	2.1	–	–	V
V_{OL}	Low-level output voltage	Digital output pins GMII (IMP) @ 3.3V VDD	I_{OL} = +8 mA	–	–	0.5	V
V_{IH}	High-level input voltage	Digital input pins	–	1.7	–	–	V
		XTALI	–	1.7	–	–	V
V_{IL}	Low-level input voltage	Digital input pins	–	-0.3	–	0.7	V
		XTALI	–	-0.3	–	0.8	V
I_I	Input current	Digital inputs w/ pull-up resistors	V_I = VSS	–	–	-200	µA
		Digital inputs w/ pull-down resistors	V_I = VSS	–	–	–10	µA
VoH	High-level output voltage	Digital output pins (GMII (IMP) @ 2.5V VDD	–	2.1V	–	–	–
VoL	Low-level output voltage	Digital output pins GMII (IMP) @ 2.5V VDD	–	–	–	0.5V	–
VoH	High-level output voltage	Digital output pins RGMII @ 2.5V VDD	–	2.0V	–	–	–
VoL	Low-level output voltage	Digital output pins RGMII @ 2.5V VDD	–	–	–	0.4V	–
VoH	High-level output voltage	Digital output of all other 2.5V pins	–	1.85V	–	–	–
VoL	Low-level output voltage	Digital output of all other 2.5V pins	–	–	–	0.4V	–

Table 164: SerDes Electrical Characteristics

Symbol	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
Vop	Transmit output peak-to-peak differential voltage	SerDes output pins	Programmable	150	500	1000	mV

Table 164: SerDes Electrical Characteristics (Cont.)

Symbol	Parameter	Pins	Conditions	Minimum	Typical	Maximum	Units
Vid	Peak-to-peak differential input voltage	SerDes input pins	AC coupled input signal, DC level biased in receiver	100	–	2000	mV
Rin	Receiver input impedance	SerDes input pins	Differential integrated on-chip	80	100	120	Ω
Ro	Transmitter output impedance	SerDes output pins	Differential	80	100	120	Ω

Section 9: Timing Characteristics

Reset and Clock Timing

Figure 22: Reset and Clock Timing

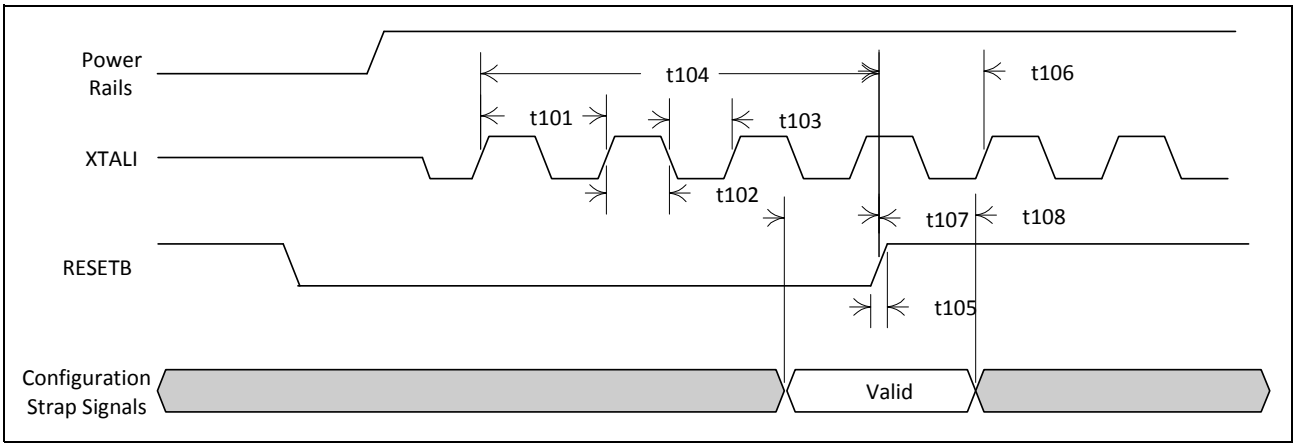


Table 165: Reset and Clock Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
XTALI Period	t101	39.998 ns	40 ns	40.002 ns
XTALI High Time	t102	18 ns	–	22 ns
XTALI Low Time	t103	18 ns	–	22 ns
$\overline{\text{RESETB}}$ Low Pulse Duration	t104	400 ns	50 ms	–
$\overline{\text{RESETB}}$ Rise Time	t105	–	–	–
Configuration Valid Setup to $\overline{\text{RESET}}$ Rising	t107	100 ns	–	–
Configuration Valid Hold from $\overline{\text{RESET}}$ Rising	t108	–	–	0 ns

Reverse MII Timing

The following specifies timing information regarding the IMP Interface pins when configured in Reverse MII mode.

Reverse MII Output Timing

Figure 23: RvMII Mode Output Timings

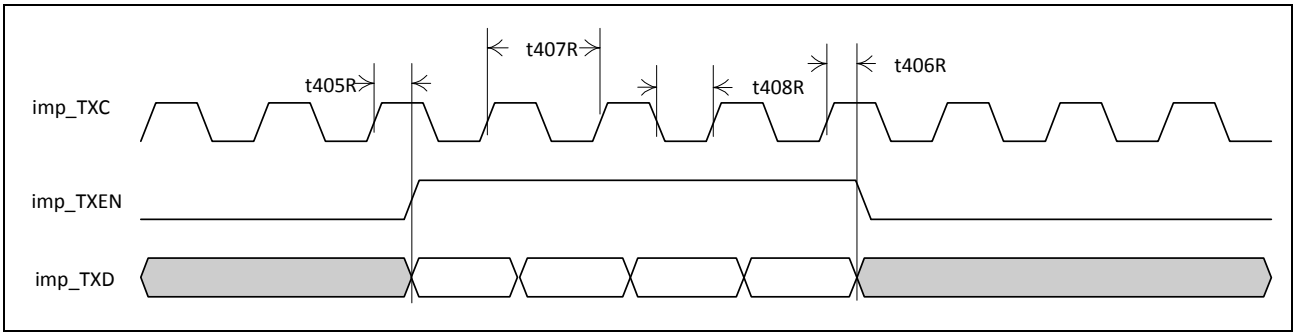


Table 166: RvMII Mode Output Timings

Description	*Parameter*	*Min*	*Typ*	*Max*
imp_TXC High to imp_TXEN, imp_TXD, imp_TXER Valid	t405R	–	–	29 ns
imp_TXC High to imp_TXEN, imp_TXD, imp_TXER Invalid	t406R	11 ns	–	–
imp_TXC Clock Period	t407R	–	40 ns	–
imp_TXC High/Low Time	t408R	14 ns	–	26 ns

Reverse MII Input Timing

Figure 24: RvMII Mode Input Timings

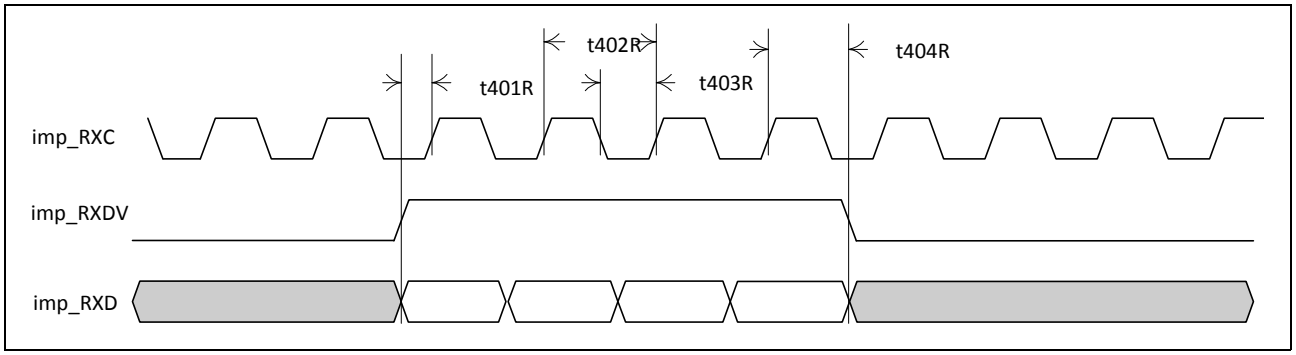


Table 167: RvMII Mode Input Timings

Description	Parameter	Min	Typ	Max
imp_RXDV, imp_RXD, imp_RXER, to imp_RXC Rising Setup Time	t401R	10 ns	–	–
imp_RXC Clock Period (100BASE-TX mode only)	t402R	–	40 ns	–
imp_RXC High/Low Time (100BASE-TX mode only)	t403R	14 ns	–	26 ns
imp_RXDV, imp_RXD, imp_RXER, to imp_RXC Rising Hold Time	t404R	0 ns	–	–

RGMII Interface Timing

The following specifies timing information regarding the IMP Interface pins when configured in RGMII Mode.

RGMII Output Timing (Normal Mode)

Figure 25: RGMII Output Timing (Normal Mode)

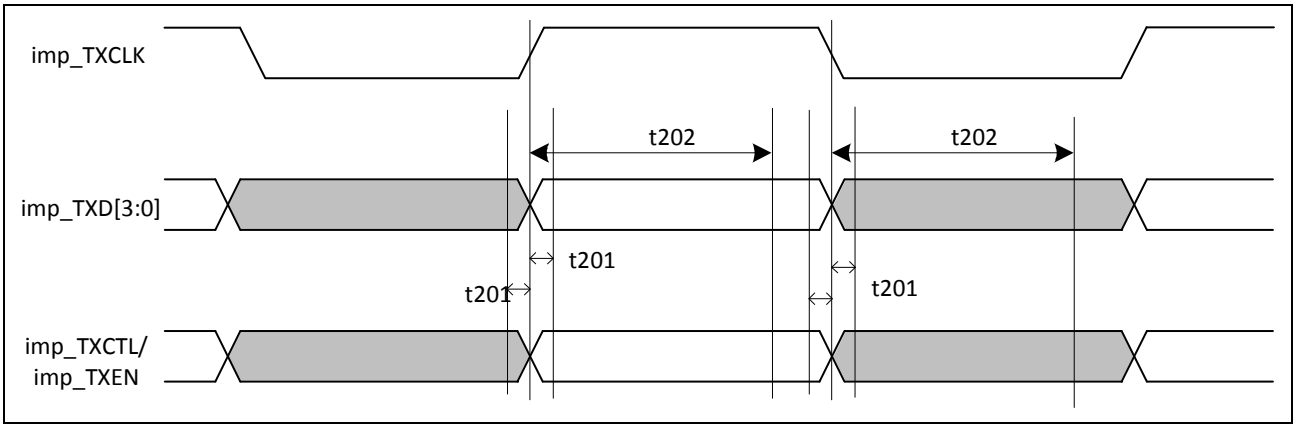


Table 168: RGMII Output Timing (Normal Mode)

Description	Parameter	Minimum	Typical	Maximum	Unit
imp_TXCLK clock period (1000 Mbps mode)	–	7.2	8	8.8	ns
imp_TXCLK clock period (100 Mbps mode)	–	32	40	48	ns
imp_TXCLK clock period (10 Mbps mode)	–	320	400	480	ns
Data valid to clock transition: Available setup time at the output source	t201	–500 (1000 Mbps)	–	+500 (1000 Mbps)	ps
Clock transition to data valid: Available hold time at the output source	t202	3.1	–	–	ns

Note: The output timing in 10/100 Mbps operation will always be as specified in the delayed mode.

RGMII Output Timing (Delayed Mode)

RGMII Output Timing defaults to the delayed mode when the TXC_DELAY pin is pulled high at power-on reset (for pin details, refer to Table 23: “Signal Descriptions,” on page 77).

Figure 26: RGMII Output Timing (Delayed Mode)

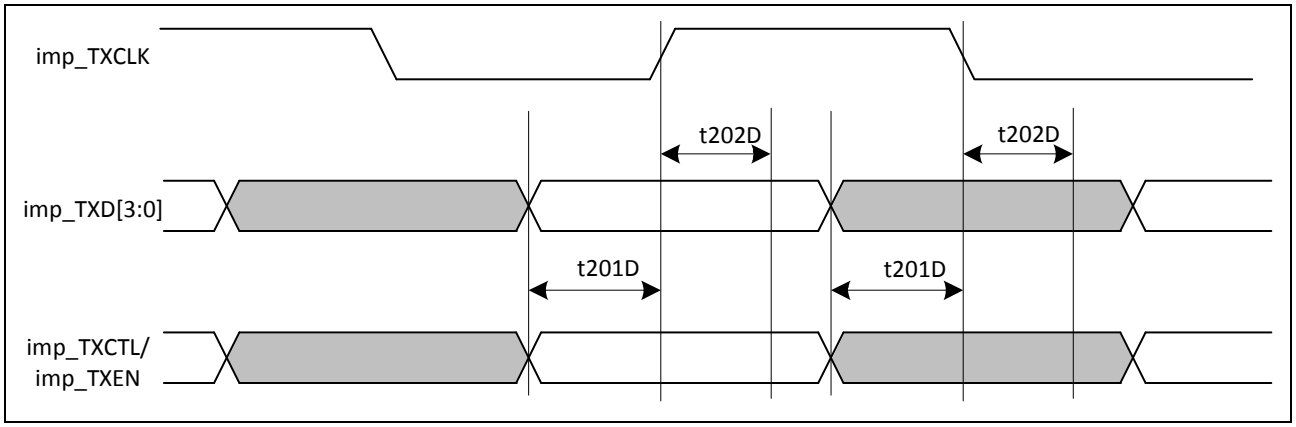


Table 169: RGMII Output Timing (Delayed Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
imp_TXCLK clock period (1000 Mbps mode)	–	7.2	8	8.8	ns
imp_TXCLK clock period (100 Mbps mode)	–	32	40	48	ns
imp_TXCLK clock period (10 Mbps mode)	–	320	400	480	ns
Data valid to clock transition: Available setup time at the output source (Delayed Mode)	t201D	1.2 (all speeds)	–	–	ns
Clock transition to data valid: Available hold time at the output source (Delayed Mode)	t202D	1.2	–	–	ns

RGMII Input Timing (Normal Mode)

Figure 27: RGMII Input Timing (Normal Mode)

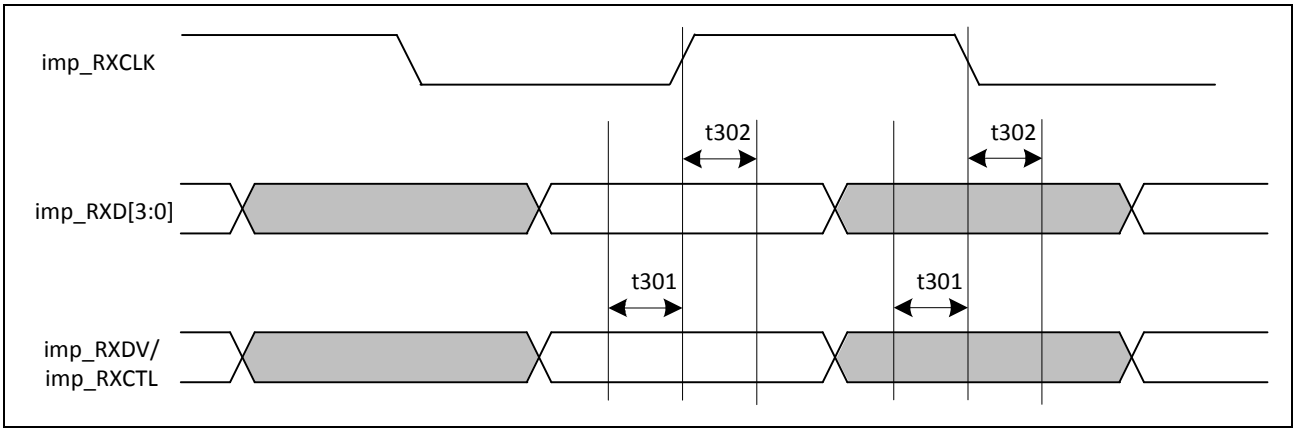


Table 170: RGMII Input Timing (Normal Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
imp_RXCLK clock period (1000 Mbps mode)	–	7.2	8	8.8	ns
imp_RXCLK clock period (100 Mbps mode)	–	36	40	44	ns
imp_RXCLK clock period (10 Mbps mode)	–	360	400	440	ns
Input setup time	t301	1.0 (all speeds)	–	–	ns
Input hold time	t302	1.0 (all speeds)	–	–	ns
Required data window at the input	t301+t302	2.0	–	–	ns

RGMII Input Timing (Delayed Mode)

RGMII input timing defaults to the delayed mode when the RXC_DELAY pin is pulled high at power-on reset (for pin details, refer to Table 23: “Signal Descriptions,” on page 77).

Figure 28: RGMII Input Timing (Delayed Mode)

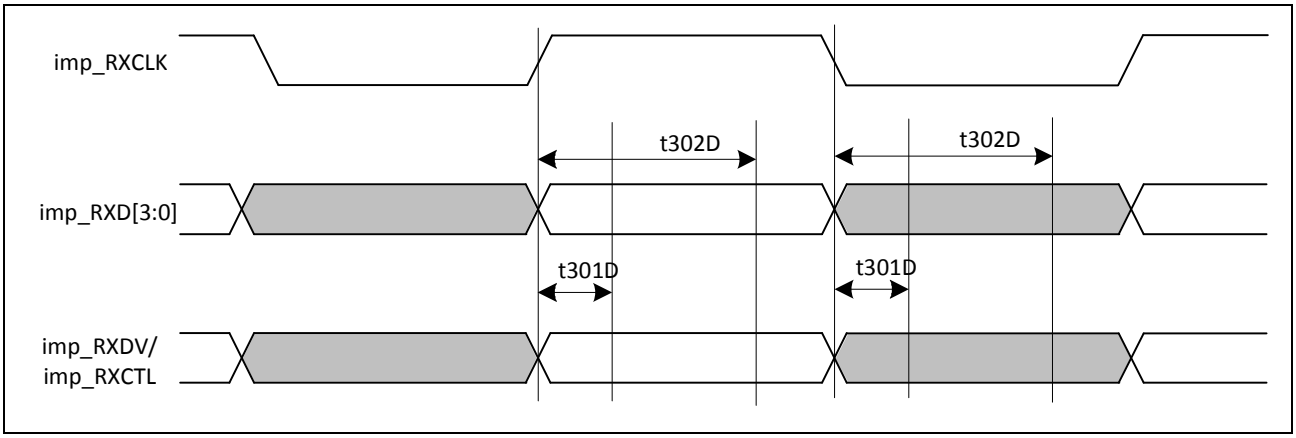


Table 171: RGMII Input Timing (Delayed Mode)

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
imp_RXCLK clock period (1000 Mbps mode)	–	7.2	8	8.8	ns
imp_RXCLK clock period (100 Mbps mode)	–	36	40	44	ns
imp_RXCLK clock period (10 Mbps mode)	–	360	400	440	ns
Input setup time (Delayed mode)	t301D	–1.0 (1000 Mbps)	–	–	ns
		-5.0 (10/100 Mbps)	–	–	ns
Input hold time (Delayed mode)	t302D	3.0 (1000 Mbps)	–	–	ns
		7.0 (10/100 Mbps)	–	–	ns
Required data window at the input	t301D+t302D	2.0	–	–	ns

GMII Interface Timing

The following specifies timing information regarding the IMP Interface pins when configured in GMII mode.

GMII Interface Output Timing

Figure 29: GMII Output Timing

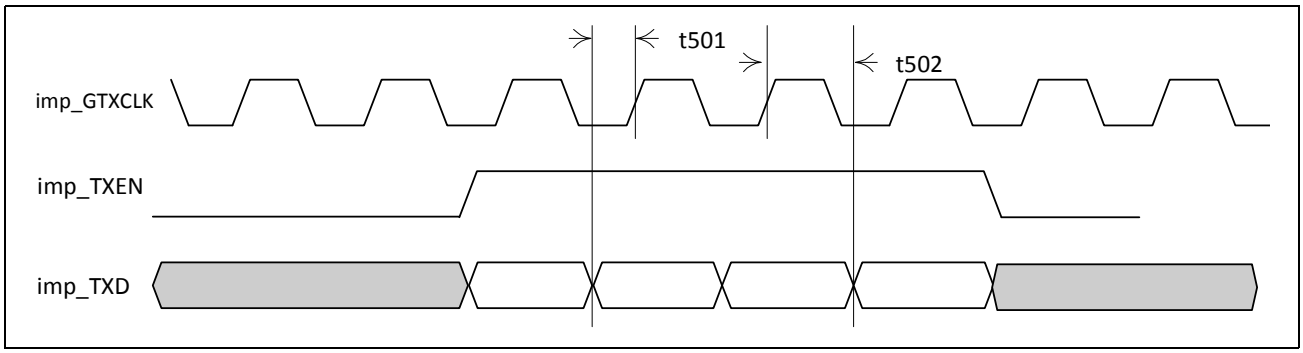


Table 172: GMII Output Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
imp_GTXCLK clock period (1000 Mbps mode)	–	7.2	8	8.8	ns
imp_GTXCLK clock period (100 Mbps mode)	–	36	40	44	ns
imp_GTXCLK clock period (10 Mbps mode)	–	360	400	440	ns
Data valid to clock transition: Available setup time at the output source	t501	2.5	–	–	ns
Clock transition to data valid: Available hold time at the output source	t502	0.5	–	–	ns

GMII Interface Input Timing

Figure 30: GMII Input Timing

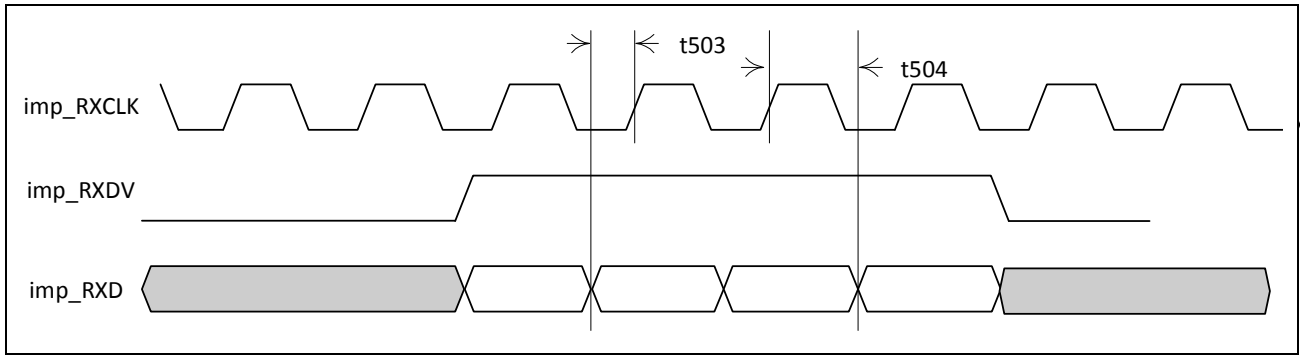


Table 173: GMII Input Timing

Description	Parameter	Minimum	Typical	Maximum	Unit
imp_RXCLK clock period (1000 Mbps mode)	–	7.2	8	8.8	ns
imp_RXCLK clock period (100 Mbps mode)	–	36	40	44	ns
imp_RXCLK clock period (10 Mbps mode)	–	360	400	440	ns
Input setup time	t503	2.0	–	–	ns
Input hold time	t504	0.0	–	–	ns

Serial Interface Timing

The Serial Interface timing specifications are outlined in the subsequent sections.

Serial Interface Output Timing

Figure 31: Serial Interface Output Timing

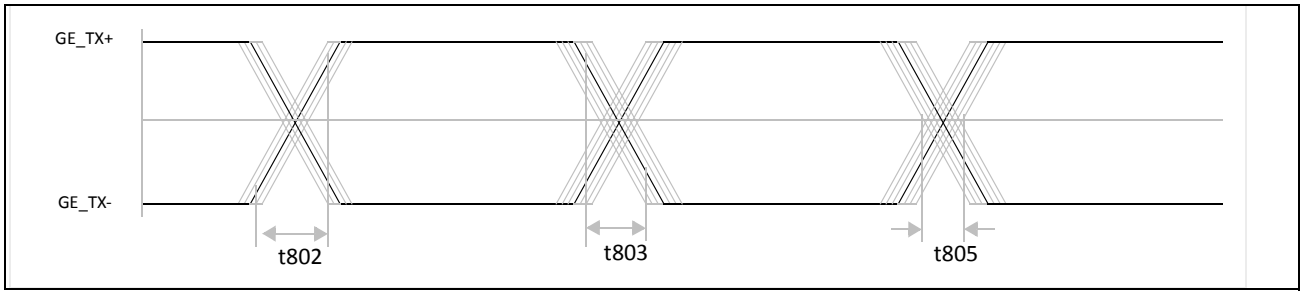


Table 174: Serial Interface Output Timings

Description	Parameter	Minimum	Typical	Maximum	Unit
SGTX Signaling Speed	t801	–	1.25	–	Gbaud
SGTX Rise Time (20%-80%)	t802	100	–	200	ps
SGTX Fall Time (20%- 80%)	t803	100	–	200	ps
SGTX Output Differential Skew (SGTX+ vs.SGTX-)	t804	–	–	20	ps
SGTX Total Jitter	t805	–	–	192	ps

Serial Interface Input Timing

Figure 32: Serial Interface Input Timing

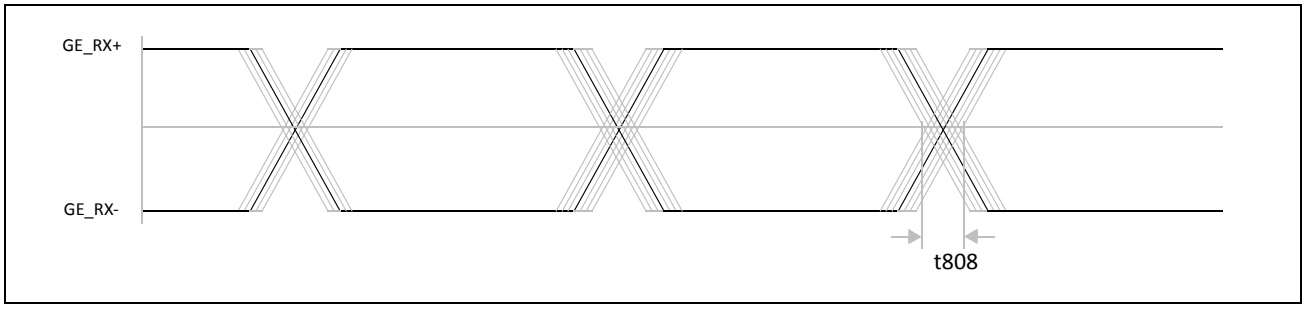


Table 175: Serial Interface Input Timings

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
SGRX Signaling Speed	t806	–	1.25	–	GBd
SGRX Input Differential Skew (SGRX+ vs.SGRX-)	t807	–	–	40	ps
SGRX Jitter (pk-pk)	t808	–	–	480	ps
SGRX Differential Input (pk-pk)	t809	0.1	–	2.0	V

MDC[0]/MDIO[0] Timing

The following specifies timing information regarding the MDC[0]/MDIO[0] Interface pins.

Figure 33: MDC[0]/MDIO[0] Timing

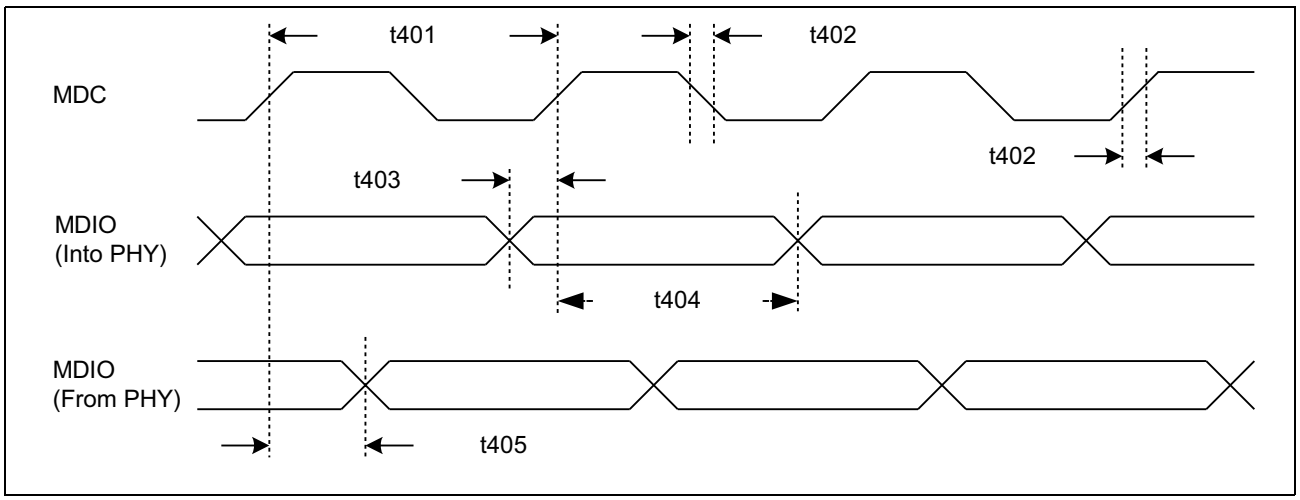


Table 176: MDC[0]/MDIO[0] Timing

Description	Parameter	Minimum	Typical	Maximum	Unit
MDC cycle time	t401	400	–	–	ns
MDC high/low	–	30	–	–	ns
MDC rise/fall time	t402	–	–	10	ns
MDIO input setup time to MDC rising	t403	10	–	–	ns
MDIO input hold time from MDC rising	t404	10	–	–	ns
MDIO output delay from MDC rising	t405	0	–	300	ns

Note: t405 (MDIO[0] output delay from MDC[0] rising) depends on MDC[0] frequency. Different MDC[0] frequency will result in different value of t405. For 2.5 MHz MDC[0] (MDC[0] cycle is 400 ns), the maximum value of t405 is 300 ns.

For some of other MDC[0] frequency, here are some typical values for t405:
When MDC[0]=1.5 MHz, t405 is about 320 ns.
When MDC[0]=12.5 MHz, t405 is about 50 ns to 60 ns.

Serial LED Interface Timing

The following specifies timing information regarding the LED interface pins.

Figure 34: Serial LED Interface Timing

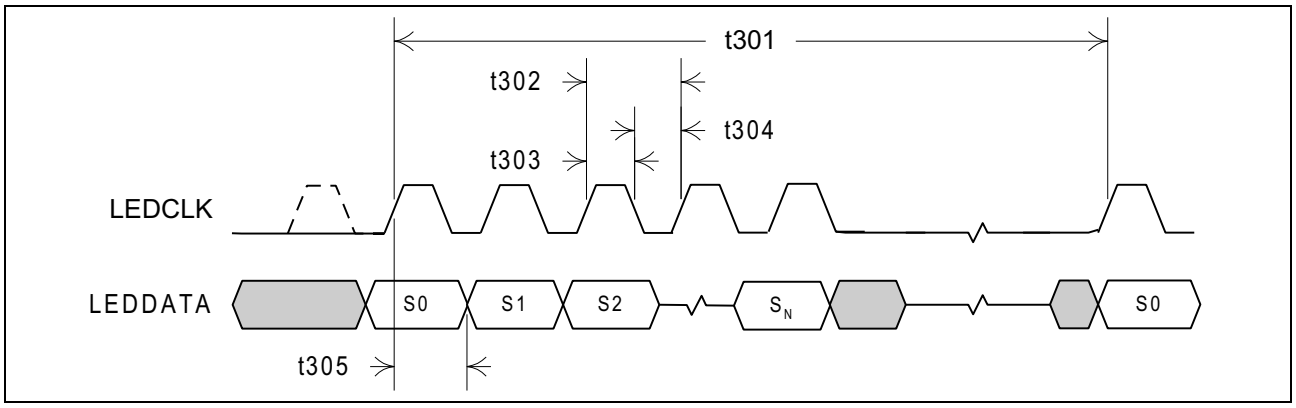


Table 177: Serial LED Interface Timing

Description	Parameter	Minimum	Typical	Maximum	Unit
LED UPDATE CYCLE PERIOD	t301	–	42	–	ms
LEDCLK PERIOD	t302	–	320	–	ns
LEDCLK High-Pulse Width	t303	150	–	170	ns
LEDCLK Low-Pulse Width	t304	150	–	170	ns

Table 177: Serial LED Interface Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*	*Unit*
LEDCLK to LEDDATA Output Time	t305	140	–	180	ns

SPI Timings

Figure 35: SPI Timings, $\overline{SS}$ Asserted During SCK High

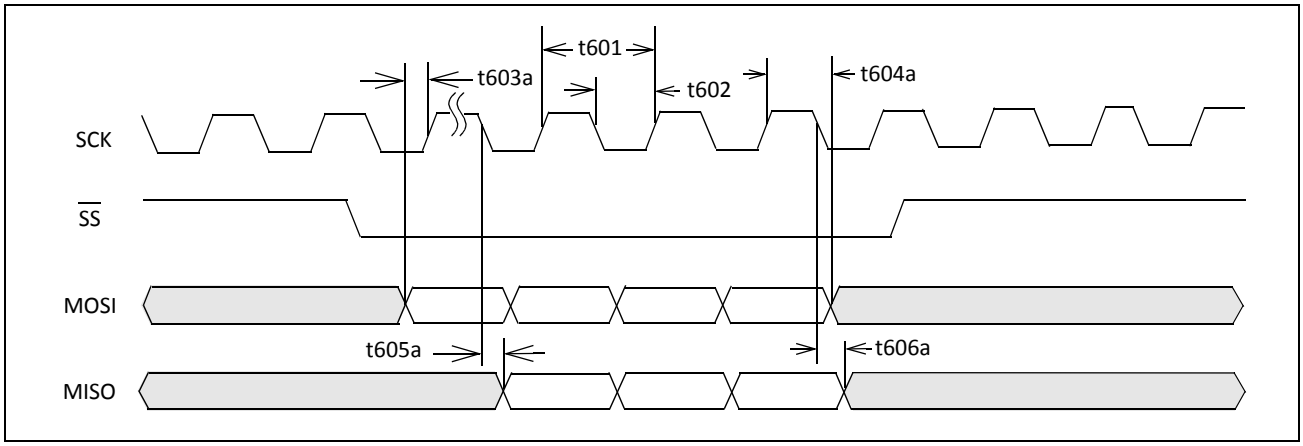


Figure 36: SPI Timings, $\overline{SS}$ Asserted During SCK Low

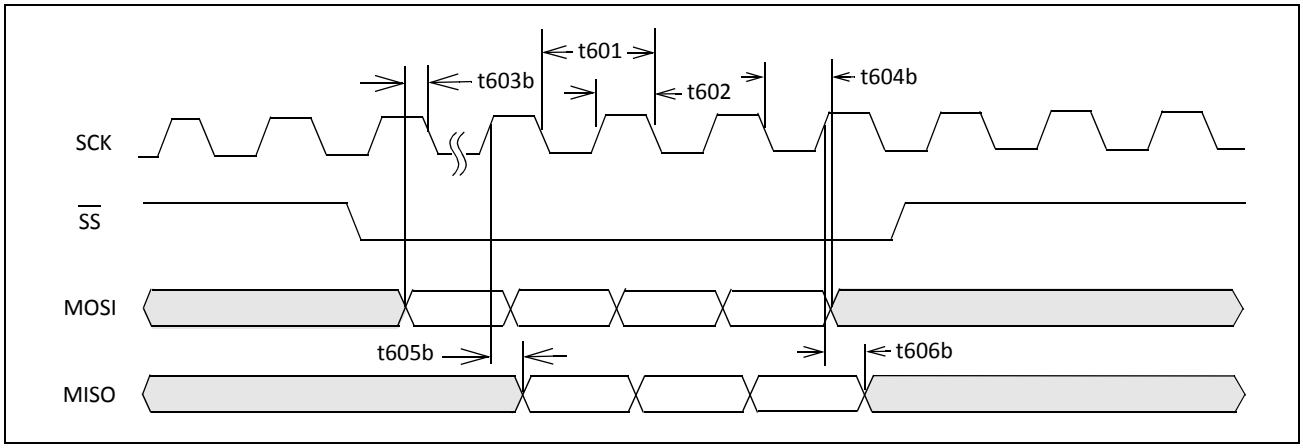


Table 178: SPI Timings

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
SCK Clock Period	t601	–	500 ns	–
SCK High/Low Time	t602	200 ns	–	300 ns
MOSI to SCK Setup Time	t603a, t603b	5 ns	–	–
MOSI to SCK Hold Time	t604a, t604b	12 ns	–	–
SCK to MISO Valid	t605a, t605b	–	–	25 ns
SCK to MISO Invalid	t606a, t606b	0 ns	–	–

Note: The BCM5396 behaves only as a slave device. $\overline{SS}$ is asynchronous. If $\overline{SS}$ is asserted during SCK high, then the BCM5396 samples data on the rising edge of SCK and references the falling edge to output data. Otherwise, the BCM5396 samples data on the falling edge and outputs data on the rising edge of SCK.

EEPROM Timing

Figure 37: EEPROM Timing

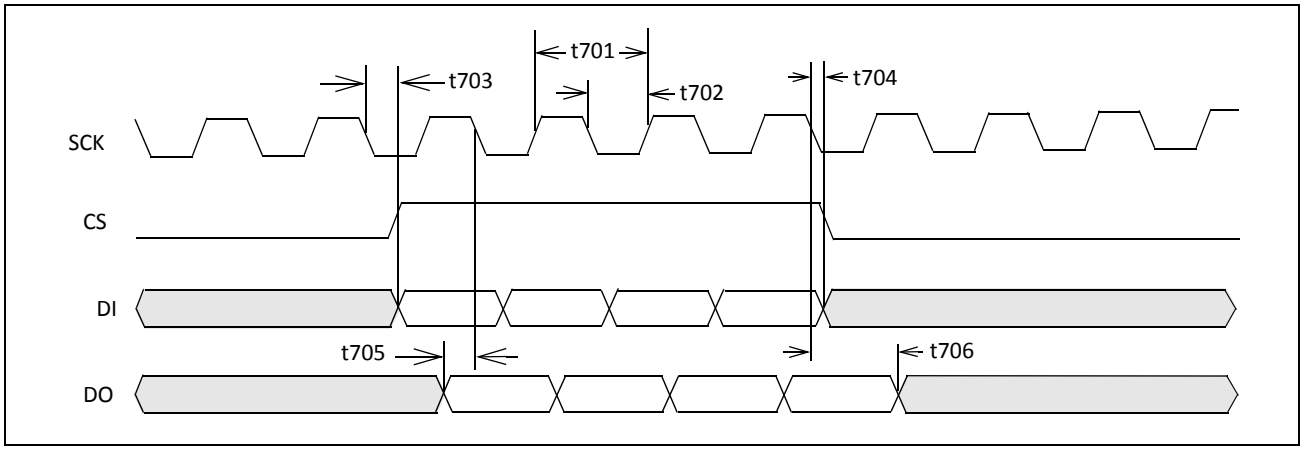


Table 179: EEPROM Timing

Description	*Parameter*	*Minimum*	*Typical*	*Maximum*
SCK Clock Frequency	t701	–	100 kHz	–
SCK High/Low Time	t702	–	5 μs	–
SCK low to CS, DI Valid	t703	–	–	500 ns
SCK low to CS, DI Invalid	t704	500 ns	–	–
DO to SCK falling Setup Time	t705	200 ns	–	–
DO to SCK falling Hold Time	t706	200 ns	–	–

Section 10: Thermal Characteristics

Table 180: Thermal Properties, With External Heat Sink, 23 mm. × 23 mm. × 15 mm. Blade Fin

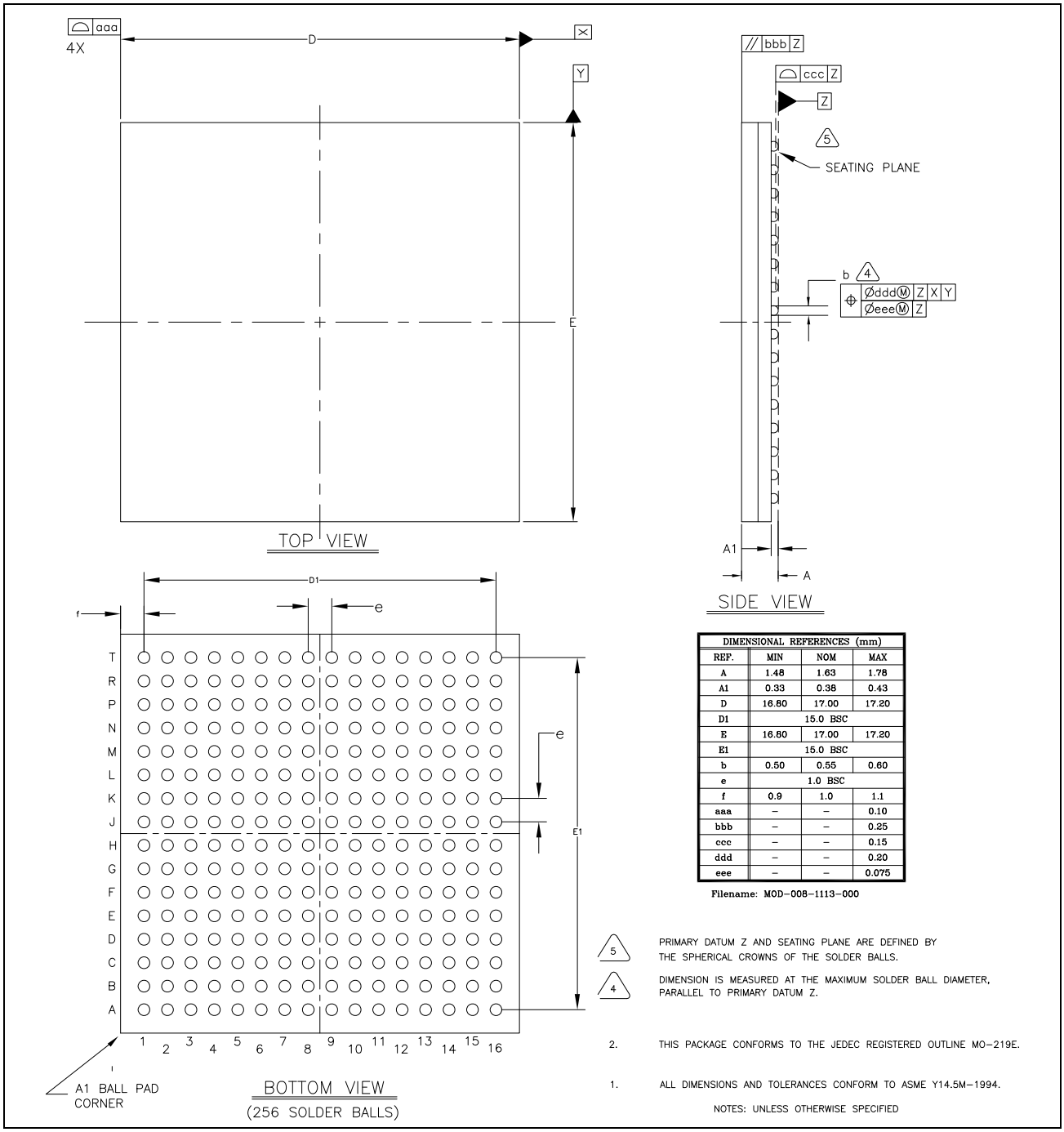
Device power dissipation, P (W)	3
Ambient air temperature, T_A (°C)	70
θ_{JA} in still air (°C/W)	16.91
θ_{JB} (°C/W)	6.56
θ_{JC} (°C/W)	6.02
	2s2p board (JEDEC standard 4-layer test board), external Heat Sink

Package Thermal Performance Data

Air Velocity		T_{J_max}	T_{C_max}	θ_{JA}	Ψ_{JT}	Ψ_{JB}
m/s	ft/min	(°C)	(°C)	(°C/W)	(°C/W)	(°C/W)
0	0	120.740	108.731	16.91	4.00	7.20
0.508	100	104.056	90.452	11.35	4.53	6.09
1.016	200	98.098	83.783	9.37	4.77	5.60
2.032	400	94.910	80.261	8.30	4.88	5.37
3.048	600	93.631	78.861	7.88	4.92	5.30

Section 11: Mechanical Information

Figure 38: 256-Pin FBGA Package Outline Drawing



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	1.48	1.63	1.78
A1	0.33	0.38	0.43
D	16.80	17.00	17.20
D1		15.0 BSC	
E	16.80	17.00	17.20
E1		15.0 BSC	
b	0.50	0.55	0.60
e		1.0 BSC	
f	0.9	1.0	1.1
aaa	–	–	0.10
bbb	–	–	0.25
ccc	–	–	0.15
ddd	–	–	0.20
eee	–	–	0.075

Filename: MOD–008–1113–000

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–219E.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Section 12: Ordering Information

Table 181: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM5396KFB	256-FBGA	0°C to 70°C
BCM5396KFBG	256-FBGA (RoHS-compliant)	0°C to 70°C
BCM5396IFB	256-FBGA	-45°C to 85°C
BCM5396IFBG	256-FBGA (RoHS-compliant)	-45°C to 85°C

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