HCPL-2503

Single Channel, High Speed Logic Interface Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

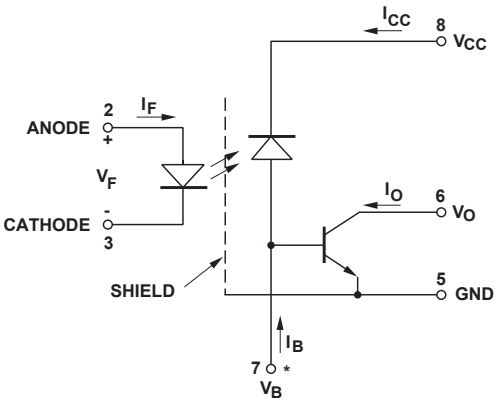
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-2503 optocoupler is specified for use in LSTTL-to-LSTTL and TTL-to-LSTTL logic interfaces. A nominal 8 mA sink current through the input LED will provide enough output current for proper operation of 1 LSTTL gate under worst-case conditions when used in the recommended circuits. The CTR of the HCPL-2503 is 15% minimum at $I_F = 8$ mA.

The HCPL-2503 contains a light emitting diode and an integrated photon detector with a 3000 Vdc withstand test between input and output. Separate connection for the photodiode bias and output transistor collector reduce the base-collector capacitance, giving improved speed compared with conventional phototransistor couplers.

Schematic



Features

- Data rates to 250 kb/s NRZ
- LSTTL compatible
- High common mode transient immunity: > 1000 V/µs
- 3750 Vdc withstand test voltage
- Open collector output
- Guaranteed performance from temperature: 0°C to 70°C
- Safety approval
  - UL Recognized - 3750Vrms for 1min (5000Vrms for 1 min Option 020 devices) per UL1577.
  - IEC/EN/DIN EN 60747-5-2 Approved
  - VIORM = 630 Vpeak for option 060

Applications

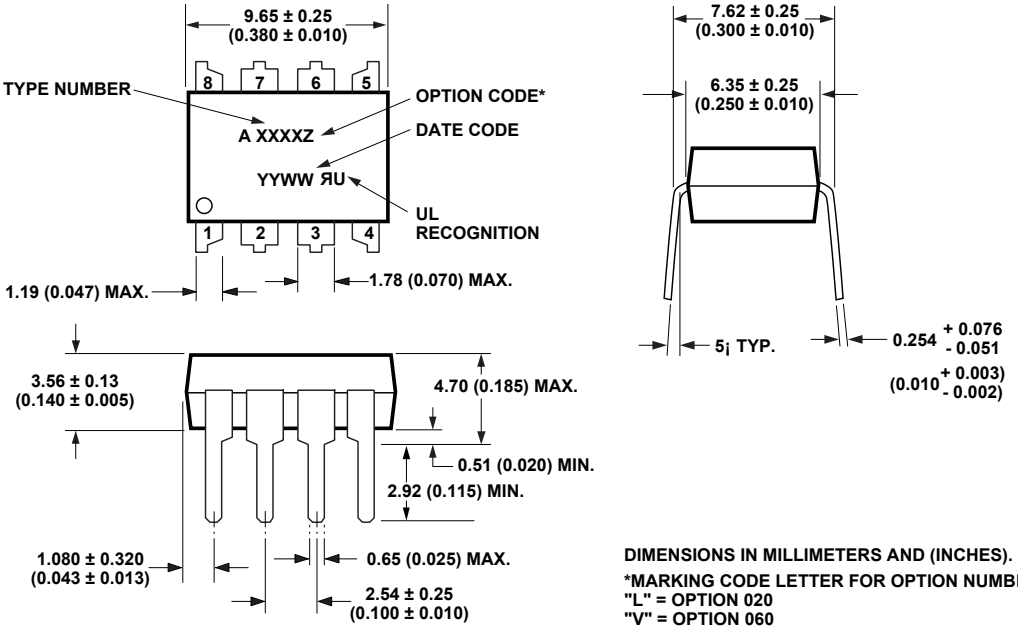
- High speed logic ground isolation – LSTTL-to-LSTTL and TTL-to-LSTTL
- High voltage isolation
- Analog signal ground isolation

- A 0.1uF bypass capacitor must be connected between 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Outline Drawing

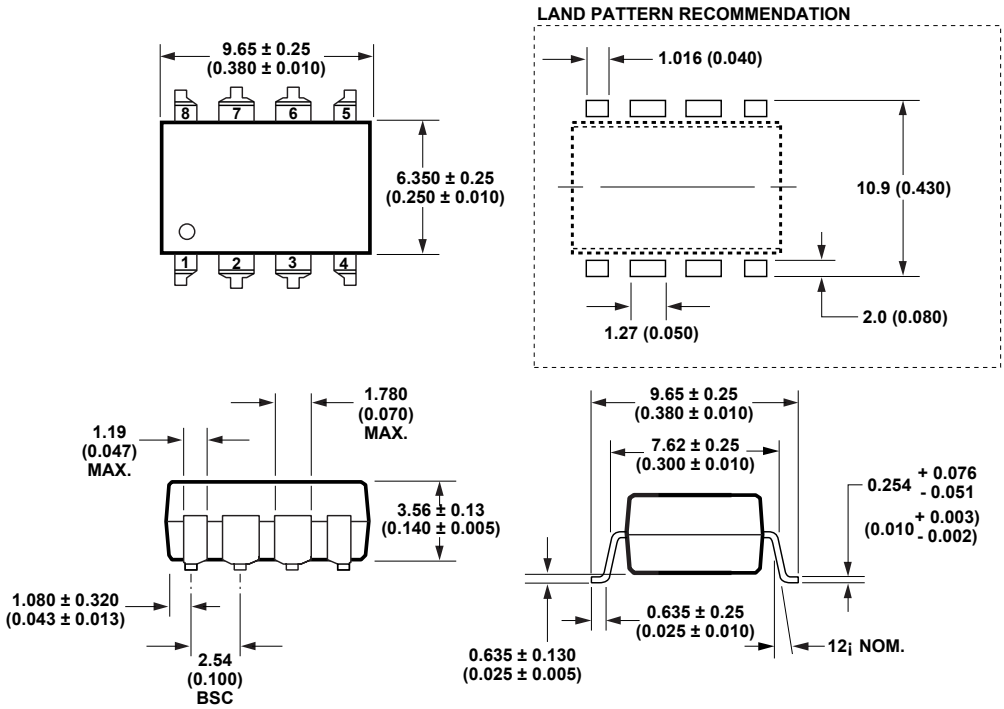
8-Pin DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).
*MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

8-Pin DIP Package with Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Ordering Information

HCPL-2503 is UL Recognized with 3750 Vrms and 5000 Vrms (option 020) for 1 minute per UL1577. All devices above listed are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	Option RoHS Compliant	Option Non RoHS Compliant	Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 Vrms/1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
HCPL-2503	-000E	No option	300mil DIP-8						50 per tube
	-300E	-300		X	X				50 per tube
	-500E	-500		X	X	X			1000 per reel
	-020E	-020					X		50 per tube
	-320E	-320		X	X		X		50 per tube
	-520E	-520		X	X	X	X		1000 per reel
	-060E	-060						X	50 per tube
	-360E	-360		X	X			X	50 per tube
	-560E	-560		X	X	X		X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-2503-000E to order product of 300mil DIP package with RoHS compliant.

Example 2:

HCPL-2503 to order product of 300mil DIP package in tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

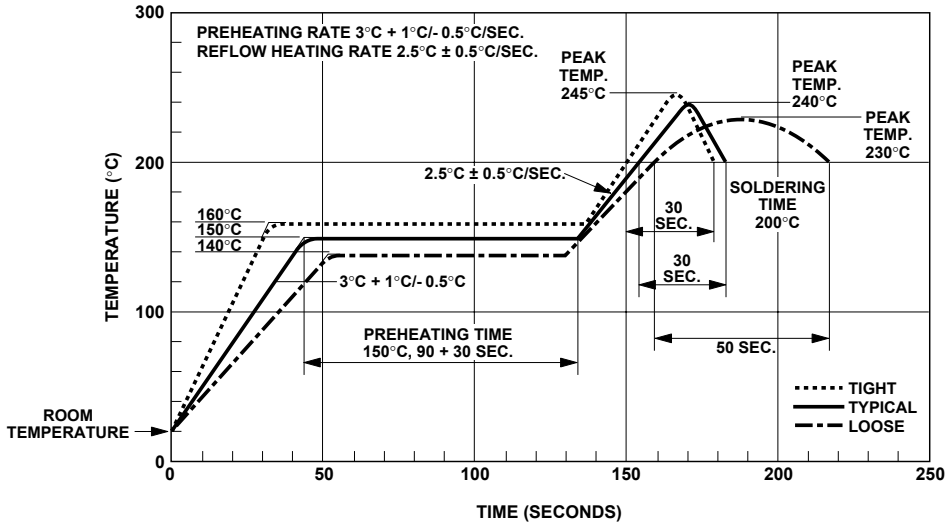
Absolute Maximum Ratings

Storage Temperature ..... –55°C to +125°C
Operating Temperature ..... –55°C to +100°C
Lead Solder Temperature (1.6 mm below seating plane) ..... 260°C for 10 s
Average Input Current – I_F ..... 25 mA[1]
Peak Input Current – I_F (50% duty cycle, 1 ms pulse width) ..... 50 mA[2]
Peak Transient Input Current – I_F (≤1 µs pulse width, 300 pps) ..... 1.0 A
Reverse Input Voltage – V_R (Pin 3-2) ..... 5 V
Input Power Dissipation ..... 45 mW[3]
Average Output Current – I_O (Pin 6) ..... 8 mA
Peak Output Current – I_O ..... 16 mA
Emitter-Base Reverse Voltage (Pin 5-7) ..... 5 V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5) ..... –0.5 V to 7 V
Base Current – I_B (Pin 7) ..... 5 mA
Output Power Dissipation ..... 100 mW[4]

Notes:

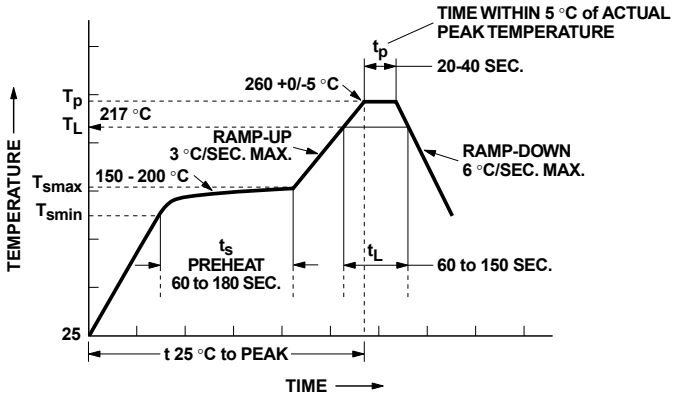
1. Derate linearly above +70˚C free-air temperature at a rate of 0.8 mA/˚C.
2. Derate linearly above +70˚C free-air temperature at a rate of 1.6 mA/˚C.
3. Derate linearly above +70˚C free-air temperature at a rate of 0.9 mW/˚C.
4. Derate linearly above +70˚C free-air temperature at a rate of 2.0 mW/˚C.

Solder Reflow Temperature Profile



Note: Non-halide flux should be used.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2

Approved under
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01
(HCNW and Option 060 only)

Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics (HCPL-2503 OPTION 060 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤300 V rms		I-IV	
for rated mains voltage ≤450 V rms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and sample test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 9, Thermal Derating curve.)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	Ω

Electrical Specifications, LSTTL-to-LSTTL

Over recommended temperature (T_A = 0°C to +70°C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	15	22		%	I_F = 8 mA, V_O = 0.5 V, V_{CC} = 4.5 V, T_A = 25°C	1	5
		11	15		%	I_F = 8 mA, V_O = 0.5 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}		0.2	0.5	V	I_F = 8 mA, I_O = 0.7 mA, V_{CC} = 4.5 V		
Logic Low Supply Current	I_{CCL}		20		µA	I_F = 8 mA V_O = Open, V_{CC} = 5.5 V		
Input Forward Voltage	V_F		1.5	1.7	V	I_F = 8 mA, T_A = 25°C	2	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		–1.6		mV/°C	I_F = 8 mA		

*All typicals at 25°C.

Switching Specifications at T_A = 25°C

V_{CC} = 5 V, I_F = 8 mA, R_L = 7.5 kΩ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		1.0	1.5	µs		4,6	8
Propagation Delay Time to Logic High at Output	t_{PLH}		1.5	2.5	µs		4,6	8
Common Mode Transient Immunity at Logic High Level Output	CM_H		1000		V/µs	I_F = 0 mA, V_{CM} = 10 V_{P-P}	7	7,8
Common Mode Transient Immunity at Logic Low Level Output	CM_L		–1000		V/µs	V_{CM} = 10 V_{P-P}	7	7,8

Electrical Specifications, TTL-to-LSTTL

Over recommended temperature (T_A = 0˚C to +70˚C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	12	18		%	I_F = 16 mA, V_O = 0.5 V, V_{CC} = 4.5 V, T_A = 25°C	1	5
		9	13		%	I_F = 16 mA, V_O = 0.5 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}		0.2	0.5	V	I_F = 16 mA, I_O = 1.1 mA, V_{CC} = 4.5 V		
Logic Low Supply Current	I_{CCL}		40		µA	I_F = 16 mA V_O = Open, V_{CC} = 5.5 V		
Input Forward Voltage	V_F		1.5	1.7	V	I_F = 16 mA, T_A = 25°C	2	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$		–1.6		mV/˚C	I_F = 16 mA		

*All typicals at 25˚C.

Switching Specifications at T_A = 25°C

V_{CC} = 5 V, I_F = 16 mA, R_L = 4.7 kΩ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}		0.4	1.5	µs		4,6	9
Propagation Delay Time to Logic High at Output	t_{PLH}		1.5	2.5	µs		4,6	9
Common Mode Transient Immunity at Logic High Level Output	CM_H		1000		V/µs	I_F = 0 mA, V_{CM} = 10 V_{P-P}	7	7,9
Common Mode Transient Immunity at Logic Low Level Output	CM_L		–1000		V/µs	V_{CM} = 10 V_{P-P}	7	7,9

Electrical Specifications

Over recommended temperature (T_A = 0˚C to +70˚C) unless otherwise specified.

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Logic High Output Current	I_{OH}		0.5		nA	T_A = 25°C, I_F = 0 mA V_O = V_{CC} = 5.5 V	5	
				50	µA	I_F = 0 mA V_O = V_{CC} = 5.5 V		
Logic High Supply Current	I_{CCH}		0.05	4	µA	I_F = 0 mA V_O = Open, V_{CC} = 5.5 V		
Input Reverse Breakdown Voltage	V_R	5			V	I_F = 10 µA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Leakage Current	I_{I-O}			1.0	µA	45% Relative Humidity, t = 5s, V_{I-O} = 3000 Vdc, T_A = 25°C		6
Resistance (Input–Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		6
Capacitance (Input–Output)	C_{I-O}		0.6		pF	f = 1 MHz		6

*All typicals at 25˚C.

Notes:

5. Current Transfer Ratio is defined as the ratio of output collector current, I/O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
8. The 7.5 k load represents 1 LSTTL until load of 0.36 mA and a 20 kΩ pull-up resistor.
9. The 4.7 k load represents 1 LSTTL unit load of 0.36 mA and an 8.2 kΩ pull-up resistor.

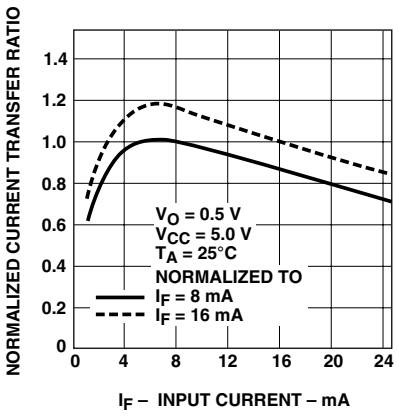


Figure 1. Current transfer ratio vs. input current

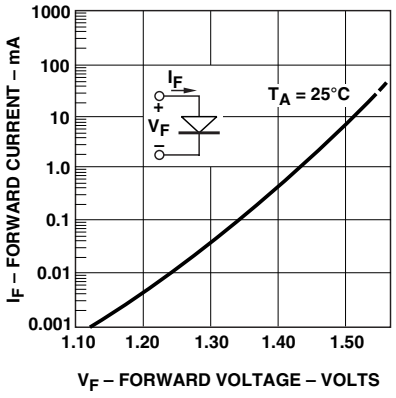


Figure 2. Input current vs. forward voltage

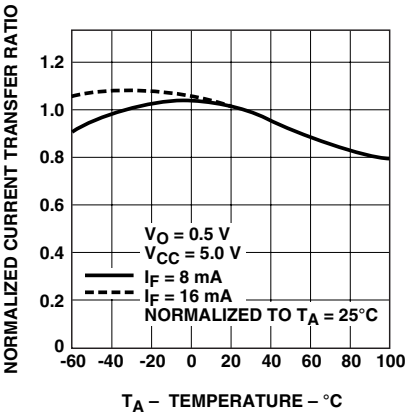


Figure 3. Current transfer ratio vs. temperature

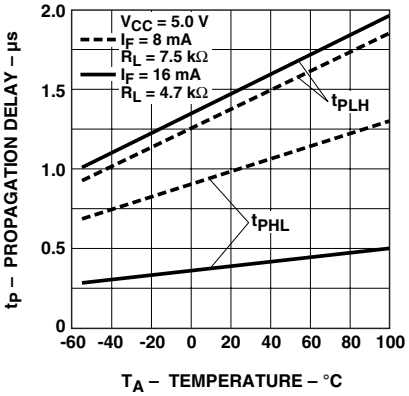


Figure 4. Propagation delay vs. temperature

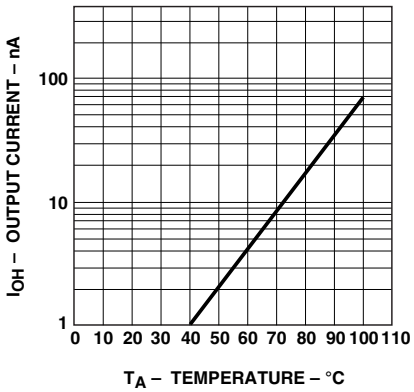
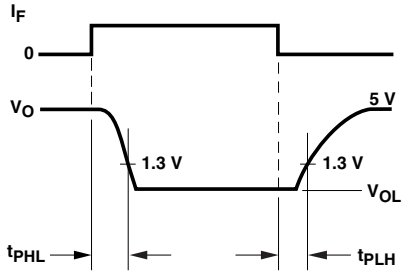


Figure 5. Logic high output current vs. temperature



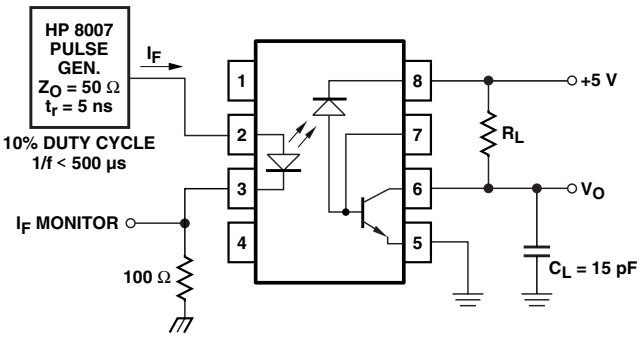


Figure 6. Switching test circuit

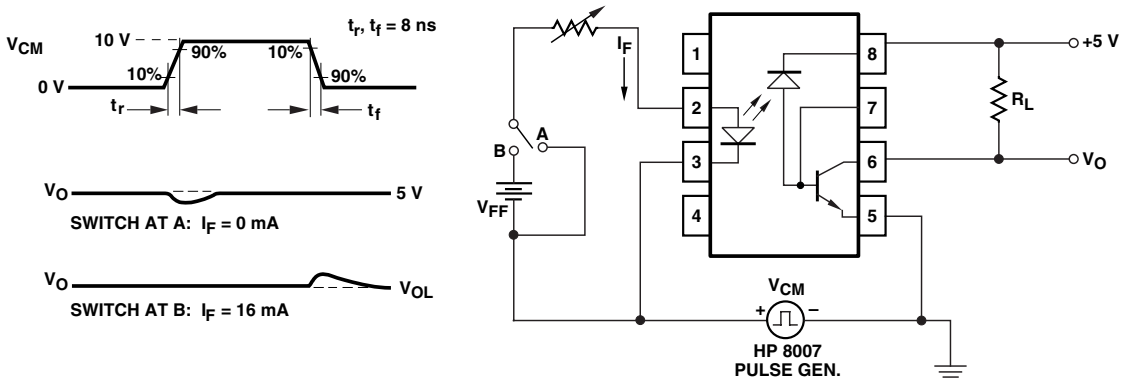


Figure 7. Test circuit for transient immunity and typical waveforms

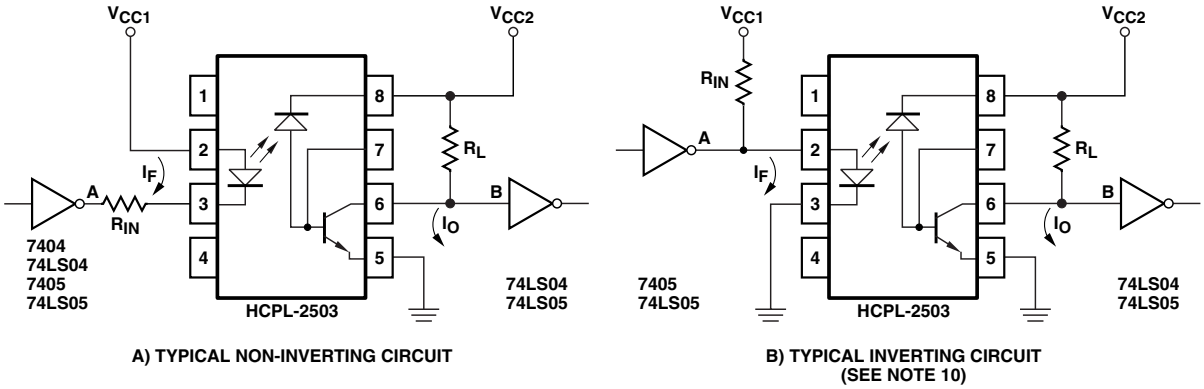


Figure 8. Recommended circuits

Recommended Operation

The HCPL-2503 optocoupler is specified for use in LSTTL-to-LSTTL and TTL-to-LSTTL interfaces. The recommended circuits show the interface design and give suggested component values. The input current I_F is given as both a nominal value and a range. The range in I_F results from the tolerances in V_{CC} and the input resistor R_{IN}. The CTR of the optocoupler is given as the minimum initial value over temperature, taken directly from the Electrical Specifications. The value given for I_{OL} (min) is based on the minimum CTR and the minimum I_F using worst case values for R_L and V_{CC}. The resulting I_{OL} (min) has ample design margin, allowing more than 20% for CTR degradation even under these worst case conditions. For additional information on CTR degradation see *Application Note 1002*.

Recommended Circuit Design Parameters

Parameter	Symbol	LSTTL-to-LSTTL	TTL-to-LSTTL	Units	Comments	Fig.	Note
Input							
Logic Low Output Voltage – Input Gate	V_{OL} (A)	0.5	0.4	V	Maximum		
Supply Voltage – Input	V_{CC1}	5.0	5.0	V	± 5%		
Input Resistor	R_{IN}	360	180	Ω	± 5%	8a	
		430	200			8b	
Input Current	I_F	8	16	mA	Nominal		
Input Current Range	I_F	6.75–10	14.0–20	mA		8a	
			14.5–20			8b	
Output							
Logic Low Output Voltage – HCPL-2503	V_{OL} (B)	0.5	0.5	V	Maximum		
Supply Voltage – Output	V_{CC2}	5.0	5.0	V	± 5%		
Pull-Up Resistor	R_L	20	8.2	kΩ	± 5%		11
Required Current Sink for Logic Low	I_{OL} (max)	0.61	1.0	mA	Worst Case V_{CC}, R_L, I_{IL} (B)		12
HCPL-2503 Current Transfer Ratio	CTR	11	9	%	Minimum T_A = 0°C to +70°C		
Logic Low Output Current – HCPL-2503	I_{OL} (min)	0.74	1.26	mA	Worst Case V_{CC}, CTR, I_F	8a	13
			1.30		T_A = 0◦C to +70◦C	8b	
Data Rate	f_D	250	250	kb/s	NRZ, T_A = 25°C		14

Notes:

10. The inverting circuit has higher power consumption and must use open collector gates on the input.
11. The load resistor R_L must be large enough to guarantee logic LOW and small enough to guarantee logic HIGH under worst case conditions:

$$\frac{V_{CC}\,(max) - V_{OL}}{I_{OL}\,(2503) - I_{IL}\,(B)} \leq R_L \leq \frac{V_{CC}\,(min) - V_{IH}\,(B)}{I_{OH}\,(2503) - I_{IH}\,(B)}$$

    The selection of R_L is the same for both inverting and non-inverting circuits.
12. The maximum current sink required for logic LOW is:

$$I_{OL}\,(max) = I_{IL}\,(B)\,(max) + I_R\,(max)$$

    where I_R is the current through R_L.
13. The ratio of I_{OL} (min) to I_{OL} (max) gives the design margin for CTR degradation. See Application Note 1002.
14. The maximum data rate is defined as:

$$f_D = \frac{1}{t_{PHL} + t_{PLH}} \quad \text{bits/second NRZ}$$

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AV02-0520EN - June 15, 2007

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