HCPL-576x*
5962-8947701

AC/DC to Logic Interface Hermetically Sealed Optocouplers

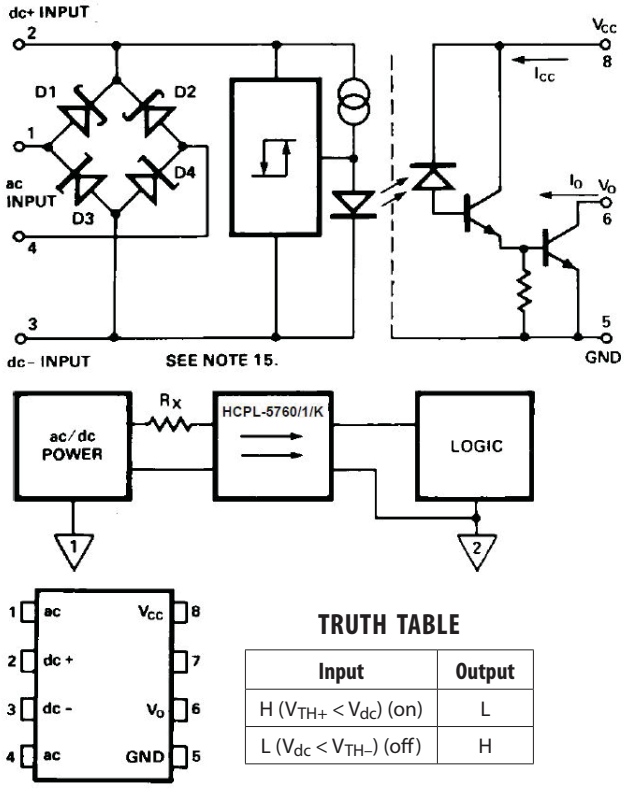
Data Sheet

Description

These devices are single channel, hermetically sealed, voltage/current threshold detection optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product, or with full MIL-PRF-38534 Class Level H or K testing, or from the DLA Standard Micro-circuit Drawing (SMD) 5962-89477. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DLA Qualified Manufacturers List, QML-38534 for Hybrid Microcircuits.

*See matrix for available extensions

Schematic



TRUTH TABLE

Input	Output
H ($V_{TH+} < V_{dc}$) (on)	L
L ($V_{dc} < V_{TH-}$) (off)	H

Features

- Dual marked with device part number and DLA standard microcircuit drawing
- Manufactured and tested on a MIL-PRF-38534 certified line
- QML-38534, class H and K
- Hermetically sealed 8-pin dual in-line packages
- Performance guaranteed over -55° C to +125° C
- AC or DC input
- Programmable sense voltage
- Hysteresis
- HCPL-3700 operating compatibility
- Logic compatible output
- 1500 Vdc withstand test voltage
- Thresholds guaranteed over temperature
- Thresholds independent of LED characteristics

Applications

- Military and space
- High reliability systems
- Transportation, medical, and life critical systems
- Limit switch sensing
- Low voltage detector
- AC/DC voltage sensing
- Relay contact monitor
- Relay coil voltage monitor
- Current sensing
- Microprocessor interface
- Telephone ring detection
- Harsh industrial environments

The connection of a 0.1 µF bypass capacitor between pins 8 and 5 is recommended.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Each unit contains a light emitting diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.6 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of any variation in optical coupling. Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with AC voltage input.

These units combine several unique functions in a single package, providing the user with an ideal component for computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

This is an eight pin DIP which may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Microcircuit Drawing (SMD) parts are available for each lead style.

Selection Guide – Package Styles and Lead Configuration Options

Avago Part # and Options	
Commercial	HCPL-5760
MIL-PRF-38534 Class H	HCPL-5761
MIL-PRF-38534 Class K	HCPL-576K
Standard Lead Finish	Gold
Solder Dipped	Option #200
Butt Joint/Gold Plate	Option #100
Gull Wing/Soldered	Option #300
Crew Cut/Gold Plate	Option #600
Class H SMD Part #	
Prescript for all below	5962-
Gold Plate	8947701PC
Solder Dipped	8947701PA
Butt Joint/Gold Plate	8947701YC
Butt Joint/Soldered	8947701YA
Gull Wing/Soldered	8947701XA
Crew Cut/Gold Plate	Available
Crew Cut/Soldered	Available
Class K SMD Part #	
Prescript for all below	5962-
Gold Plate	8947702KPC
Solder Dipped	8947702KPA
Butt Joint/Gold Plate	8947702KYC
Butt Joint/Soldered	8947702KYA
Gull Wing/Soldered	8947702KXA
Crew Cut/Gold Plate	Available
Crew Cut/Soldered	Available

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature Range	T_S	-65	+150	°C	
Operating Temperature	T_A	-55	+125	°C	
Lead Solder Temperature			260 for 10 sec	°C	2
Average Input Current	I_{IN}		15	mA	3
Surge Input Current	$I_{IN,SG}$		140	mA	3, 4
Peak Transient Input Current	$I_{IN,PK}$		500	mA	3, 4
Input Power Dissipation	P_{IN}		195	mW	5
Total Package Power Dissipation	P_d		260	mW	
Output Power Dissipation	P_O		65	mW	
Average Output Current	I_O		40	mA	
Supply Voltage (Pins 8-5)	V_{CC}	-0.5	20 V	min.	
Output Voltage (Pins 6-5)	V_O	-0.5	20 V	min.	

ESD Classification

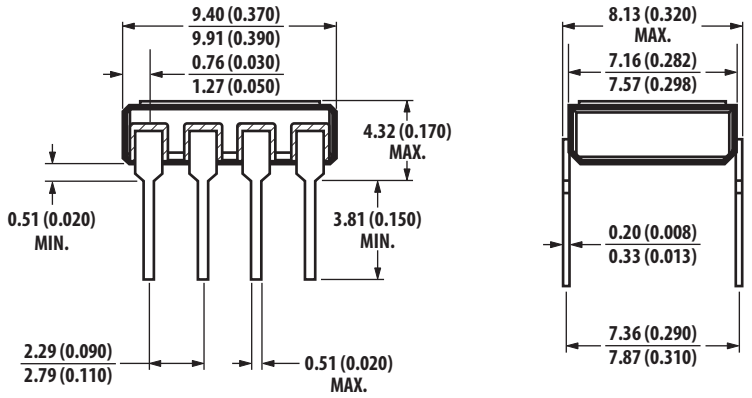
MIL-STD-883, Method 3015		(ΔΔ), Class 2

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply	V_{CC}	3.0	18	V
Operating Frequency [1]	f	0	10	KHz

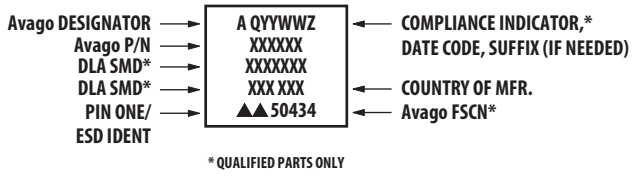
Outline Drawing

8 Pin DIP Through Hole



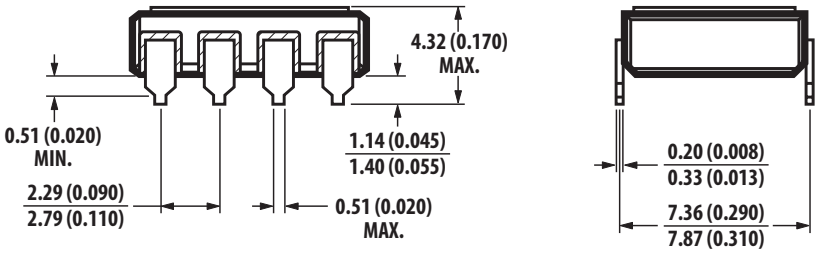
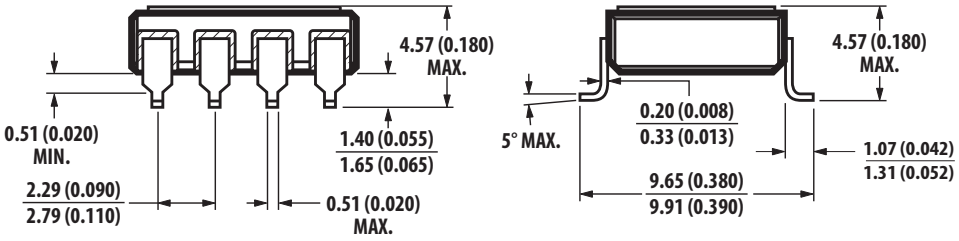
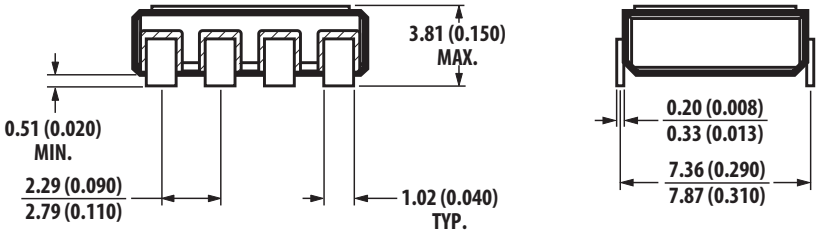
Note: Dimensions in millimeters (inches).

Device Marking



* QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. 
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product. DLA Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product. This option has solder dipped leads. 
600	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. Contact factory for the availability of this option on DLA part types. 

Note: Dimensions in millimeters (inches).

Electrical Characteristics T_A = -55° C to 125° C, unless otherwise specified. See note 16.

Parameter		Symbol	Conditions	Group A Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Input Threshold Current		I_{TH+}	$V_{IN} = V_{TH+}$; V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	1.75	2.5	3.20	mA	1, 2	7
		I_{TH-}	$V_{IN} = V_{TH-}$; V_{CC} = 4.5 V; V_O = 2.4 V; $I_{OH} \leq$ 250 µA	1, 2, 3	0.93	1.3	1.62	mA		
Input Threshold Voltage	DC (Pins 2, 3)	V_{TH+}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	3.18	3.6	4.10	V		
		V_{TH-}	$V_{IN} = V_2 - V_3$; Pins 1 & 4 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 250 µA	1, 2, 3	1.90	2.5	3.00	V		
	AC (Pins 1, 4)	V_{TH+}	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 0.4 V; $I_O \geq$ 2.6 mA	1, 2, 3	3.79	5.0	5.62	V		7, 8
		V_{TH-}	$V_{IN} = \lvert V_1 - V_4 \rvert$; Pins 2 & 3 Open V_{CC} = 4.5 V; V_O = 2.4 V; $I_O \leq$ 250 µA	1, 2, 3	2.57	3.7	4.52	V		
Input Clamp Voltage		V_{IHC1}	$V_{IHC1} = V_2 - V_3$; V_3 = GND; I_{IN} = 10 mA; Pin 1 & 4 Connected to Pin 3	1, 2, 3	5.3	5.9	7.5	V	3	15
		V_{IHC2}	$V_{IHC2} = \lvert V_1 - V_4 \rvert$; $\lvert I_{IN} \rvert$ = 10 mA; Pins 2 & 3 Open	1, 2, 3	6.0	6.6	8.0	V		
		V_{IHC3}	$V_{IHC3} = V_2 - V_3$; V_3 = GND; I_{IN} = 13.5 mA; Pins 1 & 4 Open	1, 2, 3		12.0	14.0	V		
Input Current		I_{IN}	$V_{IN} = V_2 - V_3$ = 5.0 V; Pins 1 & 4 Open	1, 2, 3	3.0	3.9	4.5	mA	4	
Logic Low Output Voltage		V_{OL}	V_{CC} = 4.5 V; I_{OL} = 2.6 mA	1, 2, 3		0.05	0.4	V	4	7
Logic High Output Current		I_{OH}	$V_{OH} = V_{CC}$ = 18 V	1, 2, 3			250	µA		
Logic Low Supply Current		I_{CCL}	$V_2 - V_3$ = 5.0 V; V_O = Open; V_{CC} = 18 V	1, 2, 3		0.8	3.0	mA		
Logic High Supply Current		I_{CCH}	V_{CC} = 18 V; V_O = Open 45% RH, t = 5 s;	1, 2, 3		0.001	20	mA	5	
Input-Output Insulation		I_{I-O}	V_{I-O} = 1500 Vdc; T_A = 25° C	1			1	µA		9, 10

Electrical Characteristics T_A = -55° C to 125° C, V_{CC} = 5.0 V, unless otherwise specified (continued)

Parameter	Symbol	Conditions		Group A Subgroup	Min.	Typ.*	Max.	Units	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}	R_L = 1.8 kΩ, C_L = 15 pF		9, 10, 11		4	20	µs	6, 7	6, 11
Propagation Delay Time to Logic High Output Level	t_{PLH}	R_L = 1.8 kΩ, C_L = 15 pF		9, 10, 11		8	40	µs		6, 12
Logic High Common Mode Transient Immunity	$\|CM_H\|$	V_{CM} = 50 V	T_A = 25° C	9	1000	≥ 10,000		V/µs	8	13, 14, 17
		V_{CM} = 450 V	I_{IN} = 0 mA			≥ 10,000				
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	V_{CM} = 50 V	T_A = 25° C	9	1000	≥ 5,000		V/µs		
		V_{CM} = 250 V	I_{IN} = 4 mA			≥ 5,000				

* All typical values are at T_A = 25° C, V_{CC} = 5 V unless otherwise noted.

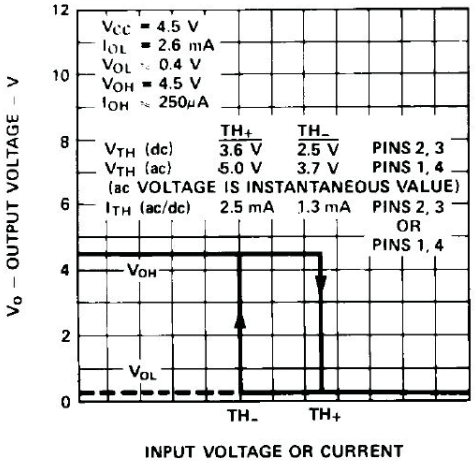


Figure 1. Typical transfer characteristics.

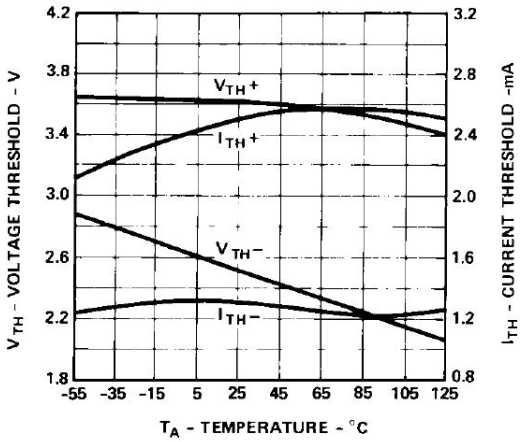


Figure 2. Typical dc threshold levels vs. temperature.

Typical Characteristics All typical values are at T_A = 25° C, V_{CC} = 5 V, unless otherwise specified.

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Hysteresis	I_{HYS}	1.2	mA	$I_{HYS} = I_{TH+} - I_{TH-}$	1	
	V_{HYS}	1.1	V	$V_{HYS} = V_{TH+} - V_{TH-}$		
Input Clamp Voltage	V_{ILC}	-0.76	V	$V_{ILC} = V_2 - V_3$; V_3 = GND; I_{IN} = -10 mA		
Bridge Diode Forward Voltage	$V_{D1,2}$	0.62		I_{IN} = 3 mA (see schematic)		
	$V_{D3,4}$	0.73				
Input-Output Resistance	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 Vdc		9
Input-Output Capacitance	C_{I-O}	2.0	pF	f = 1 MHz, V_{I-O} = 0 Vdc		
Input Capacitance	C_{IN}	50	pF	f = 1 MHz; V_{IN} = 0 V, Pins 2 & 3, Pins 1 & 4 Open		
Output Rise Time (10-90%)	t_r	10	µs		7	
Output Fall Time (90-10%)	t_f	0.5	µs		7	

Notes:

1. Maximum operating frequency is defined when output waveform (Pin 6) attains only 90% of V_{CC} with R_L = 1.8 kΩ, C_L = 15 pF using a 5 V square wave input signal.
2. Measured at a point 1.6 mm below seating plane.
3. Current into/out of any single lead.
4. Surge input current duration is 3 ms at 120 Hz pulse repetition rate. Transient input current duration is 10 µs at 120 Hz pulse repetition rate. Note that maximum input power, P_{IN}, must be observed.
5. Derate linearly above 100° C free-air temperature at a rate of 4.26 mW/°C. Maximum input power dissipation of 195 mW allows an input IC junction temperature of 150°C at an ambient temperature of T_A = 125° C with a typical thermal resistance from junction to ambient of θ_{JAi} = 235°C/W. The typical thermal resistance from junction to case is equal to 170°C/W. Excessive P_{IN} and T_J may result in device degradation.
6. The 1.8 kΩ load represents 1 TTL unit load of 1.6 mA and the 4.7 kΩ pull-up resistor.
7. Logic low output level at Pin 6 occurs under the conditions of $V_{IN} \geq V_{TH+}$ as well as the range of $V_{IN} > V_{TH}$ – once V_{IN} has exceeded V_{TH+}. Logic high output level at Pin 6 occurs under the conditions of $V_{IN} \leq V_{TH-}$ as well as the range of $V_{IN} < V_{TH+}$ once V_{IN} has decreased below V_{TH-}.
8. The AC voltage is instantaneous voltage.
9. Device considered a two terminal device: Pins 1, 2, 3, 4 connected together, Pins 5, 6, 7 8 connected together.
10. This is a momentary withstand test, not an operating condition.
11. The t_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 µs rise time) to the 1.5 V level on the leading edge of the output pulse (see Figure 7).
12. The t_{PLH} propagation delay is measured from the 2.5 V level of the trailing edge of a 5.0 V input pulse (1 µs fall time) to the 1.5 V level on the trailing edge of the output pulse (see Figure 7).
13. Common mode transient immunity in Logic High level is the maximum tolerable $dV_{CM/dt}$ of the common mode voltage, V_{CM}, to ensure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in Logic Low level is the maximum tolerable $dV_{CM/dt}$ of the common mode voltage, V_{CM}, to ensure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V). See Figure 8.
14. In applications where $dV_{CM/dt}$ may exceed 50,000 V/µs (such as static discharge), a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value for R_{CC} is 240 Ω per volt of allowable drop in V_{CC} (between Pin 8 and V_{CC}) with a minimum value of 240 Ω.
15. D_1 and D_2 are Schottky diodes; D_3 and D_4 are zener diodes.
16. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD, Class H and Class K parts receive 100% testing at 25, 125, and -55° C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively.)
17. Parameters shall be tested as part of device initial characterization and after process changes. Parameters shall be guaranteed to the limits specified for all lots not specifically tested.

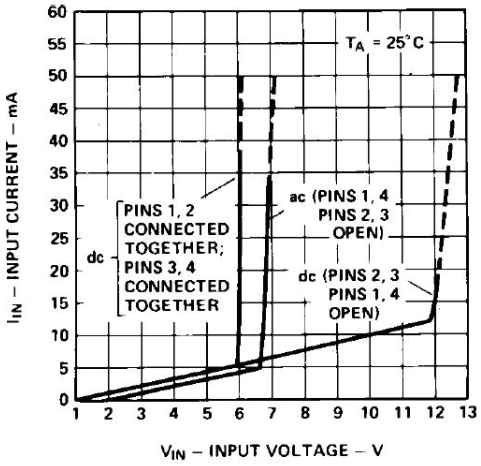


Figure 3. Typical input characteristics, I_{IN} vs. V_{IN}. (AC Voltage is Instantaneous Value.)

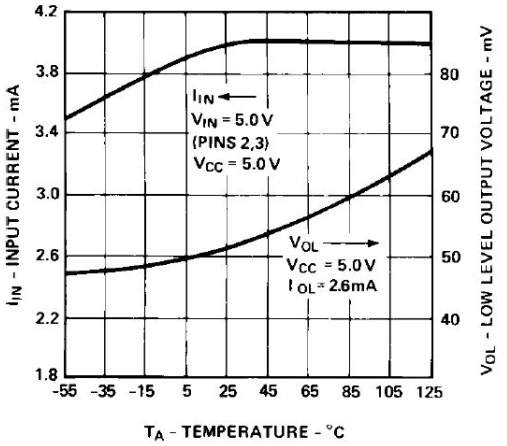


Figure 4. Typical input current, I_{IN}, and low level output voltage, V_{OL}, vs. temperature.

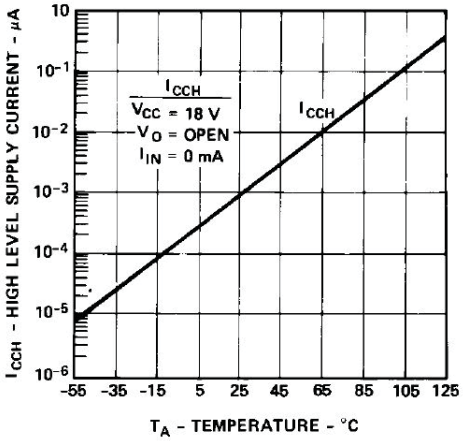


Figure 5. Typical high level supply current, I_{CCH} vs. temperature.

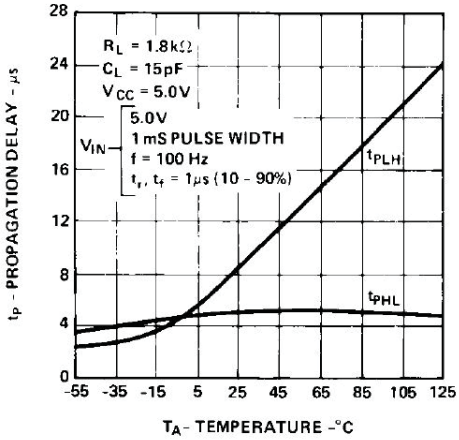


Figure 6. Typical propagation delay vs. temperature.

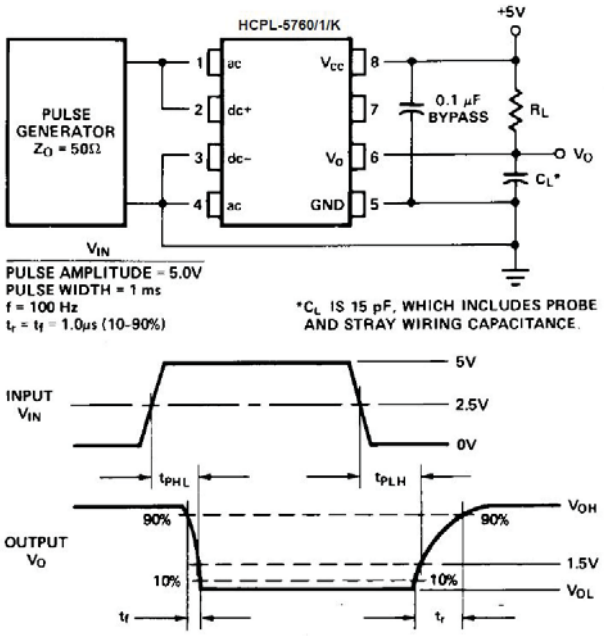


Figure 7. Switching test circuit.

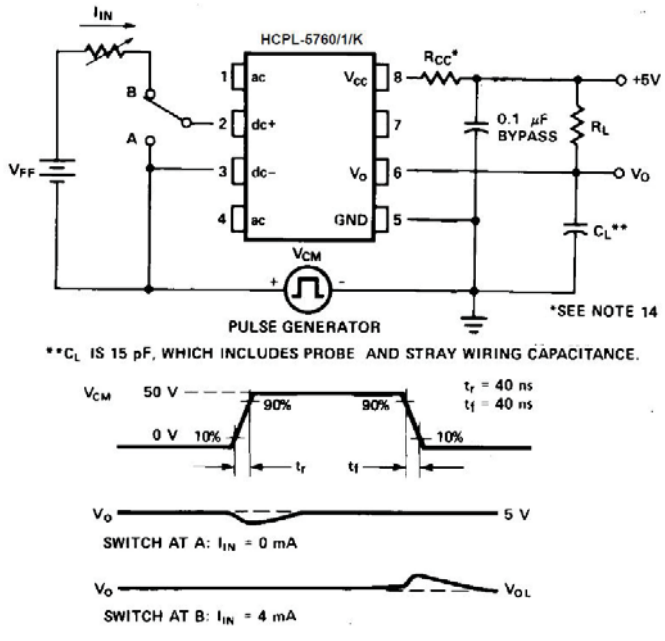


Figure 8. Test circuit for common mode transient immunity and typical waveforms.

Electrical Considerations

The HCPL-5760, HCPL-5761, HCPL-576K or 5962-89477 optocoupler has internal temperature compensated, predictable voltage and current threshold points which allow selection of an external resistor, R_x, to determine larger external threshold voltage levels. For a desired external threshold voltage, $V_{\pm}$, a corresponding typical value of R_x can be obtained from Figure 10. Specific calculation of R_x can be obtained from Equation (1) of Figure 11. Specification of both V_+ and V_- voltage threshold levels simultaneously can be obtained by the use of R_x and R_p as shown in Figure 11 and determined by Equations (2) and (3).

R_x can provide over-current transient protection by limiting input current during a transient condition. For monitoring contacts with a relay or switch, the HCPL-5760/1/K, or 5962-89477 combin-ation with R_x and R_p can be used to allow a specific current to be con-ducted through the contacts for cleaning purposes (wetting current).

The choice of which input voltage clamp level to choose depends upon the application of this device (see Figure 3). It is recommended that the low clamp condition be used when possible to lower the input power dissipation as well as the LED current, which minimizes LED degradation over time.

In applications where $dV_{CM/dt}$ may be extremely large (such as static discharge), a series resistor, R_{CC}, should be connected in series with V_{CC} and Pin 8 to protect the detector IC from destructively high surge currents. See note 14 for determination of R_{CC}. In addition, it is recommended that a ceramic disc bypass capacitor of 0.01 μF to 0.1 μF be placed between Pins 8 and 5 to reduce the effect of power supply noise.

For interfacing ac signals to TTL systems, output low pass filtering can be performed with a pullup resistor of 1.5 kΩ and 20 μF capacitor. This application requires a Schmitt trigger gate to avoid slow rise time chatter problems. For ac input applications, a filter capacitor can be placed across the dc input terminals for either signal or transient filtering.

Either AC (Pins 1, 4) or DC (Pins 2, 3) input can be used to determine external threshold levels.

For one specifically selected external threshold voltage level V_+ or V_-, R_x can be determined without use of R_p via

$$R_x = \frac{V_{+(-)} - V_{TH+(-)}}{I_{TH+(-)}} \qquad (1)$$

For two specifically selected external threshold voltage levels, V_+ and V_-, the use of R_x and R_p will permit this selection via equations (2), (3) provided the following conditions are met:

$$\frac{V_+}{V_-} \geq \frac{V_{TH+}}{V_{TH-}} \text{ and } \frac{V_+ - V_{TH+}}{V_- - V_{TH-}} < \frac{I_{TH+}}{I_{TH-}}$$

$$R_x = \frac{V_{TH+}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_{TH-}) - I_{TH-}(V_{TH+})} \qquad (2)$$

$$R_p = \frac{V_{TH+}(V_+) - V_{TH+}(V_-)}{I_{TH+}(V_- - V_{TH-}) - I_{TH-}(V_{TH+} - V_+)} \qquad (3)$$

See Application Note 1004 for more information.

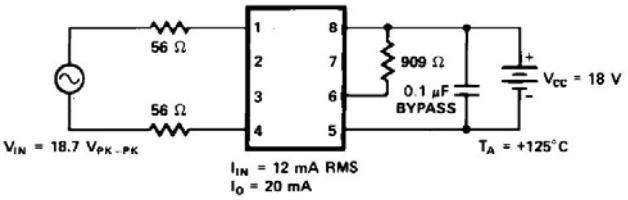


Figure 9. Operating circuit for burn-in and steady state life tests.

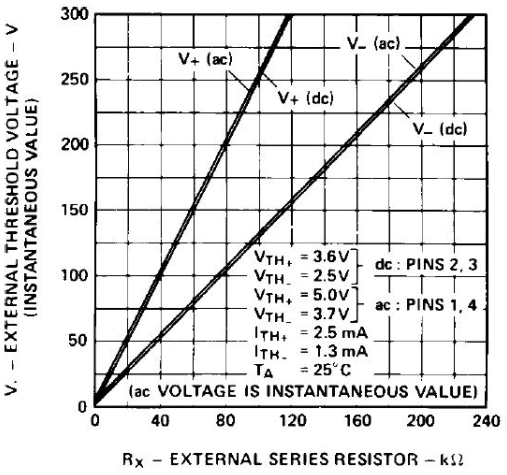


Figure 10. Typical external threshold characteristic, $V_{\pm}$ vs. R_x.

MIL-PRF-38534 Class H, Class K, and DLA SMD Test Program

Avago Technologies' Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H and K. Class H and Class K devices are also in compliance with DLA drawing 5962-89477.

Testing consists of 100% screening and quality confor-mance inspection to MIL-PRF-38534.

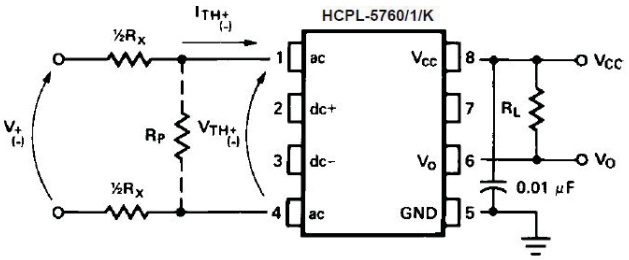


Figure 11. External threshold voltage level selection.

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