HCPL-520x, HCPL-523x, HCPL-623x, HCPL-625x, 5962-88768 and 5962-88769 [1]

Hermetically Sealed Low IF, Wide VCC, Logic Gate Optocouplers

Data Sheet

Description

These units are single, dual and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either commercial product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DLA Standard Microcircuit Drawing (SMD). All devices are manufactured and tested on a MIL-PRF-38534 certified line, and Class H and K devices are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains an AlGaAs light emitting diode that is optically coupled to an integrated high gain photon detector. The detector has a threshold with hysteresis, which provides differential mode noise immunity and eliminates the potential for output signal chatter. The detector in the single-channel units has a tri-state output stage that allows for direct connection to data buses. The output is noninverting. The detector IC has an internal shield that provides a guaranteed common mode transient immunity of up to 10,000 V/µs. Improved power supply rejection eliminates the need for special power supply bypass precautions.

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Features

- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- Manufactured and tested on a MIL-PRF-38534 certified line
- QML-38534, Class H and K
- Four hermetically sealed package configurations
- Performance guaranteed over –55°C to +125°C
- Wide V_{CC} range (4.5V to 20V)
- 350 ns maximum propagation delay
- CMR: > 10,000 V/µs typical
- 1500 Vdc withstand test voltage
- Three-state output available
- High radiation immunity
- HCPL-2200/31 function compatibility
- Reliability data available
- Compatible with LSTTL, TTL, and CMOS logic

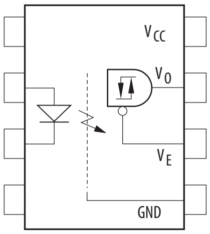
Applications

- Military and space
- High reliability systems
- Transportation and life critical systems
- High-speed line receiver
- Isolated bus driver (single channel)
- Pulse transformer replacement
- Ground loop elimination
- Harsh industrial environments
- Computer-peripheral interfaces

1. See Selection Guide–Package Styles and Lead Configuration Options for available extensions.

Functional Diagram

Multiple-channel devices are available.



Package styles for these parts are 8-pin DIP through hole (case outline P), 16-pin DIP flat pack (case outline F), and leadless ceramic chip carrier (case outline 2). Devices can be purchased with a variety of lead bend and plating options. See Selection Guide–Package Styles and Lead Configuration Options for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

Truth Tables

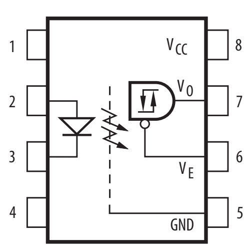
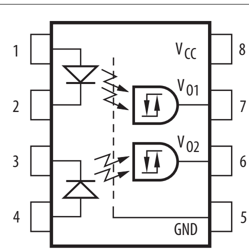
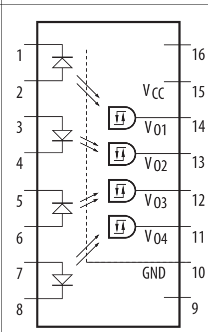
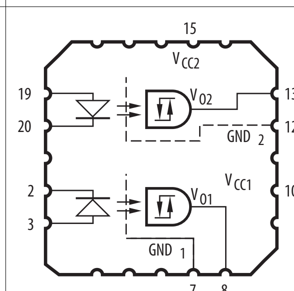
(Positive Logic)

Multichannel Devices	
Input	**Output**
On (H)	H
Off (L)	L

Single Channel Devices		
Input	**Enable**	**Output**
On (H)	H	Z
Off (L)	H	Z
On (H)	L	H
Off (L)	L	L

NOTE A 0.1-µF bypass capacitor must be connected between V_{CC} and GND pins.

Functional Diagrams

8-Pin DIP	8-Pin DIP	16-Pin Flat Pack	20-Pad LCCC
Through Hole	Through Hole	Unformed Leads	Surface Mount
1 Channel	2 Channels	4 Channels	2 Channels
			

NOTE Multichannel DIP and flat pack devices have common V_{CC} and ground. Single-channel DIP has an enable pin 6. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections. All diagrams are top view.

Selection Guide–Package Styles and Lead Configuration Options

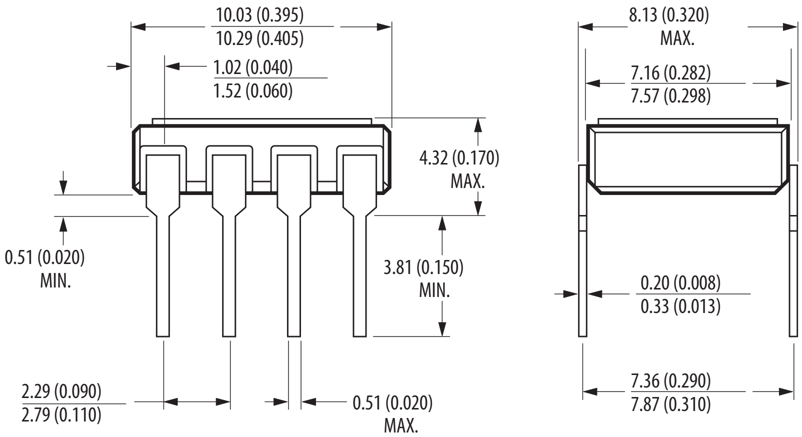
Package	8-Pin DIP	8-Pin DIP	16-Pin Flat Pack	20-Pad LCCC
Lead Style	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	1	2	4	2
Common Channel Wiring	None	V_{CC} GND	V_{CC} GND	None
Part Numbers and Options				
Commercial	HCPL-5200	HCPL-5230	HCPL-6250	HCPL-6230
MIL-PRF-38534 Class H	HCPL-5201	HCPL-5231	HCPL-6251	HCPL-6231
MIL-PRF-38534 Class K	HCPL-520K	HCPL-523K	HCPL-625K	HCPL-623K
Standard Lead Finish	Gold Plate[a]	Gold Plate[a]	Gold Plate[a]	Solder Pads[b]
Solder Dipped[b]	Option 200	Option 200		
Butt Joint/Gold Plate[a]	Option 100	Option 100		
Gull Wing/Soldered[b]	Option 300	Option 300		
Class H SMD Part Number				
Prescript for all below	5962-	5962-	5962-	5962-
Gold Plate[a]	8876801PC	8876901PC	8876903FC	
Solder Dipped[b]	8876801PA	8876901PA		88769022A
Butt Joint/Gold Plate[a]	8876801YC	8876901YC		
Butt Joint/Soldered[b]	8876801YA	8876901YA		
Gull Wing/Soldered[b]	8876801XA	8876901XA		
Class K SMD Part Number				
Prescript for all below	5962-	5962-	5962-	5962-
Gold Plate[a]	8876802KPC	8876904KPC	8876906KFC	
Solder Dipped[b]	8876802KPA	8876904KPA		8876905K2A
Butt Joint/Gold Plate[a]	8876802KYC	8876904KYC		
Butt Joint/Soldered[b]	8876802KYA	8876904KYA		
Gull Wing/Soldered[b]	8876802KXA	8876904KXA		

a. Gold Plate lead finish: Maximum gold thickness of leads is <100 micro inches. Typical is 60 to 90 micro inches.

b. Solder lead finish: Sn63/Pb37.

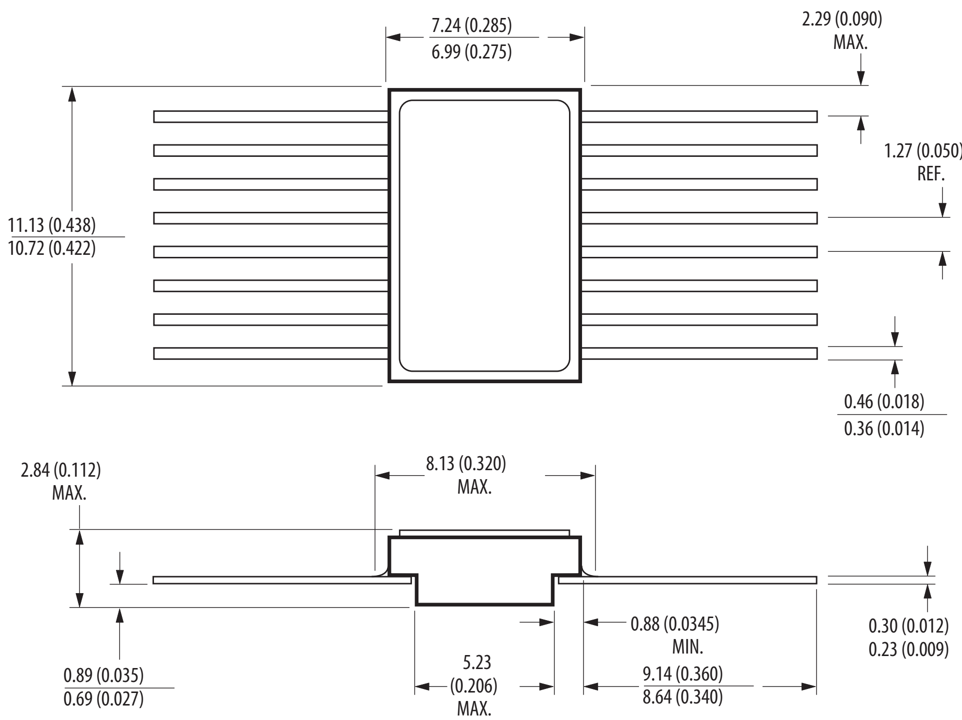
Outline Drawings

8-Pin DIP Through Hole, 1 and 2 Channel



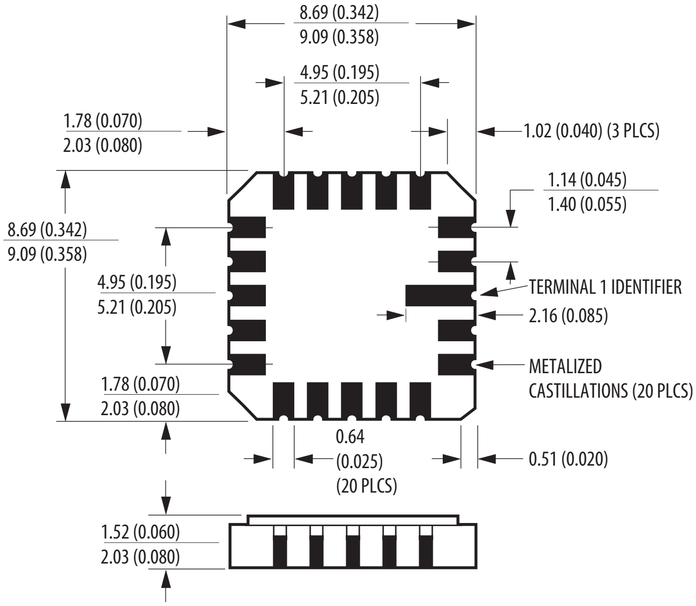
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

16-Pin Flat Pack, 4 Channels



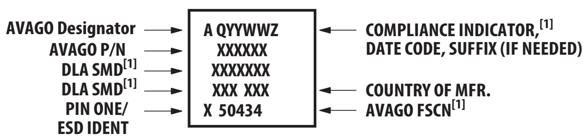
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

20-Terminal LCCC Surface Mount, 2 Channels



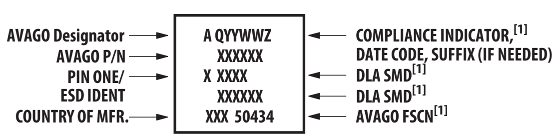
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

Leaded Device Marking



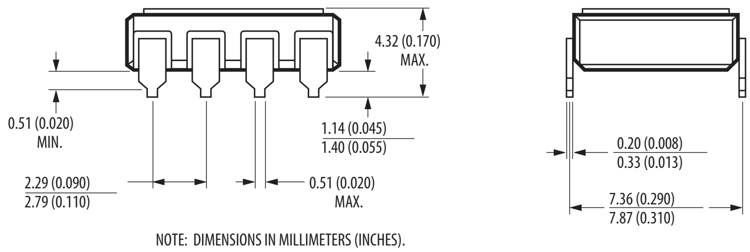
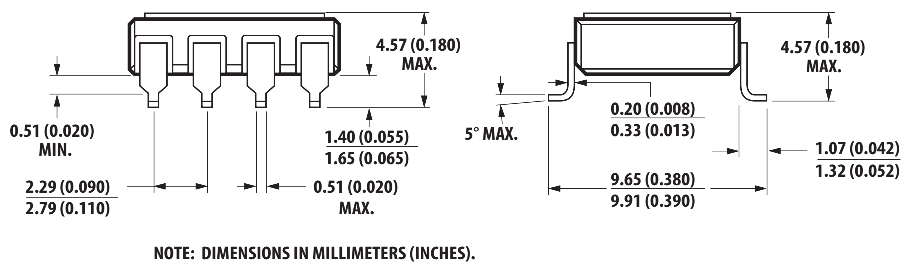
[1] QML PARTS ONLY

Leadless Device Marking



[1] QML PARTS ONLY

Hermetic Optocoupler Options

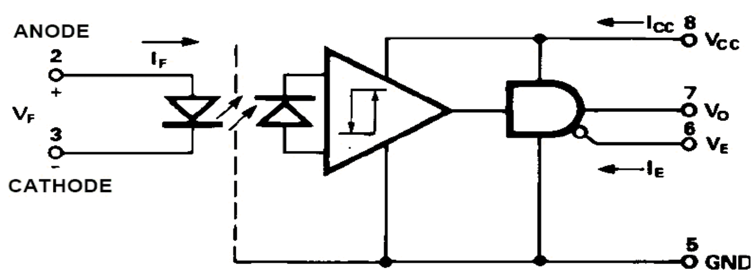
Option	Description
100	Surface-mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H and Class K product in 8-pin DIP. 
200	Lead finish is solder dipped rather than gold plated. This option is available on Commercial, Class H and Class K product in 8-pin DIP. DLA Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder-dipped terminals as a standard feature.
300	Surface-mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on Commercial, Class H and Class K product in 8-pin DIP. This option has solder-dipped leads. 

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_S	–65	+150	°C
Operating Ambient Temperature	T_A	–55	+125	°C
Junction Temperature	T_J	—	+175	°C
Case Temperature	T_C	—	+170	°C
Lead Solder Temperature		—	260 for 10 s	°C
Average Forward Current, each channel	$I_{F\ AVG}$	—	8	mA
Peak Input Current, each channel	I_{FPK}	—	20[a]	mA
Reverse Input Voltage, each channel	V_R	—	3	V
Average Output Current, each channel	I_O	—	15	mA
Supply Voltage	V_{CC}	0.0	20	V
Output Voltage, each channel	V_O	–0.3	20	V
Package Power Dissipation, each channel	P_D	—	200	mW
Single-Channel Product Only				
Tri-State Enable Voltage	V_E	–0.3	20	V

a. Peak Forward Input Current pulse width <50 µs at 1-KHz maximum repetition rate.

8-Pin Ceramic DIP Single-Channel Schematic



Note: Enable pin 6. An external 0.01-µF to 0.1-µF bypass capacitor is recommended between VCC and ground for each package type.

ESD Classification

(MIL-STD-883, Method 3015)	
HCPL-5200/01/0K and HCPL-6230/31/3K	▲, Class 1
HCPL-5230/31/3K and HCPL-6250/51/5K	●, Class 3

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	20	V
Input Current, High Level, Each Channel	I_{FH}	2	8	mA
Input Voltage, Low Level, Each Channel	V_{FL}	0	0.8	V
Fan Out (TTL Load), Each Channel	N	—	4	
Single Channel Product Only				
High Level Enable Voltage	V_{EH}	2.0	20	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

Electrical Characteristics

T_A = −55°C to +125°C, 4.5V ≤ V_{CC} ≤ 20V, 2 mA ≤ $I_{F(ON)}$ ≤ 8 mA, 0V ≤ $V_{F(OFF)}$ ≤ 0.8V, unless otherwise specified.

Parameter		Symbol	Group A Sub-groups[a]	Test Conditions		Limits			Unit	Fig	Notes
						Min	Typ[b]	Max			
Logic Low Output Voltage		V_{OL}	1, 2, 3	I_{OL} = 6.4 mA (4 TTL Loads)		—	—	0.5	V	1, 3	c
Logic High Output Voltage		V_{OH}	1, 2, 3	I_{OH} = −2.6 mA (**$V_{OH} = V_{CC} − 2.1V$)		2.4	**	—	V	2, 3	c
			NA	I_{OH} = −0.32 mA		—	3.1	—			
Output Leakage Current ($V_{OUT} > V_{CC}$)		I_{OHH}	1, 2, 3	V_O = 5.5V	I_F = 8 mA, V_{CC} = 4.5V	—	—	100	µA		c
				V_O = 20V		—	—	500			
Logic Low Supply Current	Single Channel	I_{CCL}	1, 2, 3	V_{CC} = 5.5V	V_F = 0V, V_E = Don't Care	—	4.5	6	mA		
				V_{CC} = 20V		—	5.3	7.5			
	Dual Channel			V_{CC} = 5.5V	$V_{F1} = V_{F2}$ = 0V	—	9.0	12			
				V_{CC} = 20V		—	10.6	15			
	Quad Channel			V_{CC} = 5.5V	$V_{F1} = V_{F2} = V_{F3} = V_{F4}$ = 0V	—	14	24			
				V_{CC} = 20V		—	17	30			
Logic High Supply Current	Single Channel	I_{CCH}	1, 2, 3	V_{CC} = 5.5V	I_F = 8 mA, V_E = Don't Care	—	2.9	4.5	mA		
				V_{CC} = 20V		—	3.3	6			
	Dual Channel			V_{CC} = 5.5V	$I_{F1} = I_{F2}$ = 8 mA	—	5.8	9			
				V_{CC} = 20V		—	6.6	12			
	Quad Channel			V_{CC} = 5.5V	$I_{F1} = I_{F2} = I_{F3} = I_{F4}$ = 8 mA	—	9	18			
				V_{CC} = 20V		—	11	24			
Logic Low Short Circuit Output Current		I_{OSL}	1, 2, 3	$V_O = V_{CC}$ = 5.5V	V_F = 0V	20			mA		c, d
				$V_O = V_{CC}$ = 20V		35					
Logic High Short Circuit Output Current		I_{OSH}	1, 2, 3	V_{CC} = 5.5V	I_F = 8 mA, V_O = GND	—	—	−10	mA		c, d
				V_{CC} = 20V		—	—	−25			
Input Forward Voltage		V_F	1, 2, 3	I_F = 8 mA		1.0	1.3	1.8	V	4	c
Input Reverse Breakdown Voltage		BV_R	1, 2, 3	I_R = 10 mA		3	—		V		c
Input-Output Insulation Leakage Current		I_{I-O}	1	V_{I-O} = 1500 Vdc, t = 5s, RH ≤ 65%, T_A = 25°C		—	—	1.0	µA		e, f
Logic High Common Mode Transient Immunity		$\|CM_H\|$	9, 10, 11	I_F = 2 mA, V_{CM} = 50 V_{P-P}		1000	10,000		V/µs	9	c, g, h

Parameter	Symbol	Group A Sub-groups[a]	Test Conditions	Limits			Unit	Fig	Notes
				Min	Typ[b]	Max			
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	9, 10, 11	$I_F = 0$ mA, $V_{CM} = 50V_{P-P}$	1000	10,000		V/µs	9	c, g, h
Propagation Delay Time to Logic Low	t_{PHL}	9, 10, 11		—	173	350	ns	5, 6	c, i
Propagation Delay Time to Logic High	t_{PLH}	9, 10, 11		—	118	350	ns	5, 6	c, i

a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD, Class H and Class K parts receive 100% testing at 25, 125, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

b. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$, $I_{F(ON)} = 5$ mA unless otherwise specified.

c. Each channel of a multichannel device.

d. Duration of output short circuit time not to exceed 10 ms.

e. All devices are considered two-terminal devices: measured between all input leads or terminals shorted together and all output leads or terminals shorted together.

f. This is a momentary withstand test, not an operating condition.

g. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8V$). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0V$).

h. Parameters are tested as part of device initial characterization and after design and process changes. Parameters guaranteed to limits specified for all lots not specifically tested.

i. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.

Electrical Characteristics - Single Channel Product Only

$T_A = -55°C$ to $+125°C$, $4.5V \le V_{CC} \le 20V$, $2\ mA \le I_{F(ON)} \le 8\ mA$, $0V \le V_{F(OFF)} \le 0.8V$, unless otherwise specified.

Parameter	Symbol	Group A, Sub-groups[a]	Test Conditions		Limits			Unit
					Min	Typ[b]	Max	
High Impedance State Output Current	I_{OZL}	1, 2, 3	$V_O = 0.4V$	$V_{EN} = 2V$, $V_F = 0V$	—	—	–20	µA
	I_{OZH}	1, 2, 3	$V_O = 2.4V$	$V_{EN} = 2V$, $I_F = 8$ mA	—	—	20	µA
			$V_O = 5.5V$		—	—	100	
			$V_O = 20V$		—	—	500	
Logic High Enable Voltage	V_{EH}	1, 2, 3			2.0			V
Logic Low Enable Voltage	V_{EL}	1, 2, 3			—	—	0.8	V
Logic High Enable Current	I_{EH}	1, 2, 3	$V_{EN} = 2.7V$		—	—	20	µA
			$V_{EN} = 5.5V$		—	—	100	
			$V_{EN} = 20V$		—	0.004	250	
Logic Low Enable Current	I_{EL}	1, 2, 3	$V_{EN} = 0.4V$		—	—	–0.32	mA

a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD, Class H and Class K parts receive 100% testing at 25, 125, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

b. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$, $I_{F(ON)} = 5$ mA unless otherwise specified.

Typical Characteristics

All typical values are at $T_A = 25°C$, $V_{CC} = 5V$, $I_{F(ON)} = 5$ mA.

Parameter	Symbol	Test Conditions	Typ	Unit	Fig	Notes
Input Current Hysteresis	I_{HYS}	$V_{CC} = 5V$	0.07	mA	3	a
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	$I_F = 8$ mA	–1.25	mV/°C		a
Resistance (Input-Output)	R_{I-O}	$V_{I-O} = 500$ Vdc	10^{13}	Ω		a, b
Capacitance (Input-Output)	C_{I-O}	f = 1 MHz	2.0	pF		a, b
Input Capacitance	C_{IN}	$V_F = 0$ V, f = 1 MHz	20	pF		a, c
Output Rise Time (10% to 90%)	t_r		45	ns	5, 7	a
Output Fall Time (90% to 10%)	t_f		10	ns	5, 7	a
Single-Channel Product Only						
Output Enable Time to Logic High	t_{PZH}		30	ns	8	
Output Enable Time to Logic Low	t_{PZL}		30	ns	8	
Output Disable Time from Logic High	t_{PHZ}		45	ns	8	
Output Disable Time from Logic Low	t_{PLZ}		55	ns	8	
Multi-Channel Product Only						
Input-Input Insulation Leakage Current	I_{I-I}	RH ≤ 65%, $V_{I-I} = 500V$, t = 5s	0.5	nA		d
Resistance (Input-Input)	R_{I-I}	$V_{I-I} = 500V$	10^{13}	Ω		d
Capacitance (Input-Input)	C_{I-I}	f = 1 MHz	1.5	pF		d

a. Each channel of a multichannel device.

b. Measured between each input pair shorted together and all output connections for that channel shorted together.

c. Zero-bias capacitance measured between the LED anode and cathode.

d. Measured between adjacent input pairs shorted together for each multichannel device.

Figure 1 Typical Logic Low Output Voltage vs. Temperature

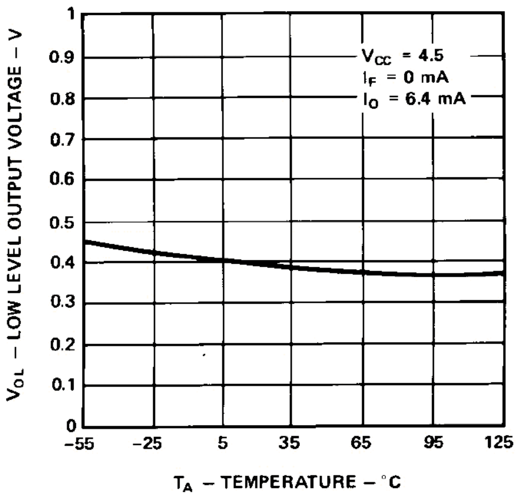


Figure 2 Typical Logic High Output Current vs. Temperature

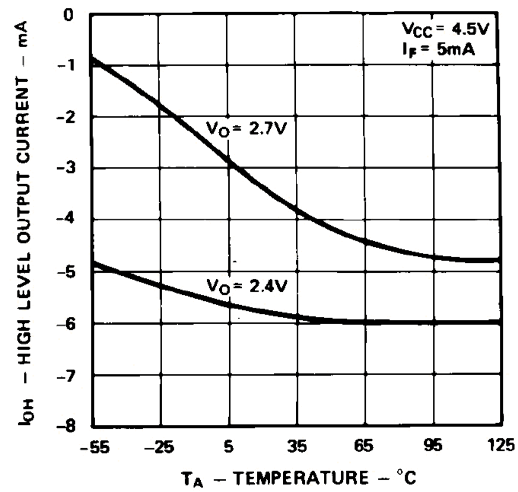


Figure 3 Output Voltage vs. Forward Input Current

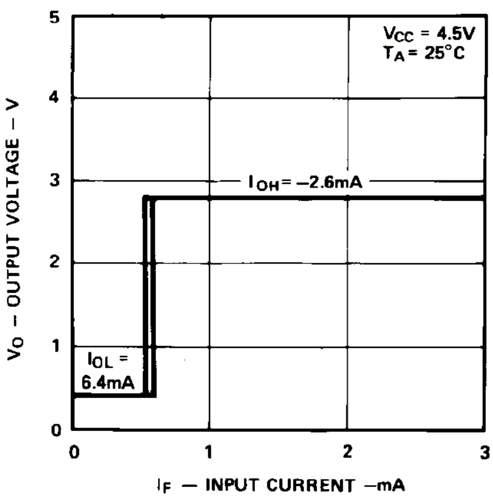


Figure 4 Typical Diode Input Forward Characteristic

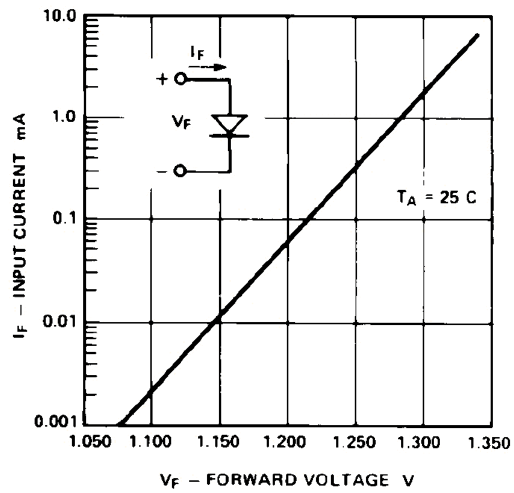


Figure 5 Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f

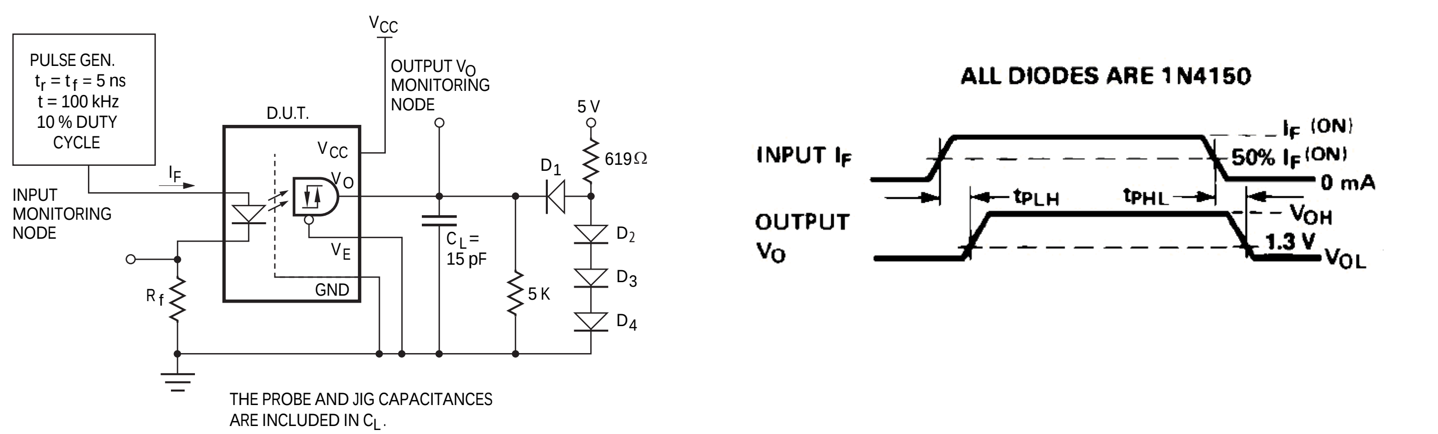


Figure 6 Typical Propagation Delay vs. Temperature

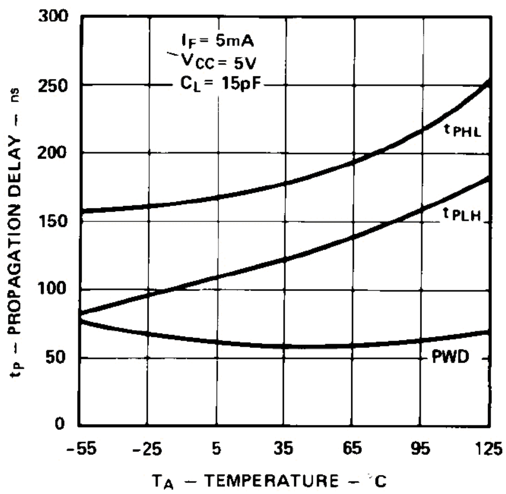


Figure 7 Typical Rise, Fall Time vs. Temperature

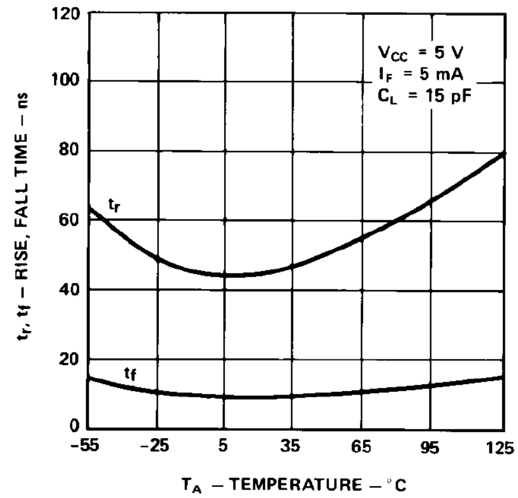


Figure 8 Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}

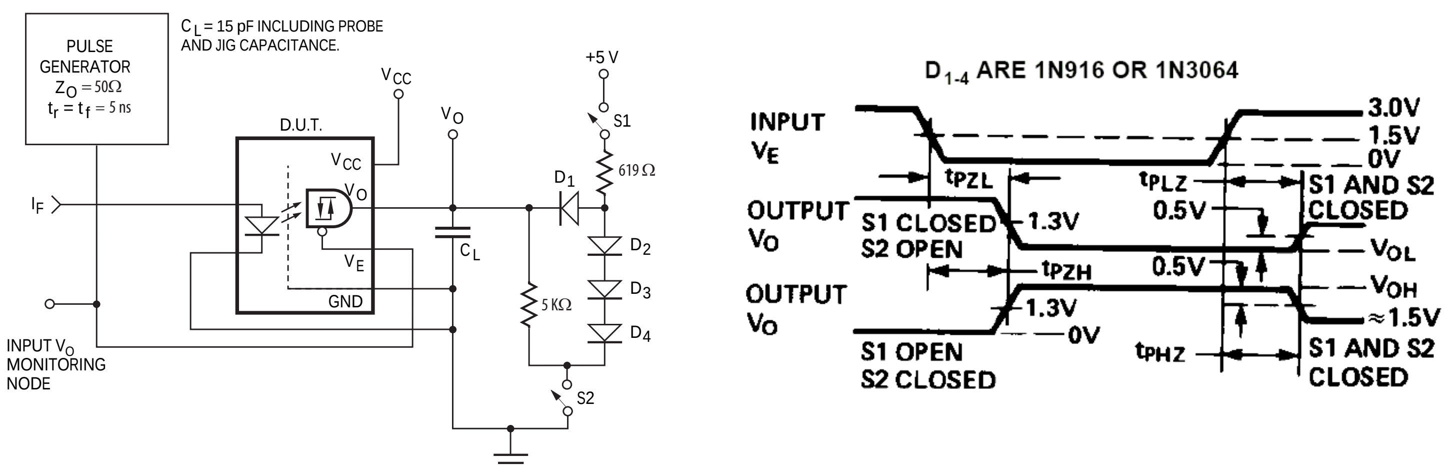


Figure 9 Test Circuit for Common Mode Transient Immunity and Typical Waveforms

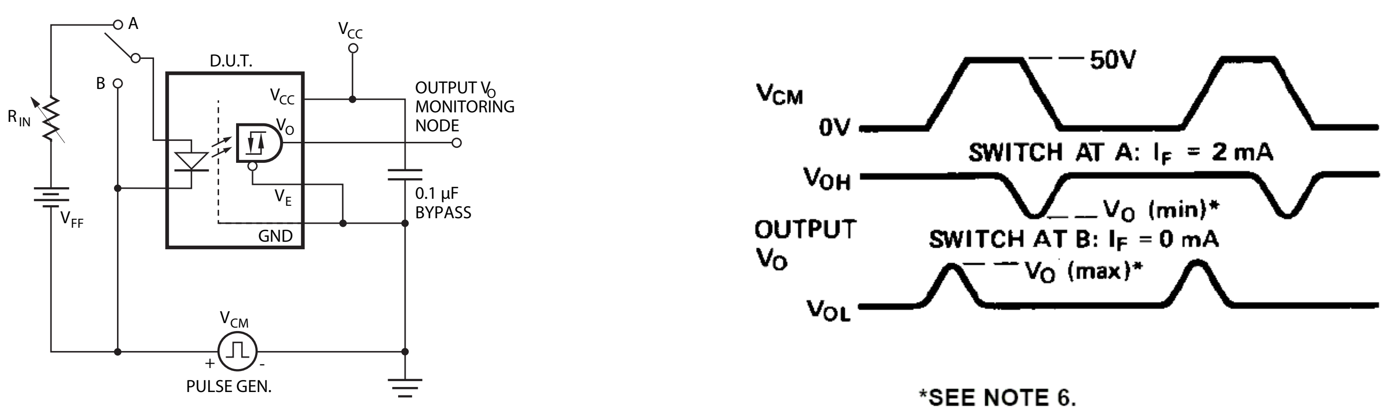


Figure 10 LSTTL to CMOS Interface Circuit

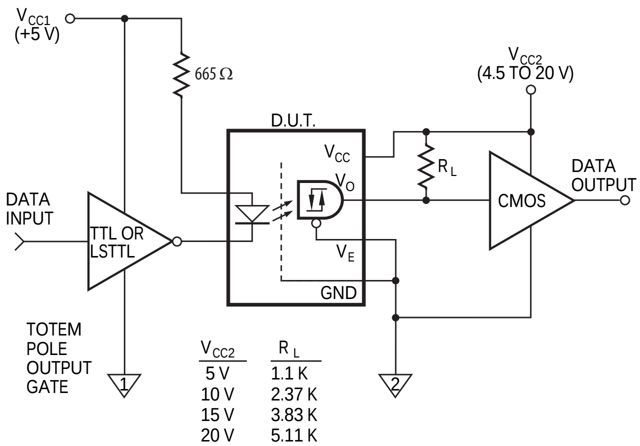


Figure 11 Recommended LED Drive Circuit

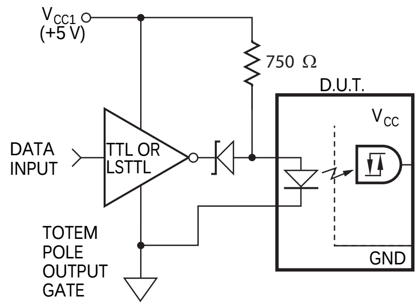


Figure 12 Series LED Drive with Open Collector Gate (4.02 kΩ Resistor Shunts I_{OH} from the LED)

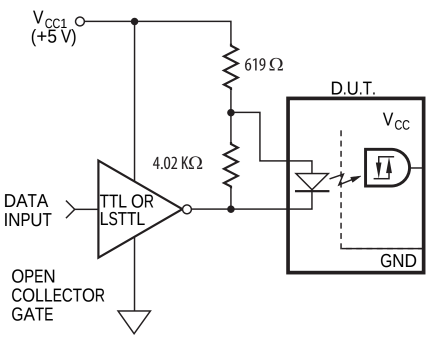


Figure 13 Recommended LSTTL to LSTTL Circuit

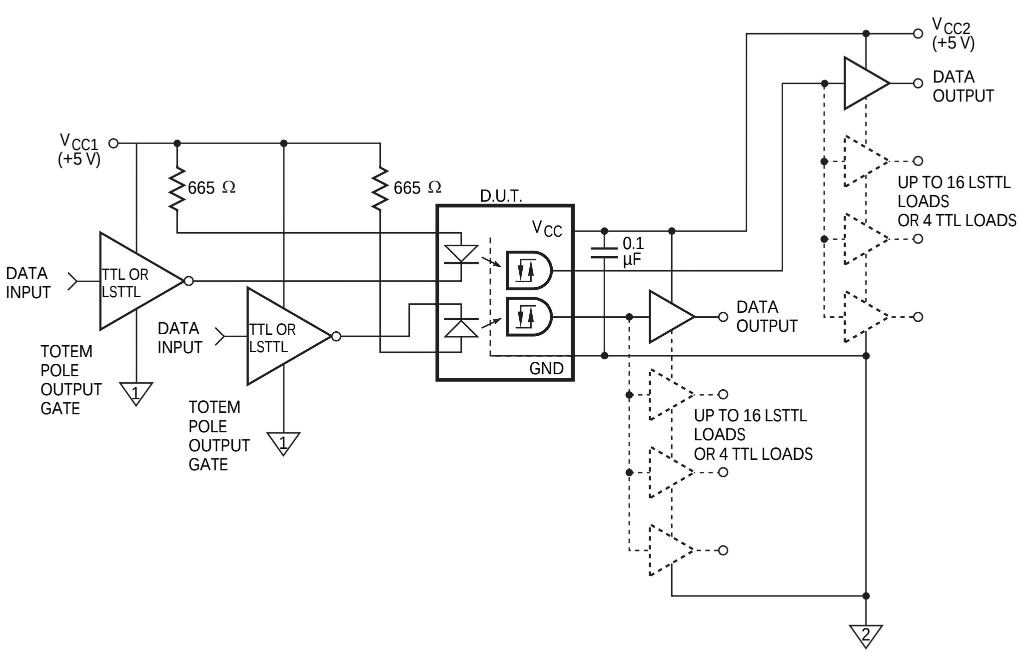
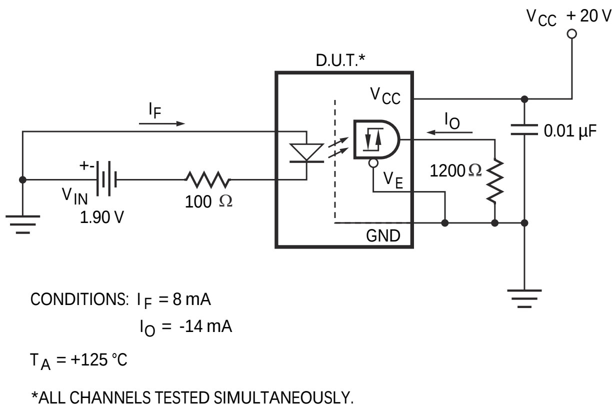


Figure 14 Single-Channel Operating Circuit for Burn-in and Steady State Life Tests



For product information and a complete list of distributors, please go to our web site: www.broadcom.com.

AV02-3840EN – January 6, 2017