Product Brief

PEX8605, PCI Express Gen 2 Switch, 4 Lanes, 4 Ports

Highlights

- **PEX8605 General Features**
  - 4-lane, 4-port PCIe Gen2 switch
    - Integrate 5.0 GT/s SerDes
  - 10 x 10mm^2, 136-pin aQFN package
  - Typical Power: 0.8 Watts

- **PEX8605 Key Features**
  - **Standards Compliant**
    - PCI Express Base Specification, r2.1 (backwards compatible w/ PCIe 1.0a/1.1)
    - PCI Power Management Spec, r1.2
    - Microsoft Windows 7 Compliant
    - Dynamic SerDes speed control
  - **High Performance**
    - Non-blocking switch fabric
    - Full line rate on all ports
    - Packet Cut-Thru with 250ns max packet latency (x1 to x1)
    - 256B Max Payload Size
  - **Flexible Configuration**
    - Ports configurable as x1, x2
    - Registers configurable with strapping pins, EEPROM, I^{2}C, or host software
    - Reference Clock Buffered Output signals for downstream ports
    - Lane and polarity reversal
    - Compatible with PCIe 1.0a PM
  - **Quality of Service (QoS)**
    - Eight traffic classes per port
    - Round-robin source port arbitration
    - Relaxed PCI Ordering
  - **Reliability, Availability, Serviceability**
    - visionPAK™
      - Per Port Performance Monitoring
      - Per port payload & header counters
      - SerDes Eye Capture
      - Error Injection and Loopback
    - All ports hot plug capable thru I^{2}C (Hot-Plug Controller on every port)
    - Data Path parity
    - Memory (RAM) Error Correction signals
    - INTA# and FATAL_ERR#
    - Advanced Error Reporting
    - Port Status bits and GPIO available
    - Per port error diagnostics
    - JTAG AC/DC boundary scan
  - **Power Management**
    - WAKE#, Beacon, Vaux support

The ExpressLane™ PEX8605 device offers PCI Express switching capability enabling users to add scalable high bandwidth non-blocking interconnection to a wide variety of applications including control plane applications, consumer applications and embedded systems. The PEX8605 is well suited for fan-out and peer-to-peer applications.

Low Packet Latency & High Performance

The PEX8605 architecture supports packet cut-thru with a maximum latency of 250ns in x1 to x1 configuration. This, combined with low power consumption and non-blocking internal switch architecture, provides full line rate on all ports for low-power applications such as consumer and embedded. The low latency enables applications to achieve high throughput and performance. In addition to low latency, the device supports a max payload size of 256 bytes.

Data Integrity

The PEX8605 provides end-to-end CRC protection (ECRC) and Poison bit support to enable designs that require guaranteed error-free packets. PLX also supports data path parity and memory (RAM) error correction as packets pass through the switch.

Power Management and Clock Buffering

The PEX8605 supports the following power management states: L0, L0s, L1, L2/L3 Ready, L2 and L3. Moreover, the PEX8605 supports Vaux along with the external signal WAKE# and the in-band Beacon for the PCIe endpoints to use to inform the system host to exit the low power savings mode.

The PEX 8605 supports three pairs of PCI Express-compliant, 100MHz, buffered HCSL output clocks, one pair for each downstream port of the switch. Each clock output pair can be disabled by software or serial EEPROM when not in use, for additional power savings. This feature greatly reduces system BOM cost by eliminating the need for extra clock buffers on the PCB.

Interoperability

The PEX8605 is designed to be fully compliant with the PCI Express Base Specification r2.1 and is backwards compatible to PCI Express Base Specification r1.1 and r1.0a. Additionally each port supports auto-negotiation and polarity reversal. Furthermore, the PEX8605 is designed for Microsoft Windows 7 compliance. All PLX switches undergo thorough interoperability testing in PLX's Interoperability Lab and compliance testing at the PCI-SIG plug-fest to ensure compatibility with PCI Express devices in the market.

Device Operation Configuration Flexibility

The PEX8605 provides several ways to configure its operations. The device can be configured through strapping pins, I^{2}C interface, CPU configuration cycles and/or an optional serial EEPROM. This allows for easy debug during the development phase and functional monitoring during the operation phase.

Flexible Port Configurations

The PEX8605 flexible architecture supports a number of port configurations as required by the target applications as shown in figure 1 below.

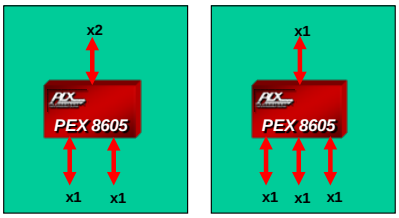

Figure 1. Port Configurations

SerDes Power and Signal Management

The PEX8605 provides low power capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be turned off when unused for even lower power. The PEX8605 supports software control of the SerDes outputs to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power – off, low, typical, and high. The SerDes block also supports loop-back modes and advanced reporting of error conditions, which enables efficient debug and management of the entire system.

Port Arbitration and QoS

The PEX8605 switch supports hardware fixed Round-Robin Ingress Port Arbitration. The PEX8605 also supports Eight Traffic Classes (TCs) as defined in the PCIe specification.

Applications

Suitable for fan-out, consumer, control plane applications, and embedded systems, PEX8605 is suited for a wide variety of form factors and applications.

Fan-Out

The PEX8605 switch, with its flexible configurations, allows user specific tuning to a variety of host-centric as well as peer-to-peer applications.

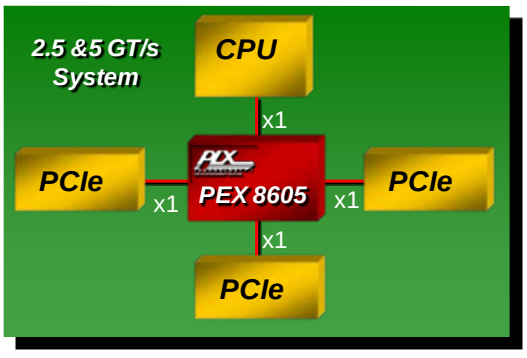

Figure 2. Fan-in/out Usage

Figure 2 shows a typical fan-out design, where the processor provides a PCI Express link that needs to be fanned into a larger number of smaller ports for a variety of I/O functions, each with different bandwidth requirements.

Multi-Function Printer

With its small footprint, the PEX8605 is ideal for consumer applications. Figure 3 shows a multi-function printer block diagram. The four ports in the PEX8605 provide connectivity between the processor to up to three peripherals each via an x1 connection. In this usage model, the PEX8605 provides connectivity to the processor as well as to the various ASICs.

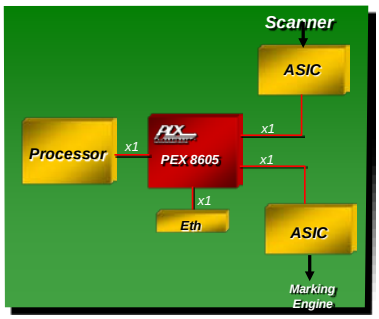

Figure 3. Printer Block Diagram

Digital TV Tuner

An example of a digital TV tuner is shown in Figure 4. In this example, the integrated SoC has a single PCIe connection. The PEX8605 is used to provide connection to the USB 3.0 endpoint, a gigabit Ethernet controller and a 3D graphics engine which are used to connect to other consumer peripherals, to a high speed home network and provide advanced graphics respectively.

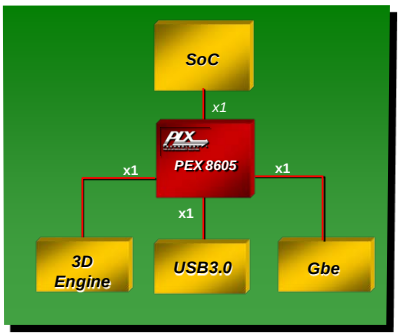

Figure 4. Digital TV Tuner Fan-in/out Usage

Bandwidth Bridge

There are four PCIe lanes available in the PEX8605. Each one can represent an individual port or alternatively two can be joined to form a x2 port. A x2 port can provide double the bandwidth of a x1 port when all lanes are operating at the same data rates (all at 2.5GT/s or 5.0GT/s). In some instances, the need to match the bandwidth between devices running at

different data rates (2.5GT/s vs 5.0GT/s) is required to sustain the performance of the faster device. Figure 5 provides an example where the PEX8605 is configured as x2, x1, x1. In this example, the x2 link is running at the lower data rate (2.5GT/s) while a single x1 port is running at the higher data rate (5.0 GT/s). In this usage model, the PEX8605 acts as a bridge between Gen 1 and Gen 2 devices allowing the faster device to operate at its full bandwidth capabilities.

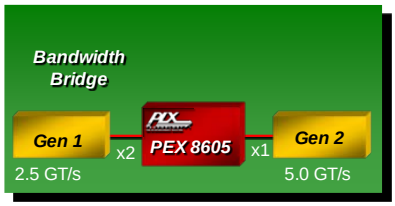

Figure 5. Gen 1 to Gen 2 Bandwidth Bridge

Software Usage Model

From a system model viewpoint, each PCI Express port is a virtual PCI to PCI bridge device and has its own set of PCI Express configuration registers. It is through the upstream port that the BIOS or host can configure the other ports using standard PCI enumeration. The virtual PCI-to-PCI bridges within the PEX8605 are compliant to the PCI and PCI Express system models. The Configuration Space Registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by type 0 configuration cycles through the virtual primary bus interface (matching bus number, device number, and function number).

Interrupt Sources/Events

The PEX8605 supports the INTx interrupt message type (compatible with PCI 2.3 Interrupt signals) or Message Signaled Interrupts (MSI) when enabled. Interrupts/messages are generated by PEX8605 for Hot-Plug events, doorbell interrupts, baseline error reporting, and advanced error reporting.

Development Tools

PLX offers hardware and software tools to enable rapid customer design activity. These tools consist of a hardware module (PEX8605 RDK), hardware documentation (available at www.plxtech.com), and a Software Development Kit (also available at www.plxtech.com).

ExpressLane PEX8605 RDK

The PEX8605 RDK is a hardware module containing the PEX8605 which plugs right into your system. The PEX8605 RDK can be used to test and validate customer software, or used as an evaluation vehicle for PEX8605 features and benefits. The PEX RDK provides everything that a user needs to get their hardware and software development started.

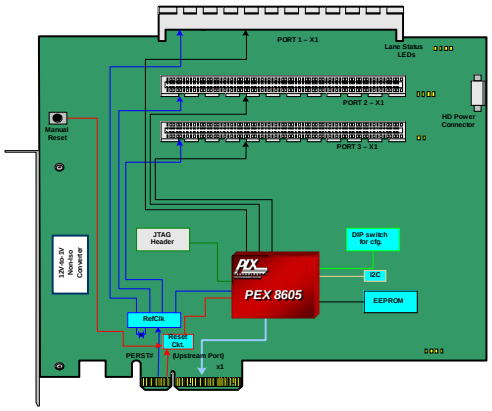

Figure 6. PEX8605 Rapid Development Kit

Software Development Kit (SDK)

PLX's Software Development Kit is available for download at www.plxtech.com/sdk. The software development kit includes drivers, source code, and interfaces to aid in configuring and debugging the PEX8605.

Both *performance*PAK and *vision*PAK are supported by PLX's RDK and SDK, the industry's most advanced hardware- and software-development kits.

Product Ordering Information

Part Number	Description
PEX8605-AA50NI G	4 Lane, 4 Port PCI Express Gen 2.0 Switch, Pb-Free (10x10mm^2 aQFN)
PEX8605-AA RDK	PEX 8605 Rapid Development Kit + CM108 (one x1 upstream port, three x1 downstream ports)
PEX 8605-AA-2U1D RDK	PEX 8605 Rapid Development Kit + CM107 (one x2 upstream port, two x1 downstream ports)

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