QCPL-341H

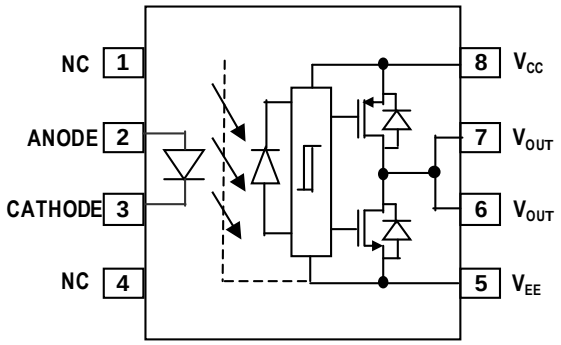
2.5 Amp Output Current IGBT Gate Drive Optocoupler

Preliminary Data Sheet

Description

The QCPL-341H contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving IGBT with ratings up to 1200V/100A. For IGBTs with higher ratings, this optocoupler can be used to drive a discrete power stage which drives the IGBT gate. The QCPL-341H has the highest insulation voltage of V_{IORM}= 630Vpeak in the IEC/ EN/DIN EN 60747-5-5.

Functional Diagram



Note: Design Note: A 1 µF bypass capacitor must be connected between pins V_{CC} and V_{EE}.

Truth Table

LED	V_{CC} – V_{EE} "POSITIVE GOING" (i.e., TURN-ON)	V_{CC} – V_{EE} "NEGATIVE GOING" (i.e., TURN-OFF)	V_O
OFF	0 - 30 V	0 – 30 V	LOW
ON	0 – 12.1V	0 – 11.1V	LOW
ON	12.1 - 13.5V	11.1 – 12.4V	TRANSITION
ON	13.5 – 30V	12.4 – 30V	HIGH

Features

- 2.5 A maximum peak output current
- 2.0 A minimum peak output current
- Rail-to-rail output voltage
- 300 ns maximum propagation delay
- 200 ns maximum propagation delay difference
- LED current input with hysteresis
- 25 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V
- I_{CC} = 5.0 mA maximum supply current
- Under Voltage Lock-Out protection (UVLO) with hysteresis
- Wide operating V_{CC} Range: 15 to 30 V
- Industrial temperature range: -40 °C to 105 °C
- Safety Approval Pending
  - UL Recognized 3750/5000 V_{RMS} for 1min.
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 630 V_{peak}

Applications

- IGBT/MOSFET gate drive
- AC and Brushless DC motor drives
- Renewable energy inverters
- Industrial inverters
- Switching power supp

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

QCPL-341H is UL Recognized with 3750 V_{RMS} for 1 minute per UL1577.

Part number	Option	Package	Surface Mount Gull Wing	Tape& Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
QCPL-341H	-000E	300mil DIP-8				50 per tube
	-300E		X			50 per tube
	-500E		X	X		1000 per reel
	-060E				X	50 per tube
	-360E		X		X	50 per tube
	-560E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

QCPL-341H-560E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

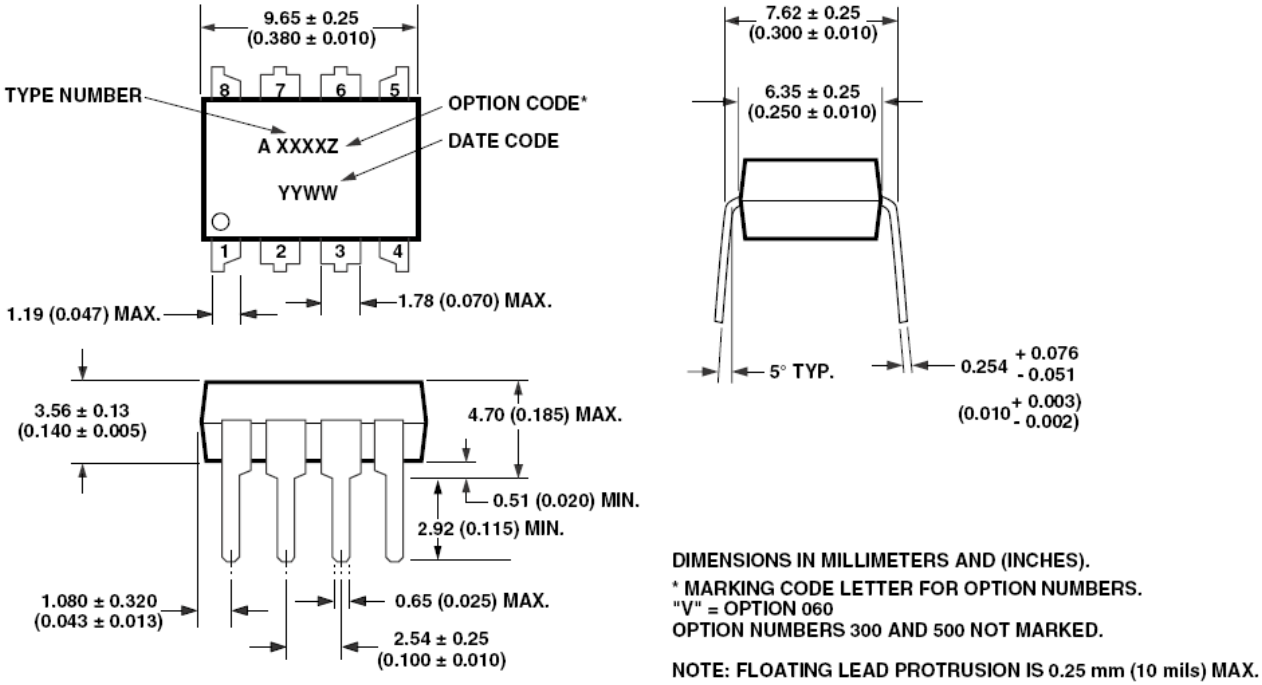
Example 2:

QCPL-341H-000E to order product of 300 mil DIP package in Tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

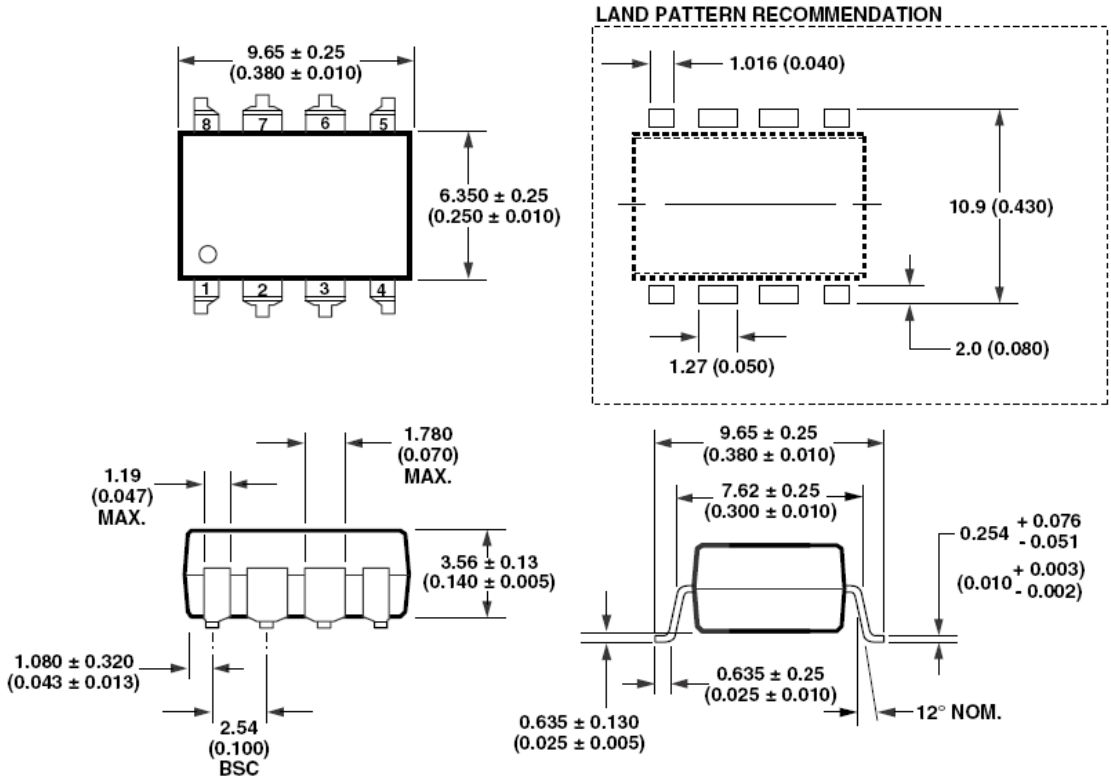
QCPL-341H Outline Drawing (Standard DIP Package)



DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS.
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

QCPL-341H Gull Wing Surface Mount Option 300 Outline Drawing



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The QCPL-341H is pending approval by the following organizations:

UL
Recognized under UL 1577, component recognition program, category, File E55361 up to V_{ISO} = 3750 V_{RMS}.

CSA
CSA Component Acceptance Notice #5, File CA 88324

IEC/EN/DIN EN 60747-5-5 (Option 060 Only)
Maximum Working Insulation Voltage V_{IORM} = 630V_{peak}

Table 1. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 060 – Under Evaluation)

Description	Symbol	QCPL-341H Option 060	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150 V_{rms} for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 450 V_{rms}		 I – IV I – IV I – III	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1008	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure Case Temperature Input Current Output Power	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.
Note: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits. Surface mount classification is Class A in accordance with CECC 00802.

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	QCPL-341H	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Notes:
1. All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements. However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered (the recommended Land Pattern does not necessarily meet the minimum creepage of the device). There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	105	°C	
Output IC Junction Temperature	T_J		125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 μs pulse width, 300pps)	$I_{F(TRAN)}$		1	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	2
Total Output Supply Voltage	(V_{CC} - V_{EE})	0	35	V	
Input Current (Rise/Fall Time)	$t_{r(IN)}$ / $t_{f(IN)}$		500	ns	
Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC}	V	
Output IC Power Dissipation	P_O		250	mW	3
Total Power Dissipation	P_T		295	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Max.	Units	Note
Operating Temperature	T_A	- 40	105	°C	
Output Supply Voltage	(V_{CC} - V_{EE})	15	30	V	
Input Current (ON)	$I_{F(ON)}$	7	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.6	0.8	V	

Table 5. Electrical Specifications (DC)

Unless otherwise noted, all typical values are at T_A = 25 °C, V_{CC} - V_{EE} = 30 V, V_{EE} = Ground; all minimum and maximum specifications are at recommended operating conditions (T_A = -40 to 105 °C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{EE} = Ground, V_{CC} = 15 to 30 V).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Peak Output Current	I_{OH}	-1.0	-2.3		A	$V_O = V_{CC} – 4$ V	14	5
		-2.0			A	$V_{CC} – V_O \leq 15$ V		6
Low Level Peak Output Current	I_{OL}	1.0	3.0		A	$V_O = V_{EE} + 2.5$ V	15	5
		2.0			A	$V_O - V_{EE} \leq 15$ V		7
High Output Transistor RDS(ON)	$R_{DS,OH}$		1.7	3.0	Ω	I_{OH} = -2.0 A		8
Low Output Transistor RDS(ON)	$R_{DS,OL}$		0.8	1.8	Ω	I_{OL} = 2.0 A		8
High Level Output Voltage	V_{OH}	Vcc-0.3	Vcc – 0.2		V	I_O = -100 mA	2, 16	9, 10
High Level Output Voltage	V_{OH}		Vcc		V	I_O = 0 mA , I_F = 10 mA	1	
Low Level Output Voltage	V_{OL}		0.1	0.2	V	I_O = 100 mA	5, 17	
High Level Supply Current	I_{CCH}		1.9	5.0	mA	R_g = 10 Ω, C_g = 25 nF, I_F = 10 mA	4, 5	
Low Level Supply Current	I_{CCL}		1.9	5.0	mA	R_g = 10 Ω, C_g = 25 nF, V_F = 0V		
Threshold Input Current Low to High	I_{FLH}		1.5	5.0	mA	R_g = 10 Ω, C_g = 25 nF, V_O > 5 V	6, 7, 8	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V			
Input Forward Voltage	V_F	1.2	1.55	1.95	V	I_F = 10 mA	13	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		-1.7		mV/°C	I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 100 µA		
Input Capacitance	C_{IN}		70		pF	f = 1 MHz, V_F = 0 V		
UVLO Threshold	V_{UVLO+}	12.1	12.8	13.5	V	V_O > 5 V, I_F = 10 mA	19	
	V_{UVLO-}	11.1	11.8	12.4				
UVLO Hysteresis	$UVLO_{HYS}$		1.0		V			

Table 6. Switching Specifications (AC)

Unless otherwise noted, all typical values are at T_A = 25 °C, V_{CC} - V_{EE} = 30 V, V_{EE} = Ground; all minimum and maximum specifications are at recommended operating conditions (T_A = -40 to 105 °C, $I_{F(ON)}$ = 7 to 16 mA, $V_{F(OFF)}$ = -3.6 to 0.8 V, V_{EE} = Ground, V_{CC} = 15 to 30 V).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	50	98	300	ns	R_g = 10 Ω, C_g = 25 nF, f = 20 kHz , Duty Cycle = 50%, I_F = 7 mA to 16 mA, V_{CC} = 15 V to 30 V	8, 9, 10, 11, 12, 20	
Propagation Delay Time to Low Output Level	t_{PHL}	50	95	300	ns			
Pulse Width Distortion	PWD		22	150	ns			11
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})	-100		200	ns		27, 28	12
Rise Time	t_R		43		ns	Vcc = 30 V	20	
Fall Time	t_F		40		ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	25	35		kV/μs	T_A = 25 °C, I_F = 10 mA, V_{CM} = 1500 V, V_{CC} = 30 V, V_{CM} = 1500 V	21	13, 14
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	25	35		kV/μs	T_A = 25°C, V_F = 0 V, V_{CM} = 1500 V, V_{CC} = 30 V, V_{CM} = 1500 V		13, 15

Table 7. Package Characteristics

Unless otherwise noted, all typical values are at T_A = 25 °C; all minimum/maximum specifications are at recommended operating conditions.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	QCPL-341H	3750			V_{RMS}	RH < 50%, t = 1 min., T_A = 25 °C		16,17
Input-Output Resistance	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 V_{DC}		17
Input-Output Capacitance	C_{I-O}			0.6		pF	f =1 MHz		
LED-to-Case Thermal Resistance	θ_{LC}			467		°C/W		25	18
LED-to-Detector Thermal Resistance	$\theta_{LD,}$			442					
Detector-to-Case Thermal Resistance	Θ_{DC}			126					

* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70 °C free-air temperature at a rate of 0.3 mA/ °C.
2. Maximum pulse width = 10 µs. This value is intended to allow for component tolerances for designs with I_O peak minimum = 2.0 A. See applications section for additional details on limiting I_{OH} peak.
3. Derate linearly above 70 °C free-air temperature at a rate of 4.8 mW/ °C.
4. Derate linearly above 70 °C free-air temperature at a rate of 5.4 mW/ °C . The maximum LED junction temperature should not exceed 125 °C.
5. Maximum pulse width = 50 µs.
6. Output is sourced at -2.0 A with a maximum pulse width = 10 µs. V_{CC}-V_O is measured to ensure 15 V or below.
7. Output is sourced at 2.0 A with a maximum pulse width = 10 µs. V_O-V_{EE} is measured to ensure 15 V or below.
8. Output is sourced at -2.0 A/2.0 A with a maximum pulse width = 10 µs.
9. In this test V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
10. Maximum pulse width = 1 ms.
11. Pulse Width Distortion (PWD) is defined as $|t_{PHL}-t_{PLH}|$ for any given device.
12. The difference between t_{PHL} and t_{PLH} between any two QCPL-341H parts under the same test condition.
13. Pin 1 and 4 need to be connected to LED common.
14. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., $V_O > 15.0$ V).
15. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., $V_O < 1.0$ V).
16. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
17. Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.
18. The device was mounted on a high conductivity test board as per JEDEC 51-7.

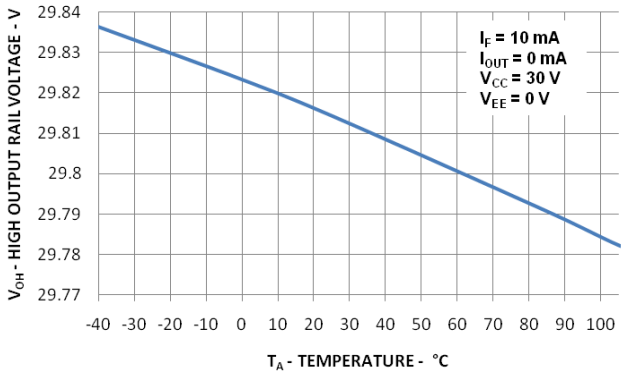


Figure 1. High output rail voltage vs. temperature.

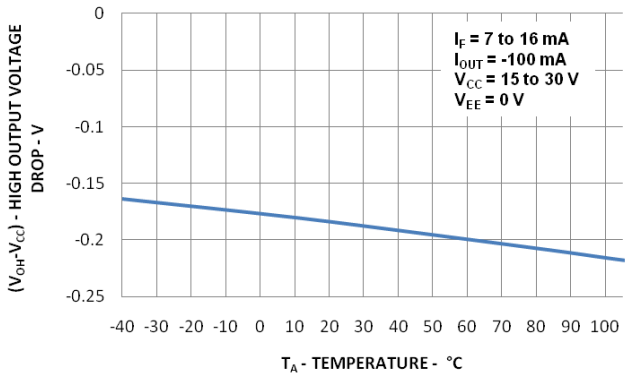


Figure 2. V_{OH} vs. temperature.

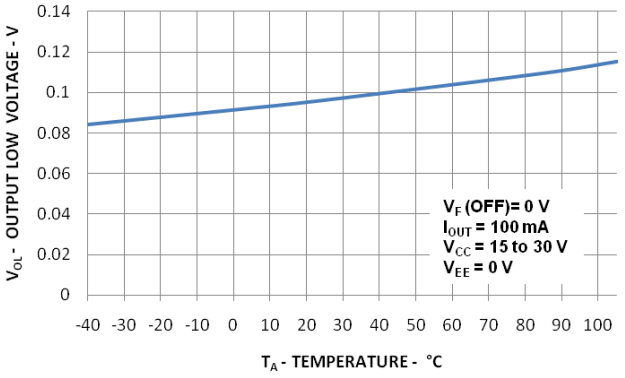


Figure 3. V_{OL} vs. Temperature.

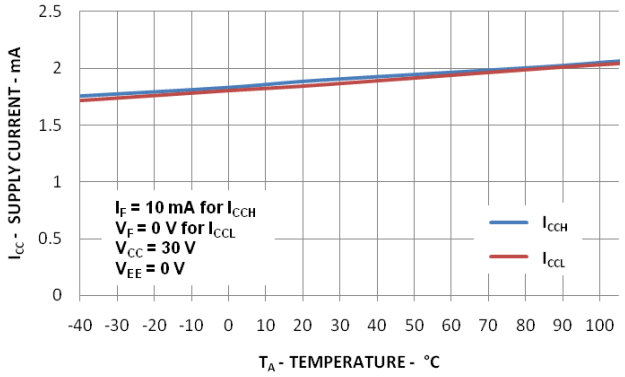


Figure 4. I_{CC} vs. temperature.

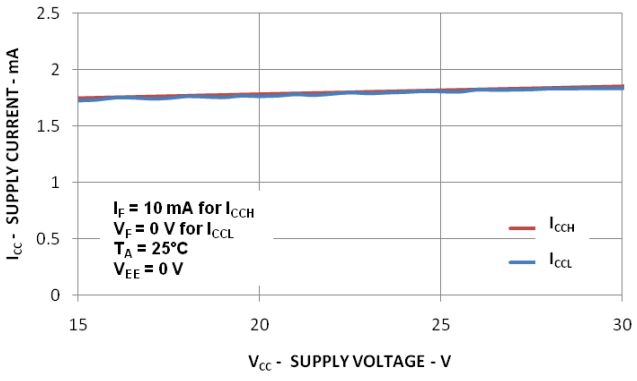


Figure 5. I_{CC} vs. V_{CC}.

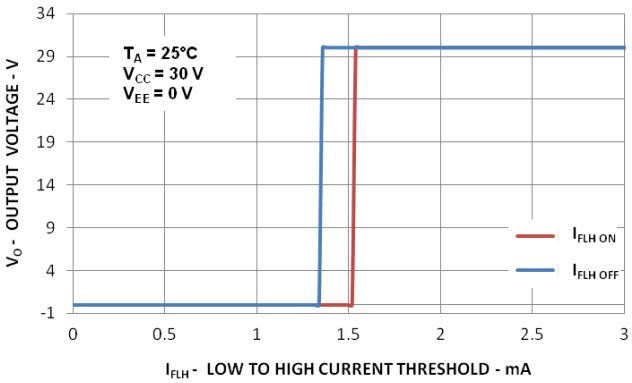


Figure 6. I_{FLH} hysteresis.

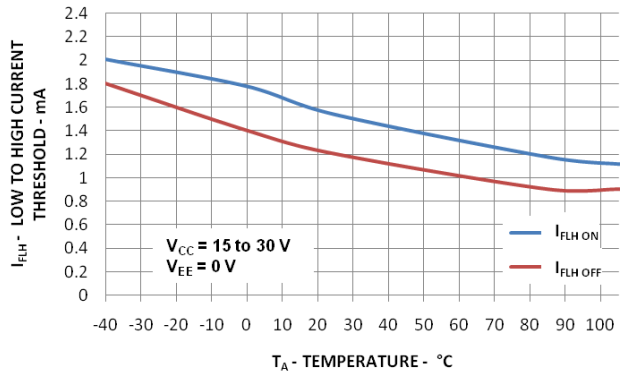


Figure 7. I_{FLH} vs. temperature.

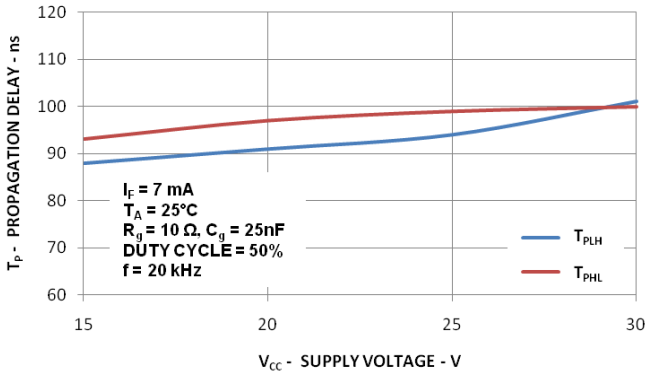


Figure 8. Propagation delay vs. V_{CC}.

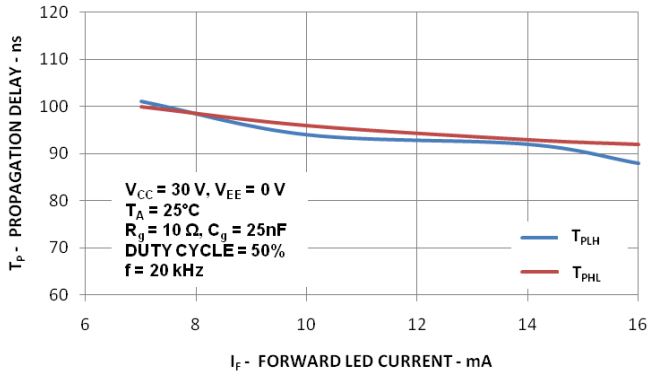


Figure 9. Propagation delay vs. I_F.

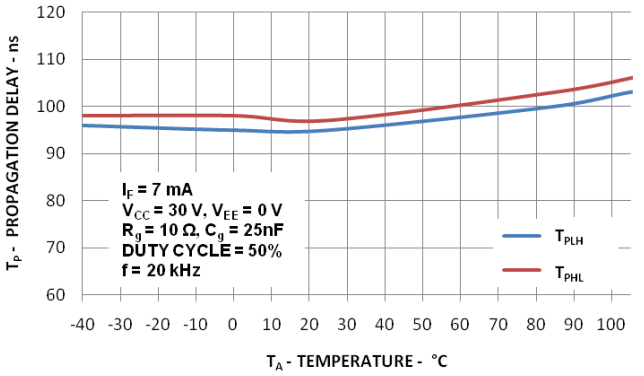


Figure 10. Propagation delay vs. temperature.

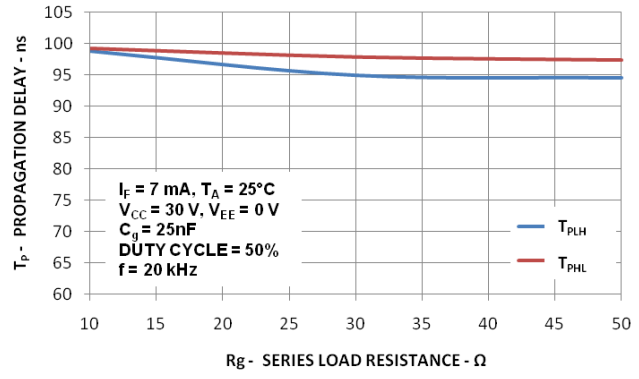


Figure 11. Propagation delay vs. Rg.

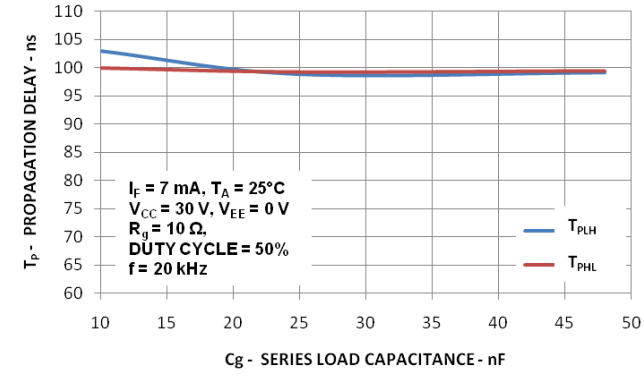


Figure 12. Propagation delay vs. Cg.

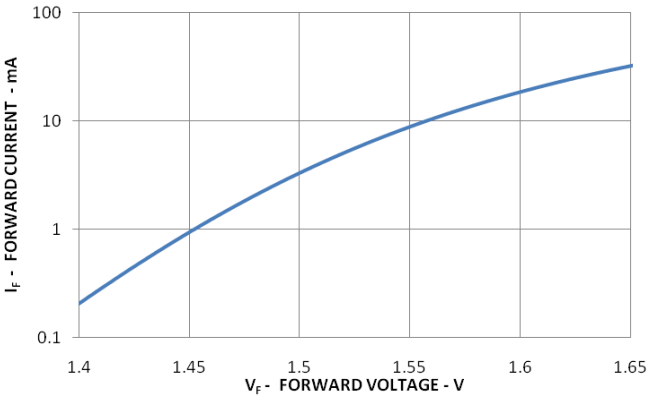


Figure 13. Input Current vs. forward voltage.

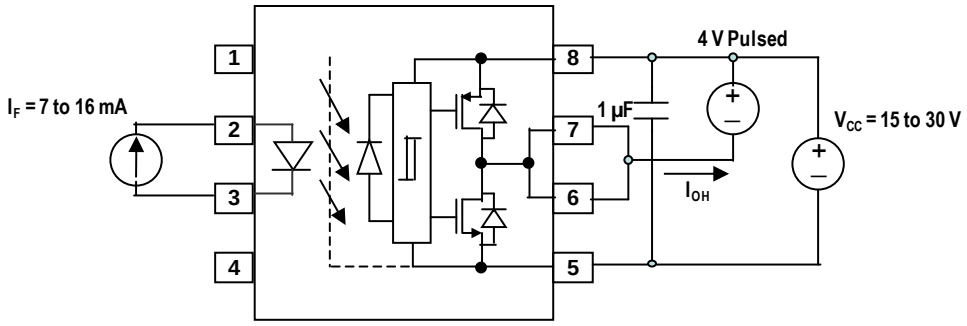


Figure 14. I_{OH} test circuit.

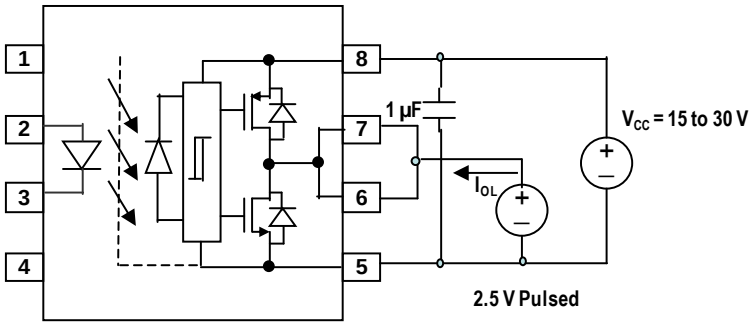


Figure 15. I_{OL} test circuit.

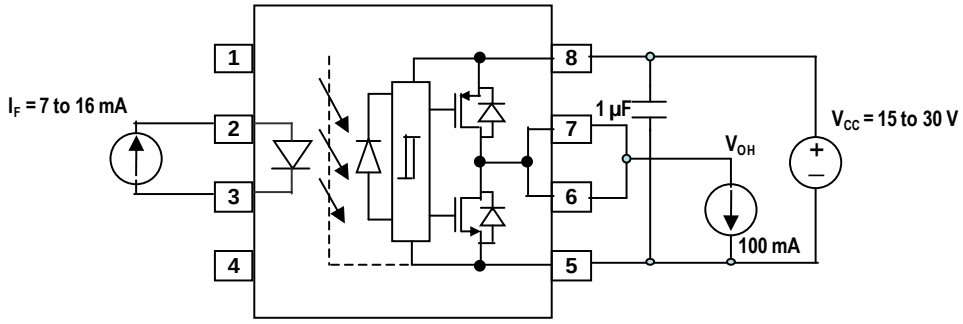


Figure 16. V_{OH} test circuit.

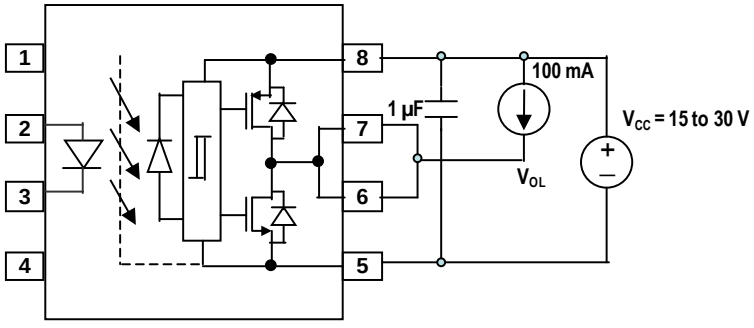


Figure 17. V_{OL} test circuit.

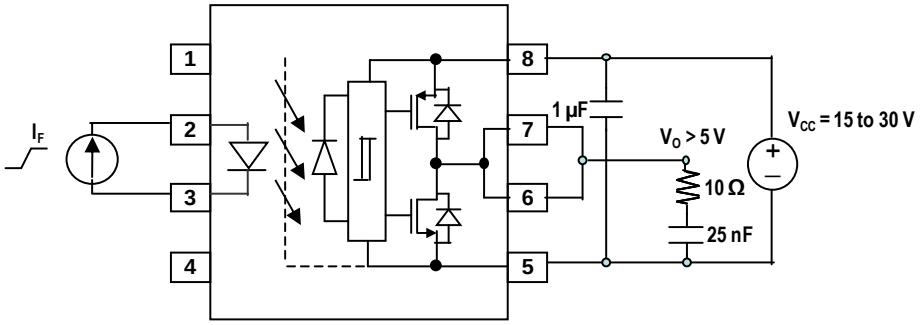


Figure 18. I_{FLH} test circuit.

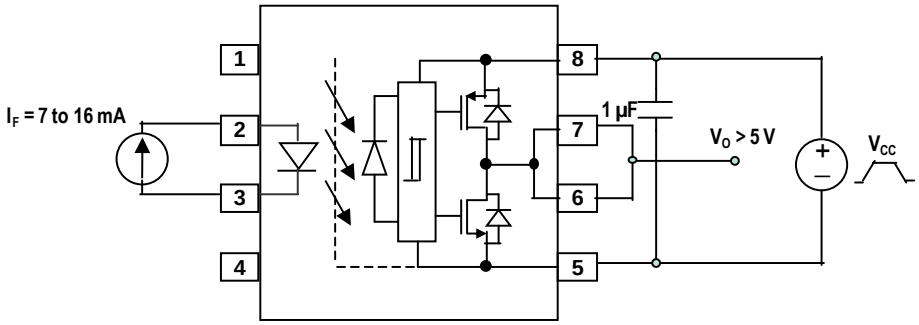


Figure 19. UVLO test circuit.

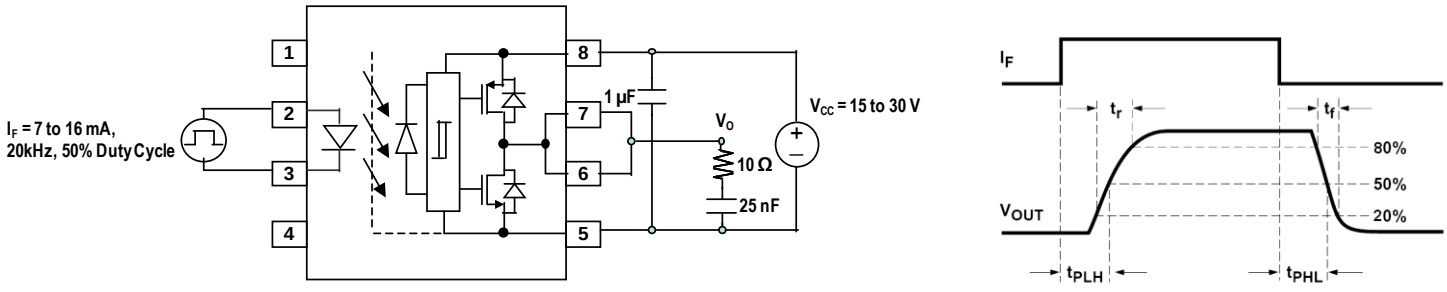


Figure 20. t_{PLH}, t_{PHL}, t_r and t_f test circuit and waveforms.

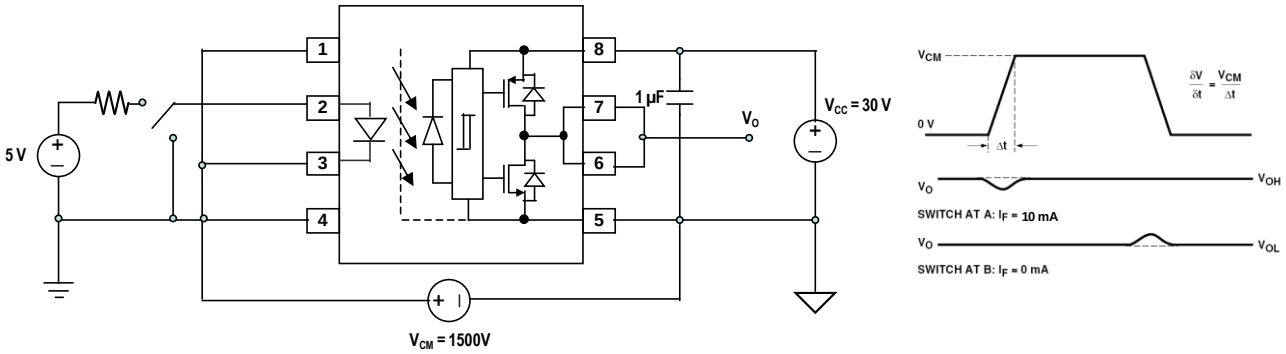


Figure 21. CMR test circuit and waveforms.

Application Information

Recommended Application Circuit

The recommended application circuit shown in Figure 22 illustrates a typical gate drive implementation using the QCPL-341H. The following describes about driving IGBT. However, it is also applicable to MOSFET. Designers will need to adjust the V_{CC} supply voltage, depending on the MOSFET or IGBT gate threshold requirements (Recommended V_{CC} = 15 V for IGBT and 12 V for MOSFET).

The supply bypass capacitors (1 µF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (5.0 mA) power supply will be enough to power the device. The gate resistor R_G serves to limit gate charge current and controls the IGBT collector voltage rise and fall times.

In PC board design, care should be taken to avoid routing the IGBT collector or emitter traces close to the QCPL-341H's inputs as this can result in unwanted coupling of transient signals into QCPL-341H and degrade performance.

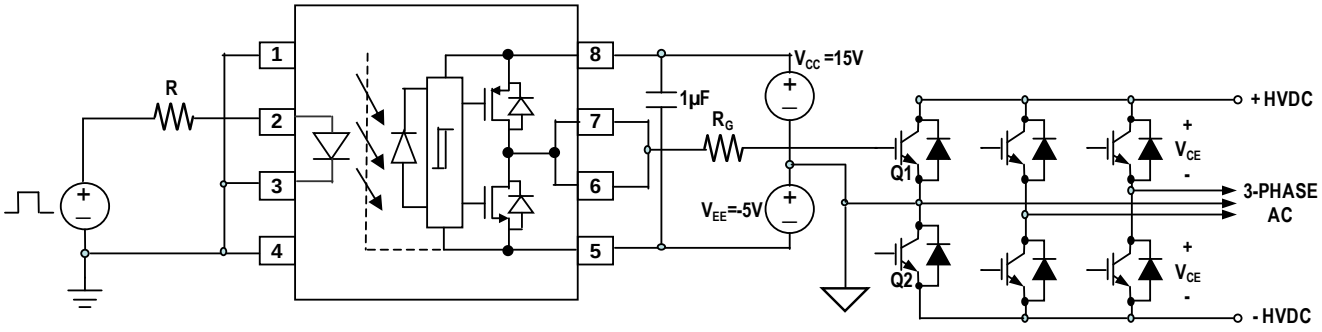


Figure 22. Recommended application circuit with split resistors LED drive.

Selecting the Gate Resistor (Rg)

Step 1: Calculate Rg minimum from the I_{OL} peak specification. The IGBT and Rg in Figure 22 can be analyzed as a simple RC circuit with a voltage supplied by QCPL-341H.

$$Rg \geq \frac{V_{CC}-V_{EE}}{I_{OLPEAK}}$$
$$= \frac{15V + 5V}{2.5A}$$
$$= 8\Omega$$

Step 1: Check the QCPL-341H power dissipation and increase Rg if necessary. The QCPL-341H total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$P_T = P_E + P_O$
$P_E = I_F \bullet V_F \bullet$ Duty Cycle
$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$
$= I_{CC} \bullet (V_{CC}-V_{EE}) + E_{SW}(Rg;Cg) \bullet f$

Using I_F(worst case) = 16 mA, Rg = 8 Ω, Max Duty Cycle = 80%, Cg = 25 nF, f = 25 kHz and T_A max = 70 °C:

P_E = 16 mA • 1.95 V • 0.8 = 25 mW

P_O = 5 mA • 20 V + 4 µJ • 25 kHz
= 100 mW + 100 mW
= 200 mW < 250 mW ($P_{O(MAX)}$ @ 70 °C)

The value of 5 mA for I_{CC} in the previous equation is the maximum I_{CC} over the entire operating temperature range.

Since P_O is less than $P_{O(MAX)}$, Rg = 8 Ω is alright for the power dissipation.

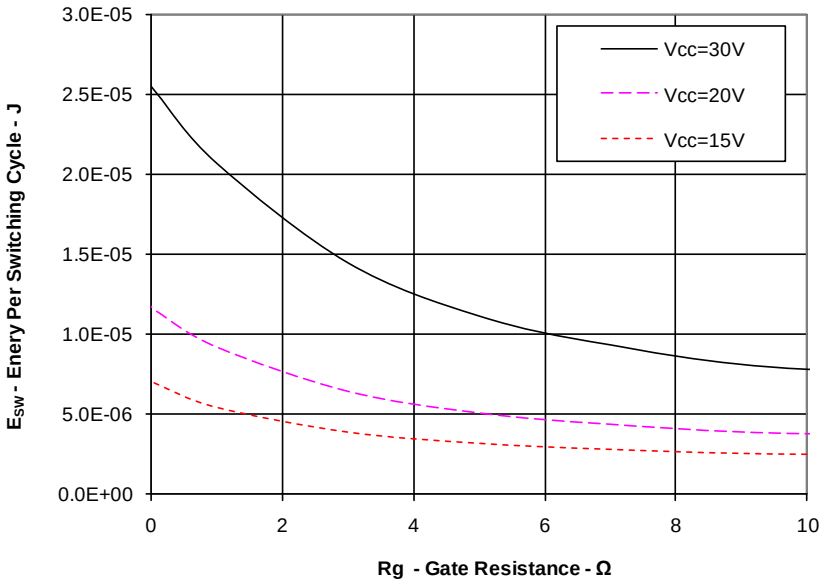


Figure 23. Energy Dissipated in the QCPL-341H for each IGBT switching cycle.

Dead Time and Propagation Delay Specifications

The QCPL-341H includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 22) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 23. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 100 ns over the operating temperature range of -40 °C to 105 °C.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 24. The maximum dead time for the QCPL-341H is 400 ns (= 200 ns - (-200 ns)) over an operating temperature range of -40 °C to 105 °C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

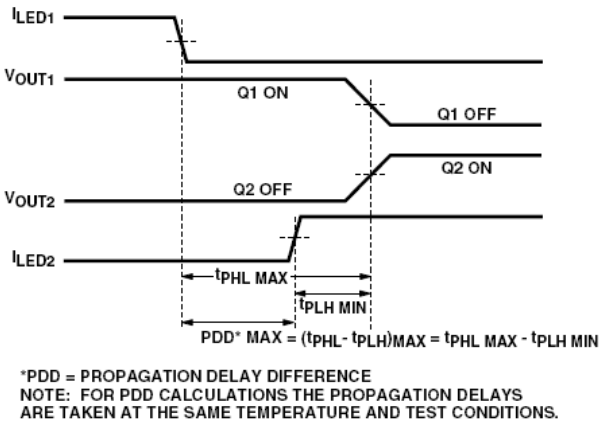


Figure 23. Minimum LED skew for zero dead time.

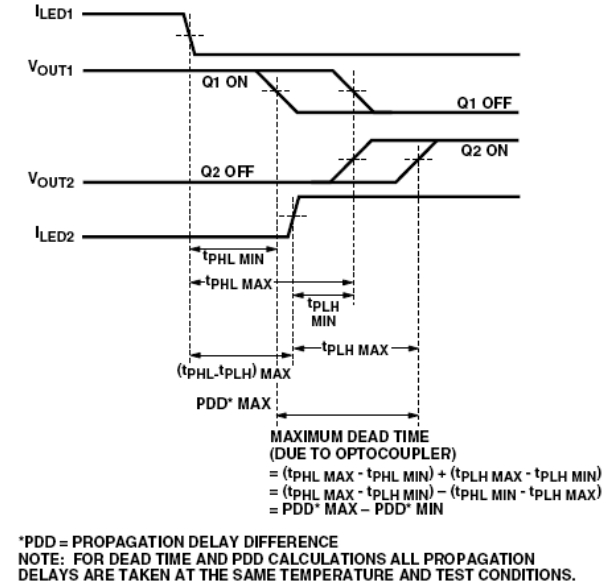


Figure 24. Waveforms for dead time.

LED Current Input with Hysteresis

The detector has optical receiver input stage with built in Schmitt trigger to provide logic compatible waveforms, eliminating the need for additional wave shaping. The hysteresis (Figure 6) provides differential mode noise immunity and minimizes the potential for output signal chatter.

Under Voltage Lockout

The QCPL-341HUnder Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the QCPL-341H output low during power-up. IGBTs typically require gate voltages of 15 V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 13 V typically, the $V_{CE(ON)}$ voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10 V), the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply (V_{CC}) is applied. Once V_{CC} exceeds V_{UVLO+} (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals.

Thermal Model for QCPL-341H

Definitions:
T_{JE}: LED junction temperature
T_{JD}: Detector IC junction temperature
T_C: Case temperature measured at the center of the package bottom
θ_{LC} : LED-to-case thermal resistance
θ_{LD}: LED-to-detector thermal resistance
θ_{DC}: Detector-to-case thermal resistance
θ_{CA}: Case-to-ambient thermal resistance
*θ_{CA} will depend on the board design and the placement of the part
T_A: Ambient temperature.

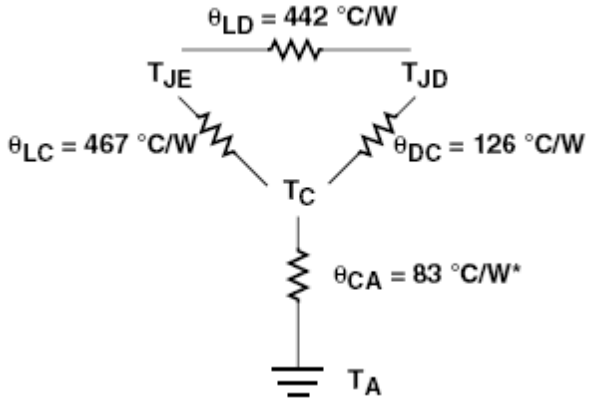


Figure 25. Thermal model.

Related Application Noted

AN5336 – Gate Drive Optocoupler Basic Design for IGBT / MOSFET

AN1043 – Common-Mode Noise: Sources and Solutions

AV02-0310EN –Plastics Optocouplers Product ESD and Moisture Sensitivity

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