QCPL-7847
Optical Isolation Amplifier

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The QCPL-7847 isolation amplifier family was designed for current sensing in electronic motor drives. In a typical implementation, motor currents flow through an external resistor and the resulting analog voltage drop is sensed by the QCPL-7847. A differential output voltage is created on the other side of the QCPL-7847 optical isolation barrier. This differential output voltage is proportional to the motor current and can be converted to a single-ended signal by using an op-amp as shown in the recommended application circuit. Since common-mode voltage swings of several hundred volts in tens of nanoseconds are common in modern switching inverter motor drives, the QCPL-7847 was designed to ignore very high common-mode transient slew rates (of at least 10 kV/µs).

The high CMR capability of the QCPL-7847 isolation amplifier provides the precision and stability needed to accurately monitor motor current in high noise motor control environments, providing for smoother control (less "torque ripple") in various types of motor control applications.

The product can also be used for general analog signal isolation applications requiring high accuracy, stability, and linearity under similarly severe noise conditions. For general applications, we recommend the QCPL-7847 (gain tolerance of ± 5%). The QCPL-7847 utilizes sigma delta (Σ-Δ) analog-to-digital converter technology, chopper stabilized amplifiers, and a fully differential circuit topology fabricated using Avago's 0.8 µm CMOS IC process. Together, these features deliver unequaled isolation-mode noise rejection, as well as excellent offset and gain accuracy and stability over time and temperature. This performance is delivered in a compact, auto-insertable, industry standard 8-pin DIP package that meets worldwide regulatory safety standards. (A gull-wing surface mount option is also available).

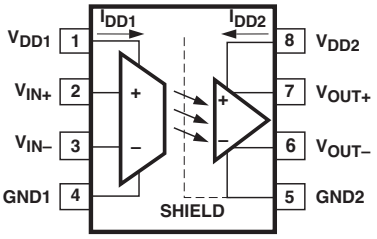
Features

- Optical Isolation Barrier
- 15 kV/µs common-mode rejection at V_{CM} = 1000 V
- Compact, auto-insertable standard 8-pin DIP package
- 0.00025 V/V/°C gain drift vs. temperature
- 0.3 mV input offset voltage
- 100 kHz bandwidth
- 0.004% nonlinearity
- Safety approval:
  UL 1577 (3750 Vrms/1 min.), CSA and IEC/EN/DIN EN 60747-5-5 (pending)
- Advanced Sigma-Delta (Σ-Δ) A/D converter technology
- Fully differential circuit topology
- 0.8 µm CMOS IC technology

Applications

- Motor phase and rail current sensing
- Inverter current sensing
- Switched mode power supply signal isolation
- General purpose current sensing and monitoring
- General purpose analog signal isolation

Functional Diagram



A 0.1 µF bypass capacitor must be connected between pins 1 and 4 and between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

QCPL-7847 is UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	RoHS Compliant	Package	Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
QCPL-7847	-000E	300 mil DIP-8				X	50 per tube
	-300E		X	X		X	50 per tube
	-500E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

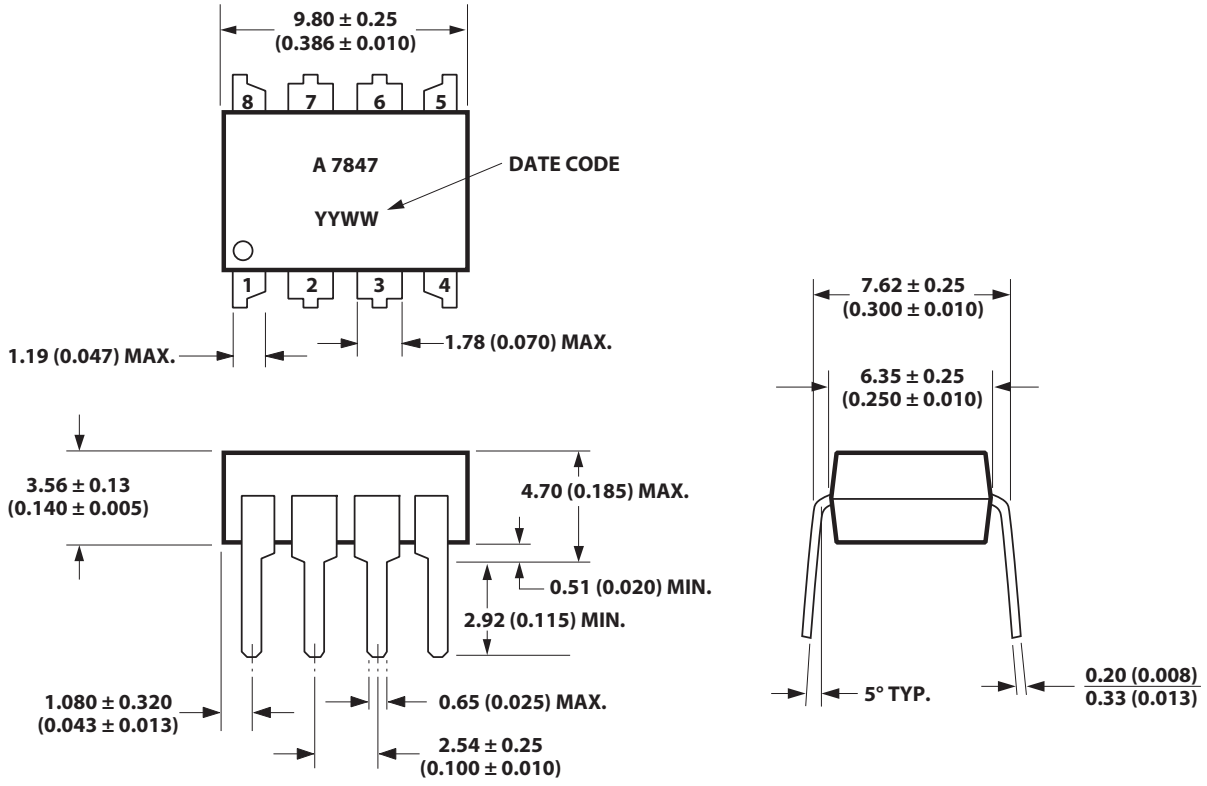
Example 1:

QCPL-7847-000E to order product of 300 mil DIP package in Tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

Standard DIP Package

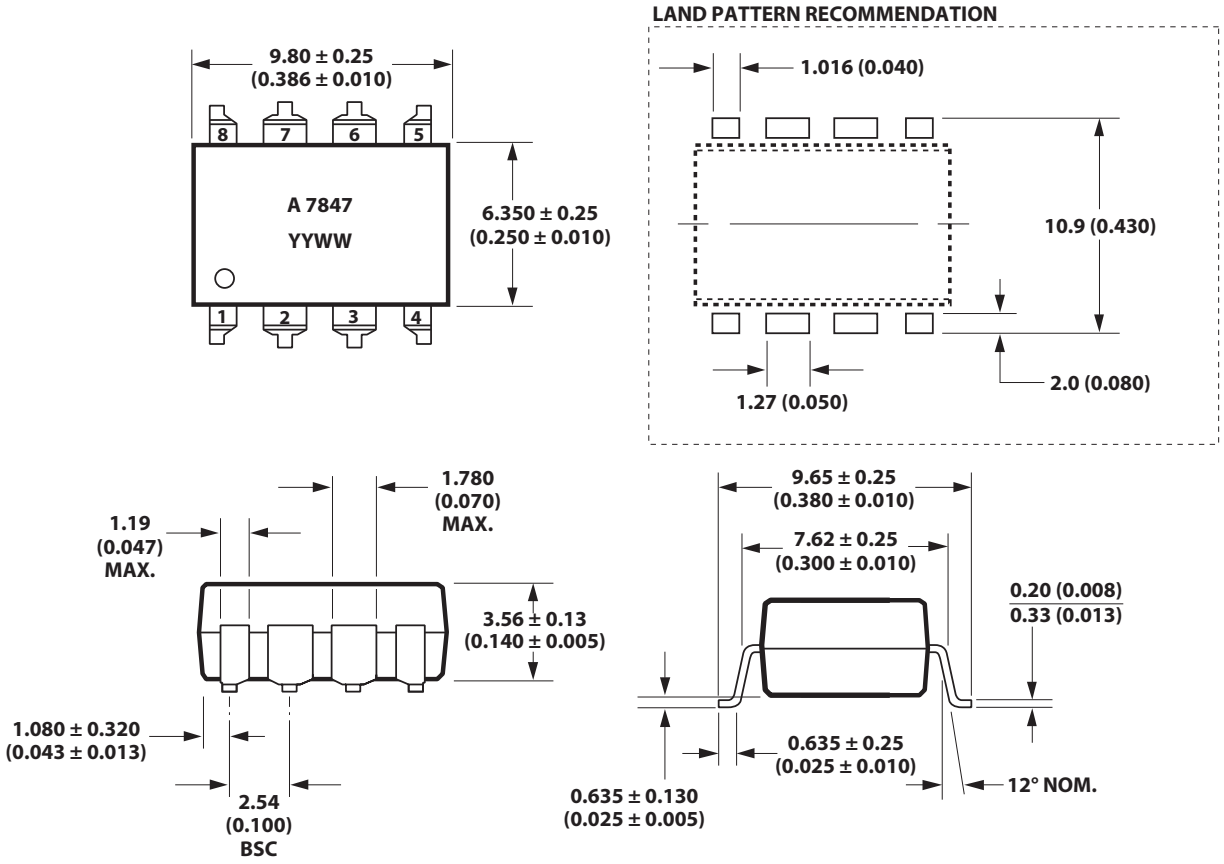


DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

Note: Initial or continued variation in the color of the QCPL-7847's white mold compound is normal and does not affect device performance or reliability.

Gull Wing Surface Mount Option 300

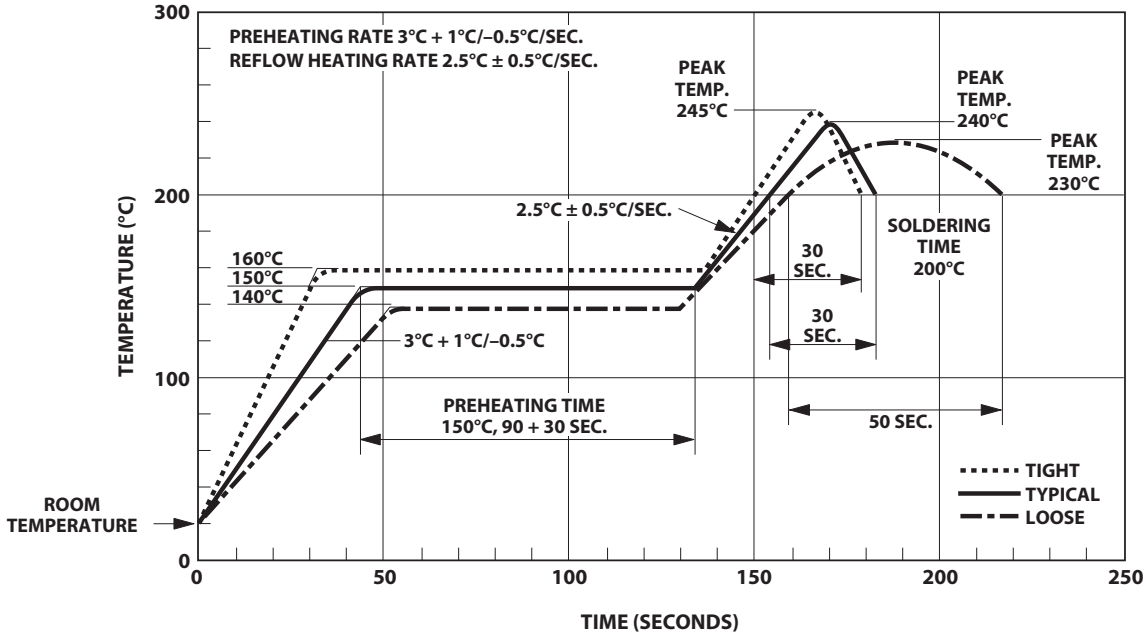


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): **xx.xx = 0.01**
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

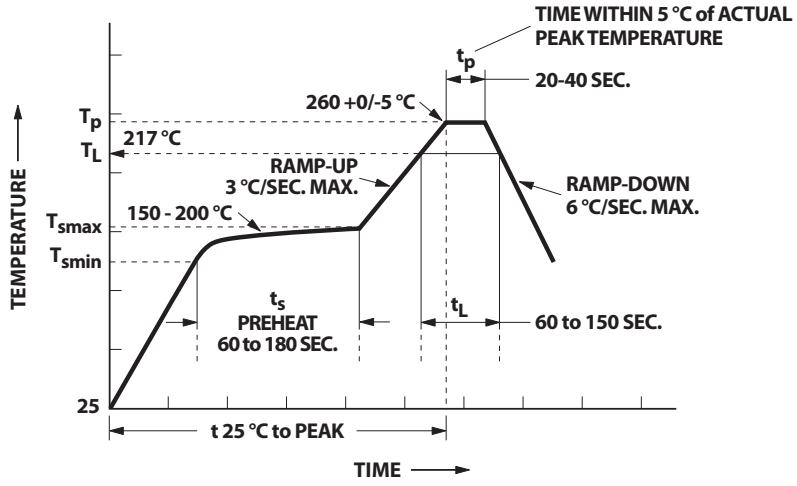
NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

Solder Reflow Temperature Profile



Note: Non-halide flux should be used..

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Regulatory Information

The QCPL-7847 is pending for approvals by the following organizations:

IEC/EN/DIN EN 60747-5-5

Approval under:
IEC 60747-5-5:1997 + A1:2002
EN 60747-5-5:2001 + A1:2002
DIN EN 60747-5-5 (VDE 0884 Teil 2):2003-01.

UL

Approval under UL 1577, compnent recognition program up to V_{ISO} = 3750 Vrms.

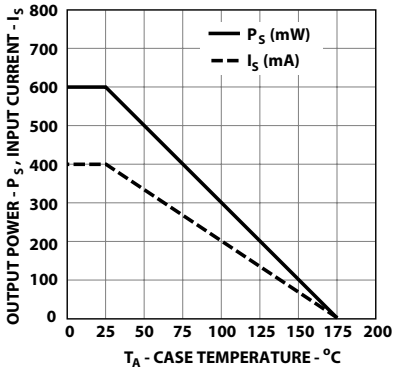
CSA

Approval under CSA component acceptance notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics [1]

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤300 Vrms		I-IV	
for rated mains voltage ≤600 Vrms		I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	891	V_{PEAK}
Input to Output Test Voltage, Method b [2]			
V_{IORM} x 1.875 = $V_{PR,}$ 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1670	V_{PEAK}
Input to Output Test Voltage, Method a [2]			
V_{IORM} x 1.5 = $V_{PR,}$ Type and Sample Test, t_m = 60 sec, Partial discharge < 5 pC	V_{PR}	1336	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	8000	V_{PEAK}
Safety-limiting values			
- maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current [3]	$I_{S,INPUT}$	400	mA
Output Power [3]	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

Notes:
1. Insulation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits within the application. Surface Mount Classification is Class A in accordance with CECC00802.
2. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, IEC/EN/DIN EN 60747-5-5, for a detailed description of Method a and Method b partial discharge test profiles.
3. Refer to the following figure for dependence of PS and IS on ambient temperature.



Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		III a		Material Group (DIN VDE 0110, 1/89, Table 1)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	100		
Supply Voltage	V_{DD1}, V_{DD2}	0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} +0.5		
2 Second Transient Input Voltage		-6.0	V_{DD1} +0.5		
Output Voltage	V_{OUT}	-0.5	V_{DD2} +0.5		
Solder Reflow Temperature Profile	See **Solder Reflow Temperature Profile** Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40	85	°C	
Supply Voltage	V_{DD1}, V_{DD2}	4.5	5.5	V	
Input Voltage (accurate and linear)	V_{IN+}, V_{IN-}	-200	200	mV	1
Input Voltage (functional)	V_{IN+}, V_{IN-}	-2	2	V	

DC Electrical Specifications

Unless otherwise noted, all typicals and figures are at the nominal operating conditions of $V_{IN+} = 0$, $V_{IN-} = 0$ V, $V_{DD1} = V_{DD2} = 5$ V and $T_A = 25°C$; all Min./Max. specifications are within the Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-2.0	0.3	2.0	mV	$T_A = 25°C$	1,2	
		-3.0		3.0	mV	$T_A = -40°C$ to $+85°C$	1,2	
Magnitude of Input Offset Change vs. Temperature	$\lvert\Delta V_{OS}/\Delta T_A\rvert$		3.0	10.0	µV/°C		3	2
Gain (± 5% Tol.)	G	7.60	8.00	8.40	V/V	-200 mV < V_{IN+} < 200 mV, $T_A = 25°C$	4,5,6	3
Magnitude of V_{OUT} Gain Change vs. Temperature	$\lvert\Delta G/\Delta T_A\rvert$		0.00025		V/V/°C			4
V_{OUT} 200 mV Nonlinearity	NL_{200}		0.0037	0.35	%	-200 mV < V_{IN+} < 200 mV	7,8	5
Magnitude of V_{OUT} 200 mV Nonlinearity Change vs. Temperature	$\lvert dNL_{200}/dT\rvert$		0.0002		% / °C			
V_{OUT} 100 mV Nonlinearity	NL_{100}		0.0027	0.2	%	-100 mV < V_{IN+} < 100 mV		6
Maximum Input Voltage before V_{OUT} Clipping	$\lvert V_{IN+}\rvert_{MAX}$		308.0		mV		9	
Input Supply Current	I_{DD1}		10.86	15.5	mA	V_{IN+} = 400 mV	10	7
Output Supply Current	I_{DD2}		11.56	15.5		V_{IN+} = -400 mV		8
Input Current	I_{IN+}		-0.5	5.0	µA		11	9
Magnitude of Input Bias Current vs. Temperature Coefficient	$\lvert dI_{IN}/dT\rvert$		+0.45		nA/°C		11	
Output Low Voltage	V_{OL}		1.29		V			10
Output High Voltage	V_{OH}		3.80		V			10
Output Common-Mode Voltage	V_{OCM}	2.2	2.545	2.8	V			
Output Short-Circuit Current	$\lvert I_{OSC}\rvert$		18.6		mA			11
Equivalent Input Impedance	R_{IN}		500		kΩ			
V_{OUT} Output Resistance	R_{OUT}		15		Ω			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		76.1		dB			12

AC Electrical Specifications

Unless otherwise noted, all typicals and figures are at the nominal operating conditions of V_{IN+} = 0, V_{IN-} = 0 V, V_{DD1} = V_{DD2} = 5 V and T_A = 25°C; all Min./Max. specifications are within the Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
V_{OUT} Bandwidth (-3 dB)	BW	50	100		kHz	V_{IN+} = 200 mV_{pk-pk} sine wave.	12,13	
V_{OUT} Noise	N_{OUT}		31.5		mVrms	V_{IN+} = 0.0 V		13
V_{IN} to V_{OUT} Signal Delay (50 – 10%)	t_{PD10}		2.03	3.3	µs	Measured at output of MC34081 on Figure 15. V_{IN+} = 0 mV to 150 mV step.	14,15	
V_{IN} to V_{OUT} Signal Delay (50 – 50%)	t_{PD50}		3.47	5.6				
V_{IN} to V_{OUT} Signal Delay (50 – 90%)	t_{PD90}		4.99	9.9				
V_{OUT} Rise/Fall Time (10 – 90%)	$t_{R/F}$		2.96	6.6				
Common Mode Transient Immunity	CMTI	10.0	15.0		kV/µs	V_{CM} = 1 kV, T_A = 25°C	16	14
Power Supply Rejection	PSR		170		mVrms	With recommended application circuit.		15

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			Vrms	RH < 50%, t = 1 min., T_A = 25°C		16,17
Resistance (Input-Output)	R_{I-O}		$>10^9$		Ω	V_{I-O} = 500 V_{DC}		18
Capacitance (Input-Output)	C_{I-O}		1.2		pF	F = 1 MHz		18

Notes:

General Note: Typical values represent the mean value of all characterization units at the nominal operating conditions. Typical drift specifications are determined by calculating the rate of change of the specified parameter versus the drift pa-rameter (at nominal operating conditions) for each characterization unit, and then averaging the individual unit rates. The corresponding drift figures are normalized to the nominal operating conditions and show how much drift occurs as the par-ticular drift parameter is varied from its nominal value, with all other parameters held at their nominal operating values. Note that the typical drift specifications in the tables below may differ from the slopes of the mean curves shown in the corresponding figures.

1. Avago recommends operation with V_{IN-} = 0 V (tied to GND1). Limiting V_{IN+} to 100 mV will improve DC nonlinearity and nonlinearity drift. If V_{IN-} is brought above V_{DD1} – 2 V, an internal test mode may be activated. This test mode is for testing LED coupling and is not intended for customer use.
2. This is the Absolute Value of Input Offset Change vs. Temperature.
3. Gain is defined as the slope of the best-fit line of differential output voltage (V_{OUT+}–V_{OUT-}) vs. differential input voltage (V_{IN+}–V_{IN-}) over the specified input range.
4. This is the Absolute Value of Gain Change vs. Temperature.
5. Nonlinearity is defined as half of the peak-to-peak output deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.
6. NL_{100} is the nonlinearity specified over an input voltage range of ±100 mV.
7. The input supply current decreases as the differential input voltage (V_{IN+}–V_{IN-}) decreases.
8. The maximum specified output supply current occurs when the differential input voltage (V_{IN+}–V_{IN-}) = -200 mV, the maximum recommended operat-ing input voltage. However, the out-put supply current will continue to rise for differential input voltages up to approximately -300 mV, beyond which the output supply current remains constant.
9. Because of the switched-capacitor nature of the input sigma-delta con-verter, time-averaged values are shown.
10. When the differential input signal exceeds approximately 308 mV, the outputs will limit at the typical values shown.
11. Short circuit current is the amount of output current generated when either output is shorted to V_{DD2} or ground.
12. CMRR is defined as the ratio of the differential signal gain (signal applied differentially between pins 2 and 3) to the common-mode gain (input pins tied together and the signal applied to both inputs at the same time), expressed in dB.
13. Output noise comes from two primary sources: chopper noise and sigma-delta quantization noise. Chopper noise results from chopper stabilization of the output op-amps. It occurs at a specific frequency (typically 400 kHz at room temperature), and is not attenuated by the internal output filter. A filter circuit can be easily added to the external post-amplifier to reduce the total rms output noise. The internal output filter does eliminate most, but not all, of the sigma-delta quantization noise. The magnitude of the output quantization noise is very small at lower frequencies (below 10 kHz) and increases with increasing frequency.
14. CMTI (Common Mode Transient Immunity or CMR, Common Mode Rejection) is tested by applying an exponentially rising/falling voltage step on pin 4 (GND1) with respect to pin 5 (GND2). The rise time of the test waveform is set to approximately 50 ns. The amplitude of the step is adjusted until the differential output (V_{OUT+}–V_{OUT-}) exhibits more than a 200 mV deviation from the average output voltage for more than 1µs. The QCPL-7847 will continue to func-tion if more than 10 kV/µs common mode slopes are applied, as long as the breakdown voltage limitations are observed.
15. Data sheet value is the differential amplitude of the transient at the output of the QCPL-7847 when a 1 V_{pk-pk}, 1 MHz square wave with 40 ns rise and fall times is applied to both V_{DD1} and V_{DD2}.
16. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
17. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 insulation characteristics table and your equipment level safety specification.
18. This is a two-terminal measurement: pins 1–4 are shorted together and pins 5–8 are shorted together.

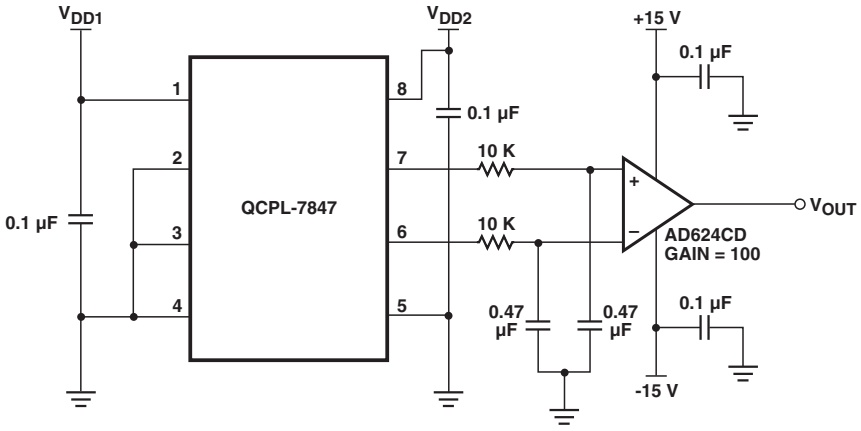


Figure 1. Input offset voltage test circuit.

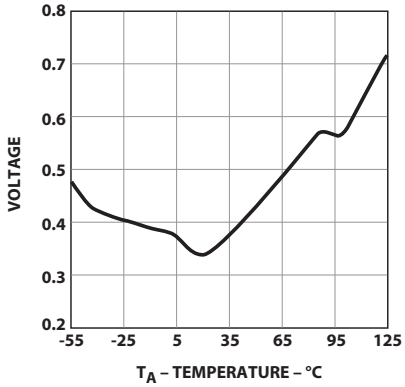


Figure 2. Input offset voltage vs. temperature.

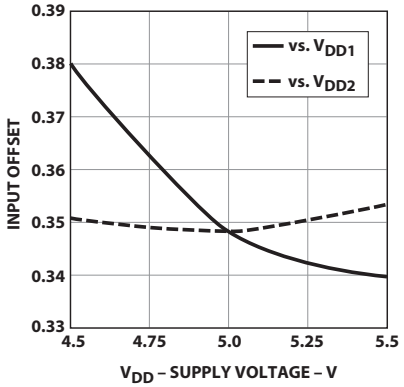


Figure 3. Input offset vs. supply.

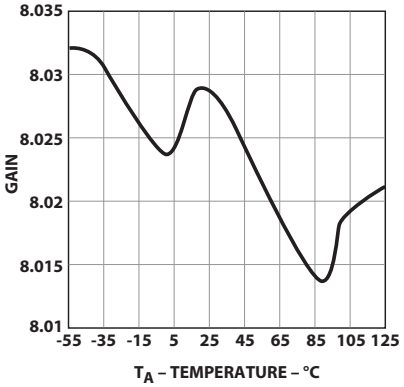


Figure 4. Gain vs. temperature.

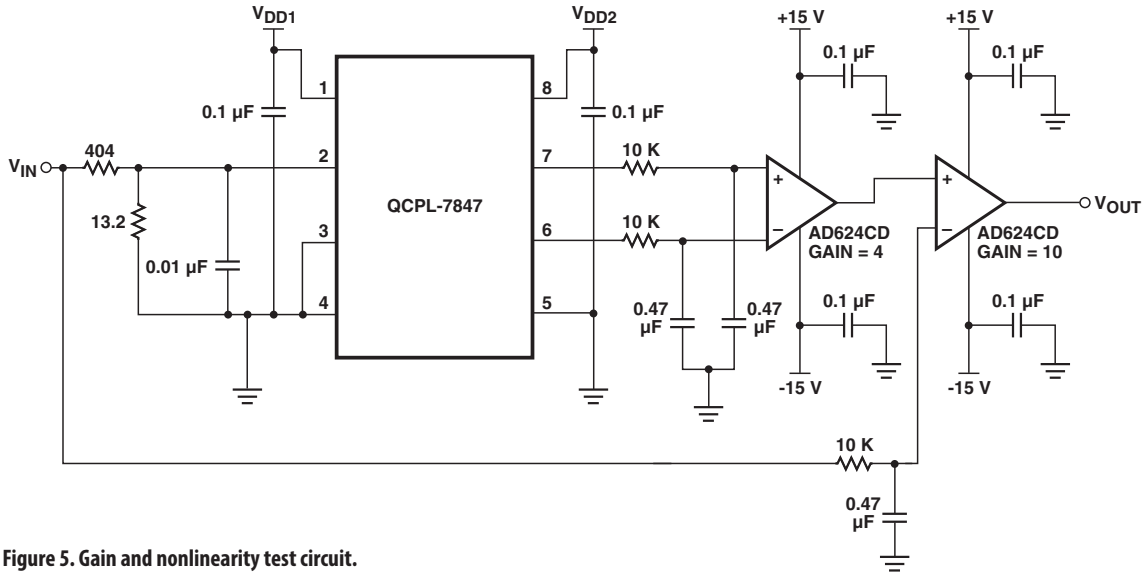


Figure 5. Gain and nonlinearity test circuit.

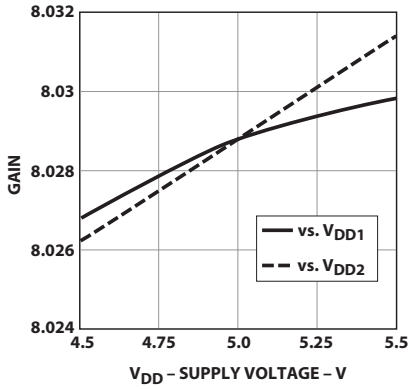


Figure 6. Gain vs. supply.

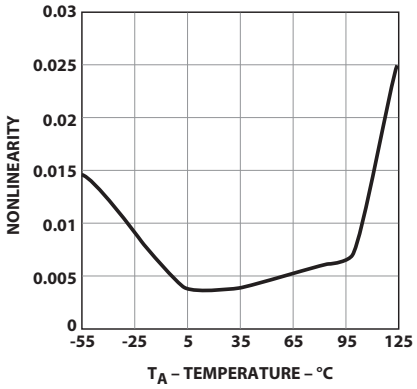


Figure 7. Nonlinearity vs. temperature.

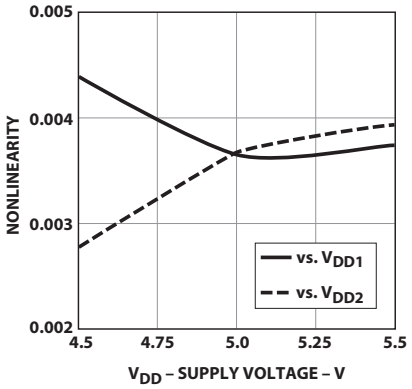


Figure 8. Nonlinearity vs. supply.

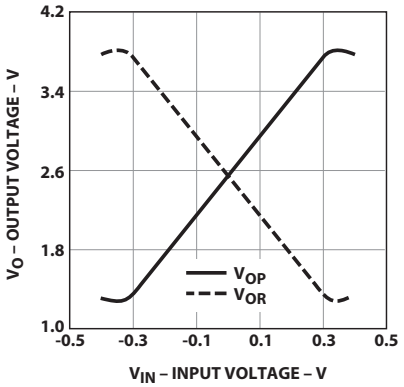


Figure 9. Output voltage vs. input voltage.

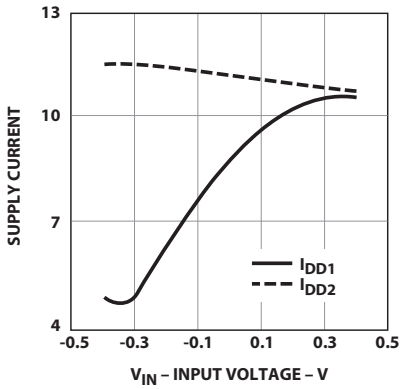


Figure 10. Supply current vs. input voltage.

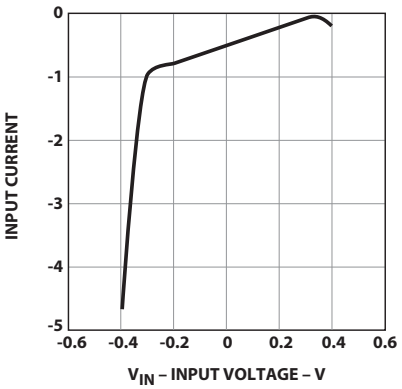


Figure 11. Input current vs. input voltage.

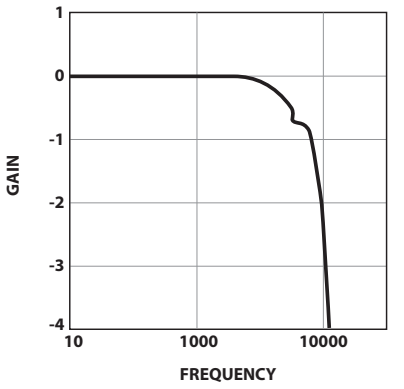


Figure 12. Gain vs. frequency.

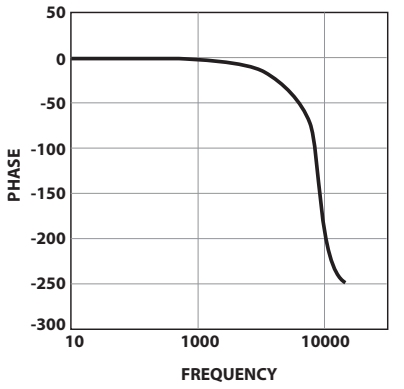


Figure 13. Phase vs. frequency.

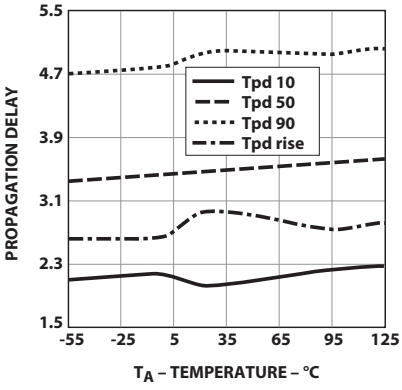
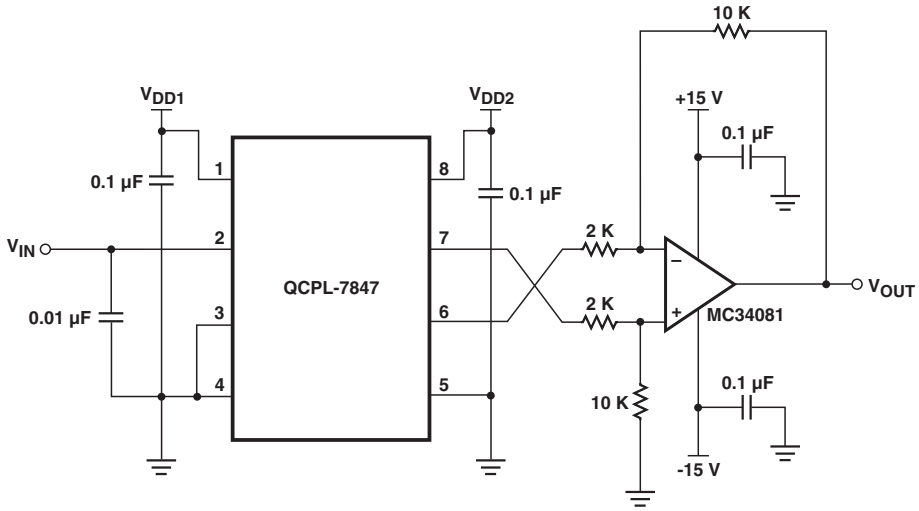


Figure 14. Propagation delay vs. temperature.



V_{IN} IMPEDANCE LESS THAN 10 Ω.

Figure 15. Propagation delay test circuits.

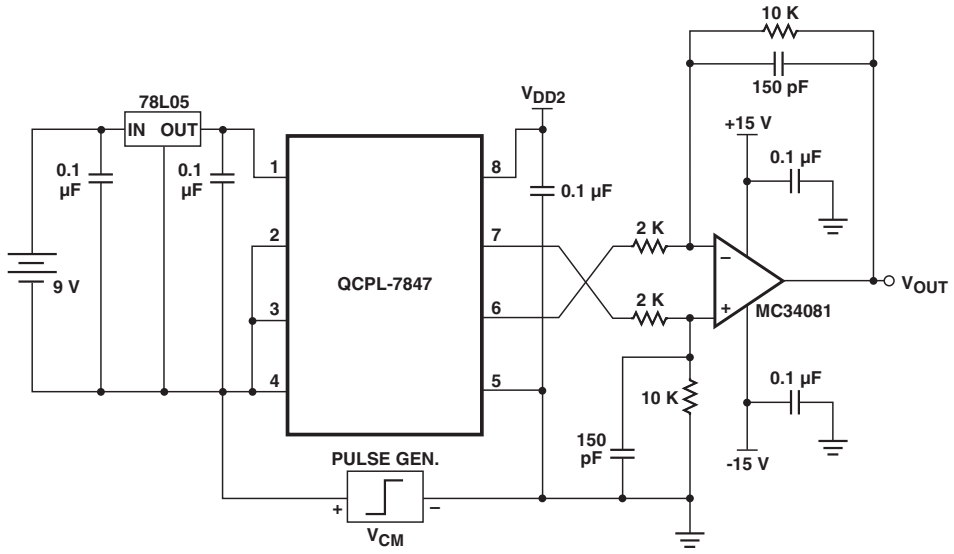


Figure 16. CMTI test circuits.

Application Information

Power Supplies and Bypassing

The recommended supply connections are shown in Figure 17. A floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a simple zener diode (D1); the value of resistor R4 should be chosen to supply sufficient current from the existing floating supply. The voltage from the current sensing resistor (Rsense) is applied to the input of the QCPL-7847 through an RC anti-aliasing filter (R2 and C2). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance.

The power supply for the QCPL-7847 is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter.

An inexpensive 78L05 three-terminal regulator can also be used to reduce the floating supply voltage to 5 V. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

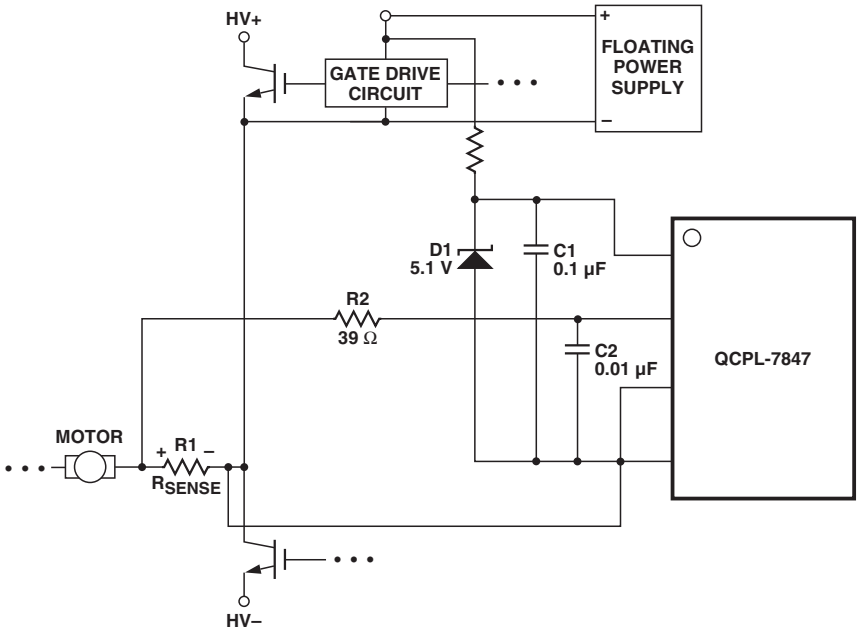


Figure 17. Recommended supply and sense resistor connections.

As shown in Figure 18, 0.1 µF bypass capacitors (C1, C2) should be located as close as possible to the pins of the QCPL-7847. The bypass capacitors are required because of the high-speed digital nature of the signals inside the QCPL-7847. A 0.01 µF bypass capacitor (C2) is also recommended at the input due to the switched-capacitor also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal. The input filter also performs an important reliability function—it reduces transient spikes from ESD events flowing through the current sensing resistor.

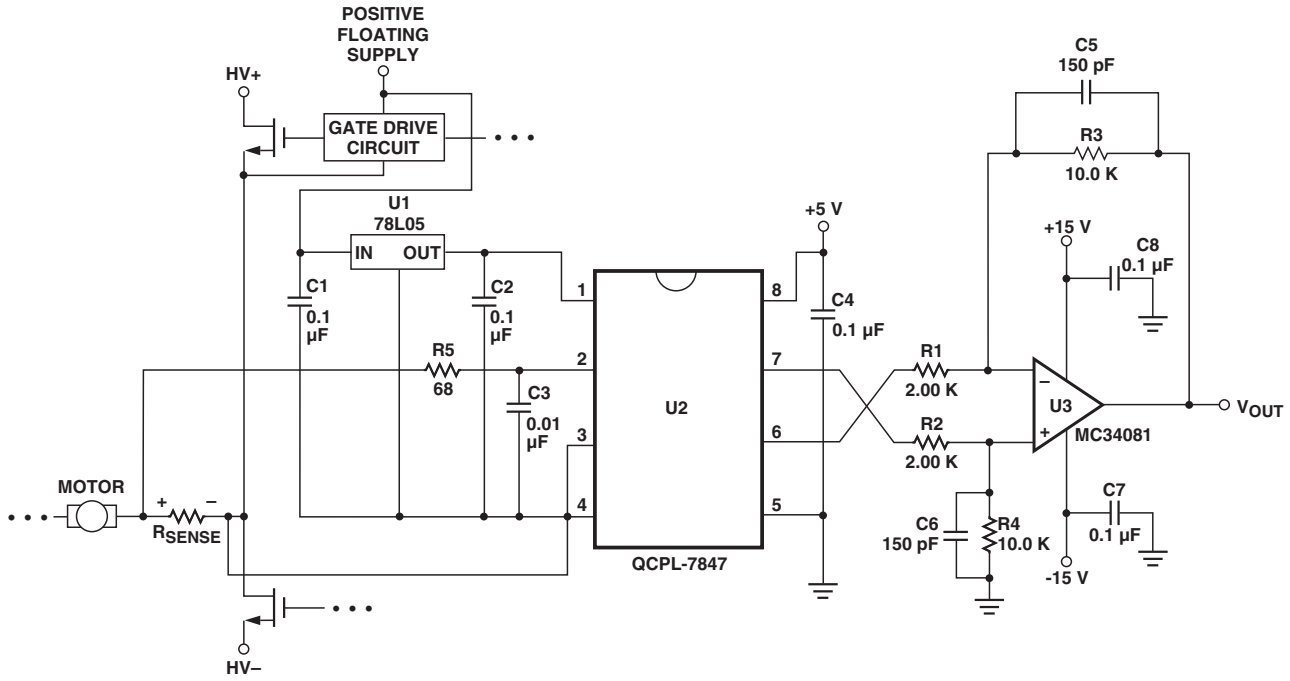


Figure 18. Recommended application circuit.

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. In addition, the layout of the PCB can also affect the isolation transient immunity (CMTI) of the QCPL-7847, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMTI performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the QCPL-7847.

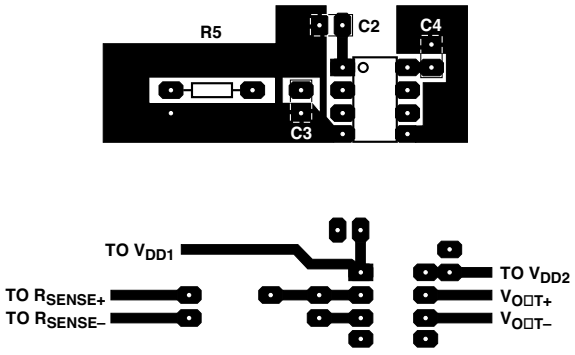


Figure 19. Example printed circuit board layout.

Current Sensing Resistors

The current sensing resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistance decreases power dissipation, while larger sense resistance can improve circuit accuracy by utilizing the full input range of the QCPL-7847.

The first step in selecting a sense resistor is determining how much current the resistor will be sensing. The graph in Figure 20 shows the RMS current in each phase of a three-phase induction motor as a function of average motor output power (in horse-power, hp) and motor drive supply voltage. The maximum value of the sense re-sistor is determined by the current being measured and the maxi-mum recommended input voltage of the isolation amplifier. The maximum sense resistance can be calculated by taking the maxi-mum recommended input voltage and dividing by the peak current that the sense resistor should see during normal operation. For example, if a motor will have a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (=10 x 1.414 x 1.5). Assuming a maximum input voltage of 200 mV, the maximum value of sense resistance in this case would be about 10 mΩ.

The maximum average power dissipation in the sense resistor can also be easily calculated by multiplying the sense resistance times the square of the maximum RMS current, which is about 1 W in the previous example. If the power dissipation in the sense resistor is too high, the resistance can be decreased below the maximum value to decrease power dissipation. The minimum value of the sense resistor is limited by precision and accuracy requirements of the design. As the resistance value is reduced, the output voltage across the resistor is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the sense resistor will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design.

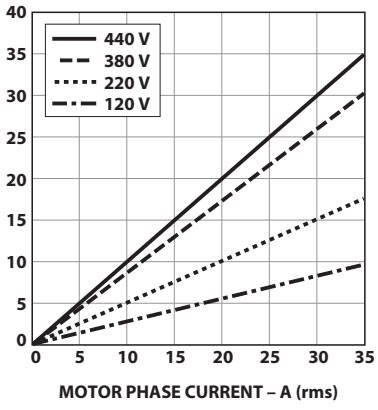


Figure 20. Motor output horsepower vs. motor phase current and supply voltage.

When sensing currents large enough to cause significant heating of the sense resistor, the temperature coefficient (tempco) of the resistor can introduce nonlinearity due to the signal dependent temperature rise of the resistor. The effect increases as the resistor-to-ambient ther-mal resistance increases. This effect can be minimized by reducing the thermal resistance of the current sensing resistor or by using a resistor with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the current sensing resistor on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink.

For a two-terminal current sensing resistor, as the value of resistance decreases, the resistance of the leads become a significant percentage of the total resistance. This has two primary effects on resistor accuracy. First, the effective resistance of the sense resistor can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the leads during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material, such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco overall.

Both of these effects are eliminated when a four-terminal current sensing resistor is used. A four-terminal resistor has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage.

When laying out a PC board for the current sensing resistors, a couple of points should be kept in mind. The Kelvin connections to the resistor should be brought together under the body of the resistor and then run very close to each other to the input of the QCPL-7847; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the sense resistor is not located on the same PC board as the QCPL-7847 circuit, a tightly twisted pair of wires can accomplish the same thing.

Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the sense resistor to help distribute the current between the layers of the PC board. The PC board should use 2 or 4 oz. copper for the layers, resulting in a current carrying capacity in excess of 20 A. Making the current carrying traces on the PC board fairly large can also improve the sense resistor's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

Sense Resistor Connections

The recommended method for connecting the QCPL-7847 to the current sensing resistor is shown in Figure 18. V_{IN+} (pin 2 of the QCPL-7847) is connected to the positive terminal of the sense resistor resistor, while V_{IN-} (pin 3) is shorted to GND1 (pin 4), with the power-supply return path functioning as the sense line to the negative terminal of the current sense resistor. This allows a single pair of wires or PC board traces to connect the QCPL-7847 circuit to the sense resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the resistor are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current sensing resistor.

If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the QCPL-7847 to the sense resistor be the only return path for supply current to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the QCPL-7847 circuit and the gate drive circuit should be the positive power supply line.

Output Side

The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C5 and C6) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isola-tion amplifier. Many different op-amps could be used in the circuit, including: MC34082A (Motorola), TLO32A, TLO52A, and TLC277 (Texas Instruments), LF412A (National Semiconductor).

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate CMRR and adequate gain toler-ance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

Please refer to Avago Applications Note 1078 for additional information on using Isolation Amplifiers.

FREQUENTLY ASKED QUESTIONS ABOUT THE QCPL-7847

1. THE BASICS

1.1: Why should I use the QCPL-7847 for sensing current when Hall-effect sensors are available which don't need an isolated supply voltage?

Available in an auto-insertable, 8-pin DIP package, the QCPL-7847 is smaller than and has better linearity, offset vs. temperature and Common Mode Rejection (CMR) performance than most Hall-effect sensors. Additionally, often the required input-side power supply can be derived from the same supply that powers the gate-drive optocoupler.

2. SENSE RESISTOR AND INPUT FILTER

2.1: Where do I get 10 mΩ resistors? I have never seen one that low.

Although less common than values above 10 Ω, there are quite a few manufacturers of resistors suitable for measuring currents up to 50 A when combined with the QCPL-7847. Example product information may be found at Dale's web site (http://www.vishay.com/vishay/dale) and Isotek's web site (http://www.isotekcorp.com).

2.2: Should I connect both inputs across the sense resistor instead of grounding V_{IN-} directly to pin 4?

This is not necessary, but it will work. If you do, be sure to use an RC filter on both pin 2 (V_{IN+}) and pin 3 (V_{IN-}) to limit the input voltage at both pads.

2.3: Do I really need an RC filter on the input? What is it for? Are other values of R and C okay?

The input anti-aliasing filter (R=39 Ω, C=0.01 μF) shown in the typical application circuit is recommended for filtering fast switching voltage transients from the input signal. (This helps to attenuate higher signal frequencies which could otherwise alias with the input sampling rate and cause higher input offset voltage.)

Some issues to keep in mind using different filter resistors or capacitors are:

1. (Filter resistor:) Input bias current for pins 2 and 3: This is on the order of 500 nA. If you are using a single filter resistor in series with pin 2 but not pin 3 the IxR drop across this resistor will add to the offset error of the device. As long as this IR drop is small compared to the input offset voltage there should not be a problem. If larger-valued resistors are used in series, it is better to put half of the resistance in series with pin 2 and half the resistance in series with pin 3. In this case, the offset voltage is due mainly to resistor mismatch (typically less than 1% of the resistance design value) multiplied by the input bias.
2. (Filter resistor:) The equivalent input resistance for QCPL-7847 is around 500 kΩ. It is therefore best to ensure that the filter resistance is not a significant percentage of this value; otherwise the offset voltage will be increased through the resistor divider effect. [As an example, if R_{filt} = 5.5 kΩ, then V_{OS} = (Vin * 1%) = 2 mV for a maximum 200 mV input and V_{OS} will vary with respect with Vin.]
3. The input bandwidth is changed as a result of this different R-C filter configuration. In fact this is one of the main reasons for changing the input-filter R-C time constant.
4. (Filter capacitance:) The input capacitance of the -78XX is approximately 1.5 pF. For proper operation the switching input-side sampling capacitors must be charged from a relatively fixed (low impedance) voltage source. Therefore, if a filter capacitor is used it is best for this capacitor to be a few orders of magnitude greater than the C_{INPUT} (A value of at least 100 pF works well.)

2.4: How do I ensure that the QCPL-7847 is not destroyed as a result of short circuit conditions which cause voltage drops across the sense resistor that exceed the ratings of the QCPL-7847's inputs?

Select the sense resistor so that it will have less than 5 V drop when short circuits occur. The only other requirement is to shut down the drive before the sense resistor is damaged or its solder joints melt. This ensures that the input of the QCPL-7847 can not be damaged by sense resistors going open-circuit.

3. ISOLATION AND INSULATION

3.1: How many volts will the QCPL-7847 withstand?

The momentary (1 minute) withstand voltage is 3750 V rms per UL 1577 and CSA Component Acceptance Notice #5.

4. ACCURACY

4.1: Can the signal to noise ratio be improved?

Yes. Some noise energy exists beyond the 100 kHz bandwidth of the QCPL-7847. Additional filtering using different filter R,C values in the post-amplifier application circuit can be used to improve the signal to noise ratio. For example, by using values of R3 = R4 = 10 kΩ, C5 = C6 = 470 pF in the application circuit the rms output noise will be cut roughly by a factor of 2. In applications needing only a few kHz bandwidth even better noise performance can be obtained. The noise spectral density is roughly 500 nV/√ Hz below 20 kHz (input referred).

4.2: I need 1% tolerance on gain. Does Avago sell a more precise version?

The HCPL-7800A is gain-trimmed and matched to within ±1% tolerance (at room temperature.)

4.3: Does the gain change if the internal LED light output degrades with time?

No. The LED is used only to transmit a digital pattern. Avago has accounted for LED degradation in the design of the product to ensure long life.

5. POWER SUPPLIES AND START-UP

5.1: What are the output voltages before the input side power supply is turned on?

V_{O+} is close to 1.29 V and V_{O-} is close to 3.80 V. This is equivalent to the output response at the condition that LED is completely off.

5.2: How long does the QCPL-7847 take to begin working properly after power-up?

Within 1 ms after V_{DD1} and V_{DD2} powered the device starts to work. But it takes longer time for output to settle down completely. In case of the offset measurement while both inputs are tied to ground there is initially V_{OS} adjustment (about 60 ms). The output completely settles down in 100 ms after device powering up.

6. MISCELLANEOUS

6.1: How does the QCPL-7847 measure negative signals with only a +5 V supply?

The inputs have a series resistor for protection against large negative inputs. Normal signals are no more than 200 mV in amplitude. Such signals do not forward bias any junctions sufficiently to interfere with accurate operation of the switched capacitor input circuit.

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