THC63LVD1023B

160MHz 67Bits LVDS Transmitter

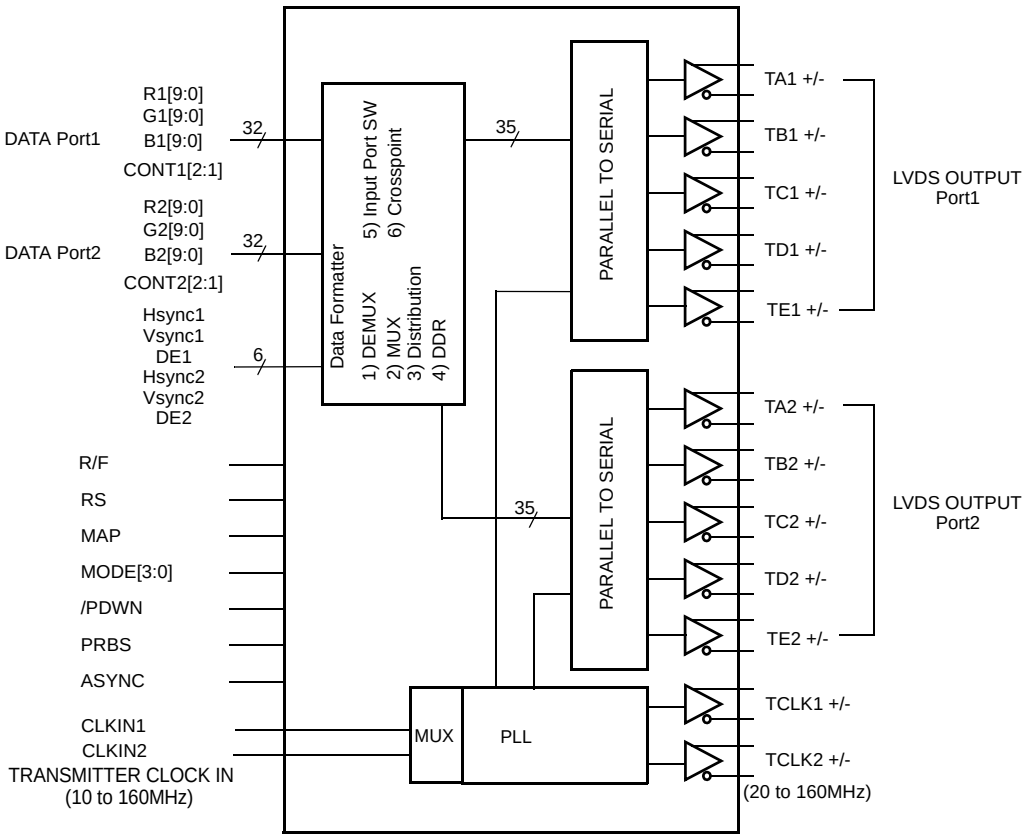
General Description

The THC63LVD1023B transmitter is designed to suport Single Link transmission between Host and Flat Panel Display up to 1080p(60Hz) resolutions and Dual Link transmission between Host and Flat Panel Display up to 1080p(120Hz).
The THC63LVD1023B converts 67bits of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin, and support double edge inputs.
In Dual Link, the transmit clock frequency of 160MHz, 67bits of RGB data are transmitted at an effective rate of 1.12Gbps per LVDS channel.
In Asynchronous mode, the THC63LVD1023B has 2 independent 35Bits Transmitter.

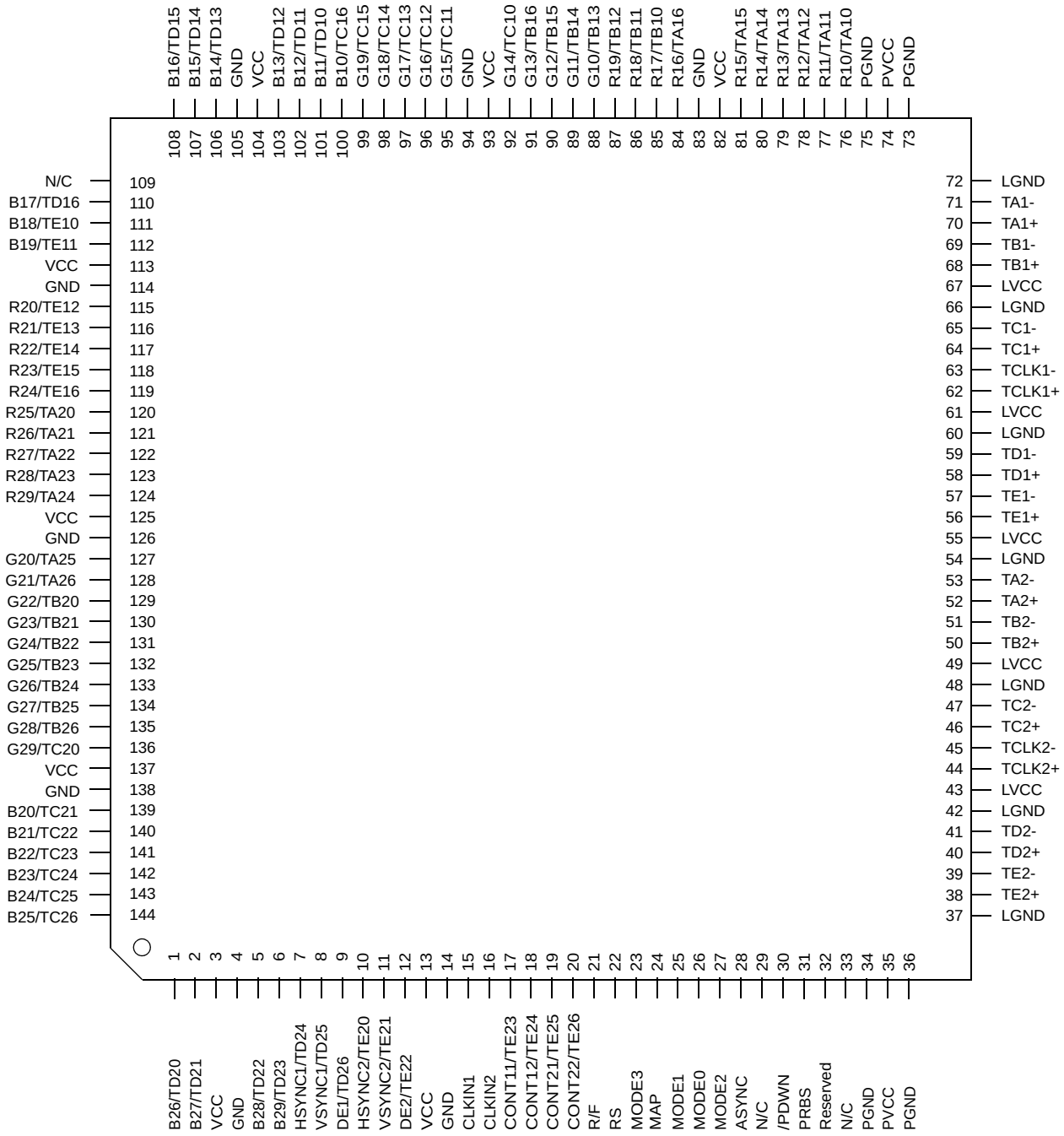
Features

- Wide dot clock range suited for TV Signal (480i-1080p), PC Signal (VGA-QXGA)
  TTL/CMOS Input: 10-160MHz
  LVDS Output: 20-160MHz
- PLL requires No external components
- Flexible Input/Output mode
  1. Single/Dual TTL IN, Single/Dual LVDS OUT
  2. Double edge input for Single TTL IN/Dual LVDS OUT
  3. Input port SW for Single TTL IN/Dual LVDS OUT
  4. Asynchronous Dual TTL IN/Dual LVDS OUT
- Clock edge selectable
- 3 LVDS data mapping for simplifying PCB layout.
- Pseudo Random pattern generation circuit
- Supports Reduced swing LVDS for Low EMI
- Power down mode
- Low power single 3.3V CMOS design
- Backward compatible with THC63LVD1023
- 144pin LQFP

Block Diagram



Pin Out (top view)



Pin Description

<table>
<tr><th colspan="2">Pin Name</th><th rowspan="2">Pin #</th><th rowspan="2">Type</th><th rowspan="2">Description</th></tr>
<tr><th>ASYNC=L</th><th>ASYNC=H</th></tr>
<tr><td colspan="2">TA1+, TA1-</td><td>70, 71</td><td rowspan="12">LVDS OUT</td><td rowspan="3">The 1st Link.
The 1st pixel output data when Dual-Link.</td></tr>
<tr><td colspan="2">TB1+, TB1-</td><td>68, 69</td></tr>
<tr><td colspan="2">TC1+, TC1-</td><td>64, 65</td></tr>
<tr><td colspan="2">TD1+, TD1-</td><td>58, 59</td><td rowspan="2">The 1st Link.
The 1st pixel output data when Dual-Link.</td></tr>
<tr><td colspan="2">TE1+, TE1-</td><td>56, 57</td></tr>
<tr><td colspan="2">TCLK1+, TCLK1-</td><td>62, 63</td><td>LVDS Clock Out for 1st and 2nd Link.</td></tr>
<tr><td colspan="2">TA2+, TA2-</td><td>52, 53</td><td rowspan="5">The 2nd Link.
These pins are disabled when Single Link.</td></tr>
<tr><td colspan="2">TB2+, TB2-</td><td>50, 51</td></tr>
<tr><td colspan="2">TC2+, TC2-</td><td>46, 47</td></tr>
<tr><td colspan="2">TD2+, TD2-</td><td>40, 41</td></tr>
<tr><td colspan="2">TE2+, TE2-</td><td>38, 39</td></tr>
<tr><td colspan="2">TCLK2+, TCLK2-</td><td>44, 45</td><td>See following table.
<table>
<tr><th>ASYNC</th><th>MODE0</th><th>MODE1</th><th>MODE2</th><th>Description</th></tr>
<tr><td>H</td><td>x</td><td>x</td><td>L</td><td>Case1</td></tr>
<tr><td>H</td><td>x</td><td>x</td><td>H</td><td>Case2</td></tr>
<tr><td>L</td><td>L</td><td>x</td><td>x</td><td>Case3</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>x</td><td>Case4</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>L</td><td>Case4</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td>Case3</td></tr>
</table>
Case1: LVDS Clock out for 2nd link.
Case2: LVDS Clock out for 1st link.
Case3: Additional LVDS Clock out.
Identical to TCLK1+/-
Case4: Not available (High-Impedance)</td></tr>
<tr><td>R19 ~ R10</td><td>TB12~TB10,
TA16~TA10</td><td>87 - 84,
81 - 76</td><td rowspan="3">IN</td><td rowspan="3">ASYNC=L
The 1st Pixel Data Inputs.
ASYNC=H
Data Inputs.</td></tr>
<tr><td>G19 ~ G10</td><td>TC15~TC10,
TB16~TB13</td><td>99 - 95,
92 - 88</td></tr>
<tr><td>B19 ~ B10</td><td>TE11~TE10,
TD16~TD10,
TC16</td><td>112 -110,
108 -106,
103 - 100</td></tr>
<tr><td>R29 ~ R20</td><td>TA24~TA20,
TE16~TE12</td><td>124 - 115</td><td rowspan="3">IN</td><td rowspan="3">ASYNC=L
The 2nd Pixel Data Inputs.
ASYNC=H
Data Inputs.</td></tr>
<tr><td>G29 ~ G20</td><td>TC20,
TB26~TB20,
TA26~TA25</td><td>136 - 127</td></tr>
<tr><td>B29 ~ B20</td><td>TD23~TD20,
TC26~TC21</td><td>6, 5, 2, 1,
144 - 139</td></tr>
</table>

Pin Description (Continued)

<table>
<tr><th colspan="2">Pin Name</th><th rowspan="2">Pin #</th><th rowspan="2">Type</th><th rowspan="2">Description</th></tr>
<tr><th>ASYNC=L</th><th>ASYNC=H</th></tr>
<tr><td>CONT11 *1,
CONT12 *1</td><td>TE23,TE24</td><td>17, 18</td><td rowspan="2">IN</td><td rowspan="2">ASYNC=L: CONTROL Data Inputs.
ASYNC=H: Data Inputs.</td></tr>
<tr><td>CONT21 *1,
CONT22 *1</td><td>TE25,TE26</td><td>19, 20</td></tr>
<tr><td>DE1,DE2</td><td>TD26,TE22</td><td>9,12</td><td>IN</td><td>ASYNC=L: Data Enable Inputs.
ASYNC=H: Data Inputs.</td></tr>
<tr><td>VSYNC1,
VSYNC2</td><td>TD25,TE21</td><td>8,11</td><td>IN</td><td>ASYNC=L: Vsync Inputs.
ASYNC=H: Data Inputs</td></tr>
<tr><td>HSYNC1,
HSYNC2</td><td>TD24,TE20</td><td>7,10</td><td>IN</td><td>ASYNC=L: Hsync Inputs.
ASYNC=H: Data Inputs</td></tr>
<tr><td colspan="2">CLKIN1</td><td>15</td><td>IN</td><td>Clock Input of following cases.
<table>
<tr><th>ASYNC</th><th>MODE1</th><th>MODE0</th><th>MODE3</th></tr>
<tr><td>H</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>L</td><td>L</td><td>x</td><td>x</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>x</td></tr>
</table></td></tr>
<tr><td colspan="2">CLKIN2</td><td>16</td><td>IN</td><td>Clock Input of following cases.
<table>
<tr><th>ASYNC</th><th>MODE1</th><th>MODE0</th><th>MODE3</th></tr>
<tr><td>H</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>L</td></tr>
</table></td></tr>
<tr><td colspan="2">R/F</td><td>21</td><td>IN</td><td>Input Clock Triggering Edge Select.
H: Rising edge, L: Falling edge</td></tr>
<tr><td colspan="2">RS</td><td>22</td><td>IN</td><td>LVDS swing mode, V_{REF} select. See Fig4, 5.
<table>
<tr><th>RS</th><th>LVDS Swing</th><th>Small Swing Input Support</th></tr>
<tr><td>V_{IHM}</td><td>350mV</td><td>N/A</td></tr>
<tr><td>V_{IMM}</td><td>350mV</td><td>RS=V_{REF} [a]</td></tr>
<tr><td>V_{ILM}</td><td>200mV</td><td>N/A</td></tr>
</table>
a. V_{REF} is Input Reference Voltage.</td></tr>
<tr><td colspan="2">MAP
(See Fig7 to 9 and Table4 to10)</td><td>24</td><td>IN</td><td>LVDS mapping table select.
<table>
<tr><th>MAP</th><th>Mapping Mode</th></tr>
<tr><td>V_{IHM}</td><td>Mapping MODE1</td></tr>
<tr><td>V_{ILM}</td><td>Mapping MODE2</td></tr>
<tr><td>V_{IMM}</td><td>Mapping MODE3</td></tr>
</table></td></tr>
<tr><td colspan="2">MODE1, MODE0</td><td>25, 26</td><td>IN</td><td>Pixel Data Mode.
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Mode</th></tr>
<tr><td>L</td><td>L</td><td>Dual Link (Dual-in/Dual-out)</td></tr>
<tr><td>H</td><td>L</td><td>Dual Link (Single-in/Dual-out)</td></tr>
<tr><td>L</td><td>H</td><td>Single Link (Dual-in/Single-out)</td></tr>
<tr><td>H</td><td>H</td><td>Single Link (Single-in/Single-out)</td></tr>
</table></td></tr>
</table>

*1: CONT## are DATA pins that user can use as data like RGB data.

Pin Name		Pin #	Type	Description
ASYNC=L	ASYNC=H			
MODE2 (See Fig.5)		27	IN	The use of these multi-function depends on the setting of MODE<1:0> or ASYNC. ASYNC=H(MODE<1:0>=Don't care.) H: Cross point switching enable. L: Cross point switching disable. ASYNC=L MODE<1:0>=HH(Single-in/Single-out Mode) H: Distribution function enable. L: Distribution function disable. MODE<1:0>=HL(Single-in/Dual-out Mode) H: DDR (Double Edge input) function enable. L: DDR (Double Edge input) function disable.
MODE3		23	IN	Input port switching function enable when MODE<1:0>=HL(Single-in/Dual-out Mode). H or Open: Port switch disable. L: Port switch enable.
ASYNC		28	IN	Asynchronous function enable. H: Asynchronous mode enable.(MODE<1:0>=Disable) L: Asynchronous mode disable.(MODE<1:0>=Enable)
/PDWN		30	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)
PRBS *2		31	IN	PRBS (Pseudo-Random Binary Sequence) generator is active in order to evaluate eye patterns when MODE<1:0> = LL (Dual-in/Dual-out mode) or ASYNC=H H: PRBS generator is enable. L: Normal Operation
Reserved		32	IN	Must be tied to GND.
N/C		29, 33, 109		Must be Open.
VCC		3, 13, 82, 93, 104, 113, 125, 137	Power	Power Supply Pins for TTL inputs and digital circuitry.
GND		4, 14, 83, 94, 105, 114, 126, 138	Ground	Ground Pins for TTL inputs and digital circuitry.
LVCC		43, 49, 55, 61, 67	Power	Power Supply Pins for LVDS Outputs.
LGND		37, 42, 48, 54, 60, 66, 72	Ground	Ground Pins for LVDS Outputs.
PVCC		35, 74	Power	Power Supply Pins for PLL circuitry.
PGND		34, 36, 73, 75	Ground	Ground Pins for PLL circuitry.

*2: Setting the PRBS pin high enables the internal test pattern generator. It generates Pseudo-Random Bit Sequence of 2^{23}-1. The generated PRBS is fed into input data latches, formatted as VGA video like data, encoded and serialized into TXOUT output. This function is normally to be used for analyzing the signal integrity of the transmission channel including PCB traces, connectors, and cables.

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Driver Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Reflow Peak Temperature / Time	+260°C / 10sec.
Maximum Power Dissipation @+25°C	2.4W

Recommended Operating Conditions

Parameter				Min.	Typ	Max	Units
All Supply Voltage				3.0	3.3	3.6	V
Operating Ambient Temperature				-20		70	°C
Clock Frequency	MODE<1:0>=LL Dual-in/Dual-out		Input	20		160	MHz
			LVDS Output	20		160	MHz
	MODE<1:0>=LH Dual-in/Single-out		Input	10		80	MHz
			LVDS Output	20		160	MHz
	MODE<1:0>=HL Single-in/Dual-out	Single Edge Input (MODE2=L)	Input	40		160	MHz
			LVDS Output	20		80	MHz
		Double Edge Input (MODE2=H)	Input	20		80	MHz
			LVDS Output	20		80	MHz
	MODE<1:0>=HH Single-in/Single-out		Input	20		160	MHz
			LVDS Output	20		160	MHz
	ASYNC=H Asynchronous Mode		Input	20		160	MHz
			LVDS Output	20		160	MHz

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}[a]	High Level Data Input Voltage	RS=V_{cc}or GND	2.0		V_{CC}	V
		RS=0.6~1.4V	V_{REF}[b]+0.1			V
V_{IL}[a]	Low Level Data Input Voltage	RS=V_{cc}or GND	GND		0.8	V
		RS=0.6~1.4V			V_{REF}-0.1	V
V_{IHC}[c]	High Level Control Input Voltage		2.0		V_{CC}	V
V_{ILC}[c]	Low Level Control Input Voltage		GND		0.8	V
V_{IHM}[d]	High Level Control Input Voltage		0.8V_{CC}		V_{CC}	V
V_{IMM}[d]	Middle Level Control Input Voltage		0.6		1.4	V
V_{ILM}[d]	Low Level Control Input Voltage		GND		0.08V_{CC}	V
I_{INC}	Input Current (except MODE3)	GND ≤ V_{IN} ≤ V_{CC}			±10	μA
I_{INCM3}	Input Current (Only MODE3)	GND ≤ V_{IN} ≤ V_{CC}			±20	μA

a. CLKIN1,R10~R19,G10~G19,B10~B19,DE1,HSYNC1,VSYNC1,CONT11,CONT12
CLKIN2,R20~R29,G20~G29,B20~B29,DE2,HSYNC2,VSYNC2,CONT21,CONT22

b. V_{REF} is input voltage of RS pin.

c. R/F,MODE0,MODE1,MODE2,MODE3,PDWN,PRBS,ASYNC

d. RS,MAP

LVDS Transmitter DC Specifications

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS= V_{cc}	250	350	450	mV
			Reduced swing RS= GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=GND, RL=100Ω				-24	mA
I_{OZ}	Output TRI-State current	/PDWN=GND, VOUT=GND to V_{CC}				±10	μA

Electrical Characteristics (Continued)

Supply Current

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter	Condition			Typ.	Max.	Units
I_{TCCW}	Transmitter Supply Current (Worst Case Pattern) Fig1.	RL=100Ω CL=5pF RS=V_{CC}	MODE<1:0>=HH Single-in/Single-out MODE2=L Distribution Off	CLKIN1=65MHz		105	mA
				CLKIN1=85MHz		121	mA
				CLKIN1=135MHz		157	mA
				CLKIN1=160MHz		179	mA
			MODE<1:0>=HH Single-in/Single-out MODE2=H Distribution On	CLKIN1=65MHz		146	mA
				CLKIN1=85MHz		172	mA
				CLKIN1=135MHz		217	mA
				CLKIN1=160MHz		250	mA
			MODE<1:0>=HL Single-in/Dual-out MODE2=L MODE3=H or L DDR Input Off	CLKIN1/2=65MHz		108	mA
				CLKIN1/2=85MHz		136	mA
				CLKIN1/2=135MHz		169	mA
				CLKIN1/2=160MHz		194	mA
			MODE<1:0>=HL Single-in/Dual-out MODE2=H MODE3=H or L DDR Input On	CLKIN1/2=32.5MHz		120	mA
				CLKIN1/2=42.5MHz		140	mA
				CLKIN1/2=67.5MHz		183	mA
				CLKIN1/2=80MHz		199	mA
			MODE<1:0>=LH Dual-in/Single-out	CLKIN1=32.5MHz		95	mA
				CLKIN1=42.5MHz		110	mA
				CLKIN1=67.5MHz		143	mA
				CLKIN1=80MHz		166	mA
			MODE<1:0>=LL Dual-in/Dual-out	CLKIN1=65MHz		167	mA
				CLKIN1=85MHz		197	mA
				CLKIN1=135MHz		261	mA
				CLKIN1=160MHz		301	mA
			ASYNC=H Asynchronous	CLKIN1/2=65MHz		183	mA
				CLKIN1/2=85MHz		214	mA
				CLKIN1/2=135MHz		286	mA
				CLKIN1=160MHz		329	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L, All Inputs = Fixed L or H				50	μA

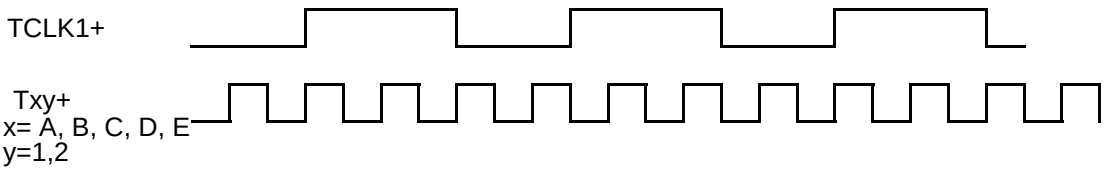


Fig1. Test Pattern (LVDS Output Full Toggle Pattern)

Switching Characteristics

V_{CC} = VCC=PVCC=LVCC

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{TCIP}	CLK IN Period(Fig4,5)		6.25		100	ns
t_{TCH}	CLK IN High Time(Fig4,5)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TCL}	CLK IN Low Time(Fig4,5)		$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TS}	TTL Data Setup to CLK IN(Fig4,5)		2.5			ns
t_{TH}	TTL Data Hold from CKL IN(Fig4,5)		0.0			ns
t_{TCD}	CLK IN to TCLK+/- Delay(Fig4,5) MODE<1:0>=LL Dual-in/Dual-out		$(4+3/7)t_{TCIP}$ +2.6		$(4+3/7)t_{TCIP}$ +7.5	ns
t_{TCOP}	CLK OUT Period(Fig6)		6.25		50	ns
t_{LVT}	LVDS Transition Time(Fig2)			0.6	1.5	ns
t_{TOP1}	Output Data Position0 (Fig6)	t_{TCOP} = 6.25ns~20ns	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (Fig6)		$\frac{t_{TCOP}}{7} - 0.15$	$\frac{t_{TCOP}}{7}$	$\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP6}	Output Data Position2 (Fig6)		$2\frac{t_{TCOP}}{7} - 0.15$	$2\frac{t_{TCOP}}{7}$	$2\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP5}	Output Data Position3 (Fig6)		$3\frac{t_{TCOP}}{7} - 0.15$	$3\frac{t_{TCOP}}{7}$	$3\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP4}	Output Data Position4 (Fig6)		$4\frac{t_{TCOP}}{7} - 0.15$	$4\frac{t_{TCOP}}{7}$	$4\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP3}	Output Data Position5 (Fig6)		$5\frac{t_{TCOP}}{7} - 0.15$	$5\frac{t_{TCOP}}{7}$	$5\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TOP2}	Output Data Position6 (Fig6)		$6\frac{t_{TCOP}}{7} - 0.15$	$6\frac{t_{TCOP}}{7}$	$6\frac{t_{TCOP}}{7} + 0.15$	ns
t_{TPLL}	PLL Lock time(Fig3)				10.0	ms
t_{DEINT}	DE input period (Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE<2:0>=LHL)		$4t_{TCIP}$	tTCIP*(2n) [a]		ns
t_{DEH}	DE High time (Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE<2:0>=LHL)		$2t_{TCIP}$	tTCIP*(2m)[a]		ns
t_{DEL}	DE Low time(Fig3-1) Single-in / Dual-out, DDR Off mode only(MODE<2:0>=LHL)		$2t_{TCIP}$			ns

a. Refer to Fig3-1 for details.

AC Timing Diagrams

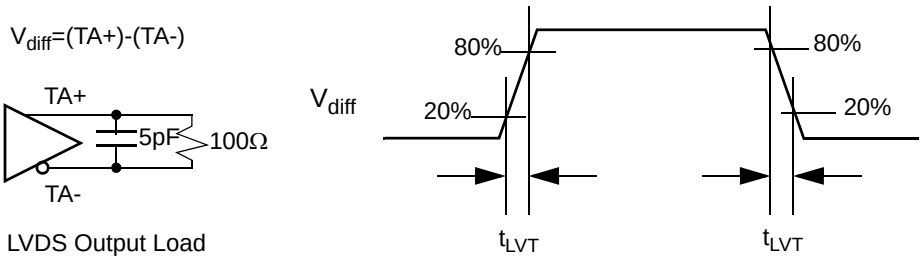


Fig2. LVDS Output Load and Transition Time

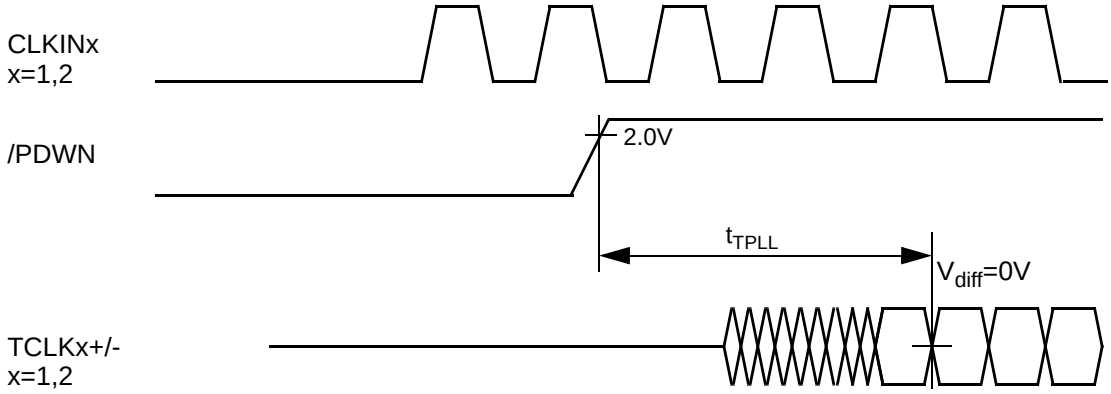
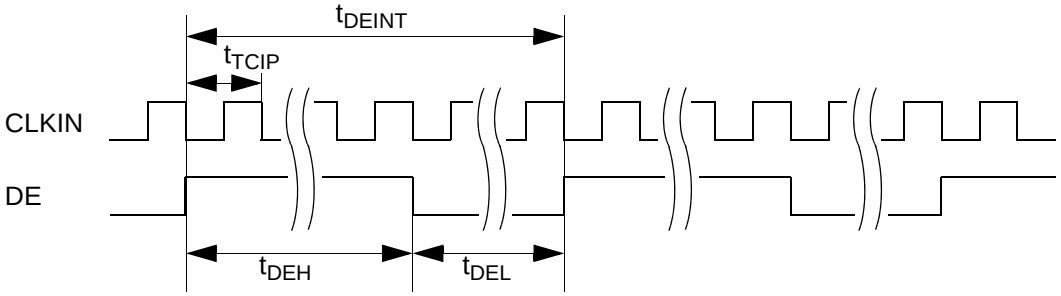


Fig3. PLL Lock Time



Note: In single-in/dual-out, DDR off mode (MODE<2:0>=LHL),
the period between rising edges of DE (t_{DEINT}), high time of DE (t_{DEH})
should always satisfy following equations.

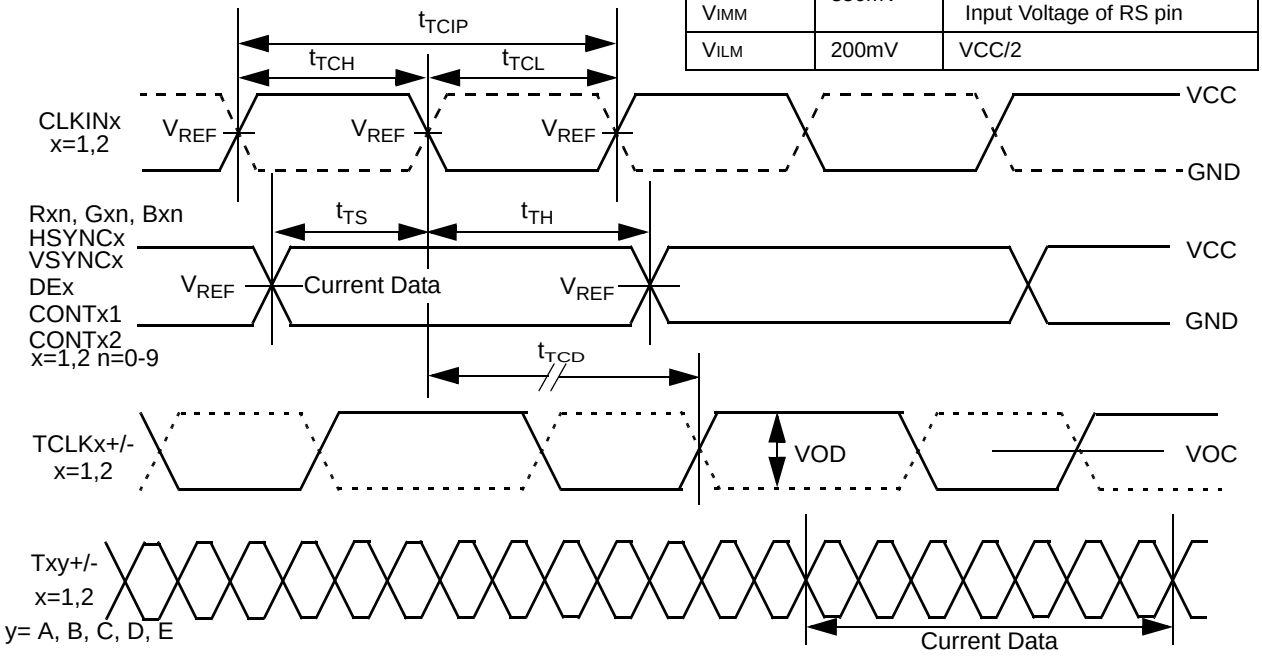
$$t_{DEH} = tTCIP * (2m)$$
$$t_{DEINT} = tTCIP * (2n)$$

m, n =integer

Fig3-1. Single IN / Dual OUT, DDR off mode DE input timing

AC Timing Diagrams (Continued)

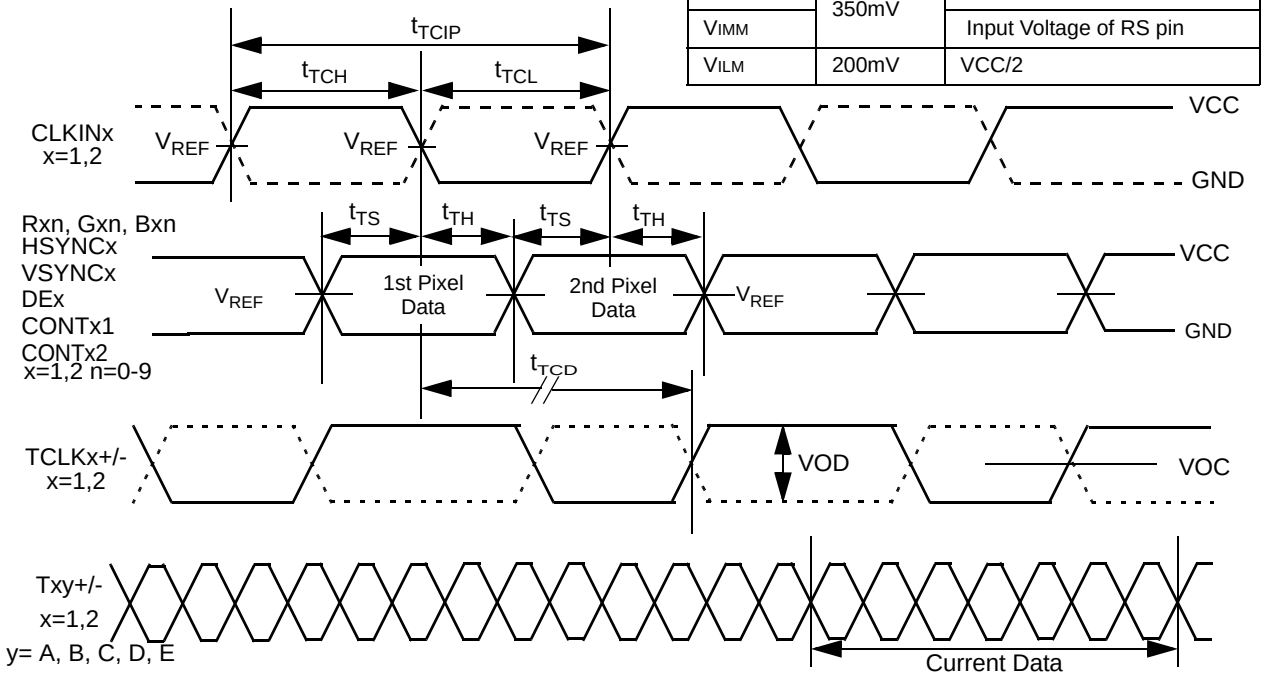
RS pin	VOD	VREF
VIHM	350mV	VCC/2
VIMM		Input Voltage of RS pin
VILM	200mV	VCC/2



Note:
CLKINx: for R/F=GND, denote as solid line,
x=1,2 for R/F=VCC, denote as dashed line.

Fig4. CLKIN Period, High/Low Time, Setup/Hold Timing

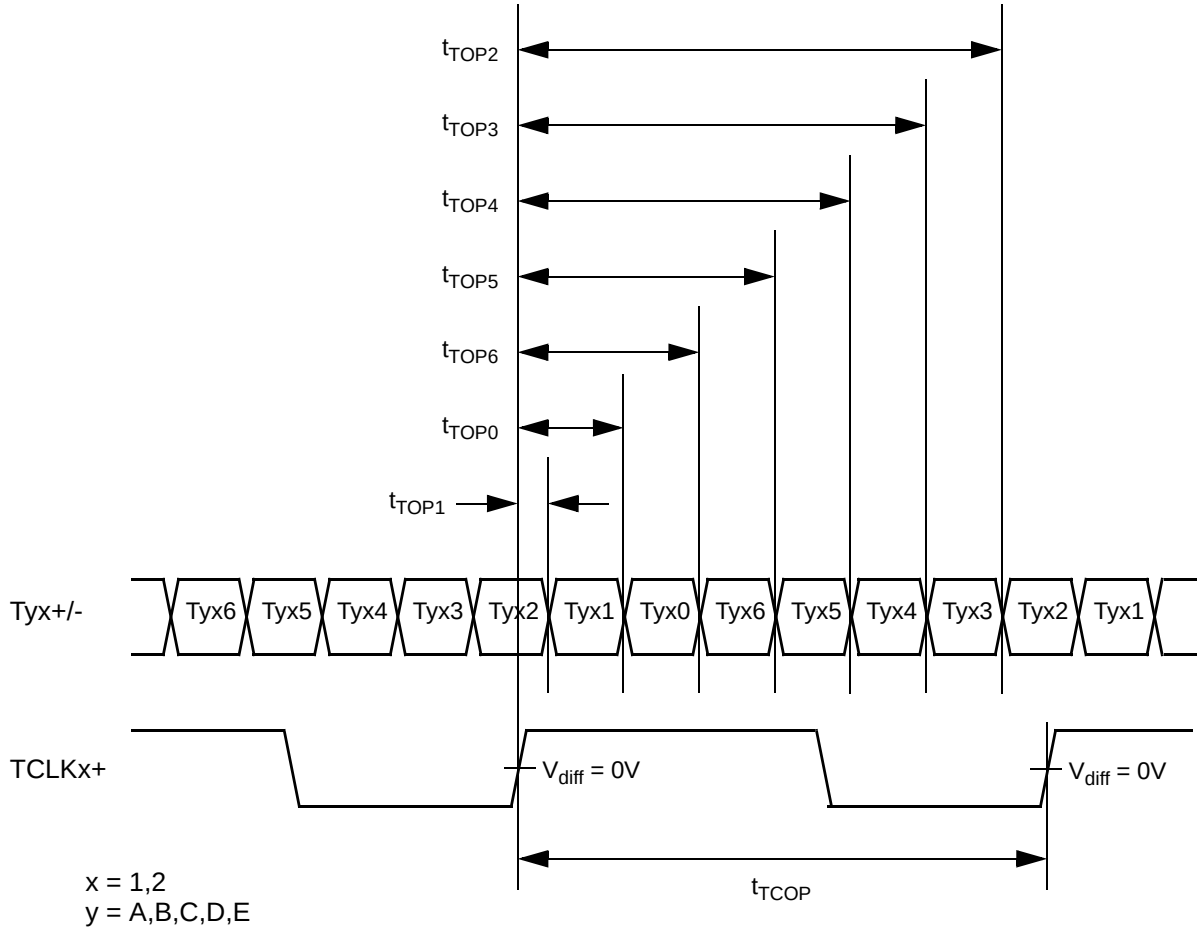
RS pin	VOD	VREF
VIHM	350mV	VCC/2
VIMM		Input Voltage of RS pin
VILM	200mV	VCC/2



Note:
CLKINx: for R/F=GND, denote as solid line,
x=1,2 for R/F=VCC, denote as dashed line.

Fig5. CLKIN Period, High/Low Time, Setup/Hold Timing for Double Edge Input Mode (DDR)
MODE<1:0>=HL, MODE2=H

AC Timing Diagrams (Continued)



Note:
V_{diff} = (Tyx+) - (Tyx-), (TCLKx+) - (TCLKx-)

Fig6. LVDS Output Data Position

Input Data Mapping

•Table1. Input Color Data naming rule

X	Y	Z	Description	
X=R			Red Color Data	
X=G			Green Color Data	
X=B			Blue Color Data	
	Y= None		Single Pixel	
	Y=E		Dual Pixel	1st Pixel Data
	Y=O			2nd Pixel Data
		Z=0-9	Bit number 0: LSB (Least Significant Bit) 9: MSB (Most Significant Bit)	

•Table2. TTL/CMOS Input Data Mapping (Single-in mode, MODE1=H)

Data Signals			Transmitter Input Pin Names		
30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
R0			R10		
R1			R11		
R2	R0		R12	R12	
R3	R1		R13	R13	
R4	R2	R0	R14	R14	R14
R5	R3	R1	R15	R15	R15
R6	R4	R2	R16	R16	R16
R7	R5	R3	R17	R17	R17
R8	R6	R4	R18	R18	R18
R9	R7	R5	R19	R19	R19
G0			G10		
G1			G11		
G2	G0		G12	G12	
G3	G1		G13	G13	
G4	G2	G0	G14	G14	G14
G5	G3	G1	G15	G15	G15
G6	G4	G2	G16	G16	G16
G7	G5	G3	G17	G17	G17
G8	G6	G4	G18	G18	G18
G9	G7	G5	G19	G19	G19
B0			B10		
B1			B11		
B2	B0		B12	B12	
B3	B1		B13	B13	
B4	B2	B0	B14	B14	B12
B5	B3	B1	B15	B15	B13
B6	B4	B2	B16	B16	B14
B7	B5	B3	B17	B17	B15
B8	B6	B4	B18	B18	B16
B9	B7	B5	B19	B19	B17

Input Data Mapping (Continued)

•Table3. TTL/CMOS Input Data Mapping (Dual-in mode, MODE1=L)

Data Signals			Transmitter Input Pin Names			Data Signals			Transmitter Input Pin Names		
30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
RE0			R10			RO0			R20		
RE1			R11			RO1			R22		
RE2	RE0		R12	R12		RO2	RO0		R22	R22	
RE3	RE1		R13	R13		RO3	RO1		R23	R23	
RE4	RE2	RE0	R14	R14	R14	RO4	RO2	RO0	R24	R24	R24
RE5	RE3	RE1	R15	R15	R15	RO5	RO3	RO1	R25	R25	R25
RE6	RE4	RE2	R16	R16	R16	RO6	RO4	RO2	R26	R26	R26
RE7	RE5	RE3	R17	R17	R17	RO7	RO5	RO3	R27	R27	R27
RE8	RE6	RE4	R18	R18	R18	RO8	RO6	RO4	R28	R28	R28
RE9	RE7	RE5	R19	R19	R19	RO9	RO7	RO5	R29	R29	R29
GE0			G10			GO0			G20		
GE1			G11			GO1			G22		
GE2	GE0		G12	G12		GO2	GO0		G22	G22	
GE3	GE1		G13	G13		GO3	GO1		G23	G23	
GE4	GE2	GE0	G14	G14	G14	GO4	GO2	GO0	G24	G24	G24
GE5	GE3	GE1	G15	G15	G15	GO5	GO3	GO1	G25	G25	G25
GE6	GE4	GE2	G16	G16	G16	GO6	GO4	GO2	G26	G26	G26
GE7	GE5	GE3	G17	G17	G17	GO7	GO5	GO3	G27	G27	G27
GE8	GE6	GE4	G18	G18	G18	GO8	GO6	GO4	G28	G28	G28
GE9	GE7	GE5	G19	G19	G19	GO9	GO7	GO5	G29	G29	G29
BE0			B10			BO0			B20		
BE1			B11			BO1			B22		
BE2	BE0		B12	B12		BO2	BO0		B22	B22	
BE3	BE1		B13	B13		BO3	BO1		B23	B23	
BE4	BE2	BE0	B14	B14	B14	BO4	BO2	BO0	B24	B24	B24
BE5	BE3	BE1	B15	B15	B15	BO5	BO3	BO1	B25	B25	B25
BE6	BE4	BE2	B16	B16	B16	BO6	BO4	BO2	B26	B26	B26
BE7	BE5	BE3	B17	B17	B17	BO7	BO5	BO3	B27	B27	B27
BE8	BE6	BE4	B18	B18	B18	BO8	BO6	BO4	B28	B28	B28
BE9	BE7	BE5	B19	B19	B19	BO9	BO7	BO5	B29	B29	B29

LVDS Output Data Mapping

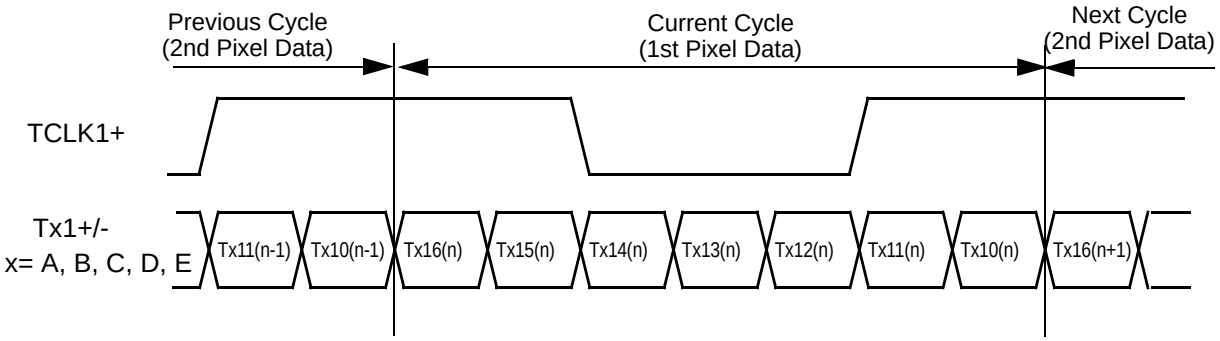


Fig7. TTL Data Inputs Mapped to LVDS outputs
MODE0= H (Single-out Mode)

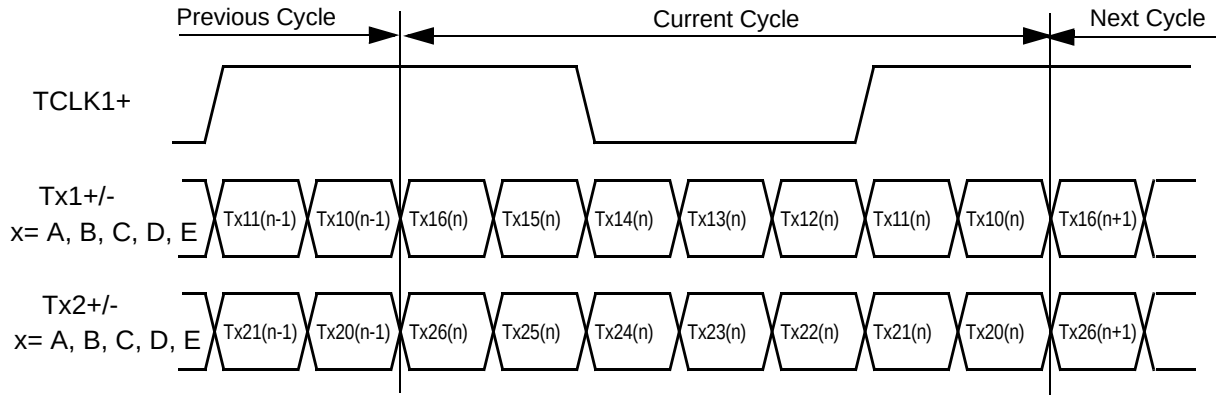


Fig8. TTL Data Inputs Mapped to LVDS outputs
MODE0= L (Dual-out Mode)

LVDS Output Data Mapping (Continued)

•Table4. LVDS Output Data Mapping (Single-in/Single-out Distribution Off, MODE<1:0>=HH, MODE2=L)

LVDS Output Data	Mapping Mode (Input Pin Name)		
	Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}
TA10	R14	R12	R10
TA11	R15	R13	R11
TA12	R16	R14	R12
TA13	R17	R15	R13
TA14	R18	R16	R14
TA15	R19	R17	R15
TA16	G14	G12	G10
TB10	G15	G13	G11
TB11	G16	G14	G12
TB12	G17	G15	G13
TB13	G18	G16	G14
TB14	G19	G17	G15
TB15	B14	B12	B10
TB16	B15	B13	B11
TC10	B16	B14	B12
TC11	B17	B15	B13
TC12	B18	B16	B14
TC13	B19	B17	B15
TC14	HSYNC1	HSYNC1	HSYNC1
TC15	VSYNC1	VSYNC1	VSYNC1
TC16	DE1	DE1	DE1
TD10	R12	R18	R16
TD11	R13	R19	R17
TD12	G12	G18	G16
TD13	G13	G19	G17
TD14	B12	B18	B16
TD15	B13	B19	B17
TD16	CONT11	CONT11	CONT11
TE10	R10	R10	R18
TE11	R11	R11	R19
TE12	G10	G10	G18
TE13	G11	G11	G19
TE14	B10	B10	B18
TE15	B11	B11	B19
TE16	CONT12	CONT12	CONT12

LVDS Output Data Mapping (Continued)

•Table5. LVDS Output Data Mapping (Single-in/Single-out Distribution On, MODE<1:0>=HH, MODE2=H)

LVDS Output Data (1st Link)	Mapping Mode (Input Pin Name)			LVDS Output Data (2nd Link)	Mapping Mode (Input Pin Name)		
	Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}		Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}
TA10	R14	R12	R10	TA20	R14	R12	R10
TA11	R15	R13	R11	TA21	R15	R13	R11
TA12	R16	R14	R12	TA22	R16	R14	R12
TA13	R17	R15	R13	TA23	R17	R15	R13
TA14	R18	R16	R14	TA24	R18	R16	R14
TA15	R19	R17	R15	TA25	R19	R17	R15
TA16	G14	G12	G10	TA26	G14	G12	G10
TB10	G15	G13	G11	TB20	G15	G13	G11
TB11	G16	G14	G12	TB21	G16	G14	G12
TB12	G17	G15	G13	TB22	G17	G15	G13
TB13	G18	G16	G14	TB23	G18	G16	G14
TB14	G19	G17	G15	TB24	G19	G17	G15
TB15	B14	B12	B10	TB25	B14	B12	B10
TB16	B15	B13	B11	TB26	B15	B13	B11
TC10	B16	B14	B12	TC20	B16	B14	B12
TC11	B17	B15	B13	TC21	B17	B15	B13
TC12	B18	B16	B14	TC22	B18	B16	B14
TC13	B19	B17	B15	TC23	B19	B17	B15
TC14	HSYNC1	HSYNC1	HSYNC1	TC24	HSYNC1	HSYNC1	HSYNC1
TC15	VSYNC1	VSYNC1	VSYNC1	TC25	VSYNC1	VSYNC1	VSYNC1
TC16	DE	DE	DE1	TC26	DE	DE	DE1
TD10	R12	R18	R16	TD20	R12	R18	R16
TD11	R13	R19	R17	TD21	R13	R19	R17
TD12	G12	G18	G16	TD22	G12	G18	G16
TD13	G13	G19	G17	TD23	G13	G19	G17
TD14	B12	B18	B16	TD24	B12	B18	B16
TD15	B13	B19	B17	TD25	B13	B19	B17
TD16	CONT11	CONT11	CONT11	TD26	CONT11	CONT11	CONT11
TE10	R10	R10	R18	TE20	R10	R10	R18
TE11	R11	R11	R19	TE21	R11	R11	R19
TE12	G10	G10	G18	TE22	G10	G10	G18
TE13	G11	G11	G19	TE23	G11	G11	G19
TE14	B10	B10	B18	TE24	B10	B10	B18
TE15	B11	B11	B19	TE25	B11	B11	B19
TE16	CONT12	CONT12	CONT12	TE26	CONT12	CONT12	CONT12

LVDS Output Data Mapping (Continued)

•Table6. LVDS Output Data Mapping

(Single-in/Dual-out, DDR On or Off, Port Switch Off, MODE<1:0>=HL, MODE2=H or L, MODE3=H or Open)

LVDS Output Data (1st Link)	Mapping Mode (Input Pin Name)			LVDS Output Data (2nd Link)	Mapping Mode (Input Pin Name)		
	Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}		Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}
TA10	R14	R12	R10	TA20	R14	R12	R10
TA11	R15	R13	R11	TA21	R15	R13	R11
TA12	R16	R14	R12	TA22	R16	R14	R12
TA13	R17	R15	R13	TA23	R17	R15	R13
TA14	R18	R16	R14	TA24	R18	R16	R14
TA15	R19	R17	R15	TA25	R19	R17	R15
TA16	G14	G12	G10	TA26	G14	G12	G10
TB10	G15	G13	G11	TB20	G15	G13	G11
TB11	G16	G14	G12	TB21	G16	G14	G12
TB12	G17	G15	G13	TB22	G17	G15	G13
TB13	G18	G16	G14	TB23	G18	G16	G14
TB14	G19	G17	G15	TB24	G19	G17	G15
TB15	B14	B12	B10	TB25	B14	B12	B10
TB16	B15	B13	B11	TB26	B15	B13	B11
TC10	B16	B14	B12	TC20	B16	B14	B12
TC11	B17	B15	B13	TC21	B17	B15	B13
TC12	B18	B16	B14	TC22	B18	B16	B14
TC13	B19	B17	B15	TC23	B19	B17	B15
TC14	HSYNC1	HSYNC1	HSYNC1	TC24	HSYNC1	HSYNC1	HSYNC1
TC15	VSYNC1	VSYNC1	VSYNC1	TC25	VSYNC1	VSYNC1	VSYNC1
TC16	DE1	DE1	DE1	TC26	DE1	DE1	DE1
TD10	R12	R18	R16	TD20	R12	R18	R16
TD11	R13	R19	R17	TD21	R13	R19	R17
TD12	G12	G18	G16	TD22	G12	G18	G16
TD13	G13	G19	G17	TD23	G13	G19	G17
TD14	B12	B18	B16	TD24	B12	B18	B16
TD15	B13	B19	B17	TD25	B13	B19	B17
TD16	CONT11	CONT11	CONT11	TD26	CONT11	CONT11	CONT11
TE10	R10	R10	R18	TE20	R10	R10	R18
TE11	R11	R11	R19	TE21	R11	R11	R19
TE12	G10	G10	G18	TE22	G10	G10	G18
TE13	G11	G11	G19	TE23	G11	G11	G19
TE14	B10	B10	B18	TE24	B10	B10	B18
TE15	B11	B11	B19	TE25	B11	B11	B19
TE16	CONT12	CONT12	CONT12	TE26	CONT12	CONT12	CONT12

LVDS Output Data Mapping (Continued)

•Table7. LVDS Output Data Mapping

(Single-in/Dual-out, DDR On or Off, Port Switch On, MODE<1:0>=HL, MODE2=H or L, MODE3=L)

LVDS Output Data (1st Link)	Mapping Mode (Input Pin Name)			LVDS Output Data (2nd Link)	Mapping Mode (Input Pin Name)		
	Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}		Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}
TA10	R24	R22	R20	TA20	R24	R22	R20
TA11	R25	R23	R21	TA21	R25	R23	R21
TA12	R26	R24	R22	TA22	R26	R24	R22
TA13	R27	R25	R23	TA23	R27	R25	R23
TA14	R28	R26	R24	TA24	R28	R26	R24
TA15	R29	R27	R25	TA25	R29	R27	R25
TA16	G24	G22	G20	TA26	G24	G22	G20
TB10	G25	G23	G21	TB20	G25	G23	G21
TB11	G26	G24	G22	TB21	G26	G24	G22
TB12	G27	G25	G23	TB22	G27	G25	G23
TB13	G28	G26	G24	TB23	G28	G26	G24
TB14	G29	G27	G25	TB24	G29	G27	G25
TB15	B24	B22	B20	TB25	B24	B22	B20
TB16	B25	B23	B21	TB26	B25	B23	B21
TC10	B26	B24	B22	TC20	B26	B24	B22
TC11	B27	B25	B23	TC21	B27	B25	B23
TC12	B28	B26	B24	TC22	B28	B26	B24
TC13	B29	B27	B25	TC23	B29	B27	B25
TC14	HSYNC2	HSYNC2	HSYNC2	TC24	HSYNC2	HSYNC2	HSYNC2
TC15	VSYNC2	VSYNC2	VSYNC2	TC25	VSYNC2	VSYNC2	VSYNC2
TC16	DE2	DE2	DE2	TC26	DE2	DE2	DE2
TD10	R22	R28	R26	TD20	R22	R28	R26
TD11	R23	R29	R27	TD21	R23	R29	R27
TD12	G22	G28	G26	TD22	G22	G28	G26
TD13	G23	G29	G27	TD23	G23	G29	G27
TD14	B22	B28	B26	TD24	B22	B28	B26
TD15	B23	B29	B27	TD25	B23	B29	B27
TD16	CONT21	CONT21	CONT21	TD26	CONT21	CONT21	CONT21
TE10	R20	R20	R28	TE20	R20	R20	R28
TE11	R21	R21	R29	TE21	R21	R21	R29
TE12	G20	G20	G28	TE22	G20	G20	G28
TE13	G21	G21	G29	TE23	G21	G21	G29
TE14	B20	B20	B28	TE24	B20	B20	B28
TE15	B21	B21	B29	TE25	B21	B21	B29
TE16	CONT22	CONT22	CONT22	TE26	CONT22	CONT22	CONT22

LVDS Output Data Mapping (Continued)

•Table8. LVDS Output Data Mapping (Dual-in/Single-out, MODE<1:0>=LH)

LVDS Output Data (1st Pixel)	Mapping Mode (Input Pin Name)			LVDS Output Data (2nd Pixel)	Mapping Mode (Input Pin Name)		
	Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}		Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}
TA10(n)	R14	R12	R10	TA10(n+1)	R24	R22	R20
TA11(n)	R15	R13	R11	TA11(n+1)	R25	R23	R21
TA12(n)	R16	R14	R12	TA12(n+1)	R26	R24	R22
TA13(n)	R17	R15	R13	TA13(n+1)	R27	R25	R23
TA14(n)	R18	R16	R14	TA14(n+1)	R28	R26	R24
TA15(n)	R19	R17	R15	TA15(n+1)	R29	R27	R25
TA16(n)	G14	G12	G10	TA16(n+1)	G24	G22	G20
TB10(n)	G15	G13	G11	TB10(n+1)	G25	G23	G21
TB11(n)	G16	G14	G12	TB11(n+1)	G26	G24	G22
TB12(n)	G17	G15	G13	TB12(n+1)	G27	G25	G23
TB13(n)	G18	G16	G14	TB13(n+1)	G28	G26	G24
TB14(n)	G19	G17	G15	TB14(n+1)	G29	G27	G25
TB15(n)	B14	B12	B10	TB15(n+1)	B24	B22	B20
TB16(n)	B15	B13	B11	TB16(n+1)	B25	B23	B21
TC10(n)	B16	B14	B12	TC10(n+1)	B26	B24	B22
TC11(n)	B17	B15	B13	TC11(n+1)	B27	B25	B23
TC12(n)	B18	B16	B14	TC12(n+1)	B28	B26	B24
TC13(n)	B19	B17	B15	TC13(n+1)	B29	B27	B25
TC14(n)	HSYNC1	HSYNC1	HSYNC1	TC14(n+1)	HSYNC1	HSYNC1	HSYNC1
TC15(n)	VSYNC1	VSYNC1	VSYNC1	TC15(n+1)	VSYNC1	VSYNC1	VSYNC1
TC16(n)	DE1	DE1	DE1	TC16(n+1)	DE1	DE1	DE1
TD10(n)	R12	R18	R16	TD10(n+1)	R22	R28	R26
TD11(n)	R13	R19	R17	TD11(n+1)	R23	R29	R27
TD12(n)	G12	G18	G16	TD12(n+1)	G22	G28	G26
TD13(n)	G13	G19	G17	TD13(n+1)	G23	G29	G27
TD14(n)	B12	B18	B16	TD14(n+1)	B22	B28	B26
TD15(n)	B13	B19	B17	TD15(n+1)	B23	B29	B27
TD16(n)	CONT11	CONT11	CONT11	TD16(n+1)	CONT21	CONT21	CONT21
TE10(n)	R10	R10	R18	TE10(n+1)	R20	R20	R28
TE11(n)	R11	R11	R19	TE11(n+1)	R21	R21	R29
TE12(n)	G10	G10	G18	TE12(n+1)	G20	G20	G28
TE13(n)	G11	G11	G19	TE13(n+1)	G21	G21	G29
TE14(n)	B10	B10	B18	TE14(n+1)	B20	B20	B28
TE15(n)	B11	B11	B19	TE15(n+1)	B21	B21	B29
TE16(n)	CONT12	CONT12	CONT12	TE16(n+1)	CONT22	CONT22	CONT22

LVDS Output Data Mapping (Continued)

•Table9. LVDS Output Data Mapping (Dual-in/Dual-out, MODE<1:0>=LL)

LVDS Output Data (1st Link)	Mapping Mode (Input Pin Name)			LVDS Output Data (2nd Link)	Mapping Mode (Input Pin Name)		
	Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}		Mode1 MAP=V_{IHM}	Mode2 MAP=V_{ILM}	Mode3 MAP=V_{IMM}
TA10	R14	R12	R10	TA20	R24	R22	R20
TA11	R15	R13	R11	TA21	R25	R23	R21
TA12	R16	R14	R12	TA22	R26	R24	R22
TA13	R17	R15	R13	TA23	R27	R25	R23
TA14	R18	R16	R14	TA24	R28	R26	R24
TA15	R19	R17	R15	TA25	R29	R27	R25
TA16	G14	G12	G10	TA26	G24	G22	G20
TB10	G15	G13	G11	TB20	G25	G23	G21
TB11	G16	G14	G12	TB21	G26	G24	G22
TB12	G17	G15	G13	TB22	G27	G25	G23
TB13	G18	G16	G14	TB23	G28	G26	G24
TB14	G19	G17	G15	TB24	G29	G27	G25
TB15	B14	B12	B10	TB25	B24	B22	B20
TB16	B15	B13	B11	TB26	B25	B23	B21
TC10	B16	B14	B12	TC20	B26	B24	B22
TC11	B17	B15	B13	TC21	B27	B25	B23
TC12	B18	B16	B14	TC22	B28	B26	B24
TC13	B19	B17	B15	TC23	B29	B27	B25
TC14	HSYNC1	HSYNC1	HSYNC1	TC24	HSYNC1	HSYNC1	HSYNC1
TC15	VSYNC1	VSYNC1	VSYNC1	TC25	VSYNC1	VSYNC1	VSYNC1
TC16	DE1	DE1	DE1	TC26	DE1	DE1	DE1
TD10	R12	R18	R16	TD20	R22	R28	R26
TD11	R13	R19	R17	TD21	R23	R29	R27
TD12	G12	G18	G16	TD22	G22	G28	G26
TD13	G13	G19	G17	TD23	G23	G29	G27
TD14	B12	B18	B16	TD24	B22	B28	B26
TD15	B13	B19	B17	TD25	B23	B29	B27
TD16	CONT11	CONT11	CONT11	TD26	CONT21	CONT21	CONT21
TE10	R10	R10	R18	TE20	R20	R20	R28
TE11	R11	R11	R19	TE21	R21	R21	R29
TE12	G10	G10	G18	TE22	G20	G20	G28
TE13	G11	G11	G19	TE23	G21	G21	G29
TE14	B10	B10	B18	TE24	B20	B20	B28
TE15	B11	B11	B19	TE25	B21	B21	B29
TE16	CONT12	CONT12	CONT12	TE26	CONT22	CONT22	CONT22

LVDS Output Data Mapping (Continued)

•Table10. LVDS Output Data Mapping (Asynchronous Cross point switching Off, ASYNC=H MODE2=L)

LVDS Output Data (1st Link)	Mapping (MAP= Don't care) (Input Pin Name)	LVDS Output Data (2nd Link)	Mapping (MAP= Don't care) (Input Pin Name)
TA10	TA10	TA20	TA20
TA11	TA11	TA21	TA21
TA12	TA12	TA22	TA22
TA13	TA13	TA23	TA23
TA14	TA14	TA24	TA24
TA15	TA15	TA25	TA25
TA16	TA16	TA26	TA26
TB10	TB10	TB20	TB20
TB11	TB11	TB21	TB21
TB12	TB12	TB22	TB22
TB13	TB13	TB23	TB23
TB14	TB14	TB24	TB24
TB15	TB15	TB25	TB25
TB16	TB16	TB26	TB26
TC10	TC10	TC20	TC20
TC11	TC11	TC21	TC21
TC12	TC12	TC22	TC22
TC13	TC13	TC23	TC23
TC14	TC14	TC24	TC24
TC15	TC15	TC25	TC25
TC16	TC16	TC26	TC26
TD10	TD10	TD20	TD20
TD11	TD11	TD21	TD21
TD12	TD12	TD22	TD22
TD13	TD13	TD23	TD23
TD14	TD14	TD24	TD24
TD15	TD15	TD25	TD25
TD16	TD16	TD26	TD26
TE10	TE10	TE20	TE20
TE11	TE11	TE21	TE21
TE12	TE12	TE22	TE22
TE13	TE13	TE23	TE23
TE14	TE14	TE24	TE24
TE15	TE15	TE25	TE25
TE16	TE16	TE26	TE26

LVDS Output Data Mapping (Continued)

•Table11. LVDS Output Data Mapping (Asynchronous Cross point switching On, ASYNC=H MODE2=H)

LVDS Output Data (1st Link)	Mapping (MAP= Don't care) (Input Pin Name)	LVDS Output Data (2nd Link)	Mapping (MAP= Don't care) (Input Pin Name)
TA10	TA20	TA20	TA10
TA11	TA21	TA21	TA11
TA12	TA22	TA22	TA12
TA13	TA23	TA23	TA13
TA14	TA24	TA24	TA14
TA15	TA25	TA25	TA15
TA16	TA26	TA26	TA16
TB10	TB20	TB20	TB10
TB11	TB21	TB21	TB11
TB12	TB22	TB22	TB12
TB13	TB23	TB23	TB13
TB14	TB24	TB24	TB14
TB15	TB25	TB25	TB15
TB16	TB26	TB26	TB16
TC10	TC20	TC20	TC10
TC11	TC21	TC21	TC11
TC12	TC22	TC22	TC12
TC13	TC23	TC23	TC13
TC14	TC24	TC24	TC14
TC15	TC25	TC25	TC15
TC16	TC26	TC26	TC16
TD10	TD20	TD20	TD10
TD11	TD21	TD21	TD11
TD12	TD22	TD22	TD12
TD13	TD23	TD23	TD13
TD14	TD24	TD24	TD14
TD15	TD25	TD25	TD15
TD16	TD26	TD26	TD16
TE10	TE20	TE20	TE10
TE11	TE21	TE21	TE11
TE12	TE22	TE22	TE12
TE13	TE23	TE23	TE13
TE14	TE24	TE24	TE14
TE15	TE25	TE25	TE15
TE16	TE26	TE26	TE16

Note

1)Cable Connection and Disconnection

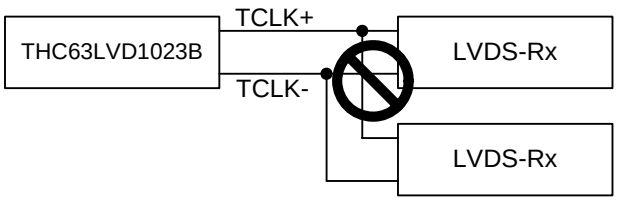
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2)GND Connection

Connect the each GND of the PCB which THC63LVD1023B and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

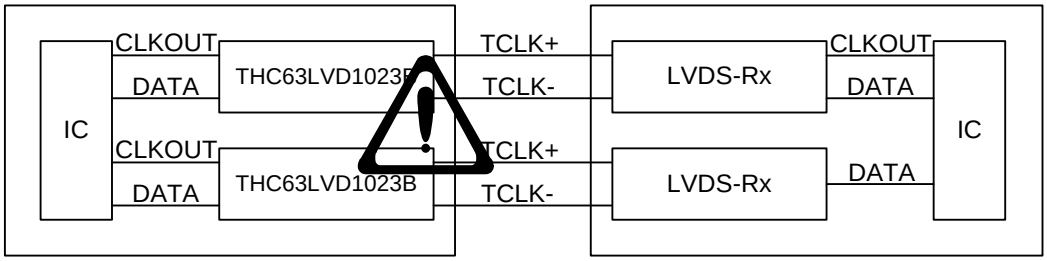
3)Multi Drop Connection

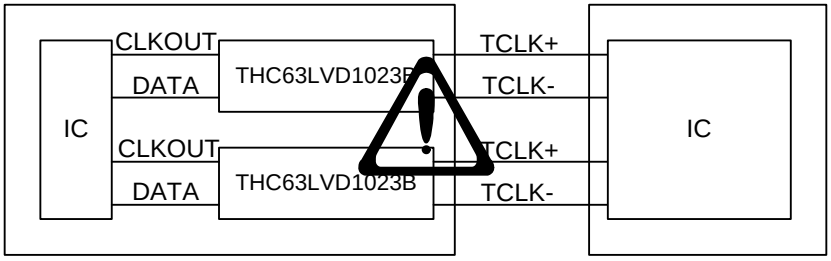
Multi drop connection is not recommended.



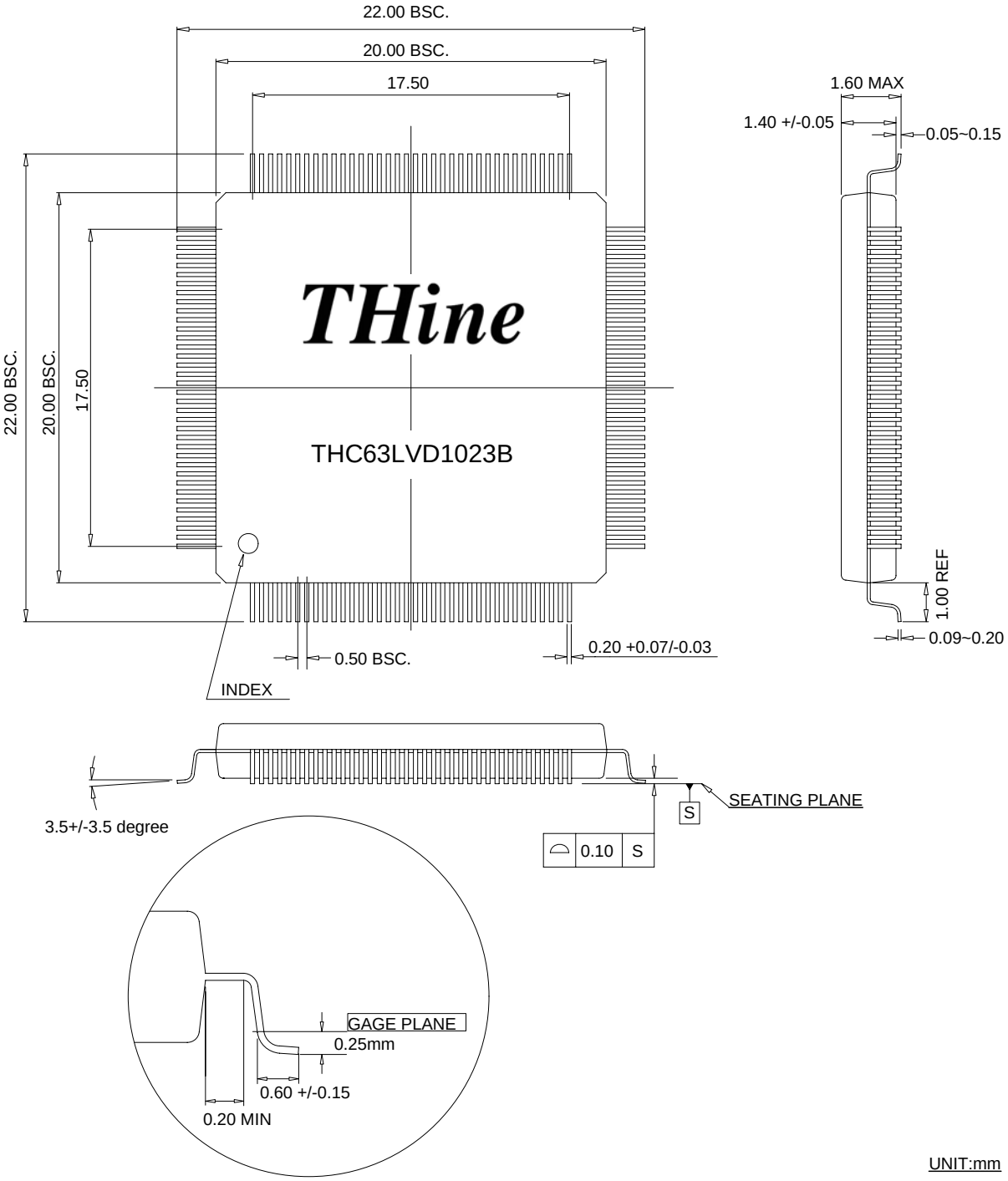
4)Asynchronous use

Asynchronous use such as following systems are not recommended.





Package


22.00 BSC.
20.00 BSC.
17.50
1.60 MAX
1.40 +/-0.05
0.05~0.15
THine
THC63LVD1023B
1.00 REF
0.09~0.20
0.50 BSC.
0.20 +0.07/-0.03
INDEX
3.5+/-3.5 degree
SEATING PLANE
S
0.10
S
GAGE PLANE
0.25mm
0.60 +/-0.15
0.20 MIN
UNIT:mm

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