THC63LVD103D

160MHz 30bit COLOR LVDS TRANSMITTER

General Description

The THC63LVD103D transmitter is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to 1080p(60Hz) .
The THC63LVD103D converts 35bits of CMOS/TTL data into four LVDS data streams. The transmitter can be programmed for rising edge or falling edge clock through a dedicated pin. At a transmit clock frequency of 160MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC, VSYNC, DE, CONT1) are transmitted at an effective rate of 1120Mbps per LVDS channel.

Application

- Medium and Small Size Panel
- Tablet PC / Notebook PC
- Security Camera / Industrial Camera
- Multi Function Printer
- Industrial Equipment
- Medical Equipment Monitor

Features

- Compatible with TIA/EIA-644 LVDS Standard
- 7:1 LVDS Transmitter
- Operating Temperature Range : 0 to +70°C
- No Special Start-up Sequence Required
- Spread Spectrum Clocking Tolerant up to 100kHz Frequency Modulation and +/-2.5% Deviations.
- Wide Dot Clock Range: 8 to 160MHz Suited for
  TV Signal : NTSC(12.27MHz) - 1080p(148.5MHz)
  PC Signal : QVGA(8MHz) - WUXGA(154MHz)
- 64pin TQFP Package
- 1.2V to 3.3V LVCMOS/ inputs are supported.
- LVDS swing is reducible as 200mV by RS-pin to reduce EMI and power consumption.
- PLL requires no external components.
- Power Down Mode.
- Input clock triggering edge is selectable by R/F-pin
- EU RoHS Compliant.

Block Diagram

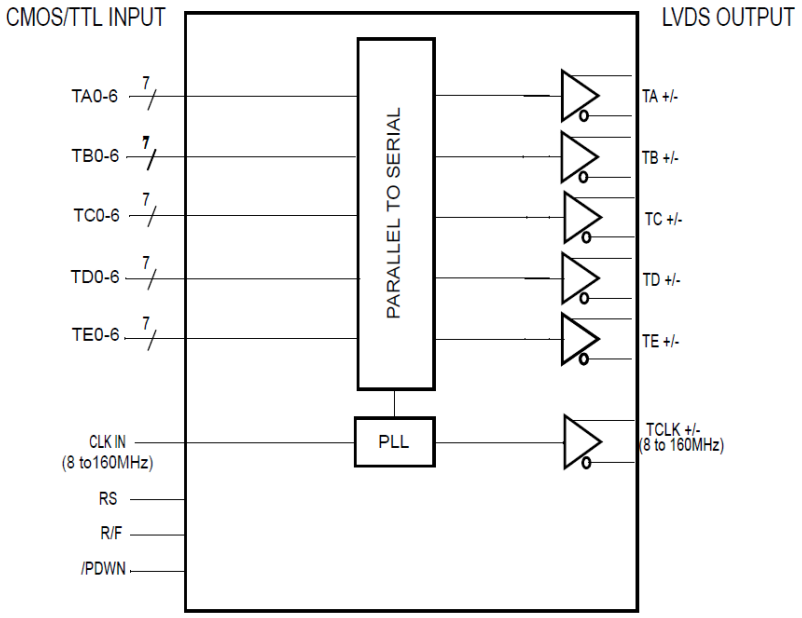


Figure 1. Block Diagram

Pin Diagram

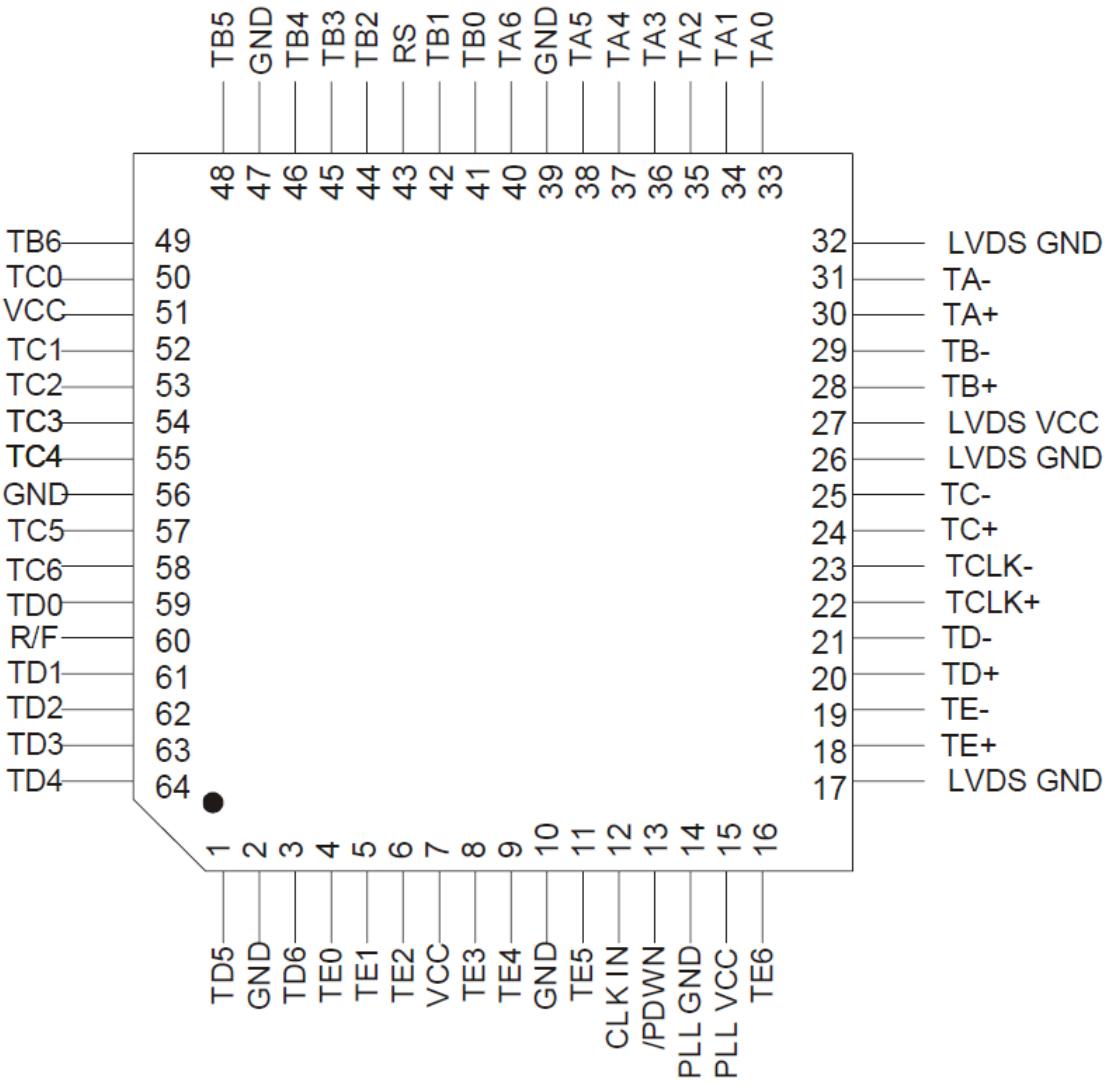


Figure 2. Pin Diagram

Pin Description

Pin Name	Pin #	Direction	Type	Description
TA+, TA-	30, 31	Output	LVDS	LVDS Data Out
TB+, TB-	28, 29			
TC+, TC-	24, 25			
TD+, TD-	20, 21			
TE+, TE-	18, 19			
TCLK+, TCLK-	22, 23			LVDS Clock Out
TA0 ~ TA6	33, 34, 35, 36, 37, 38, 40	Input	LVCMOS /TTL	Pixel Data Input
TB0 ~ TB6	41, 42, 44, 45, 46, 48, 49			
TC0 ~ TC6	50, 52, 53, 54, 55, 57, 58			
TD0 ~ TD6	59, 61, 62, 63, 64, 1, 3			
TE0 ~ TE6	4, 5, 6, 8, 9, 11, 16			
/PDWN	13			H : Normal Operation L : Power Down (All outputs are Hi-Z)
RS	43			LVDS Swing Mode, VREF Select See Fig.8, 9 RS / LVDS Swing / Small Swing Input Support VCC / 350mV / N/A 0.6 ~ 1.4V / 350mV / RS=VREF GND / 200mV / N/A VREF : is Input Reference Voltage
R/F	60			Input Clock Triggering Edge Select H : Rising Edge L : Falling Edge
CLKIN	12			Input Clock
VCC	51, 7	Power	-	Power Supply Pins for LVCMOS/TLL Inputs and Digital Circuitry.
GND	2, 10, 39, 47, 56			Ground Pins for LVCMOS/TTL Inputs and Digital Circuitry.
LVDS VCC	27			Power Supply Pins for LVDS Outputs.
LVDS GND	17, 26, 32			Ground Pins for LVDS Outputs.
PLL VCC	15			Power Supply Pin for PLL Circuitry.
PLL GND	14			Ground Supply Pin for PLL Circuitry.

Table 1. Pin Description

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage (VCC)	-0.3	+4.0	V
LVCMOS/TTL Input Voltage	-0.3	VCC + 0.3	V
LVCMOS/TTL Output Voltage	-0.3	VCC + 0.3	V
LVDS Output Pin	-0.3	VCC + 0.3	V
Output Current			mA
Junction Temperature	-	+125	°C
Storage Temperature	-55	+150	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	1.8	W

Table 2. Absolute Maximum Ratings

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
-	All Supply Voltage	3.0	3.3	3.6	V
Ta	Operating Ambient Temperature	0	25	+70	°C
-	Clock Frequency	8	-	160	MHz

Table 3. Recommended Operating Conditions

"Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics Table4, 5, 6, 7" specify conditions for device operation.
"Absolute Maximum Rating" value also includes behavior of overshooting and undershooting.

Equivalent LVDS Output Schematic Diagram

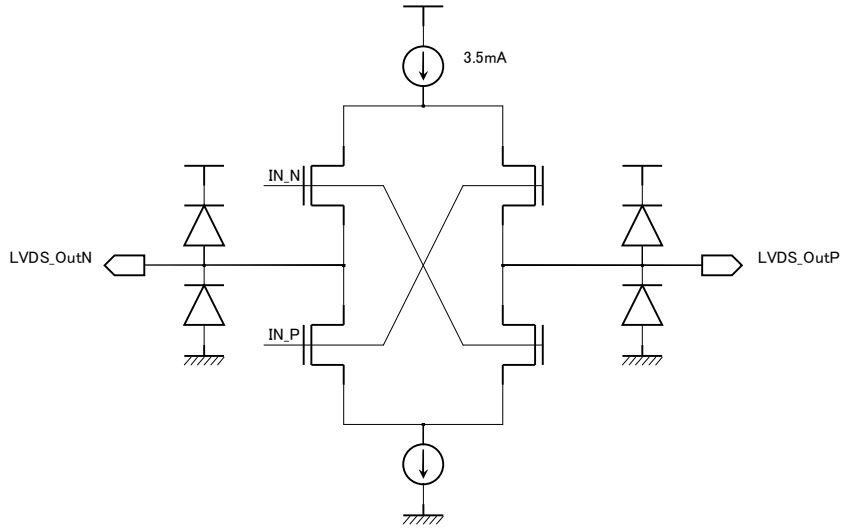


Figure 3. LVDS Output Schematic Diagram

Power Consumption

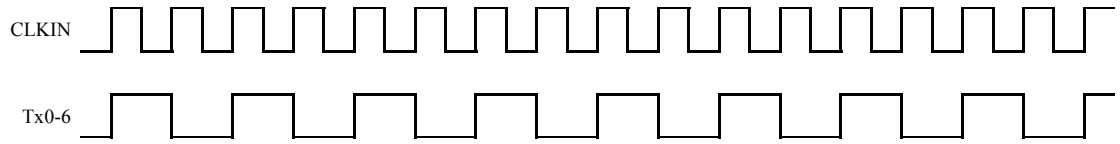
Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions	Typ*	Max	Unit
I_{TCCW}	LVDS Transmitter Operating Current Worst Case Pattern (Fig.5)	RL=100Ω, CL=5pF, f=85MHz, RS=VCC	69	75	mA
		RL=100Ω, CL=5pF, f=135MHz, RS=VCC	87	93	mA
		RL=100Ω, CL=5pF, f=160MHz, RS=VCC	97	104	mA
	LVDS Transmitter Operating Current Worst Case Pattern (Fig.5)	RL=100Ω, CL=5pF, f=85MHz, RS=GND	55	61	mA
		RL=100Ω, CL=5pF, f=160MHz, RS=GND	73	79	mA
		RL=100Ω, CL=5pF, f=160MHz, RS=GND	83	89	mA
I_{TCCS}	LVDS Transmitter Power Down Current	/PDWN=L, All Inputs=L or H	-	10	µA

*Typ values are at the conditions of VCC=3.3V and Ta = +25ºC

Table 4. Power Consumption

Worst Case Pattern



x=A,B,C,D

Figure 4. Worst Case Pattern

Electrical Characteristics

LVCMOS/TTL DC Specifications

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
V_{IH}	High Level Input Voltage	RS=VCC or GND	2.0	-	VCC	V
V_{IL}	Low Level Input Voltage	RS=VCC or GND	GND	-	0.8	V
V_{DDQ} [1]	Small Swing Voltage		1.2	-	2.8	V
V_{REF}	Input Reference Voltage	Small Swing (RS=V_{DDQ}/2)	-	V_{DDQ}/2	-	
V_{SH} [2]	Small Swing High Level Input Voltage	$V_{REF=}$ V_{DDQ}/2	V_{DDQ}/2 +100mV	-	-	V
V_{SL} [2]	Small Swing Low Level Input Voltage	$V_{REF=}$ V_{DDQ}/2	-	-	V_{DDQ}/2 -100mV	V
I_{INC}	Input Current	GND ≤ V_{IN} ≤ VCC	-	-	±10	µA

*Typ values are at the conditions of VCC=3.3V and Ta = +25ºC

Notes : [1] V_{DDQ} voltage defines the max voltage of small swing inputs at RS=VREF. It is not an actual input voltage.

[2] Small swing signals are applied to TA0-6, TB0-6, TC0-6, TD0-6 and CLKIN.

Table 5. LV-CMOS/TTL DC Specifications

LVDS Transmitter DC Specifications

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ*	Max	Unit
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS=VCC	250	350	450	mV
			Reduced swing RS=GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω		-	-	35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states			-	-	35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=GND, RL=100Ω		-	-	-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=GND, V_{OUT}=GND to VCC		-	-	±10	µA

*Typ values are at the conditions of VCC=3.3V and Ta = +25ºC

Table 6. LVDS Transmitter DC Specifications

LVCMOS/TTL & LVDS Transmitter AC Specifications

Over recommended operating supply and temperature range unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
t_{TCIT}	CLK IN Transition Time	-	-	5.0	ns
t_{TCP}	CLK IN Period	6.25	T	125	ns
t_{TCH}	CLK IN High Time	0.35T	0.5T	0.65T	ns
t_{TCL}	CLK IN Low Time	0.35T	0.5T	0.65T	ns
t_{TCD}	CLK IN to TCLK+/- Delay	-	3T	-	ns
t_{TS}	LVCMOS/TTL Data Setup to CLK IN	2.0	-	-	ns
t_{TH}	LVCMOS/TTL Data Hold from CLK IN	0.0	-	-	ns
t_{LVT}	LVDS Transition Time	-	0.6	1.5	ns
t_{TOP1}	Output Data Position0 (T=6.25ns ~ 20ns)	-0.15	0.0	+0.15	ns
t_{Top0}	Output Data Position1 (T=6.25ns ~ 20ns)	T/7-0.15	T/7	T/7+0.15	ns
t_{Top6}	Output Data Position2 (T=6.25ns ~ 20ns)	2T/7-0.15	2T/7	2T/7+0.15	ns
t_{Top5}	Output Data Position3 (T=6.25ns ~ 20ns)	3T/7-0.15	3T/7	3T/7+0.15	ns
t_{Top4}	Output Data Position4 (T=6.25ns ~ 20ns)	4T/7-0.15	4T/7	4T/7+0.15	ns
t_{Top3}	Output Data Position5 (T=6.25ns ~ 20ns)	5T/7-0.15	5T/7	5T/7+0.15	ns
t_{Top2}	Output Data Position6 (T=6.25ns ~ 20ns)	6T/7-0.15	6T/7	6T/7+0.15	ns
t_{TPLL}	Phase Lock Loop Set	-	-	10.0	ms

*Typ values are at the conditions of VCC=3.3V and Ta = +25ºC

Table 7. LVCMOS/TTL & LVDS Transmitter AC Specifications

LVCMOS/TTL Input

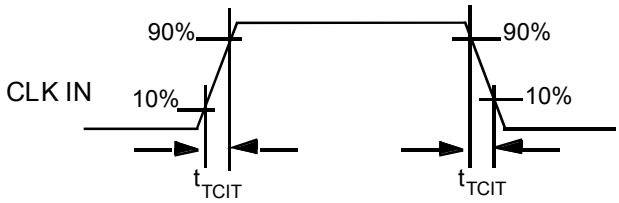
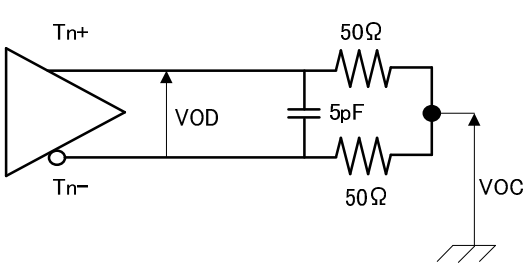


Figure 5. CLKIN Transmission Time

LVDS Output



LVDS Output Load

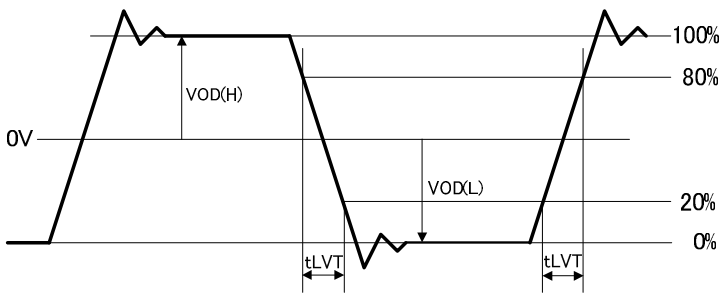
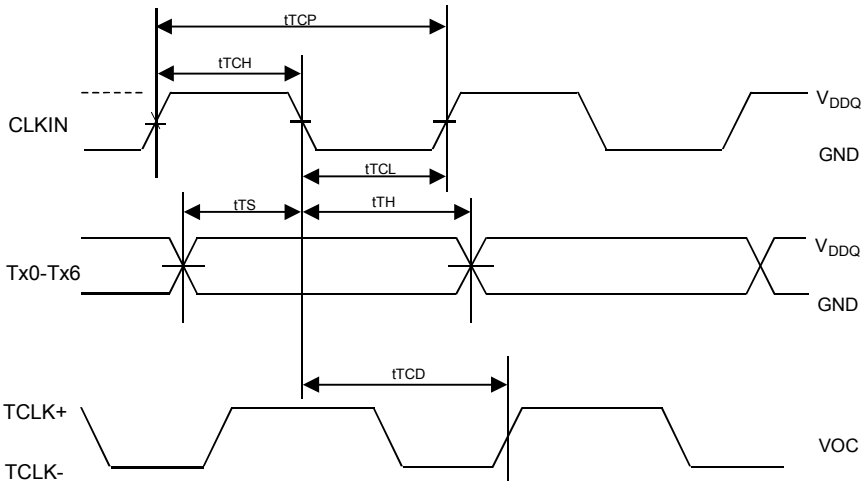


Figure 6. LVDS Output Load and Transmission Time

AC Timing Diagrams

LVCMOS/TTL Inputs

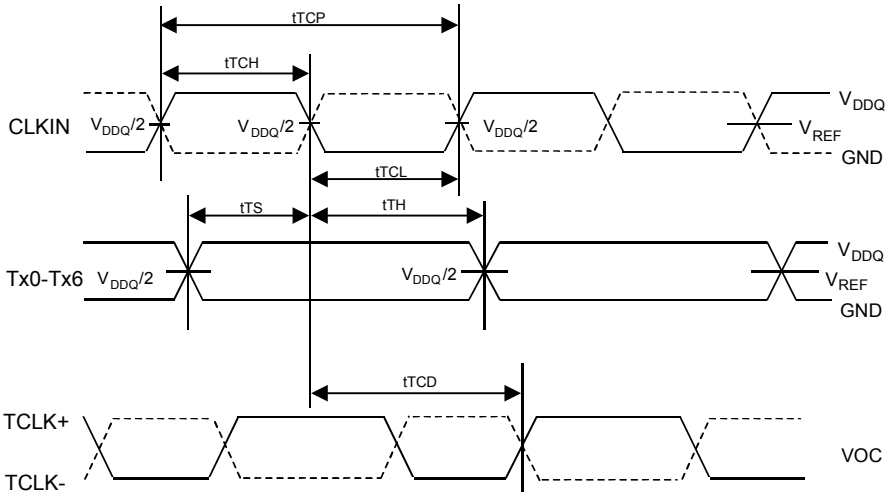


RS	VOD
VCC	350mV
0.6 ~ 1.4V	
GND	200mV

Note :
CLKIN : Solis line denotes the setting of R/F=GND
Dashed line denotes the setting of R/F = VCC

Figure 7. LVCOMS/TTL Inputs and LVDS Clock Output Timing 1

Small Swing Inputs



RS	VREF
VCC	---
0.6 ~ 1.4V	$V_{DDQ}/2$
GND	---

Note :
CLKIN : Solid line denotes the setting of R/F=GND
Dashed line denotes the setting of R/F = VCC

Figure 8. LVCMOS/TTL Inputs and LVDS Output Timing 2

LVDS Output Data Position

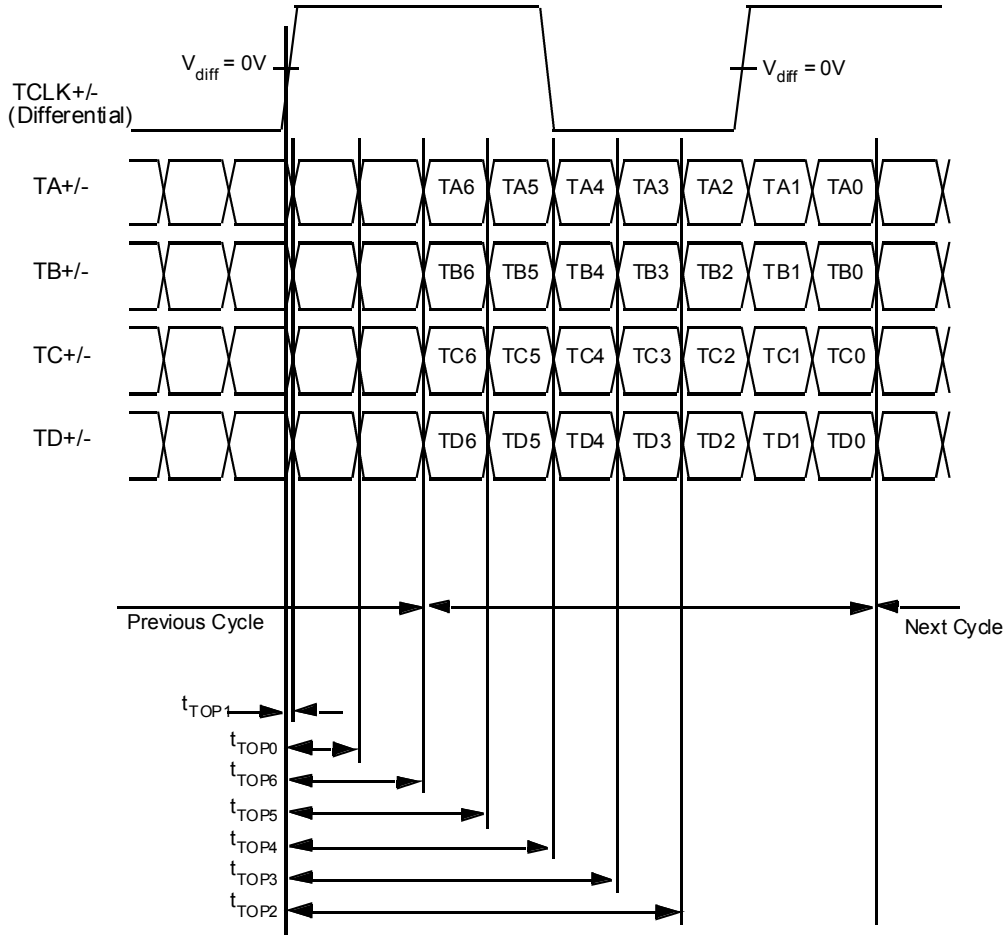


Figure 9. LVDS Output Data Position

Phase Lock Loop Set Time

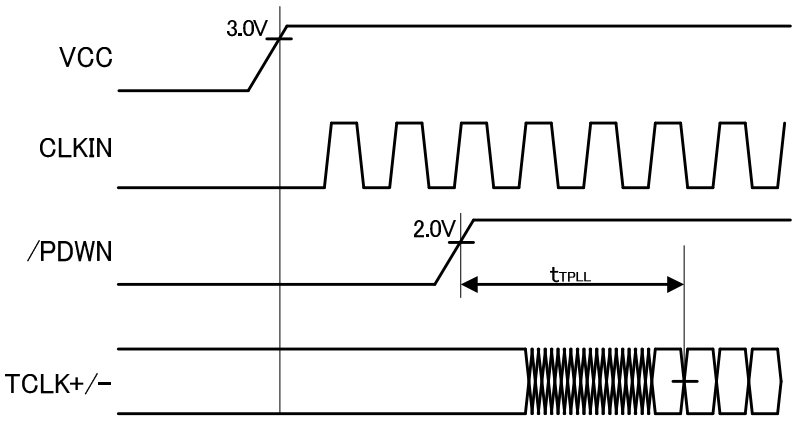


Figure 10. PLL Lock Loop Set Time

Spread Spectrum Clocking Tolerant

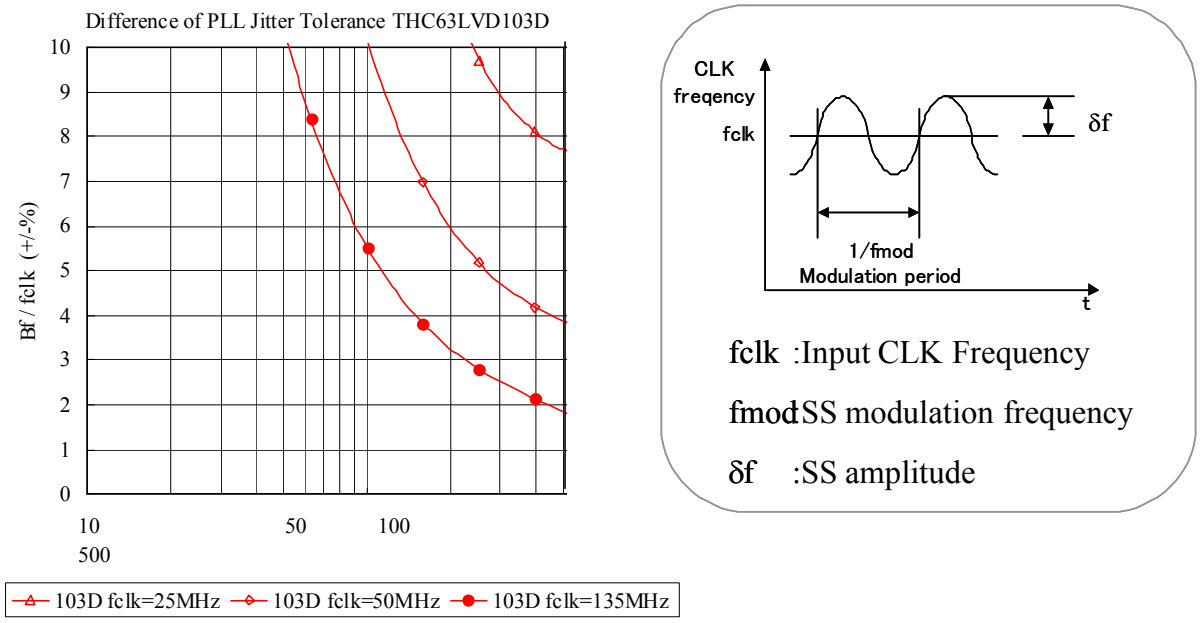


Figure 11. Spread Spectrum Clocking Tolerant

The graph indicates the range that the IC works normally under SS clock input operation.
The results are measured with a typical sample on condition of +25Cº and 3.3V, therefore these values are for reference and do not guarantee the performance of a product under other circumstance.

LVDS Data Timing Diagram

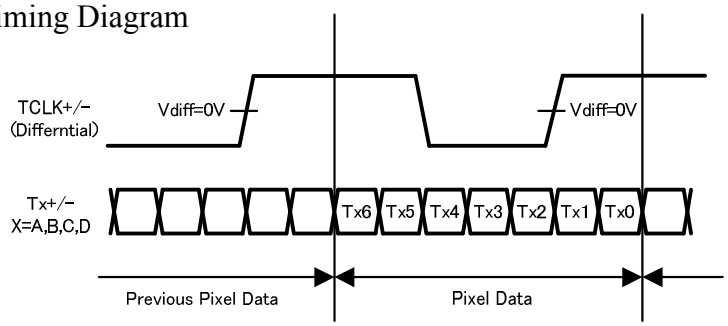


Figure 12. LVDS Data Timing Diagram

THC63LVD103D Pixel Data Mapping for JEIDA Format (6bit, 8bit and 10bit Application)

	6bit	8bit	10bit
TA0	R4	R4	R4
TA1	R5	R5	R5
TA2	R6	R6	R6
TA3	R7	R7	R7
TA4	R8	R8	R8
TA5	R9	R9	R9
TA6	G4	G4	G4
TB0	G5	G5	G5
TB1	G6	G6	G6
TB2	G7	G7	G7
TB3	G8	G8	G8
TB4	G9	G9	G9
TB5	B4	B4	B4
TB6	B5	B5	B5
TC0	B6	B6	B6
TC1	B7	B7	B7
TC2	B8	B8	B8
TC3	B9	B9	B9
TC4	Hsync	Hsync	Hsync
TC5	Vsync	Vsync	Vsync
TC6	DE	DE	DE
TD0	-	R2	R2
TD1	-	R3	R3
TD2	-	G2	G2
TD3	-	G3	G3
TD4	-	B2	B2
TD5	-	B3	B3
TD6	-	N/A	N/A
TE0	-	-	R0
TE1	-	-	R1
TE2	-	-	G0
TE3	-	-	G1
TE4	-	-	B0
TE5	-	-	B1
TE6	-	-	N/A

Note : Use TA to TC channels and open TD channel for 6bit application.
Use TA to TD channels and open TE channel for 8bit application.

Table 8. Data Mapping for JEIDA Format

THC63LVD103D Pixel Data Mapping for VESA Format (6bit, 8bit and 10bit Application)

	6bit	8bit	10bit
TA0	R0	R0	R0
TA1	R1	R1	R1
TA2	R2	R2	R2
TA3	R3	R3	R3
TA4	R4	R4	R4
TA5	R5	R5	R5
TA6	G0	G0	G0
TB0	G1	G1	G1
TB1	G2	G2	G2
TB2	G3	G3	G3
TB3	G4	G4	G4
TB4	G5	G5	G5
TB5	B0	B0	B0
TB6	B1	B1	B1
TC0	B2	B2	B2
TC1	B3	B3	B3
TC2	B4	B4	B4
TC3	B5	B5	B5
TC4	Hsync	Hsync	Hsync
TC5	Vsync	Vsync	Vsync
TC6	DE	DE	DE
TD0	-	R6	R6
TD1	-	R7	R7
TD2	-	G6	G6
TD3	-	G7	G7
TD4	-	B6	B6
TD5	-	B7	B7
TD6	-	N/A	N/A
TE0	-	-	R8
TE1	-	-	R9
TE2	-	-	G8
TE3	-	-	G9
TE4	-	-	B8
TE5	-	-	B9
TE6	-	-	N/A

Note : Use TA to TC channels and open TD channel for 6bit application.
Use TA to TD channels and open TE channel for 8bit application.

Table 9. Data Mapping for VESA Format

Normal Connection with JEIDA Format

Example

THC63LVD103D : Falling Edge / Normal Swing

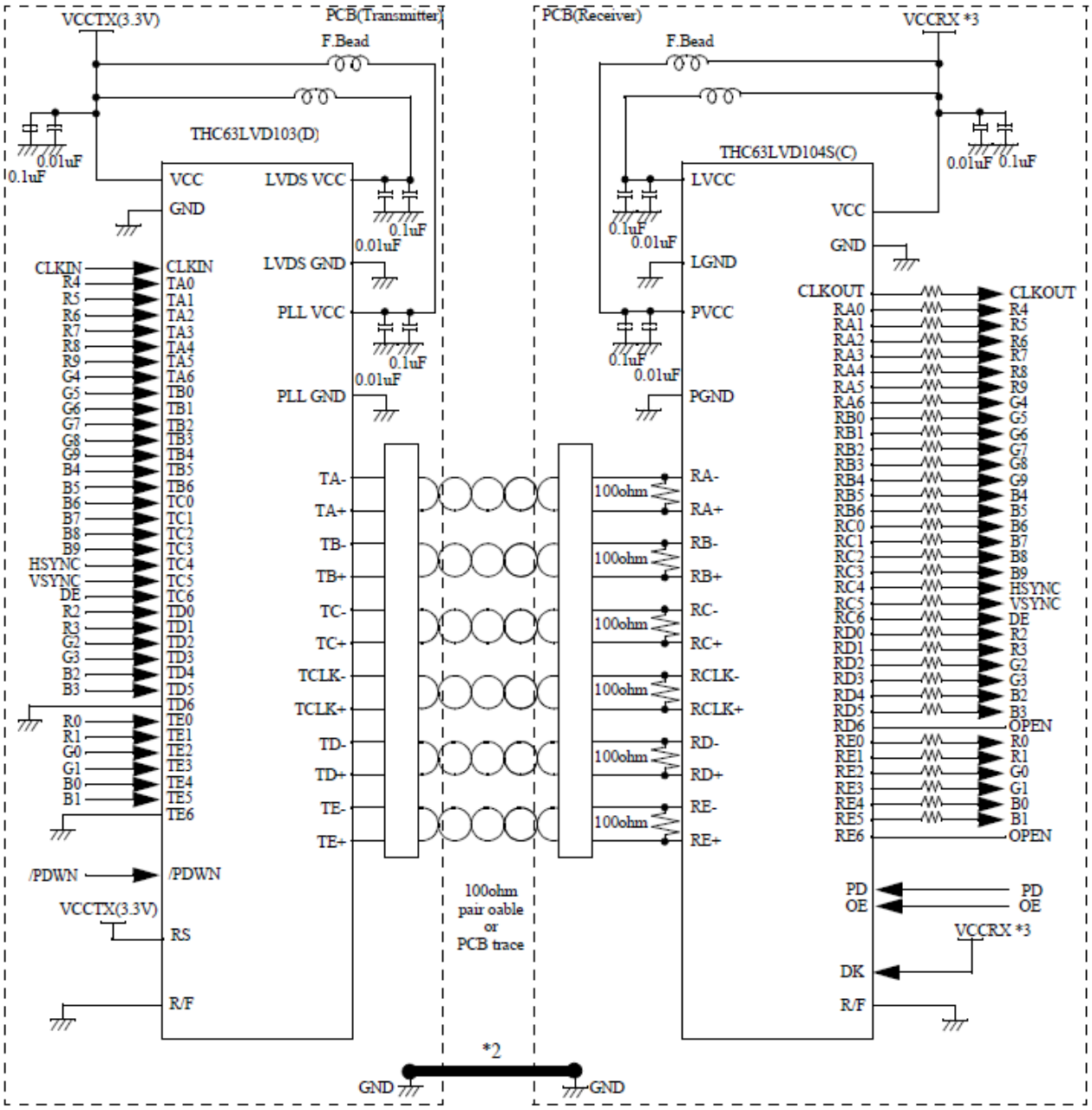


Figure 13. Typical Connection Diagram

Notes

1) Cable Connection and Disconnection
Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection
Connect each GND of the PCB which THC63LVDM83D and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3) Multi Drop Connection
Multi drop connection is not recommended.

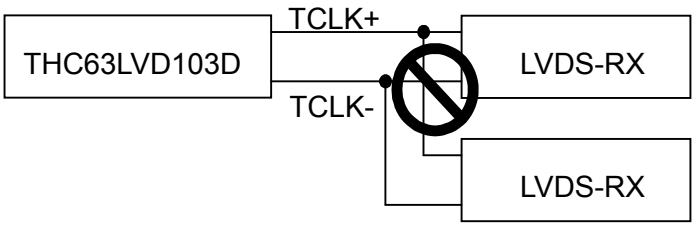


Figure 14. Multi Drop Connection

4) Asynchronous use
Asynchronous using such as following systems is not recommended.

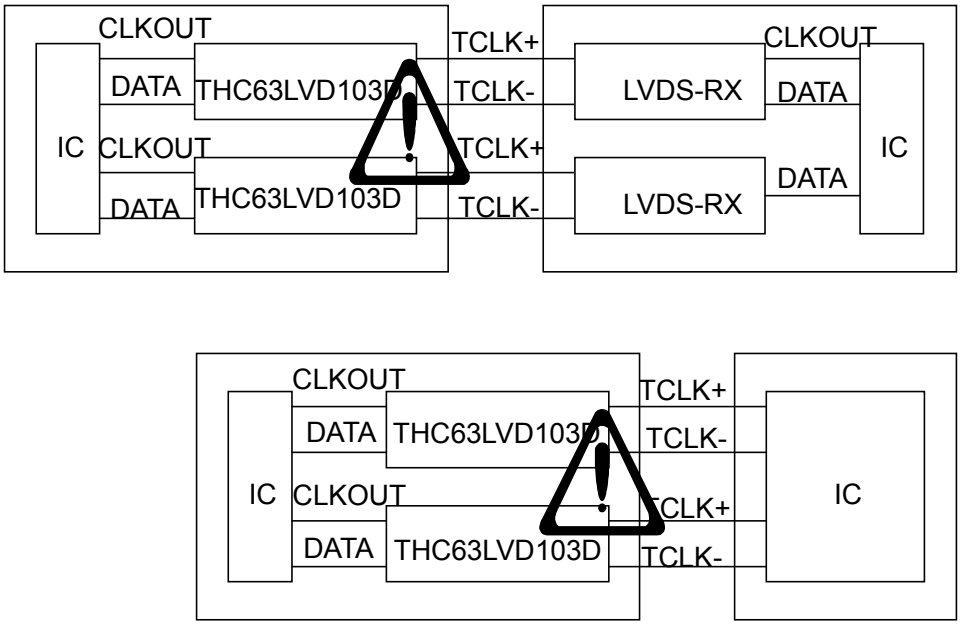


Figure 15. Asynchronous Use

Package

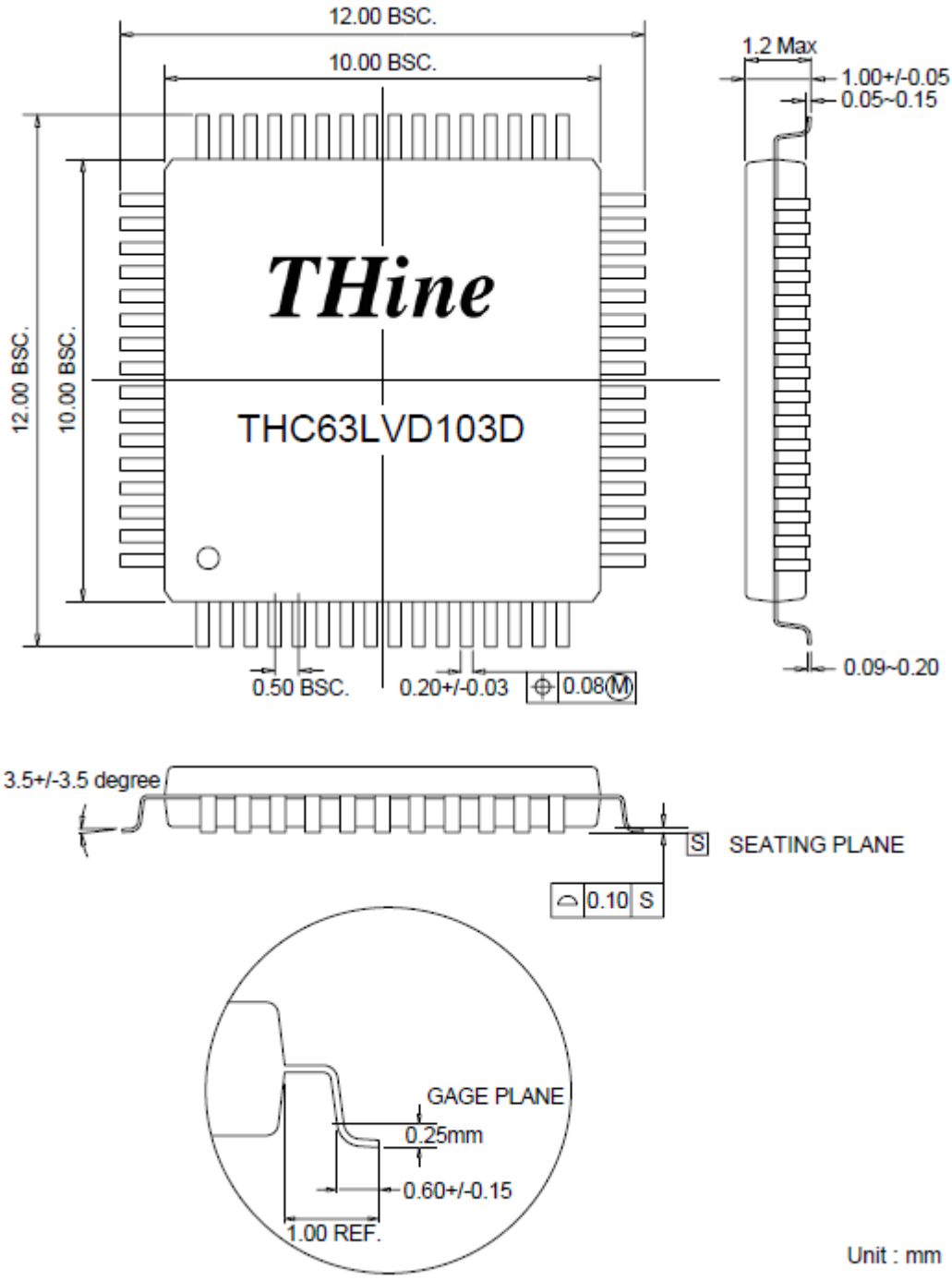


Figure 16. Package Diagram

Reference Land Pattern

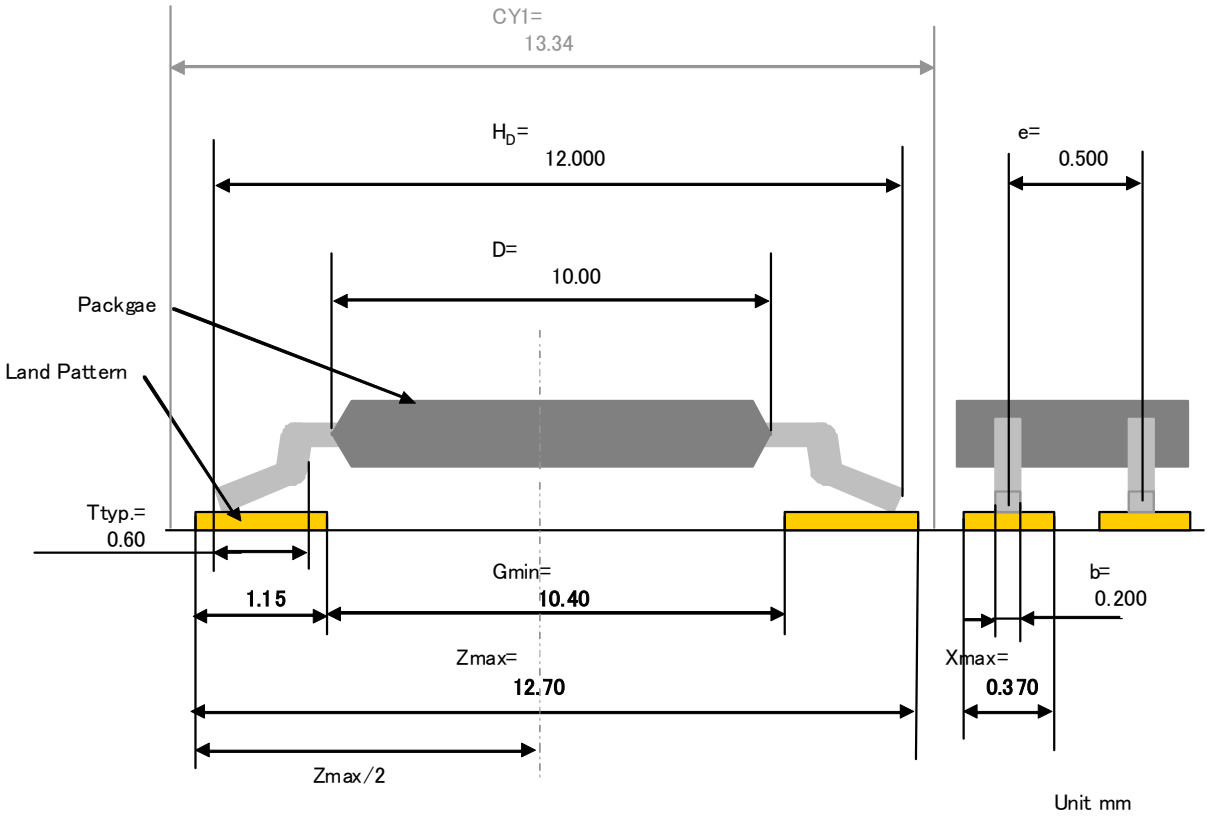


Figure 17. Reference of Land Pattern

The recommendation mounting method of THine device is reflow soldering.
The reference pattern is using the calculation result on condition of reflow soldering.

Notes
This land pattern design is a calculated value based on JEITA ET-7501.
Please take into consideration in an actual substrate design about enough the ease of mounting, the intensity of connection, the density of mounting, and the solder paste used, etc… The optimal land pattern size changes with these parameters. Please use the value shown by the land pattern as reference data.

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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