CWQ1100® Datasheet

Qi Compliant 15W Wireless Power Receiver IC

General Description

CWQ1100 can deliver up to 15W as a highly-integrated single-chip wireless medium power receiver IC. As wireless power transfer systems are getting more popular, they require more fast charging and high efficiency solution. The CWQ1100 wireless power receiver IC is compliant with WPC 1.2.4 standard and supports the 5W baseband power profile (BPP) and 15W extended power profile (EPP). The CWQ1100 power receiver integrates a synchronous rectifier, a low drop-out regulator, and communication controllers which use Amplitude Shift Keying (ASK) and Frequency Shift Keying (FSK). The chip also supports the Foreign Object Detection (FOD) extension in WPC 1.2.4. For achieving chip stability, protection tools are implemented, such as over-current-protection, over-voltage-protection, thermal shutdown, and under voltage lock-out (UVLO). Configurable analog blocks can be used independently and co-operated with the control and communication unit.

Features Overview

- **Single-chip dual mode 15W receiver for WPC 1.2.4 compliance**
  - WPC 1.2.4 TPT#MP1 (15W)
- **Support 5W baseline power profile (BPP) and 15W extended power profile (EPP)**
- **FOD extension supports**
- **Integrated Synchronous Rectifier Receiver.**
  - Support Output Power up to 15W.
  - High Rectifier Efficiency up to 95%.
  - High System Efficiency up to 90%.
  - Topology Auto Selection operation.
- **Programmable Dynamic Rectifier Voltage Control.**
- **Integrated Programmable Linear Regulator.**
  - Output voltage range of 4.5~12V with 0.5V control step.
  - Output current limit up to 2A.
- Bi-directional channel communication
  - FSK demodulation for PTx to PRx
  - ASK modulation for PRx to PTx
- **24-bit Power Calculation support**
- **Received Power Calculation for FOD function**
  - 12-bit ADC for voltage/current measurement.
  - Adaptive Coil Power loss/offset compensation.
- **Programmable Temperature Control.**
- **Charger Complete and Enable control inputs**
- **End of Power Transfer (EPT) Packet management.**
- **Over Current Limit**
- **Over Voltage Protection**
- **Thermal Shutdown**
- **WLCSP 50B 2.64mm x 3.94mm, 0.4mm pitch**
- **QFN 40-pin 6mm x 6mm, 0.5mm pitch**
- **384-bit One-Time-Programmable Device**

Applications

- WPC Compliant Receivers.
- Cell phones and smart phones.
- Digital Cameras.
- Power Banks.
- Wireless Power Embedded Batteries
- Bluetooth Headsets
- Portable Media Players
- Other Hand-held Device

1. Description for Implementation

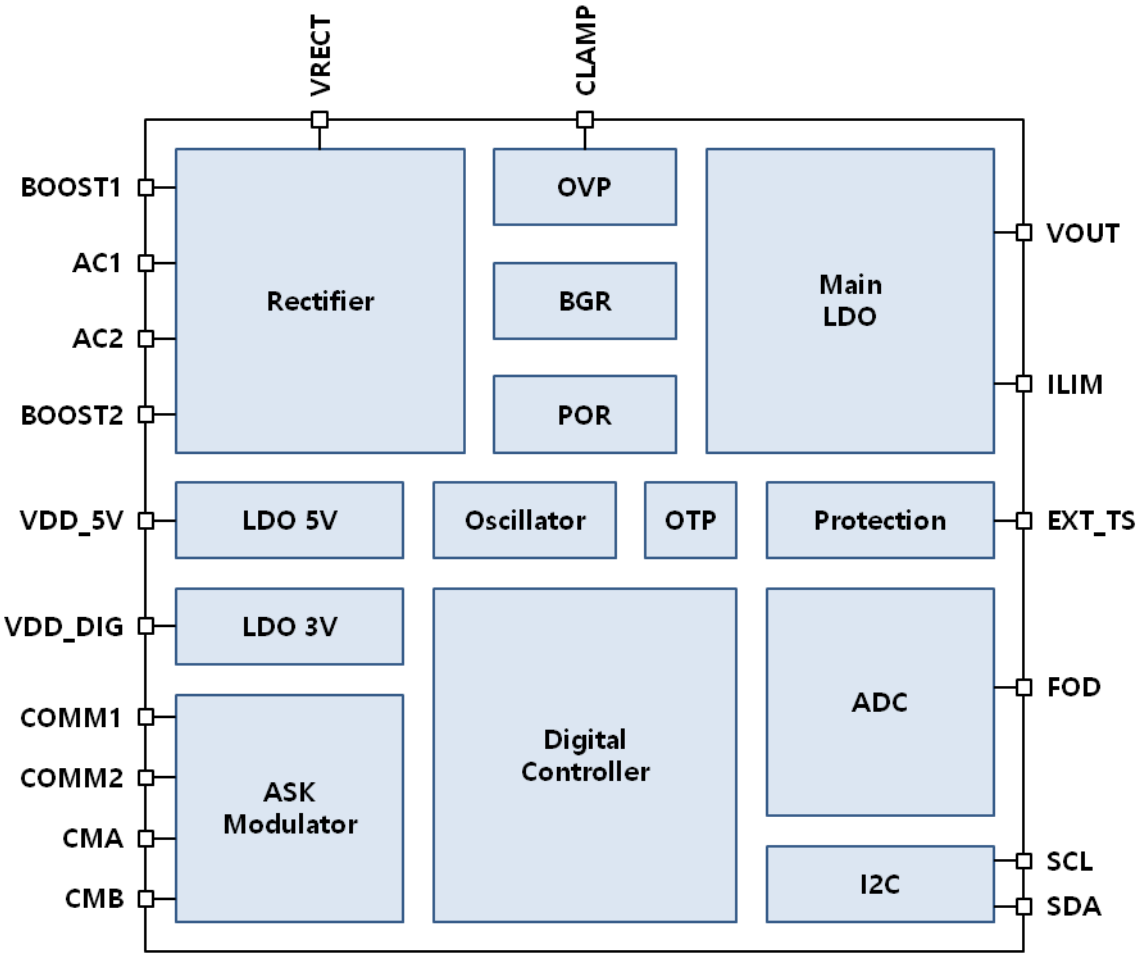


Figure 1. CWQ1100 Block Diagram

1.1 Overview

A wireless power charging system is composed of transmitter and receiver. In general, wireless power transmitter will transfer AC power using a power amplifier through a TX inductor coil. Then wireless power receiver will receive AC power through an RX inductor coil which is strongly coupled with the TX coil. In receiver part, rectifier will change the AC power to DC power and LDO will transfer the DC power to battery charger.

Figure1 shows the block diagram of CWQ1100 wireless charging receiver IC. CWQ1100 receiver will support power transfer up to 15W and it is compliant with WPC1.2.4 standards. It consists of rectifier, main LDO, internal LDOs, ADC, digital controller and etc.

1.2 Rectifier

CWQ1100 employs a synchronous active rectifier in order to improve AC to DC power conversion efficiency. The rectifier power conversion efficiency is very important because it has a large influence on overall receiver efficiency. The rectifier in CWQ1100 will support full-wave, half-wave and passive mode according to the transferred power level. When the power transfer is started initially, the rectifier will operate in passive mode and supply the system power to overall receive IC.

1.3 Main LDO

Main LDO regulator will transfer DC power from rectifier output to battery charger. LDO in CWQ1100 is designed to transfer power up to 15W and its output voltage level can be changed by user. The LDO power transistor is designed to minimize its on-resistance because the LDO drop-out voltage is directly related to overall system efficiency. Especially, in case of large power transfer, the LDO drop-out voltage (VRECT-VOUT) should be controlled as small as possible.

1.4 ASK Modulator

CWQ1100 power receiver communicates with the power transmitter by ASK modulator. The ASK modulator make up the WPC standard 2kHz bi-phase signal by switching the capacitors between COMM1/2 and AC1/AC2. Switching the capacitance at AC1/AC2 nodes will change the impedance of transmitter coil. As a result, amplitude modulation is built up.

1.5 ADC

CWQ1100 power receiver employs 12-bit SAR ADC because it has low power, small area characteristics and moderate speed performance. ADC monitors important internal voltages and currents and gives the system information to the digital controller.

1.6 Protection

CWQ1100 power receiver employs various protection schemes in order to prevent system damage. When the VRECT voltage is too high, the OVP (Over Voltage Protection) function will turn on the clamp path or send the EPT (End Power Transfer) packet to the transmitter. When the main LDO current is too large, the OCL (Over Current Limit) function will limit the output current. When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will send the EPT packet to transmitter or shutdown the receiver system.

1.7 Digital Controller

Digital controller in CWQ1100 controls all the analog blocks and entire system to perform power transfer operation according to the wireless power transfer standard, that is, WPC 1.2.4. It also supports I2C interface to communicate with external host.

2. Pin-out and description

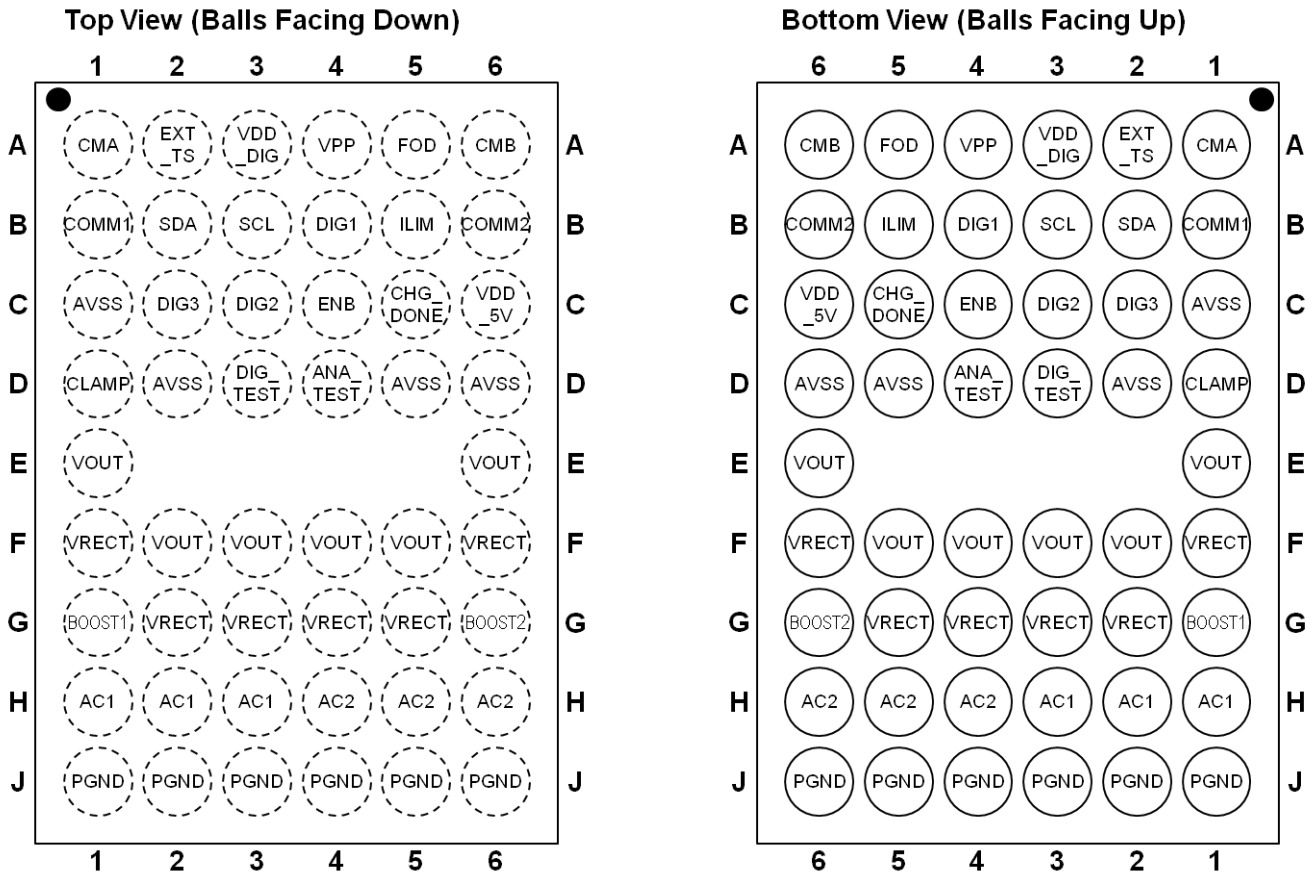


Figure 2. CWQ1100 Pin Configuration (WLCSP 50B 2.64mm x 3.94mm, 0.4mm pitch)

2.1 Pin Description (WLCSP 50B 2.64mm x 3.94mm, 0.4mm pitch)

Pin Number	Name	Type	Description
A1	CMA	O	NC
A6	CMB	O	
A2	EXT_TS	I	External temperature sensor input. Connect this pin to external NTC thermistor. If not used, connect this pin to VDD_DIG.
A3	VDD_DIG	P	Internal 3V LDO output for digital block and etc. 1uF capacitor connect to GND. Not for external use
A4	VPP	I	8V high voltage power for OTP programming. During the normal operation, connect this pin to VDD_DIG.
A5	FOD	I	FOD offset setting pin. Connect a resistor between this pin and GND.
B1	COMM1	O	High voltage open drain output for ASK modulation. Connect 47nF capacitor from AC1/AC2 to COMM1/COMM2 separately
B6	COMM2	O	
B2	SDA	I/O	I^2C data input/output for internal register access.

B3	SCL	I	I^2C clock input for internal register access.
B4	DIG1	I	Enable scan test mode. Connect to GND directly in normal application.
B5	ILIM	I	Output current or over-current limit level programming pin.
C1,D2,D5,D6	AVSS	P	Analog ground pin.
C2	DIG3	I	Scan clock for scan test mode. Connect to GND directly in normal application.
C3	DIG2	I	Scan enable for scan test mode. Connect to GND directly in normal application.
C4	ENB	I	Active-low enable pin for the entire chip.
C5	CHG_DONE	I	Active-high input from the external battery charger to terminate power transfer.
C6	VDD_5V	P	Internal 5V LDO output pin for 1uF capacitor connection. Not for external use
D1	CLAMP	O	High voltage open drain output for analog linear over-voltage protection.
D3	DIG_TEST	O	Digital test output pin. Floating for normal application
D4	ANA_TEST	O	Analog test output pin. Floating for normal application
E1,E6,F2,F3 F4,F5	VOUT	P	Main LDO output pin for delivering power to the battery charger. 3.3uF capacitor connect to GND.
F1,F6,G2,G3 G4,G5	VRECT	P	Internal synchronous rectifier output for 20uF capacitor connection.
G1	BOOST1	O	Bootstrap capacitor connection pin for driving the high-side FETs of synchronous rectifier. Connect 100nF capacitor to AC1/AC2 separately
G6	BOOST2	O	
H1,H2,H3	AC1	I	AC power input of synchronous rectifier.
H4,H5,H6	AC2	I	
J1,J2,J3,J4 J5,J6	PGND	P	Power ground for synchronous rectifier.

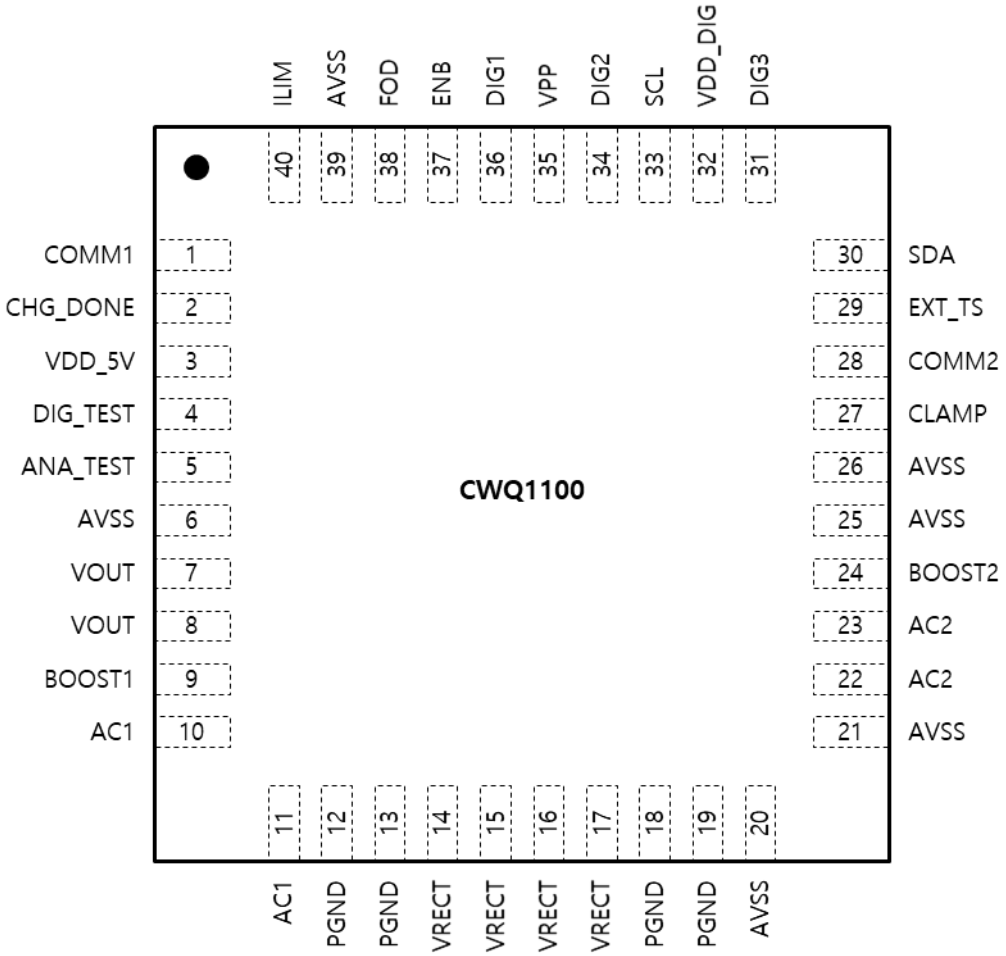


Figure 3. CWQ1100 Pin Configuration (QFN 40-pin 6mm x 6mm, 0.5mm pitch)

2.2 Pin Description (QFN 40-pin 6mm x 6mm, 0.5mm pitch)

Pin Number	Name	Type	Description
1	COMM1	O	High voltage open drain output for ASK modulation. Connect 47nF capacitor from AC1/AC2 to COMM1/COMM2 separately
28	COMM2	O	
2	CHG_DONE	I	Active-high input from the external battery charger to terminate power transfer.
3	VDD_5V	P	Internal 5V LDO output pin for 1uF capacitor connection, not for external use
4	DIG_TEST	O	Digital test output pin. Floating for normal application
5	ANA_TEST	O	Analog test output pin. Floating for normal application
6,20,21,25 26,39	AVSS	P	Analog ground pin.
7,8	VOUT	P	Main LDO output pin for delivering power to the battery charger, 3.3uF capacitor connect to GND.

9	BOOST1	O	Bootstrap capacitor connection pin for driving the high-side FETs of synchronous rectifier. Connect 100nF capacitor to AC1/AC2 separately
24	BOOST2	O	
10,11	AC1	I	AC power input of synchronous rectifier.
22,23	AC2	I	
12,13,18,19	PGND	P	Power ground for synchronous rectifier.
14,15,16,17	VRECT	P	Internal synchronous rectifier output for 20uF capacitor connection.
27	CLAMP	O	High voltage open drain output for analog linear over-voltage protection.
29	EXT_TS	I	External temperature sensor input. Connect this pin to external NTC thermistor. If not used, connect this pin to VDD_DIG.
30	SDA	I/O	I^2C data input/output for internal register access.
31	DIG3	I	Scan clock for scan test mode. Connect to GND directly in normal application.
32	VDD_DIG	P	Internal 3V LDO output for digital block and etc.1uF capacitor connect to GND. Not for external use
33	SCL	I	I^2C clock input for internal register access.
34	DIG2	I	Scan enable for scan test mode. Connect to GND directly in normal application.
35	VPP	I	8V high voltage power for OTP programming. During the normal operation, connect this pin to VDD_DIG.
36	DIG1	I	Enable scan test mode. Connect to GND directly in normal application.
37	ENB	I	Active-low enable pin for the entire chip.
38	FOD	I	FOD offset setting pin. Connect a resistor between this pin and GND.
40	ILIM	I	Output current or over-current limit level programming pin.

3. Application Guide

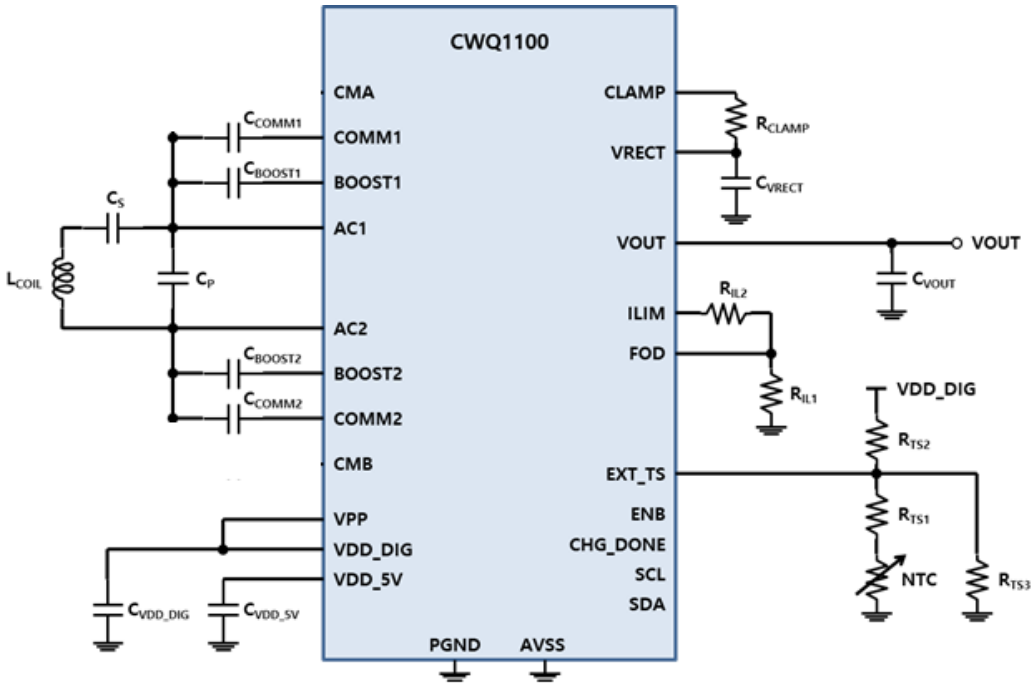


Figure 4. CWQ1100 Typical Application Diagram

3.1 Receiver Coil and Resonant Capacitors

The receiver coil design is related to the overall system application. The coil inductance, shape and material can be chosen according to the applications. The recommended receiver coil inductance for dual mode operation is between 5uH to 10uH. Series and parallel resonant capacitors C_S and C_d are set according to WPC specification. The capacitance of the resonant capacitors can be calculated by the following equations.

$$C_S = \frac{1}{L'_S \times (2\pi f_S)^2}$$

$$C_d = \frac{1}{L_S \times (2\pi f_D)^2 - \frac{1}{C_S}}$$

In these equations, f_S and f_D are the dual resonant frequencies which cover the power transfer frequency range. Follow WPC Qi 1.2.4 specifications, f_S is set to 100 kHz and f_D is set to 1000kHz, respectively. L'_S is coil self-inductance when placed on the transmitter, and L_S is the self-inductance when placed away from the transmitter.

3.2 Boost and Communication Capacitors

As shown in Figure 4, two external bootstrap capacitors C_{BOOST1} and C_{BOOST2} are needed to drive the high-side FETs of synchronous rectifier. Bootstrap capacitors should have voltage rating of more than 25V and their recommended capacitances are 100nF.

In order to communicate with transmitter, external capacitors should be connected between high voltage open drain output and AC1/AC2 input. CWQ1100 will be switching COMM1/COMM2 output in WPC mode. Typical recommended capacitance values are C_{COMM1}=C_{COMM2}=47nF.

3.3 Output Regulating Capacitors

As shown in Figure 4, rectifier output VRECT and internal LDOs' output VOUT, VDD_5V, VDD_DIG should be connected to external capacitor for voltage regulation. Typical recommended capacitance values are C_{VRECT}=20uF, C_{VOUT}=3.3uF, C_{VDD_5V}=1uF, C_{VDD_DIG}=1uF, respectively.

3.4 Clamp Resistor

When the VRECT voltage is too high, the OVP (Over Voltage Protection) function will turn on the clamp path or send the EPT (End Power Transfer) packet to the transmitter. The clamp path uses high voltage open drain output for analog linear OVP. The recommended resistance value of R_{CLAMP} is between 10Ω to 50Ω according to the transfer power level of application.

3.5 Current Limit and FOD Setting Resistors

When the main LDO current is too large, the OCL (Over Current Limit) function will limit the output current. The current limit level can be adjusted by external resistors and it is calculated as follows,

$$I_{LIM} = \frac{45000}{R_{ILIM}} = \frac{45000}{R_{IL1} + R_{IL2}}$$

In this equation, the R_{ILIM} is the total resistance from the ILIM pin to ground, that is, R_{IL1} + R_{IL2} as shown in Figure 4. It is recommended to use the resistors of good tolerance less than 1%, because the current estimation in wireless power receiver is very important.

CWQ1100 adds an FOD offset proportional to output power level when it sends the received power packet to transmitter. The amount of the added FOD offset can be adjusted by the ratio of R_{IL1} to (R_{IL1} + R_{IL2}).

3.6 External Temperature Sensor

When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will send the EPT packet to transmitter or shutdown the receiver system. In order to sense the temperature outside chip, connect EXT_TS pin to external NTC (Negative temperature Coefficient) thermistor as shown in Figure 4. The NTC thermistor should be placed close to the heat emission device.

The EXT_TS voltage V_{EXT_TS} can be calculated as follows,

$$V_{EXT\_TS} = VDD\_DIG \times \frac{\frac{(R_{NTC} + R_{TS1}) \times R_{TS3}}{(R_{NTC} + R_{TS1}) + R_{TS3}}}{\frac{(R_{NTC} + R_{TS1}) \times R_{TS3}}{(R_{NTC} + R_{TS1}) + R_{TS3}} + R_{TS2}}$$

In this equation, VDD_DIG is 3V from the internal LDO.

CWQ1100 compares V_{EXT_TS} with internal reference voltages V_{TS_HOT} and V_{TS_COLD}. If V_{EXT_TS}<V_{TS_HOT}, it means external temperature is too high and CWQ1100 sends the EPT packet (value=0x03) to transmitter. On the other hand, if V_{EXT_TS}>V_{TS_COLD}, it means external temperature is too low and CWQ1100 also sends the EPT packet (value=0x03) to transmitter. Remind that V_{EXT_TS} is negative slope curve vs temperature.

The internal reference voltages V_{TS_HOT} and V_{TS_COLD} are fixed values as follows,

Internal TS Reference	Threshold Voltage [V]	Hysteresis [mV]
V_{TS_HOT}	0.315	20
V_{TS_COLD}	0.980	80

Recommended NTC resistance range is from hundreds of Ω to hundreds of kΩ vs temperature. After choosing the appropriate NTC thermistor, you can design R_{TS1}, R_{TS2} and R_{TS3} according to your thermal protection specification. Table 1 shows an EXT_TS thermal protection design example.

Temp [℃]	VDD_DIG [V]	R_{NTC} [kΩ]	R_{TS1} [kΩ]	R_{TS2} [kΩ]	R_{TS3} [kΩ]	V_{EXT_TS} [V]	Status
-40	3.0	188.5	3.9	47	68	1.550	$V_{EXT\_TS} > V_{TS\_COLD}$ Send EPT packet
-30	3.0	111.3	3.9	47	68	1.429	
-20	3.0	67.8	3.9	47	68	1.278	
-10	3.0	42.5	3.9	47	68	1.109	
0	3.0	27.3	3.9	47	68	0.938	$V_{TS\_HOT} < V_{EXT\_TS} < V_{TS\_COLD}$ Normal charging operation
10	3.0	18.0	3.9	47	68	0.782	
20	3.0	12.1	3.9	47	68	0.648	
30	3.0	8.31	3.9	47	68	0.541	
40	3.0	5.83	3.9	47	68	0.460	
50	3.0	4.16	3.9	47	68	0.399	
60	3.0	3.02	3.9	47	68	0.354	
70	3.0	2.23	3.9	47	68	0.321	
80	3.0	1.67	3.9	47	68	0.296	$V_{EXT\_TS} < V_{TS\_HOT}$ Send EPT packet
90	3.0	1.27	3.9	47	68	0.278	
100	3.0	0.98	3.9	47	68	0.265	
110	3.0	0.76	3.9	47	68	0.255	
120	3.0	0.60	3.9	47	68	0.247	

Table 1. EXT_TS Thermal Protection Design Example

In this example, the hot temperature threshold T_{TS_HOT} and the cold temperature threshold T_{TS_COLD} are designed to be 80℃ and -10℃ respectively. You can change the hot and cold temperature threshold according to your application by changing the related resistors.

3.7 CHG_DOWN

When CHG_DOWN is from low to high, CWQ1100 send “charging complete” EPT (0x01) to TX to inform TX that battery is charging complete.

3.8 ENB

When applying logic high to ENB, CWQ1100 is suspended and IC leakage current will be smaller than 10uA. When ENB is logic low level, CWQ1100 is enabled for wireless charging.

3.9 PCB Layout Guide

- Keep the trace resistance as low as possible on large current nets as shown in Table 2.
- Resonant capacitors C_S and C_d need to be as close to the device as possible.
- Clamp, boost and communication capacitors (C_{CLAMP}, C_{BOOST1}, C_{BOOST2}, C_{COMM1}, C_{COMM2}, C_{CMA} and C_{CMB}) need to be as close to the device as possible.

- Output regulating capacitors C_{VRECT} and C_{VOUT} need to be as close to the device as possible.
- LDO capacitors C

Net (Ball)	Type	Maximum Current [A]
AC1, AC2	AC	2
VRECT	AC	2
VOUT	DC	2
PGND	AC	2
COMM1, COMM2, CMA, CMB	AC	1
CLAMP	AC	2

Table 2. Large Current Nets

3.10 Register Map

7bit Address: 0x24H.

Register index (hex)	Bit Number								W/R
	B7	B6	B5	B4	B3	B2	B1	B0	
27h	SET_VOUT_EXTENDED[3:0]				SET_VOUT_BASE_LINE[3:0]				W/R
2Eh	COLD_UTP[1:0]		TSD[1:0]		OVP[1:0]		HOT_OTP[1:0]		W/R
2Fh	PEN_PROT	OCL_ON_MASK	RELEASE_TIME[1:0]		TSD_OUT_MASK	OVP_OUT_MASK	OTP_HOT_MASK	OTP_COLD_MASK	W/R
41h	REF_Q_FACTOR								W/R
42h	PTC_GUARANTEED_PWR								R
5Ch	ADC_CODE								W/R
5Dh	Reserved				ADC_OUT[11:8]				R
5Eh	ADC_OUT[7:0]								R
62h	8bit RP								R
63h	24bit RP[15:8]								R
64h	24bit RP[7:0]								R
68h	POWER_CLASS		GUARANTEED_POWER_VALUE						R
69h	Reserved		POTENTIAL_POWER_VALUE						R

DETAILED REGISTER INFORMATION

REG	Bit	Field	Type	Default	Description
27H	7	VOUT_EPP[3]	R/W	1	Setup bits of VOUT voltage for extended profile ,Offset: 4.5 V, Range 4.5 V – 12 V; Unit=0.5V Default: 9 V (1001)
	6	VOUT_EPP[2]	R/W	0	
	5	VOUT_EPP[1]	R/W	0	
	4	VOUT_EPP[0]	R/W	1	
	3	VOUT_BPP[3]	R/W	0	Setup bits of VOUT voltage for base line profile Offset: 4.5 V, Range 4.5 V – 12 V; Unit=0.5V Default: 5 V (0001). Normal case, VOUT=5V in BPP mode
	2	VOUT_BPP[2]	R/W	0	
	1	VOUT_BPP[1]	R/W	0	
	0	VOUT_BPP[0]	R/W	1	

REG	Bit	Field	Type	Default	Description	
2EH	7	COLD_UTP[1]	R/W	1	00	1.163V / 1.073V (Detection / Release)
					01	1.069V / 0.984V (Detection / Release)
	6	COLD_UTP[0]	R/W	0	10	0.980V / 0.898V (Detection / Release)
					11	0.894V / 0.820V (Detection / Release)
	5	TSD[1]	R/W	1	00	130 ℃ / 110 ℃ (Die OTP Detection / Release)
					01	140 ℃ / 120 ℃ (Die OTP Detection / Release)
	4	TSD[0]	R/W	0	10	150 ℃ / 130 ℃ (Die OTP Detection / Release)
					11	160 ℃ / 140 ℃ (Die OTP Detection / Release)
	3	OVP[1]	R/W	1	00	14.0 V / 12.5 V (Detection / Release)
					01	14.5 V / 13.0 V (Detection / Release)
	2	OVP[0]	R/W	0	10	15.0 V / 13.5 V (Detection / Release)
					11	15.5 V / 14.0 V (Detection / Release)
	1	HOT_OTP[1]	R/W	1	00	0.339V / 0.367V (Detection / Release)
					01	0.326V / 0.351V (Detection / Release)
	0	HOT_OTP[0]	R/W	0	10	0.314V / 0.335V (Detection / Release)
					11	0.306V / 0.322V (Detection / Release)

REG	Bit	Field	Type	Default	Description
2FH	7	PEN_PROT	R/W	1	0:disable protection function, 1:enable protection function
	6	OCL_ON_MASK	R/W	1	0: No mask; 1: mask
	5	RELEASE_TIME[1]	R/W	0	Initially all signals are masked and release masks after a time delay. 00:No release; 01: Release after 5s; 10: Release after 10s; 11:Release after 20s;
	4	RELEASE_TIME[0]	R/W	0	
	3	TSD_OUT_MASK	R/W	1	0: No mask; 1: mask
	2	OVP_OUT_MASK	R/W	1	0: No mask; 1: mask
	1	OTP_HOT_MASK	R/W	1	0: No mask; 1: mask
	0	OTP_COLD_MASK	R/W	1	0: No mask; 1: mask

REG	Bit	Field	Type	Default	Description
41H	7	REF_Q_FACTOR[7]	R/W	0	Quality factor reference value
	6	REF_Q_FACTOR[6]	R/W	0	
	5	REF_Q_FACTOR[5]	R/W	0	
	4	REF_Q_FACTOR[4]	R/W	1	
	3	REF_Q_FACTOR[3]	R/W	0	
	2	REF_Q_FACTOR[2]	R/W	1	
	1	REF_Q_FACTOR[1]	R/W	0	
	0	REF_Q_FACTOR[0]	R/W	0	
REG	**Bit**	**Field**	**Type**	**Default**	**Description**
42H	7	Reserved	-	-	Reserved
	6	Reserved	-	-	
	5	PTC_GUARANTEED_POWER[5]	R	0	Guaranteed Power Value in Power Transfer Contract. Unit=0.5W
	4	PTC_GUARANTEED_POWER[4]	R	0	
	3	PTC_GUARANTEED_POWER[3]	R	1	
	2	PTC_GUARANTEED_POWER[2]	R	0	
	1	PTC_GUARANTEED_POWER[1]	R	1	
	0	PTC_GUARANTEED_POWER[0]	R	0	
REG	**Bit**	**Field**	**Type**	**Default**	**Description**
5CH	7	Reserved	-	-	Reserved
	6	Reserved	-	-	
	5	Reserved	-	-	
	4	Reserved	-	-	
	3	ADC_CODE[3]	R/W	0	The related ADC_OUT value is loaded to Reg: 0x5D and Reg 0x5E. 4'b0000:VRECT; 4'0001:VOUT 4'b0010:IOUT; 4'b0011:ILIM 4'b0100:FOD; 4'b0101：EXT_TS 4'b0110:VCTAT
	2	ADC_CODE[2]	R/W	0	
	1	ADC_CODE[1]	R/W	0	
	0	ADC_CODE[0]	R/W	0	
REG	**Bit**	**Field**	**Type**	**Default**	**Description**
5DH	**7**	Reserved	-	-	Reserved
	6	Reserved	-	-	
	5	Reserved	-	-	
	4	Reserved	-	-	
	3	ADC_OUT[11]	R	0	ADC value with Reg 5EH according to ADC_CODE register select ADC channel ADC MSB 4bits
	2	ADC_OUT[10]	R	0	
	1	ADC_OUT[9]	R	0	
	0	ADC_OUT[8]	R	0	

REG	Bit	Field	Type	Default	Description
5EH	**7**	ADC_OUT[7]	R	0	ADC value with Reg5DH according to ADC_COUD register select ADC channel ADC LSB 8bits
	6	ADC_OUT[6]	R	0	
	5	ADC_OUT[5]	R	0	
	4	ADC_OUT[4]	R	0	
	3	ADC_OUT[3]	R	0	
	2	ADC_OUT[2]	R	0	
	1	ADC_OUT[1]	R	0	
	0	ADC_OUT[0]	R	0	
REG	**Bit**	**Field**	**Type**	**Default**	**Description**
62H	**7**	8bit RP[7]	R	0	8bits Receiver Power Package Value-BPP only
	6	8bit RP[6]	R	0	
	5	8bit RP[5]	R	0	
	4	8bit RP[4]	R	0	
	3	8bit RP[3]	R	0	
	2	8bit RP[2]	R	0	
	1	8bit RP[1]	R	0	
	0	8bit RP[0]	R	0	
REG	**Bit**	**Field**	**Type**	**Default**	**Description**
63H	7	24bit RP[15]	R	0	24bits Receiver Power Package Value High 8bits-EPP only
	6	24bit RP[14]	R	0	
	5	24bit RP[13]	R	0	
	4	24bit RP[12]	R	0	
	3	24bit RP[11]	R	0	
	2	24bit RP[10]	R	0	
	1	24bit RP[9]	R	0	
	0	24bit RP[8]	R	0	
REG	**Bit**	**Field**	**Type**	**Default**	**Description**
64H	7	24bit RP[7]	R	0	24bits Receiver Power Package Value Low 8bits-EPP only
	6	24bit RP[6]	R	0	
	5	24bit RP[5]	R	0	
	4	24bit RP[4]	R	0	
	3	24bit RP[3]	R	0	
	2	24bit RP[2]	R	0	
	1	24bit RP[1]	R	0	
	0	24bit RP[0]	R	0	

REG	Bit	Field	Type	Default	Description
68H	7	TX POWER CLASS[1]	R	0	TX Power Class Value by FSK
	6	TX POWER CLASS[0]	R	0	
	5	TX_GUARANTEED_POWER[5]	R	0	TX Guaranteed Power Value by FSK
	4	TX_GUARANTEED_POWER[4]	R	0	
	3	TX_GUARANTEED_POWER[3]	R	0	
	2	TX_GUARANTEED_POWER[2]	R	0	
	1	TX_GUARANTEED_POWER[1]	R	0	
	0	TX_GUARANTEED_POWER[0]	R	0	
REG	**Bit**	**Field**	**Type**	**Default**	**Description**
69H	7	Reserved	-	-	Reserved
	6	Reserved	-	-	
	5	TX_POTENTIAL_POWER[5]	R	0	TX Potential Power Value by FSK
	4	TX_POTENTIAL_POWER[4]	R	0	
	3	TX_POTENTIAL_POWER[3]	R	0	
	2	TX_POTENTIAL_POWER[2]	R	0	
	1	TX_POTENTIAL_POWER[1]	R	0	
	0	TX_POTENTIAL_POWER[0]	R	0	

4. Package Outline

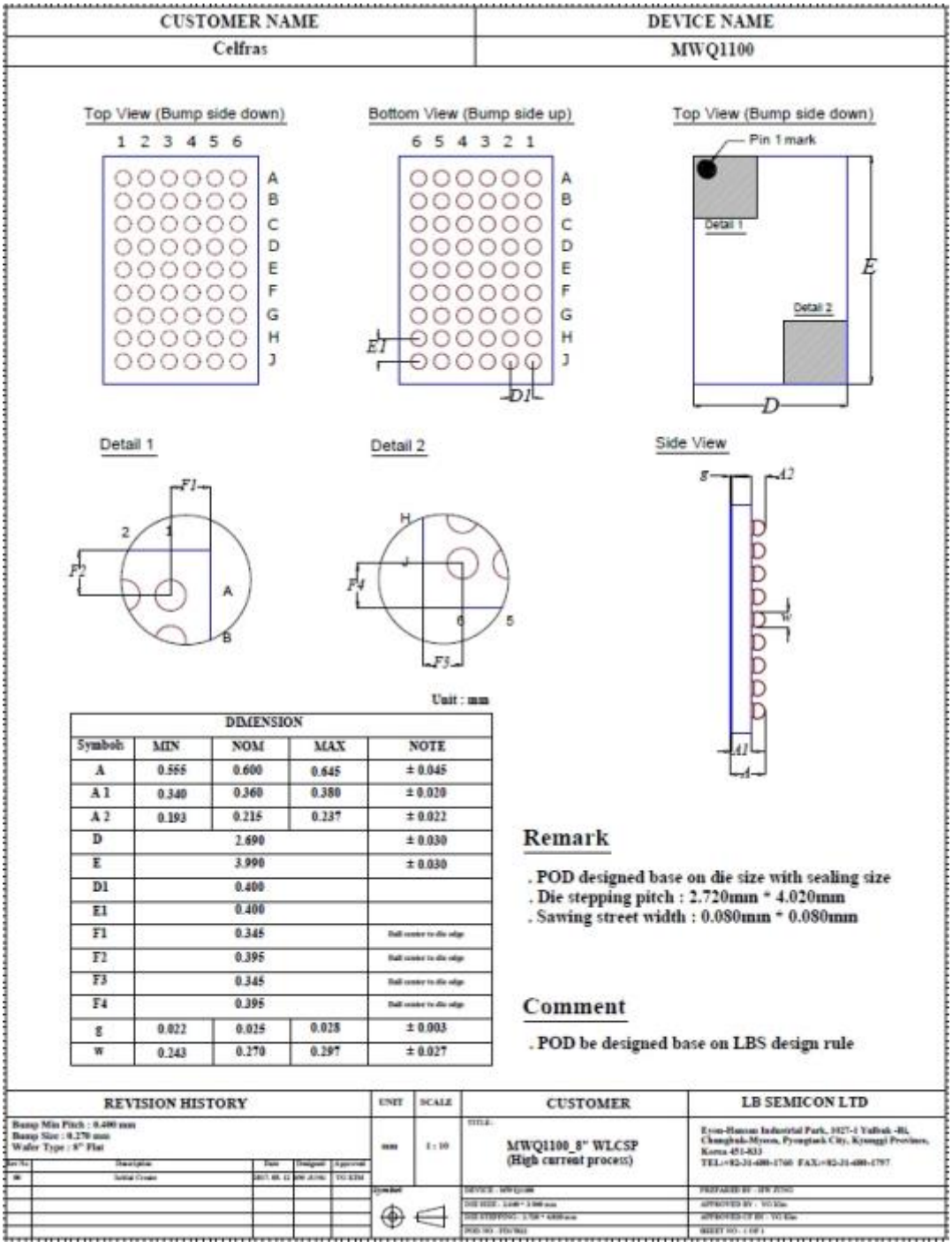
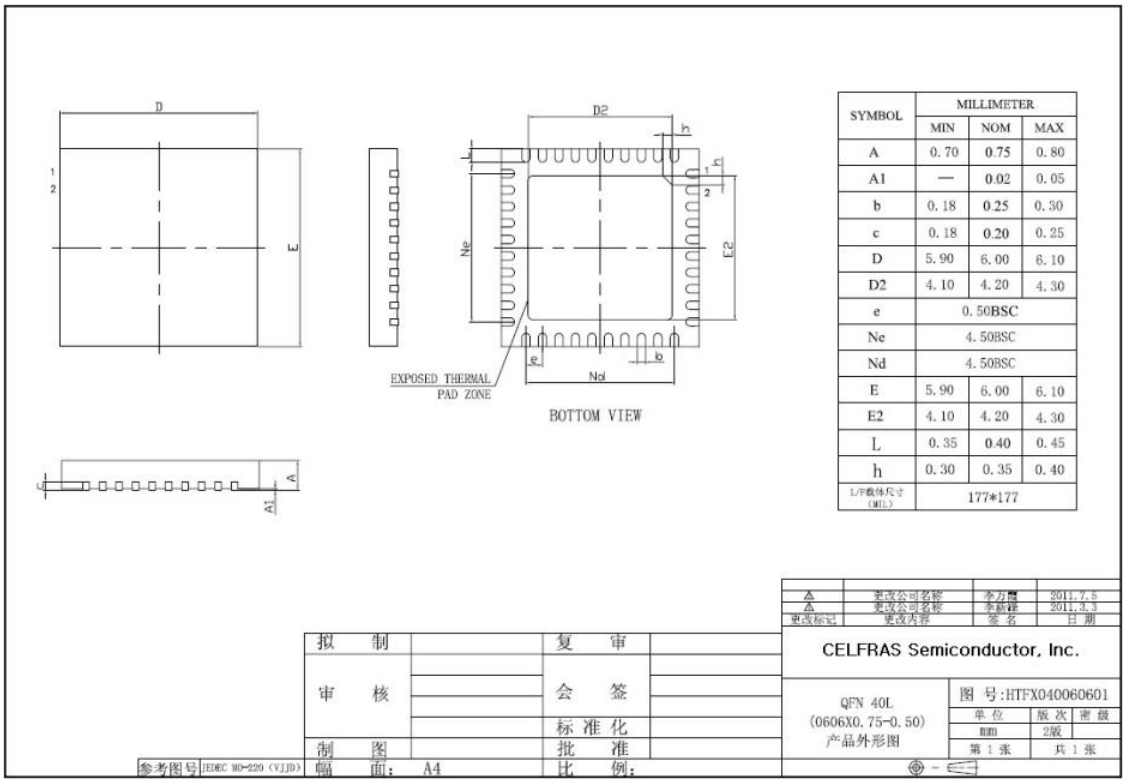


Figure 5. WLCSP 50B Package Outline, 2.64mm x 3.94mm, 0.4mm pitch



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	177*177		

更改标记	更改内容	签名	日期
△	更改公司名称	李万鹰	2011.7.5
△	更改公司名称	李新建	2011.3.3

拟制		复审	
审核		会签	
		标准化	
制图		批准	
参考图号 JEDEC MO-220 (VJJD)	幅面: A4	比例:	

CELFRAS Semiconductor, Inc.

QFN 40L
(0606X0.75-0.50)
产品外形图

图号:HTFX040060601

单位	版次	密级
MM	2版	
第 1 张	共 1 张	

Figure 6. QFN 40-pin Package Outline, 6.0mm x 6.0mm, 0.5mm pitch

5. Electrical Characteristics

5.1 Absolute Maximum Rating

PIN	Parameter	Rating	Unit
AC1, AC2, COMM1, COMM2, CMA, CMB VRECT, CLAMP	Voltage	-0.3 to 20	V
BOOST1, BOOST2	Voltage	-0.3 to 26	V
VOUT	Voltage	-0.3 to 15	V
VPP	Voltage	-0.3 to 8	V
VDD_5V, VDD_DIG, ENB, CHG_DONE ILIM, FOD, EXT_TS, SCL, SDA	Voltage	-0.3 to 6	V
PGND	Voltage	-0.3 to 0.3	V
AC1, AC2, VRECT, VOUT, CLAMP, PGND	Current	2	A
COMM1, COMM2, CMA, CMB	RMS Current	1	A

5.2 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit
V_{RECT}	Rectifier voltage range	4		15	V
I_{OUT}	Main LDO output current			2	A
I_{COMM}	COMM1, COMM2 sink current			500	mA
I_{CM}	CMA, CMB sink current			500	mA
T_J	Junction temperature	-30		125	℃
T_A	Ambient temperature	-30		85	℃

5.3 Thermal Information

Parameters	CWQ1100 WLCSP 50B 2.64mm x 3.94mm	UNITS
Junction-to-ambient thermal resistance		℃/W
Junction-to-case thermal resistance		℃/W
Junction-to-board thermal resistance		℃/W
Junction temperature，T_J		℃
Ambient operation temperature		℃
Storage temperature，T_{stg}		℃
Lead soldering temperature，T_L(10s)		℃

Parameters	CWQ1100 QFN40 6mm x 6mm	UNITS
Junction-to-ambient thermal resistance		℃/W
Junction-to-case thermal resistance		℃/W
Junction-to-board thermal resistance		℃/W
Junction temperature，T_J		℃
Ambient operation temperature		℃
Storage temperature，T_{stg}		℃
Lead soldering temperature，T_L(10s)		℃

5.4 ESD

Test Model	RATINGS	UNITS
HBM: all pins		V
CDM: all pins		V

5.5 ELECTRICAL Characteristics

Unless otherwise specified: T_A = -20°C to 70°C. Typical values are for T_A = 25°C

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Synchronous Active Rectifier						
V_{IN_RECT}	AC1, AC2 input voltage range		4.0		20	V
f_{IN_RECT}	AC1, AC2 input frequency range		80		500	kHz
E_{ff_RECT}	AC to DC power conversion efficiency			92		%
V_{UVLO}	Under voltage lockout	V_{RECT}: 0V to 4V		3.2	3.3	V
V_{UVLO_HYS}	Under voltage lockout hysteresis	V_{RECT}: 4V to 0V		400		mV
Main LDO						
V_{IN_MLDO}	Main LDO input voltage range		4.0		15	V
V_{OUT_MLDO}	Main LDO output voltage range Register programmable	V_{RECT}>5V	4.5		12	V
$V_{OUT\_MLDO\_STEP}$	Main LDO output voltage control step			0.5		V
I_{OUT_MLDO}	Main LDO output current range				1.7	A
P_{SRR_MLDO}	Main LDO power supply rejection ratio	C_{VOUT}=3.3uF DC to 100MHz	20			dB
Internal LDO						
$V_{OUT\_VDD\_5V}$	Internal VDD_5V LDO output voltage range	V_{RECT}>5V, C_{VDD_5V}=1uF, External load<30mA	4.62	5	5.38	V
$V_{OUT\_VDD\_DIG}$	Internal VDD_DIG LDO output voltage range	V_{RECT}>3V, C_{VDD_DIG}=1uF External load<30mA	2.85	3	3.32	V
BGR						

V_{BGR}	Internal BGR output voltage Register programmable	V_{RECT}>3V		1.22		V
Oscillator						
f_{OSC}	Internal oscillator frequency Register programmable	V_{RECT}>3V		15		MHz
ADC						
N_{ADC}	ADC resolution	V_{RECT}>3V		12		bit
f_{SAMPLE}	ADC sampling rate	f_{OSC}=15MHz		217		kSa/s
N_{CH_ADC}	ADC channel			7		
ENB/CHG_DOWN						
V_{IH}	ENB/CHG_DOWN input threshold high		1.5			V
V_{IL}	ENB/CHG_DOWN input threshold low				0.5	V
Protection						
V_{OVP}	VRECT over voltage protection Register programmable	V_{RECT}: 5V to 16V	14.8	15	15.2	V
V_{OVP_HYS}	OVP hysteresis	V_{RECT}: 16V to 5V		1.5		V
I_{OCL}	I_{OUT} over current limit protection Programmable by R_{ILIM}	R_{ILIM}=24kΩ I_{OUT}: 0A to 2A		1.875		A
I_{OCL_HYS}	OCL hysteresis	I_{OUT}: 2A to 0A		50		mA
T_{OTP}	Over temperature protection Thermal shutdown temperature	Temperature: 30℃ to 160℃		150		℃
T_{OTP_HYS}	OTP hysteresis	Temperature: 160℃ to 30℃		20		℃
V_{TS_HOT}	EXT_TS hot temperature protection threshold voltage	V_{EXT_TS}: 0V to 0.5V		0.315		V
$V_{TS\_HOT\_HYS}$	V_{TS_HOT} hysteresis	V_{EXT_TS}: 0.5V to 0V		20		mV
V_{TS_COLD}	EXT_TS cold temperature protection threshold voltage	V_{EXT_TS}: 0.5V to 1.5V		0.980		V
$V_{TS\_COLD\_HYS}$	V_{TS_COLD} hysteresis	V_{EXT_TS}: 1.5V to 0.5V		80		mV

6. I²C Signal Timing

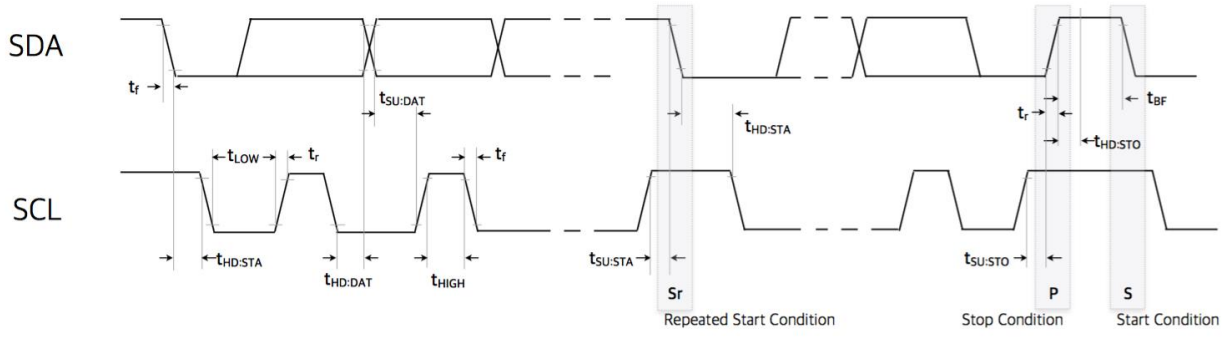


Figure 7. Timing Diagram for I²C interface

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL_SDA}	Input low threshold level SDA	V_{PULLUP}=VDD_DIG=3V			0.7	V
V_{IH_SDA}	Input high threshold level SDA	V_{PULLUP}=VDD_DIG=3V	2.3			V
V_{IL_SCL}	Input low threshold level SCL	V_{PULLUP}=VDD_DIG=3V			0.7	V
V_{IH_SCL}	Input high threshold level SCL	V_{PULLUP}=VDD_DIG=3V	2.3			V
f_{SCL}	SCL clock frequency				400	kHz
t_{LOW}	SCL clock low time		1.3			us
t_{HIGH}	SCL clock high time		0.6			us
t_r	Rise time of both SDA and SCL				0.3	us
t_f	Fall time of both SDA and SCL				0.3	us
$t_{SU,STA}$	Setup time for START condition		0.6			us
$t_{HD,STA}$	Hold time for START condition		0.6			us
$t_{SU,DAT}$	Data setup time		0.1			us
$t_{HD,DAT}$	Data hold time				0.9	us
$t_{SU,STO}$	Setup time for STOP condition		0.6			us
t_{BF}	Bus free time between STOP and START condition		1.3			us

Table 3. I^2C Characteristics

Revision History

Date	Version No.	Description
2017/07/27	1.0	Preliminary Release
2017/09/15	1.1	Initial Formal Version
2017/12/28	2.0	Added QFN package information
2018/8/28	2.1	Modify Sales Contact point
2018/5/04	2.2	Updated EC table and description, add register map

Ordering Information

Part Number	Package Type	Shipping Carrier	Package Qty	Eco Plan	MSL Peak Temp	Description	Device Marking
CWQ1100-W5	WLCSP 50, 2.64mm x 3.94 mm	Tape and Reel		Green (RoHS&noSb/Br)	Level-1-260C-UNLIM	VOUT=5V(BPP), 5V(EPP)	
CWQ1100-W9	WLCSP 50, 2.64mm x 3.94mm	Tape and Reel		Green (RoHS& no Sb/Br)	Level-1-260C-UNLIM	VOUT=5V(BPP), 9V(EPP)	
CWQ1100-WC	WLCSP 50, 2.64mm x 3.94mm	Tape and Reel		Green (RoHS& no Sb/Br)	Level-1-260C-UNLIM	VOUT=5V(BPP), 12V(EPP)	
CWQ1100-Q5	QFN 40, 6mm x 6mm	Tray		Green (RoHS&noSb/Br)		VOUT=5V(BPP), 5V(EPP)	
CWQ1100-Q9	QFN 40, 6mm x 6mm	Tray		Green (RoHS& no Sb/Br)		VOUT=5V(BPP), 9V(EPP)	
CWQ1100-QC	QFN 40, 6mm x 6mm	Tray		Green (RoHS& no Sb/Br)		VOUT=5V(BPP), 12V(EPP)	

Contact US

➢ *Headquarters*

CELFRAS Semiconductor Inc. 江西联智集成电路有限公司

59 Chuangxin No.1 Road, Nanchang Hi-tech Development Zone, Nanchang, Jiangxi, P.R.CHINA, Zip:330000

➢ *International*

CELFRAS Design Center Inc.

7F, 225-14, Pangyoyeok-ro, Bundang-gu, Seongnam-si, Gyeonggi-do, 13494, Korea

Tel. +82-70-4055-6466

Fax +82-31-707-8825

➢ *Contact*

Website

Technical Support

cts@celfras.com, ken_zhang@celfras.com

Sales Contact

marketing@celfras.com

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