CWR500® Datasheet

Qi Compliant 5W
Wireless Power Receiver IC

General Description

CWR500 can deliver up to 5W as a highly-integrated single-chip wireless medium power receiver IC. As wireless power transfer systems are getting more popular, they require more fast charging and high efficiency solution. The CWR500 wireless power receiver IC is compliant with WPC 1.2.4 standard and supports the 5W baseband power profile (BPP). The CWR500 power receiver integrates a synchronous rectifier, a low drop-out regulator, and communication controllers which use Amplitude Shift Keying (ASK). The chip also supports the Foreign Object Detection (FOD) extension in WPC 1.2.4. For achieving chip stability, protection tools are implemented, such as over-current-protection, over-voltage-protection, thermal shutdown, and under voltage lock-out (UVLO). Configurable analog blocks can be used independently and co-operated with the control and communication unit.

Features Overview

- **Single-chip dual mode 5W receiver for WPC 1.2.4 compliance**
- **Support 5W baseline power profile (BPP)**
- **FOD extension supports**
- **Integrated Synchronous Rectifier Receiver.**
  - Support Output Power up to 5W.
  - High Rectifier Efficiency up to 95%.
  - High System Efficiency up to 90%.
- **Programmable Dynamic Rectifier Voltage Control.**
- **Integrated Programmable Linear Regulator.**
  - Output voltage range of 4.5~5.5V with 0.5V control step.
  - Output current limit up to 1A.
- Bi-directional channel communication
  - ASK modulation for PRx to PTx
- **24-bit Power Calculation support**
- **Received Power Calculation for FOD function**
  - 12-bit ADC for voltage/current measurement.
  - Adaptive Coil Power loss/offset compensation.
- **Programmable Temperature Control.**
- **Charger Complete and Enable control inputs**
- **End of Power Transfer (EPT) Packet management.**
- **Over Current Limit**
- **Over Voltage Protection**
- **Thermal Shutdown**
- **QFN 40-pin 6mm x 6mm, 0.5mm pitch**
- **384-bit One-Time-Programmable Device**

Applications

- WPC Compliant Receivers.
- Cell phones and smart phones.
- Digital Cameras.
- Power Banks.
- Wireless Power Embedded Batteries
- Bluetooth Headsets
- Portable Media Players
- Other Hand-held Device

1. Description for Implementation

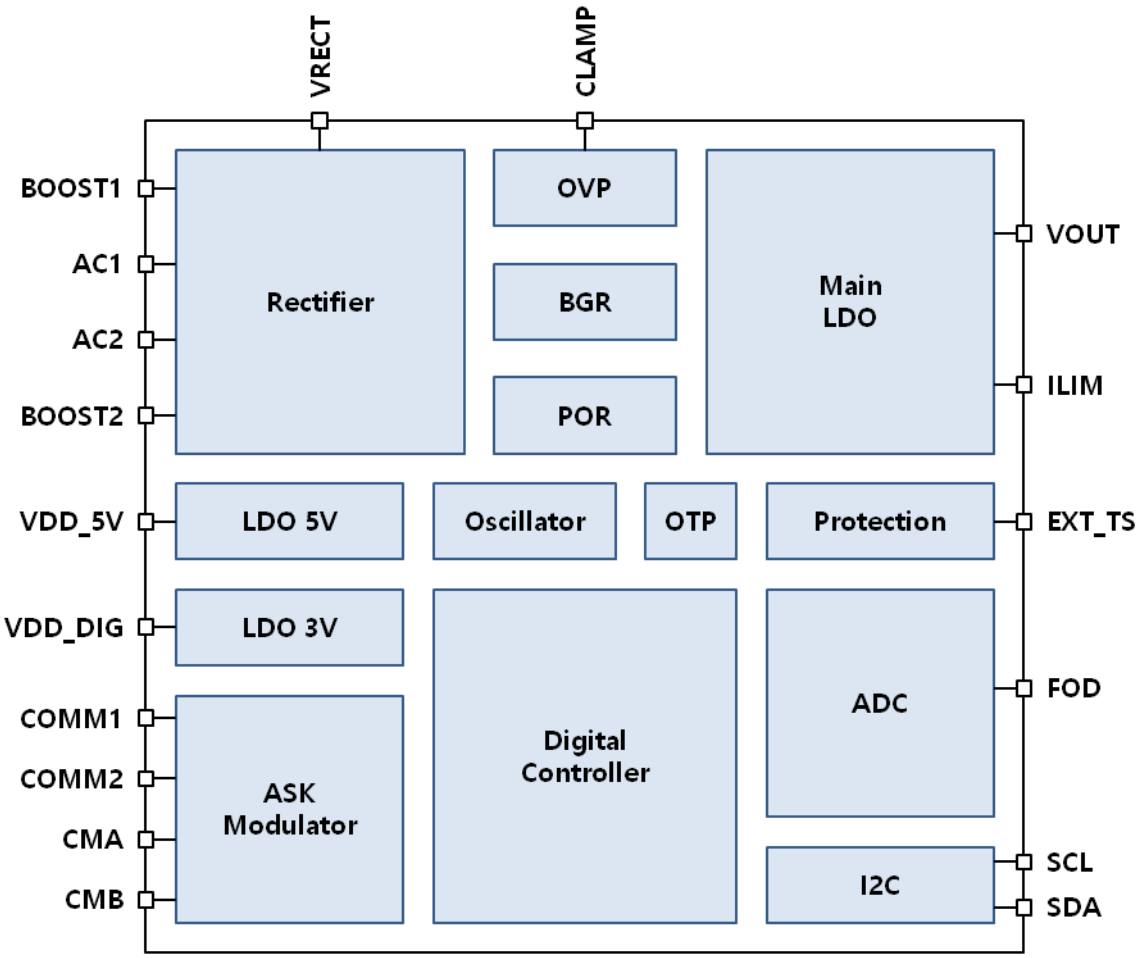


Figure 1. CWR500 Block Diagram

1.1 Overview

A wireless power charging system is composed of transmitter and receiver. In general, wireless power transmitter will transfer AC power using a power amplifier through a TX inductor coil. Then wireless power receiver will receive AC power through an RX inductor coil which is strongly coupled with the TX coil. In receiver part, rectifier will change the AC power to DC power and LDO will transfer the DC power to battery charger.

Figure1 shows the block diagram of CWR500 wireless charging receiver IC. CWR500 receiver will support power transfer up to 5W and it is compliant with WPC 1.2.4 standard. It consists of rectifier, main LDO, internal LDOs, ADC, digital controller and etc.

1.2 Rectifier

CWR500 employs a synchronous active rectifier in order to improve AC to DC power conversion efficiency. The rectifier power conversion efficiency is very important because it has a large influence on overall

receiver efficiency. The rectifier in CWR500 will support full-wave, half-wave and passive mode according to the transferred power level. When the power transfer is started initially, the rectifier will operate in passive mode and supply the system power to overall received IC.

1.3 Main LDO

Main LDO regulator will transfer DC power from rectifier output to battery charger. LDO in CWR500 is designed to transfer power up to 5W and its output voltage level can be changed by user. The LDO power transistor is designed to minimize its on-resistance because the LDO drop-out voltage is directly related to overall system efficiency. Especially, in case of large power transfer, the LDO drop-out voltage (VRECT-VOUT) should be controlled as small as possible.

1.4 ASK Modulator

CWR500 power receiver communicates with the power transmitter by ASK modulator. The ASK modulator make up the WPC standard 2kHz bi-phase signal by switching the capacitors between COMM1/2 and AC1/AC2. Switching the capacitance at AC1/AC2 nodes will change the impedance of transmitter coil. As a result, amplitude modulation is built up.

1.5 ADC

CWR500 power receiver employs 12-bit SAR ADC because it has low power, small area characteristics and moderate speed performance. ADC monitors important internal voltages and currents and gives the system information to the digital controller.

1.6 Protection

CWR500 power receiver employs various protection schemes in order to prevent system damage. When the VRECT voltage is too high, the OVP (Over Voltage Protection) function will turn on the clamp path or send the EPT (End Power Transfer) packet to the transmitter. When the main LDO current is too large, the OCL (Over Current Limit) function will limit the output current. When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will send the EPT packet to transmitter or shutdown the receiver system.

1.7 Digital Controller

Digital controller in CWR500 controls all the analog blocks and entire system to perform power transfer operation according to the wireless power transfer standard, that is, WPC 1.2.4. It also supports I2C interface to communicate with external host.

2. Pin-out and description

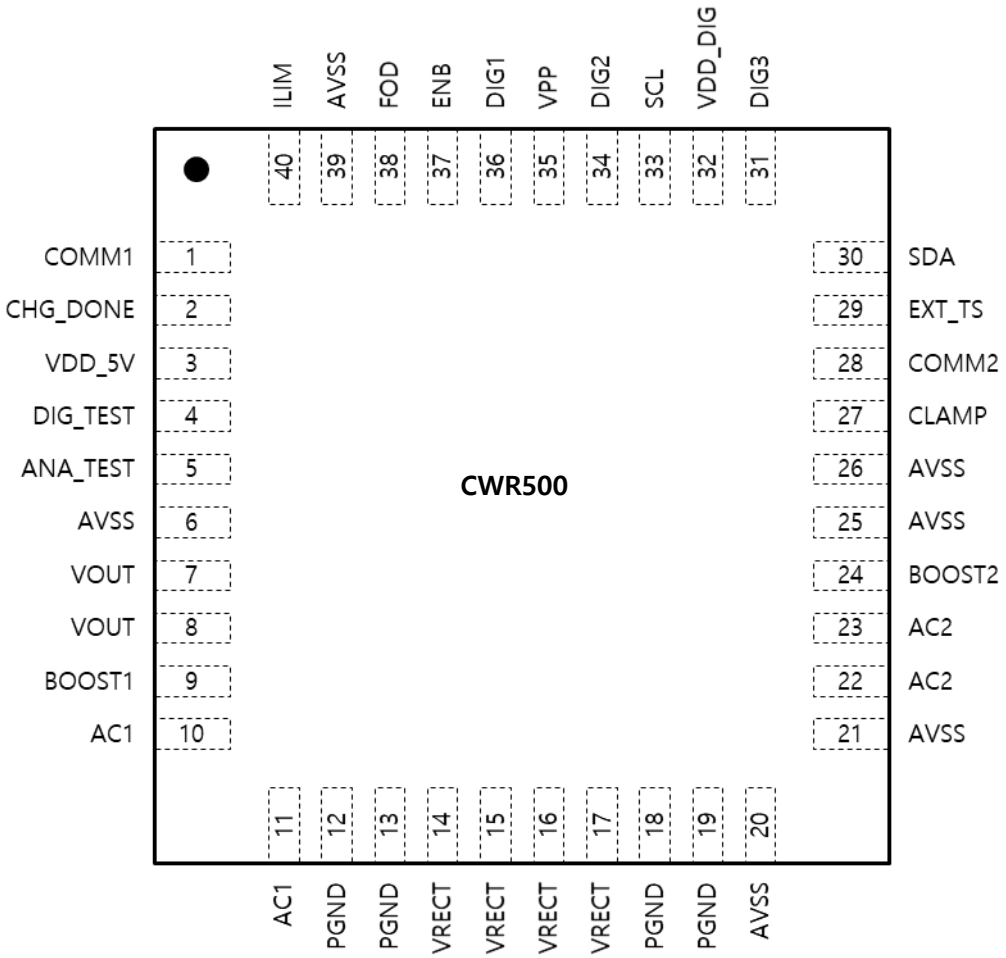


Figure 3. CWR500 Pin Configuration (QFN 40-pin 6mm x 6mm, 0.5mm pitch)

2.1 Pin Description (QFN 40-pin 6mm x 6mm, 0.5mm pitch)

Pin Number	Name	Type	Description
1	COMM1	O	High voltage open drain output for ASK modulation.
28	COMM2	O	
2	CHG_DONE	I	Active-high input from the external battery charger to terminate power transfer.
3	VDD_5V	O	Internal 5V LDO output pin for capacitor connection.
4	DIG_TEST	O	Digital test output pin.
5	ANA_TEST	O	Analog test output pin.

6,20,21,25 26,39	AVSS		Analog ground pin.
7,8	VOUT	O	Main LDO output pin for delivering power to the battery charger.
9	BOOST1	O	Bootstrap capacitor connection pin for driving the high-side FETs of synchronous rectifier.
24	BOOST2	O	
10,11	AC1	I	AC power input of synchronous rectifier.
22,23	AC2	I	
12,13,18,19	PGND		Power ground for synchronous rectifier.
14,15,16,17	VRECT	O	Internal synchronous rectifier output for capacitor connection.
27	CLAMP	O	High voltage open drain output for analog linear over-voltage protection.
29	EXT_TS	I	External temperature sensor input. Connect this pin to external NTC thermistor. If not used, connect this pin to VDD_DIG.
30	SDA	I/O	I^2C data input/output for internal register access.
31	DIG3	I	Scan clock for scan test mode.
32	VDD_DIG	I/O	Internal 3V LDO output for digital block and etc.
33	SCL	I	I^2C clock input for internal register access.
34	DIG2	I	Scan enable for scan test mode.
35	VPP	I	8V high voltage power for OTP programming. During the normal operation, connect this pin to VDD_DIG.
36	DIG1	I	Enable scan test mode.
37	ENB	I	Active-low enable pin for the entire chip.
38	FOD	I	FOD offset setting pin. Connect a resistor between this pin and GND.
40	ILIM	I	Output current or over-current limit level programming pin.

3. Application Guide

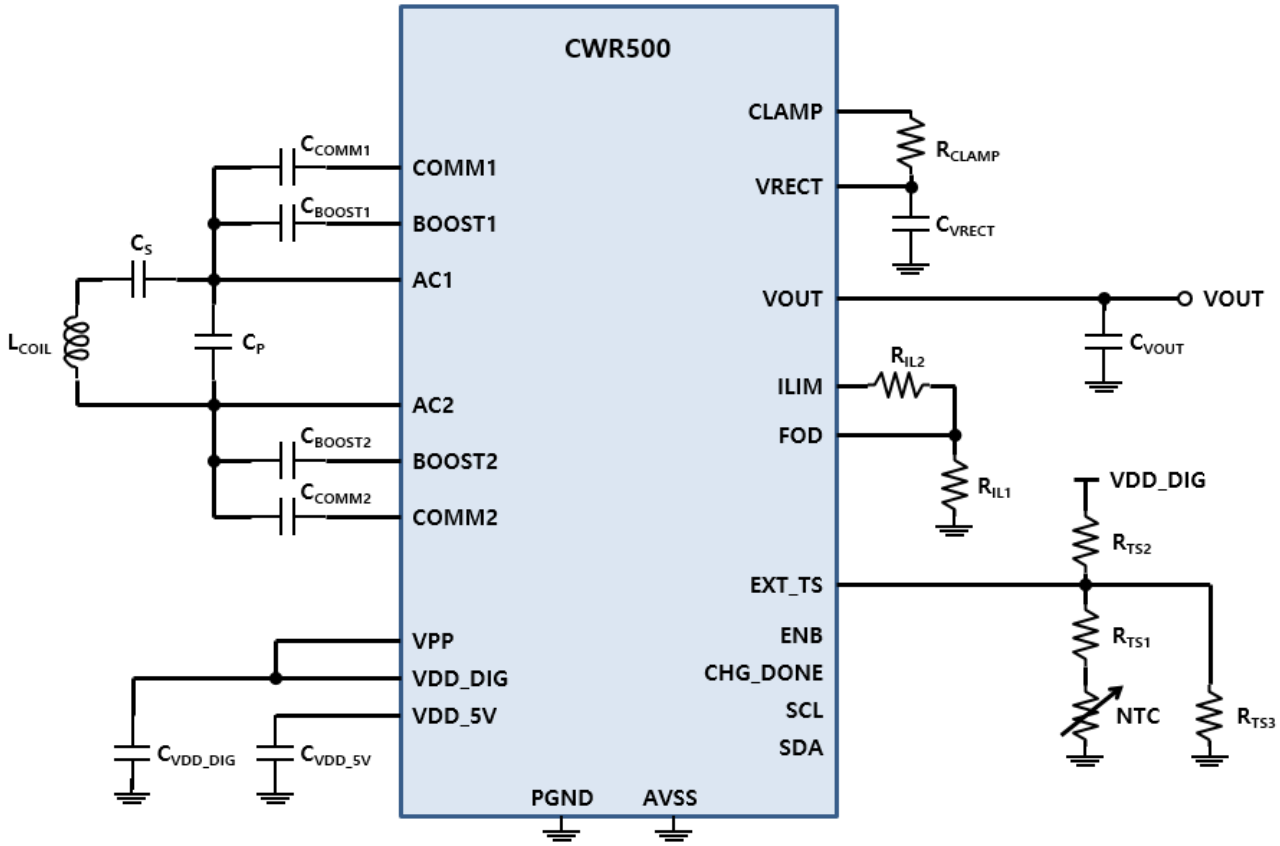


Figure 4. CWR500 Typical Application Diagram

3.1 Receiver Coil and Resonant Capacitors

The receiver coil design is related to the overall system application. The coil inductance, shape and material can be chosen according to your applications. The recommended receiver coil inductance for dual mode operation is between 5uH to 10uH. Series and parallel resonant capacitors C_S and C_P are set according to WPC specification. The capacitance of the resonant capacitors can be calculated by the following equations.

$$C_S = \frac{1}{L'_S \times (2\pi f_S)^2}$$

$$C_P = \frac{1}{L_S \times (2\pi f_D)^2 - \frac{1}{C_S}}$$

In these equations, f_S and f_D are the dual resonant frequencies which cover the power transfer frequency range. For example, f_S can be set to 100kHz and f_D can be set to 1000kHz, respectively. L'_S is coil self inductance when placed on the transmitter, and L_S is the self inductance when placed away from the transmitter.

3.2 Boost and Communication Capacitors

As shown in Figure 4, two external bootstrap capacitors C_{BOOST1} and C_{BOOST2} are needed to drive the high-side FETs of synchronous rectifier. Bootstrap capacitors should have voltage rating of more than 25V and their recommended capacitances are 15nF.

In order to communicate with transmitter, external capacitors should be connected between high voltage open drain output and AC1/AC2 input. CWR500 will be switching COMM1/COMM2 output in WPC mode. Typical recommended capacitance values are C_{COMM1}=C_{COMM2}=22nF.

3.3 Output Regulating Capacitors

As shown in Figure 4, rectifier output VRECT and internal LDOs' output VOUT, VDD_5V, VDD_DIG should be connected to external capacitor for voltage regulation. Typical recommended capacitance values are C_{VRECT}=20uF, C_{VOUT}=3.3uF, C_{VDD_5V}=1uF, C_{VDD_DIG}=1uF, respectively.

3.4 Clamp Resistor

When the VRECT voltage is too high, the OVP (Over Voltage Protection) function will turn on the clamp path or send the EPT (End Power Transfer) packet to the transmitter. The clamp path uses high voltage open drain output for analog linear OVP. The recommended resistance value of R_{CLAMP} is between 5Ω to 20Ω according to the transfer power level of application.

3.5 Current Limit and FOD Setting Resistors

When the main LDO current is too large, the OCL (Over Current Limit) function will limit the output current. The current limit level can be adjusted by external resistors and it is calculated as follows,

$$I_{LIM} = \frac{45000}{R_{ILIM}} = \frac{45000}{R_{IL1} + R_{IL2}}$$

In this equation, the R_{ILIM} is the total resistance from the ILIM pin to ground, that is, R_{IL1} + R_{IL2} as shown in Figure 4. It is recommended to use the resistors of good tolerance less than 1%, because the current estimation in wireless power receiver is very important.

CWR500 adds an FOD offset proportional to output power level when it sends the received power packet to transmitter. The amount of the added FOD offset can be adjusted by the ratio of R_{IL1} to (R_{IL1} + R_{IL2}).

3.6 External Temperature Sensor

When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will send the EPT packet to transmitter or shutdown the receiver system. In order to sense the temperature outside chip, connect EXT_TS pin to external NTC (Negative temperature Coefficient) thermistor as shown in Figure 4. The NTC thermistor should be placed close to the heat emission device.

The EXT_TS voltage V_{EXT_TS} can be calculated as follows,

$$V_{EXT\_TS} = VDD\_DIG \times \frac{\frac{(R_{NTC} + R_{TS1}) \times R_{TS3}}{(R_{NTC} + R_{TS1}) + R_{TS3}}}{\frac{(R_{NTC} + R_{TS1}) \times R_{TS3}}{(R_{NTC} + R_{TS1}) + R_{TS3}} + R_{TS2}}$$

In this equation, VDD_DIG is 3V from the internal LDO.

CWR500 compares V_{EXT_TS} with internal reference voltages V_{TS_HOT} and V_{TS_COLD}. If V_{EXT_TS}<V_{TS_HOT}, it means external temperature is too high and CWR500 sends the EPT packet to transmitter. On the other hand, if

V_{EXT_TS}>V_{TS_COLD}, it means external temperature is too low and CWR500 also sends the EPT packet to transmitter. Remind that V_{EXT_TS} is negative slope curve vs temperature.

The internal reference voltages V_{TS_HOT} and V_{TS_COLD} are fixed values as follows,

Internal TS Reference	Threshold Voltage [V]	Hysteresis [mV]
V_{TS_HOT}	0.315	20
V_{TS_COLD}	0.980	80

Recommended NTC resistance range is from hundreds of Ω to hundreds of kΩ vs temperature. After choosing the appropriate NTC thermistor, you can design R_{TS1}, R_{TS2} and R_{TS3} according to your thermal protection specification. Table 1 shows an EXT_TS thermal protection design example.

Temp [℃]	VDD_DIG [V]	R_{NTC} [kΩ]	R_{TS1} [kΩ]	R_{TS2} [kΩ]	R_{TS3} [kΩ]	V_{EXT_TS} [V]	Status
-40	3.0	188.5	3.9	47	68	1.550	V_{EXT_TS} > V_{TS_COLD} Send EPT packet
-30	3.0	111.3	3.9	47	68	1.429	
-20	3.0	67.8	3.9	47	68	1.278	
-10	3.0	42.5	3.9	47	68	1.109	
0	3.0	27.3	3.9	47	68	0.938	V_{TS_HOT} < V_{EXT_TS} < V_{TS_COLD} Normal charging operation
10	3.0	18.0	3.9	47	68	0.782	
20	3.0	12.1	3.9	47	68	0.648	
30	3.0	8.31	3.9	47	68	0.541	
40	3.0	5.83	3.9	47	68	0.460	
50	3.0	4.16	3.9	47	68	0.399	
60	3.0	3.02	3.9	47	68	0.354	
70	3.0	2.23	3.9	47	68	0.321	
80	3.0	1.67	3.9	47	68	0.296	V_{EXT_TS} < V_{TS_HOT} Send EPT packet
90	3.0	1.27	3.9	47	68	0.278	
100	3.0	0.98	3.9	47	68	0.265	
110	3.0	0.76	3.9	47	68	0.255	
120	3.0	0.60	3.9	47	68	0.247	

Table 1. EXT_TS Thermal Protection Design Example

In this example, the hot temperature threshold T_{TS_HOT} and the cold temperature threshold T_{TS_COLD} are designed to be 80℃ and -10℃ respectively. You can change the hot and cold temperature threshold according to your application by changing the related resistors.

3.7 PCB Layout Guide

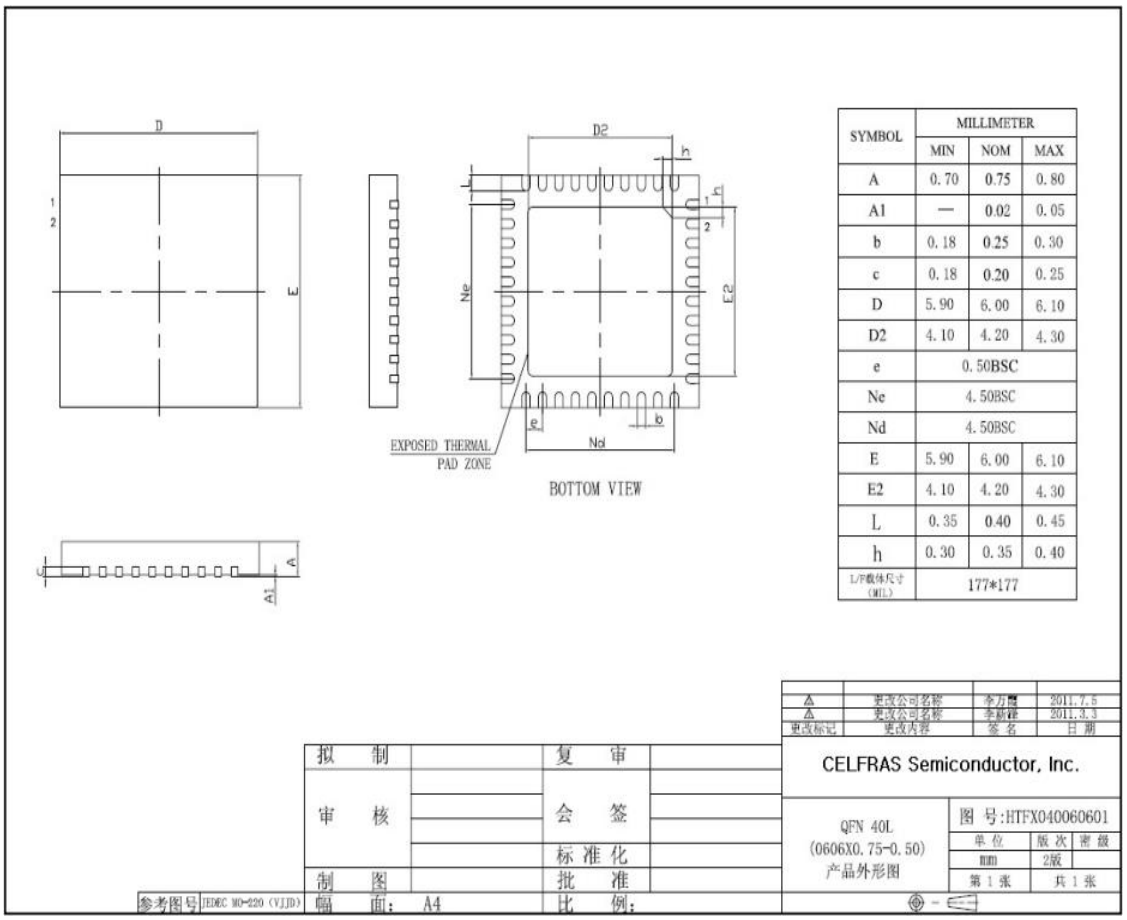
- Keep the trace resistance as low as possible on large current nets as shown in Table 2.
- Resonant capacitors C_S and C_P need to be as close to the device as possible.

- Clamp, boost and communication capacitors (C_{CLAMP}, C_{BOOST1}, C_{BOOST2}, C_{COMM1}, C_{COMM2}) need to be as close to the device as possible.
- Output regulating capacitors C_{VRECT} and C_{VOUT} need to be as close to the device as possible.

Net (Ball)	Type	Maximum Current [A]
AC1, AC2	AC	1
VRECT	AC	1
VOUT	DC	1
PGND	AC	1
COMM1, COMM2	AC	0.5
CLAMP	AC	1

Table 2. Large Current Nets

4. Package Outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	177*177		

△	更改公司名称	李力强	2011.7.5
△	更改公司名称	李松霞	2011.3.3
更改标记	更改内容	签 名	日 期

拟 制		复 审	
审 核		会 签	
		标准化	
制 图		批 准	
参考图号 JEDEC MO-220 (VJJD)	幅 面: A4	比 例:	

CELFRAS Semiconductor, Inc.

QFN 40L
(0606X0.75-0.50)
产品外形图

图 号:HTFX040060601

单位	版 次	密 级
mm	2版	
第 1 张	共 1 张	

Figure 6. QFN 40-pin Package Outline, 6.0mm x 6.0mm, 0.5mm pitch

5. Electrical Characteristics

5.1 Absolute Maximum Rating

PIN	Parameter	Rating	Unit
AC1, AC2, COMM1, COMM2, VRECT, CLAMP	Voltage	-0.3 to 20	V
BOOST1, BOOST2	Voltage	-0.3 to 26	V
VOUT	Voltage	-0.3 to 15	V
VPP	Voltage	-0.3 to 8	V
VDD_5V, VDD_DIG, ENB, CHG_DONE ILIM, FOD, EXT_TS, SCL, SDA	Voltage	-0.3 to 6	V
PGND	Voltage	-0.3 to 0.3	V
AC1, AC2, VRECT, VOUT, CLAMP, PGND	Current	2	A
COMM1, COMM2	Current	1	A

5.2 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit
V_{RECT}	Rectifier voltage range	4		10	V
I_{OUT}	Main LDO output current			1	A
I_{COMM}	COMM1, COMM2 sink current			500	mA
T_J	Junction temperature	-30		125	℃
T_A	Ambient temperature	-30		85	℃

5.3 Device Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Synchronous Active Rectifier						
V_{IN_RECT}	AC1, AC2 input voltage range		4.0		10	V
f_{IN_RECT}	AC1, AC2 input frequency range		80		500	kHz
E_{ff_RECT}	AC to DC power conversion efficiency			92		%
V_{UVLO}	Under voltage lockout	V_{RECT}: 0V to 4V		3.2	3.3	V
V_{UVLO_HYS}	Under voltage lockout hysteresis	V_{RECT}: 4V to 0V		400		mV
Main LDO						
V_{IN_MLDO}	Main LDO input voltage range		4.0		10	V

V_{OUT_MLDO}	Main LDO output voltage range Register programmable	V_{RECT}>5V	4.5	5.0	5.5	V
$V_{OUT\_MLDO\_STEP}$	Main LDO output voltage control step			0.5		V
I_{OUT_MLDO}	Main LDO output current range				1.3	A
P_{SRR_MLDO}	Main LDO power supply rejection ratio	C_{VOUT}=3.3uF DC to 100MHz	20			dB
Internal LDO						
$V_{OUT\_VDD\_5V}$	Internal VDD_5V LDO output voltage range	V_{RECT}>5V		5		V
$V_{OUT\_VDD\_DIG}$	Internal VDD_DIG LDO output voltage range	V_{RECT}>3V		3		V
BGR						
V_{BGR}	Internal BGR output voltage Register programmable	V_{RECT}>3V		1.22		V
Oscillator						
f_{OSC}	Internal oscillator frequency Register programmable	V_{RECT}>3V		15		MHz
ADC						
N_{ADC}	ADC resolution	V_{RECT}>3V		12		bit
f_{SAMPLE}	ADC sampling rate	f_{OSC}=15MHz		217		kSa/s
N_{CH_ADC}	ADC channel			7		
Protection						
I_{OCL}	I_{OUT} over current limit protection Programmable by R_{ILIM}	R_{ILIM}=24kΩ I_{OUT}: 0A to 2A		1.875		A
I_{OCL_HYS}	OCL hysteresis	I_{OUT}: 2A to 0A		50		mA
T_{OTP}	Over temperature protection Thermal shutdown temperature	Temperature: 30℃ to 160℃		150		℃
T_{OTP_HYS}	OTP hysteresis	Temperature: 160℃ to 30℃		20		℃
V_{TS_HOT}	EXT_TS hot temperature protection threshold voltage	V_{EXT_TS}: 0V to 0.5V		0.315		V
$V_{TS\_HOT\_HYS}$	V_{TS_HOT} hysteresis	V_{EXT_TS}: 0.5V to 0V		20		mV
V_{TS_COLD}	EXT_TS cold temperature protection threshold voltage	V_{EXT_TS}: 0.5V to 1.5V		0.980		V
$V_{TS\_COLD\_HYS}$	V_{TS_COLD} hysteresis	V_{EXT_TS}: 1.5V to 0.5V		80		mV

6. I²C Signal Timing

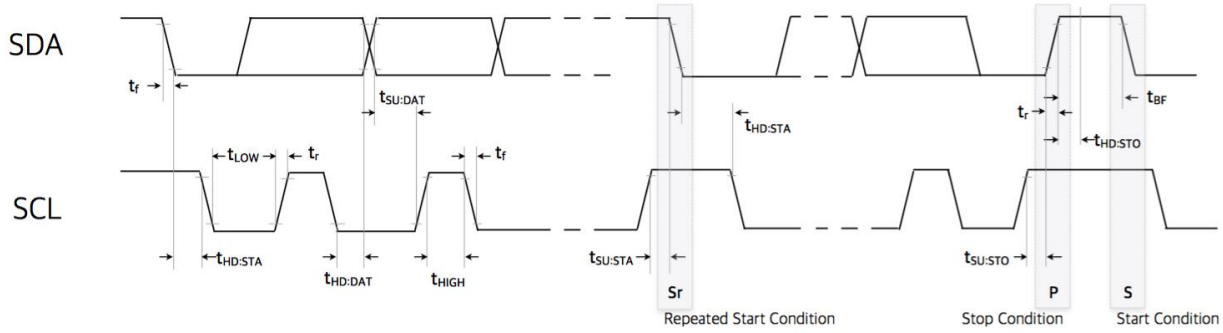


Figure 7. Timing Diagram for I²C interface

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL_SDA}	Input low threshold level SDA	V_{PULLUP}=VDD_DIG=3V			0.7	V
V_{IH_SDA}	Input high threshold level SDA	V_{PULLUP}=VDD_DIG=3V	2.3			V
V_{IL_SCL}	Input low threshold level SCL	V_{PULLUP}=VDD_DIG=3V			0.7	V
V_{IH_SCL}	Input high threshold level SCL	V_{PULLUP}=VDD_DIG=3V	2.3			V
f_{SCL}	SCL clock frequency				400	kHz
t_{LOW}	SCL clock low time		1.3			us
t_{HIGH}	SCL clock high time		0.6			us
t_r	Rise time of both SDA and SCL				0.3	us
t_f	Fall time of both SDA and SCL				0.3	us
$t_{SU,STA}$	Setup time for START condition		0.6			us
$t_{HD,STA}$	Hold time for START condition		0.6			us
$t_{SU,DAT}$	Data setup time		0.1			us
$t_{HD,DAT}$	Data hold time				0.9	us
$t_{SU,STO}$	Setup time for STOP condition		0.6			us
t_{BF}	Bus free time between STOP and START condition		1.3			us

Table 3. I²C Characteristics

Revision History

Date	Version No.	Description
2018/07/01	1.0	Preliminary Release

Ordering Information

Part Number	Package	Shipping Carrier	Description
CWR500	QFN 40	Tray	VOUT=5V(BPP)

Contact US

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