

## General Description

CWT1541 can deliver up to 15W as a highly-integrated single-chip wireless medium power transmitter IC. It can be configured to receive its input power from USB or AC adapter. Our chip integrates a power amp driver, a precise clock generator for PA frequency control, and communication controllers which use Amplitude Shift Keying (ASK) and Frequency Shift Keying (FSK). CWT1541 can support multi-coil transmitter with CWP1500 companion PA chip and it also can support precise fixed frequency PA operation with external crystal. Our chip includes a 32-bit ARM Cortex M0 processor in order to offer high level of programmability according to its applications. Communication and control units (CCU) can accommodate WPC protocol including fault condition handling associated with power transfer. The CCU supports the foreign object detection (FOD) extension. Also, the chip includes over-temperature and voltage protection.

## Features Overview

- WPC-1.2.4 compliant for MP-A8 medium power specification
- High-efficiency power transfer system supporting baseline power profile (<5W) and extended power profile (<15W)
  - Overall system efficiency up to 90%
- Input operating voltage of 4.5V to 13V, supporting USB and AC adapter
- Integrated pre-amplify drivers for external power amp
- Support multi-coil transmitter with CWP1500 companion PA chip
- Support up to 17 GPIO ports for multi-coil transmitter
- Support precise 127.7kHz fixed frequency PA operation
- Integrated 32-bit ARM Cortex M0 processor
  - SRAM for program memory and data memory
- Bi-directional channel communication
- 12-bit ADC for voltage/current measurement
- I2C programmable interface
- Foreign object detection
- Precise current sensor
- Over voltage protection
- Over current limit
- Over temperature protection
- Optional external power amp configuration
- 128-bit One-Time-Programmable Device
- Low stand-by power
- QFN 48-pin 6mm x 6mm, 0.4mm pitch

## Applications

- Wireless charging pads
- Wireless power solutions for Mobile Applications

## 1. Description for Implementation

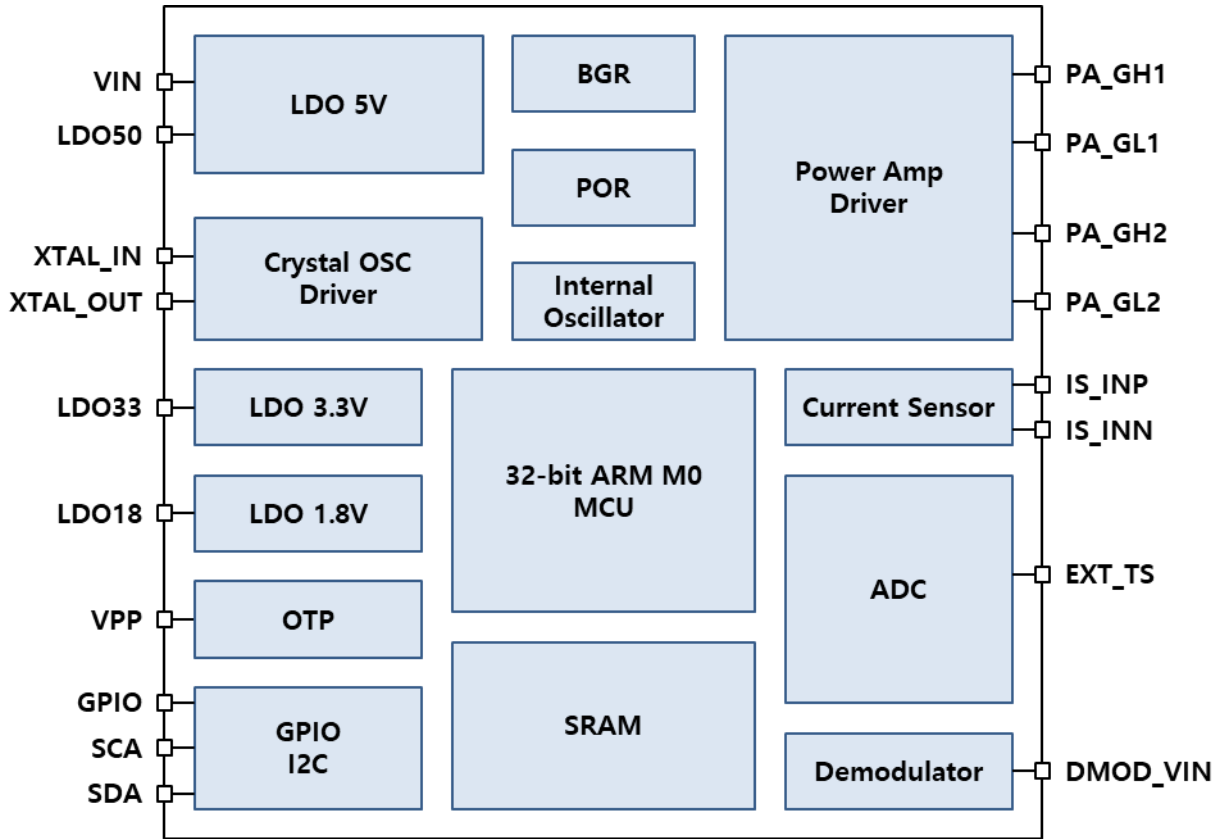


Figure 1. CWT1541 Block Diagram

### 1.1 Overview

A wireless power charging system is composed of transmitter and receiver. In general, wireless power transmitter will transfer AC power using a power amplifier through a TX inductor coil. Then wireless power receiver will receive AC power through an RX inductor coil which is strongly coupled with the TX coil. In transmitter part, power amplifier (PA) will change the DC power to AC power and transfer the AC power to the TX coil.

Figure1 shows the block diagram of CWT1541 wireless charging transmitter IC. CWT1541 transmitter will support power transfer up to 15W and it is compliant with WPC 1.2.4 standard. It consists of power amp driver, step down DC-DC converter, internal LDOs, ADC, 32-bit ARM M0 MCU, SRAM and etc.

### 1.2 Crystal OSC Driver

CWT1541 employs an internal negative Gm driver in order to drive external crystal. CWT1541 can implement the precise power transfer frequency by using this crystal oscillator. Some applications often require accurate PA frequency implementation. With an external crystal, CWT1541 can tune to tens of ppm accurately.

On the other hand, CWT1541 also supports the internal oscillator. For applications which do not require the correct frequency, we can lower the BOM by using the internal oscillator.

### 1.3 Power Amp Driver

The power amplifier of CWT1541 consists of four external power NLD MOSs and internal driver circuits. The power amp driver also includes boosting circuits for driving external high side NLD MOS. Each gate control signal can be adjusted by internal control and MCU.

The power amplifier of CWT1541 converts input DC power to AC power and transfers it directly to the TX coil. Since power amplifier directly influences the overall transmitter efficiency, the gate control of power MOSFET switches is very important. The power amp driver of CWT1541 changes its switching frequency and duty cycle according to the load current and feedback from the receiver.

#### 1.4 FSK Modulator

The Qi extended power profile (EPP) uses two-way communication for power transfer. In the Qi standard, TX to RX communication is accomplished by frequency shift keying (FSK) modulation over the power signal frequency.

CWT1541 power transmitter uses FSK modulation for transmitting protocol data to the power receiver. CWT1541 changes the period of the power transfer signal by counting the internal 60MHz oscillator. The frequency deviation between the base operating frequency  $f_{OP}$  and the modulation frequency  $f_{MOD}$  is designed according to the Qi EPP standard.

#### 1.5 ASK Demodulator

In the Qi standard, RX to TX communication is accomplished by amplitude shift keying (ASK) modulation with a bit rate of 2Kbps. CWT1541 power transmitter uses an external peak detection circuit and an internal comparator circuit for ASK demodulation. The external peak detection circuit include diode and filtering capacitors and resistors. The ASK demodulator in CWT1541 demodulates the WPC standard 2kHz bi-phase signal from the power receiver.

#### 1.6 ADC

CWT1541 power transmitter employs 12-bit SAR ADC because it has low power, small area characteristics and moderate speed performance. ADC monitors important internal voltages and currents and gives the system information to the digital controller.

#### 1.7 Protection

CWT1541 power transmitter employs various protection schemes in order to prevent system damage. When the external power amplifier current is too large, the OCL (Over Current Limit) function will limit the output current. When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will shut down the transmitter system to prevent damage resulting from excessive thermal stress under fault conditions.

#### 1.8 Digital Controller

Digital controller of CWT1541 is composed of a 32-bit ARM Cortex M0 processor, OTP, SRAM for program and data memory, etc. Digital controller controls all the analog blocks and entire system to perform power transfer operation according to the wireless power transfer Qi standard. CWT1541 supports the eight GPIO pins and two of them can be dedicated to I2C interface for communication with external host.

## 2. Pin-out and description

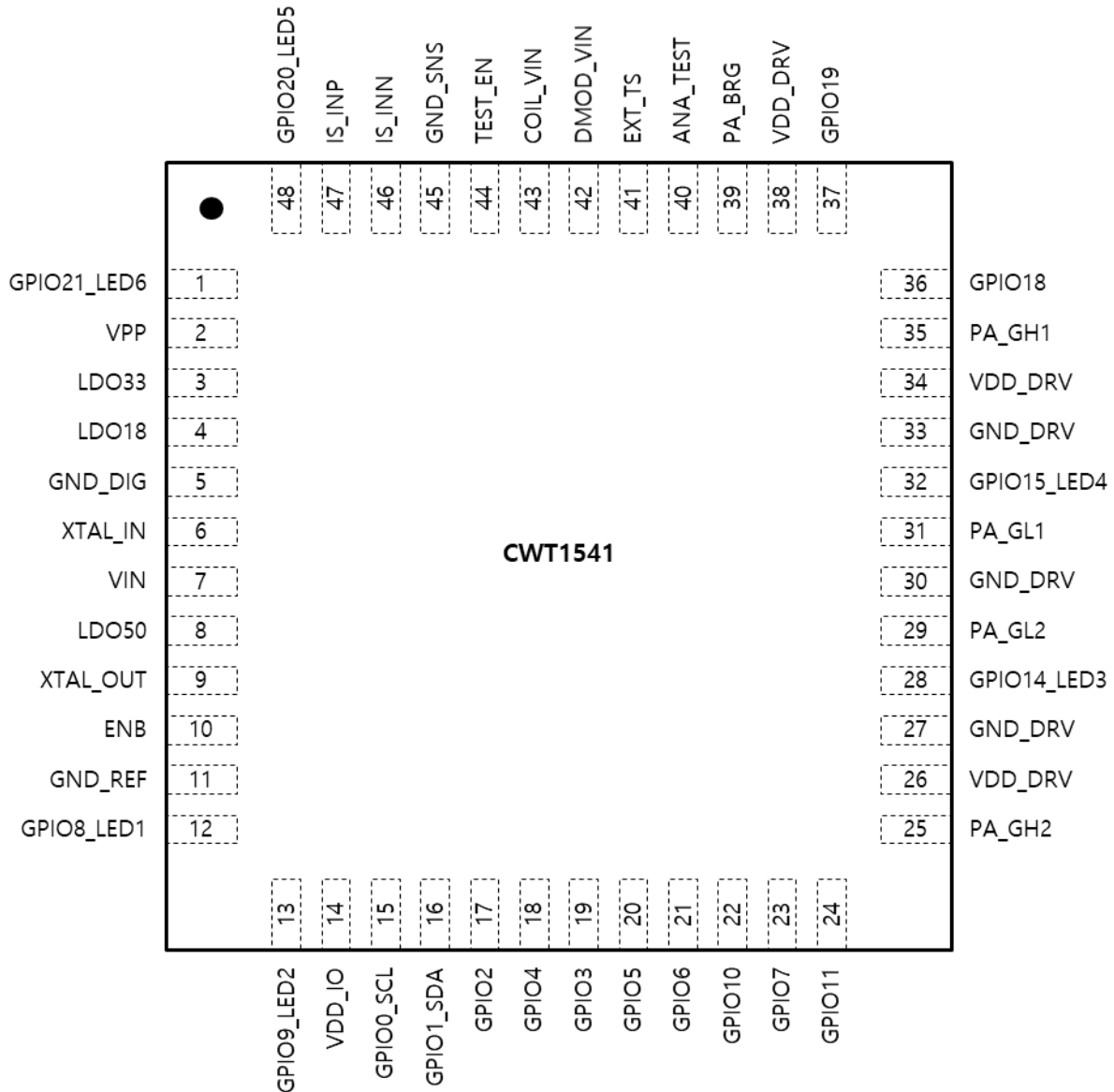


Figure 2. CWT1541 Pin Configuration (QFN 48-pin 6mm x 6mm, 0.4mm pitch)

### 2.1 Pin Description

Pin Number	Name	Type	Description
1	GPIO21_LED6	I/O	General purpose inputs/outputs. These pins can drive large pull-down current for high brightness LED applications.
12	GPIO8_LED1		
13	GPIO9_LED2		
28	GPIO14_LED3		
32	GPIO15_LED4		
48	GPIO20_LED5		

2	VPP	I	8V high voltage power for OTP programming. During the normal operation, connect this pin to LDO33.
3	LDO33	O	Internal 3.3V LDO output pin for capacitor connection.
4	LDO18	O	Internal 1.8V LDO output pin for capacitor connection.
5	GND_DIG		Ground for internal digital block.
6	XTAL_IN	I	External crystal input
7	VIN	I	DC power input for power transmission.
8	LDO50	O	Internal 5V LDO output pin for capacitor connection.
9	XTAL_OUT	O	External crystal output
10	ENB	I	Active-low enable pin for the entire chip.
11	GND_REF		Ground for internal reference block.
14	VDD_IO	I	Input power supply for GPIO0-7. The operating range of this pin is 1.8-5.0V.
15	GPIO0_SCL	I/O	General purpose input/output 0. This pin can be dedicated for I <sup>2</sup> C clock input for internal register access.
16	GPIO1_SDA	I/O	General purpose input/output 1. This pin can be dedicated for I <sup>2</sup> C data input/output for internal register access.
17 18 19 20 21 22 23 24 36 37	GPIO2 GPIO4 GPIO3 GPIO5 GPIO6 GPIO10 GPIO7 GPIO11 GPIO18 GPIO19	I/O	General purpose inputs/outputs.
25	PA_GH2	O	PA gate driver output for the high side FET of half bridge 2.
26,34,38	VDD_DRV	I	Input power supply for the PA drivers.
27,30,33	GND_DRV		Ground for PA driver.
29	PA_GL2	O	PA gate driver output for the low side FET of half bridge 2.
31	PA_GL1	O	PA gate driver output for the low side FET of half bridge 1.
35	PA_GH1	O	PA gate driver output for the high side FET of half bridge 1.
39	PA_BRG	I	PA bridge voltage sensing pin.
40	ANA_TEST	O	Analog test output pin.
41	EXT_TS	I	External temperature sensor input. Connect this pin to external NTC thermistor. If not used, connect this pin to LDO33.
42	DMOD_VIN	I	Voltage sensing input pin for ASK demodulation.
43	COIL_VIN	I	Q factor Measurement
44	TEST_EN	I	Digital scan test enable

45	GND_SNS		Ground for internal sensors.
46	IS_INN	I	Input current sensor negative input.
47	IS_INP	I	Input current sensor positive input.

## 3. Application Guide

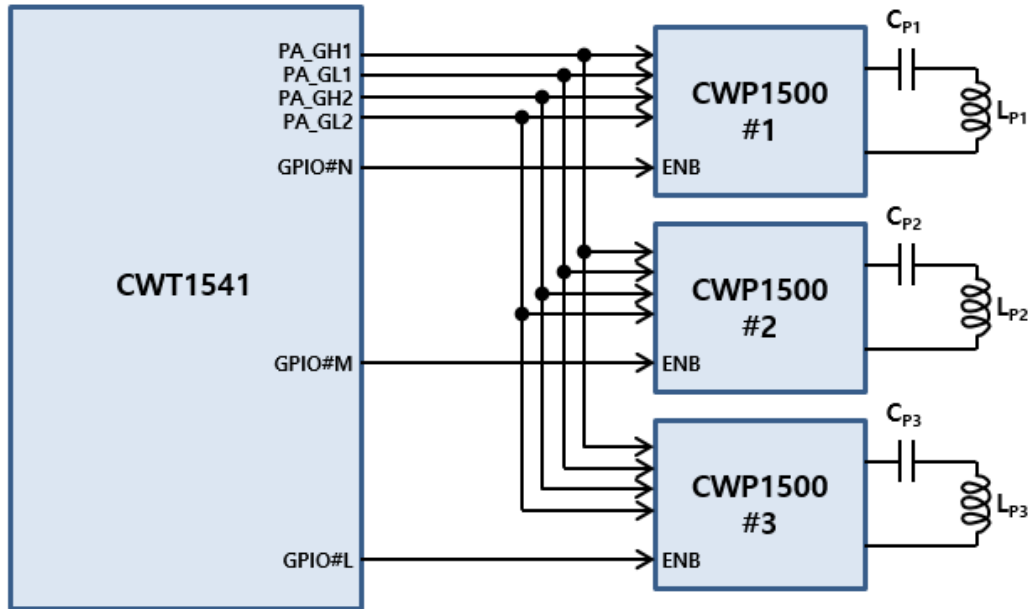


Figure 3. CWT1541 Multi-coil Application Diagram with CWP1500

### 3.1 Transmitter Coil and Resonant Capacitors

The transmitter coil design is related to the overall system application. The coil inductance, shape and material can be chosen according to its applications. However, it must comply with the WPC recommendations which include the self-inductance value, DC resistance, Q factor, etc. The resonant circuits of the power transmitter consist of an inductance  $L_p$ , a capacitance  $C_p$ , and a resistance  $R_p$ , where the  $R_p$  is the parasitic resistance. With respect to TX coil and capacitor, the resonant frequency  $f_p$  and the quality factor  $Q_p$  can be calculated by the following equations.

$$f_p = \frac{1}{2\pi\sqrt{L_p C_p}}$$

$$Q_p = \frac{2\pi f_p L_p}{R_p}$$

The resonant frequency  $f_p$  and the quality factor  $Q_p$  must be in the range of WPC recommendation.

### 3.2 Power MOSFETs and Boost Capacitors

As shown in Figure 3, CWT1541 power transmitter uses four external power MOSFETs for the power amplifier configuration. Since the input voltage range of CWT1541 is 0 to 13V, the external power MOSFETs should be high voltage devices. CWT1541 power transmitter uses two high side N-channel MOSFETs to

improve efficiency and uses boosting circuits to drive them. The recommended power MOSFETs are 30V N-channel LDMOS.

As explained, two external bootstrap capacitors  $C_{BOOST1}$  and  $C_{BOOST2}$  are needed to drive the high-side FETs of external power amplifier. Bootstrap capacitors should have voltage rating of more than 25V and their recommended capacitances are 0.1uF.

### 3.3 Output Regulating Capacitors

As shown in Figure 3, internal LDOs' output LDO50, LDO33, LDO18 should be connected to external capacitor for voltage regulation. Typical recommended capacitance values are  $C_{LDO50}=1\mu F$ ,  $C_{LDO33}=1\mu F$ ,  $C_{LDO18}=1\mu F$ , respectively.

### 3.4 Input Current Sensing Resistor

The CWT1541 power transmitter uses an external resistor for the PA input current path to sense the input current. The sensing resistor tolerance should be less than 1% to meet the WPC FOD specification. Also, the current capacity of the resistor must be large because its maximum current reaches up to 2A.

### 3.5 External Temperature Sensor

When the temperature inside or outside the chip is too high, the OTP (Over Temperature Protection) function will send the EPT packet to transmitter or shutdown the receiver system. In order to sense the temperature outside chip, connect EXT\_TS pin to external NTC (Negative temperature Coefficient) thermistor as shown in Figure 3. The NTC thermistor should be placed close to the heat emission device.

The EXT\_TS voltage  $V_{EXT\_TS}$  can be calculated as follows,

$$V_{EXT\_TS} = V_{LDO33} \times \frac{\frac{(R_{NTC} + R_{TS1}) \times R_{TS3}}{(R_{NTC} + R_{TS1}) + R_{TS3}}}{\frac{(R_{NTC} + R_{TS1}) \times R_{TS3}}{(R_{NTC} + R_{TS1}) + R_{TS3}} + R_{TS2}}$$

In this equation,  $V_{LDO33}$  is 3.3V from the internal LDO.

CWT1541 compares  $V_{EXT\_TS}$  with internal reference voltages  $V_{TS\_HOT}$  and  $V_{TS\_COLD}$ . If  $V_{EXT\_TS} < V_{TS\_HOT}$ , it means external temperature is too high and CWT1541 sends the EPT packet to transmitter. On the other hand, if  $V_{EXT\_TS} > V_{TS\_COLD}$ , it means external temperature is too low and CWT1541 also sends the EPT packet to transmitter. Remind that  $V_{EXT\_TS}$  is negative slope curve vs temperature.

The reference voltages  $V_{TS\_HOT}$  and  $V_{TS\_COLD}$  are programmable values by firmware. For example,  $V_{TS\_HOT}$  and  $V_{TS\_COLD}$  are programmed as follows,

Internal TS Reference	Threshold Voltage [V]	Hysteresis [mV]
$V_{TS\_HOT}$	0.315	20
$V_{TS\_COLD}$	0.980	80

Recommended NTC resistance range is from hundreds of  $\Omega$  to hundreds of  $k\Omega$  vs temperature. After choosing the appropriate NTC thermistor, you can design  $R_{TS1}$ ,  $R_{TS2}$  and  $R_{TS3}$  according to your thermal protection specification. Table 1 shows an EXT\_TS thermal protection design example.

Temp [°C]	$V_{LDO33}$ [V]	$R_{NTC}$ [k $\Omega$ ]	$R_{TS1}$ [k $\Omega$ ]	$R_{TS2}$ [k $\Omega$ ]	$R_{TS3}$ [k $\Omega$ ]	$V_{EXT\_TS}$ [V]	Status
-40	3.3	188.5	3.9	47	68	1.550	$V_{EXT\_TS} > V_{TS\_COLD}$ Send EPT packet
-30	3.3	111.3	3.9	47	68	1.429	



-20	3.3	67.8	3.9	47	68	1.278	$V_{TS\_HOT} < V_{EXT\_TS} < V_{TS\_COLD}$ Normal charging operation
-10	3.3	42.5	3.9	47	68	1.109	
0	3.3	27.3	3.9	47	68	0.938	
10	3.3	18.0	3.9	47	68	0.782	
20	3.3	12.1	3.9	47	68	0.648	
30	3.3	8.31	3.9	47	68	0.541	
40	3.3	5.83	3.9	47	68	0.460	
50	3.3	4.16	3.9	47	68	0.399	
60	3.3	3.02	3.9	47	68	0.354	
70	3.3	2.23	3.9	47	68	0.321	
80	3.3	1.67	3.9	47	68	0.296	$V_{EXT\_TS} < V_{TS\_HOT}$ Send EPT packet
90	3.3	1.27	3.9	47	68	0.278	
100	3.3	0.98	3.9	47	68	0.265	
110	3.3	0.76	3.9	47	68	0.255	
120	3.3	0.60	3.9	47	68	0.247	

**Table 1. EXT\_TS Thermal Protection Design Example**

In this example, the hot temperature threshold  $T_{TS\_HOT}$  and the cold temperature threshold  $T_{TS\_COLD}$  are designed to be 80°C and -10°C respectively. You can change the hot and cold temperature threshold according to your application by changing the related resistors.

### 3.6 PCB Layout Guide

- Keep the trace resistance as low as possible on large current nets associated with the external power MOSFETs.
- Resonant capacitor  $C_p$  needs to be as close to the device as possible.
- Boost capacitors ( $C_{BOOST1}$ ,  $C_{BOOST2}$ ) need to be as close to the device as possible.
- Output regulating capacitors  $C_{LDO\_IN}$ ,  $C_{LDO50}$ ,  $C_{LDO33}$  and  $C_{LDO18}$  need to be as close to the device as possible.



## 5. Electrical Characteristics

### 5.1 Absolute Maximum Rating

PIN	Parameter	Rating	Unit
VIN, ENB, PA_BRG IS_INP, IS_INN	Voltage	-0.3 to 26	V
VPP	Voltage	-0.3 to 8	V
LDO33, LDO50, VDD_IO GPIO0_SCL, GPIO1_SDA, GPIO2, GPIO3, GPIO4 GPIO5, GPIO6, GPIO7, GPIO8_LED1, GPIO9_LED2 GPIO10, GPIO11, GPIO14_LED3, GPIO15_LED4 GPIO18, GPIO19, GPIO20_LED5, GPIO21_LED6 PA_GH2, PA_GH1, PA_GL2, PA_GL1 VDD_DRV, ANA_TEST, EXT_TS, DMOD_VIN COIL_VIN, TEST_EN, XTAL_IN, XTAL_OUT	Voltage	-0.3 to 6	V
LDO18	Voltage	-0.3 to 2	V
GND_DIG, GND_REF, GND_SNS, GND_DRV	Voltage	-0.3 to 0.3	V

### 5.2 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>IN</sub>	DC power input for power transmission.	4.5		13.0	V
T <sub>J</sub>	Junction temperature	-30		125	°C
T <sub>A</sub>	Ambient temperature	-30		85	°C

### 5.3 Device Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
<b>Input Supply and Current Consumption</b>						
V <sub>IN</sub>	Input supply voltage range		4.5	12	13.0	V
V <sub>UVLO</sub>	Under voltage lockout	V <sub>IN</sub> : 0V to 5V		4.0	4.2	V
V <sub>UVLO_HYS</sub>	Under voltage lockout hysteresis	V <sub>IN</sub> : 5V to 0V		500		mV
I <sub>IN</sub>	Input current at power transfer mode	V <sub>IN</sub> =12V		10		mA
I <sub>STD_BY</sub>	Input current at stand-by mode (periodic ping)	V <sub>IN</sub> =12V		1		mA
I <sub>PDN</sub>	Input current at power down mode	ENB=V <sub>IN</sub> =12V		25		uA
<b>Power Amplifier and Driver</b>						
f <sub>PA</sub>	Power amplifier switching frequency		85		205	kHz
T <sub>LS_SW</sub>	Low side gate driver rising and falling times			50		ns
T <sub>HS_SW</sub>	High side gate driver rising and falling times			150		ns

$P_{OUT\_PA\_MAX}$	Power amplifier maximum output power			15		W
<b>Internal LDOs</b>						
$V_{OUT\_LDO50}$	Internal LDO50 output voltage range	$V_{IN}>5V$		5		V
$I_{OUT\_LDO50\_MAX}$	LDO50 maximum output current				20	mA
$V_{OUT\_LDO33}$	Internal LDO33 output voltage range	$V_{IN}>5V$		3.3		V
$I_{OUT\_LDO33\_MAX}$	LDO33 maximum output current				20	mA
$V_{OUT\_LDO18}$	Internal LDO18 output voltage range	$V_{IN}>5V$		1.8		V
$I_{OUT\_LDO18\_MAX}$	LDO18 maximum output current				10	mA
<b>BGR</b>						
$V_{BGR}$	Internal BGR output voltage Register programmable	$V_{IN}>3.3V$		1.22		V
<b>Internal Oscillators</b>						
$f_{OSC50K}$	Internal low speed oscillator frequency Register programmable	$V_{IN}>3.3V$		50		kHz
$f_{OSC60M}$	Internal main oscillator frequency Register programmable	$V_{IN}>3.3V$		60		MHz
<b>ADC</b>						
$N_{ADC}$	ADC resolution	$V_{IN}>3.3V$		12		bit
$f_{SAMPLE}$	ADC sampling rate	$f_{OSC60M}=60MHz$		217		kSa/s
$N_{CH\_ADC}$	ADC channel			6		
<b>Protection</b>						
$I_{OCL}$	$I_{IN}$ over current limit protection	$R_{SENSE}=20m\Omega$		2		A
$T_{OTP}$	Over temperature protection Thermal shutdown temperature	Temperature: 30°C to 160°C		150		°C
$T_{OTP\_HYS}$	OTP hysteresis	Temperature: 160°C to 30°C		20		°C
$V_{TS\_HOT}$	EXT_TS hot temperature protection threshold voltage	$V_{EXT\_TS}: 0V$ to 0.5V		0.315		V
$V_{TS\_HOT\_HYS}$	$V_{TS\_HOT}$ hysteresis	$V_{EXT\_TS}: 0.5V$ to 0V		20		mV
$V_{TS\_COLD}$	EXT_TS cold temperature protection threshold voltage	$V_{EXT\_TS}: 0.5V$ to 1.5V		0.980		V
$V_{TS\_COLD\_HYS}$	$V_{TS\_COLD}$ hysteresis	$V_{EXT\_TS}: 1.5V$ to 0.5V		80		mV

## 6. I<sup>2</sup>C Signal Timing

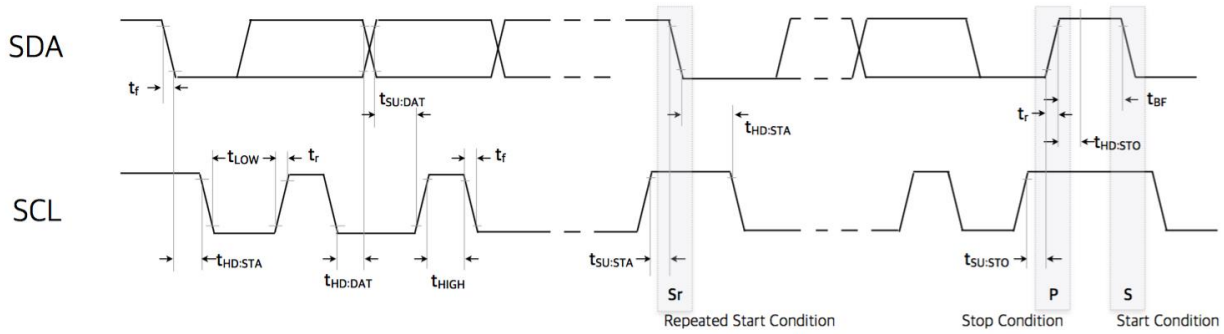


Figure 5. Timing Diagram for I<sup>2</sup>C interface

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IL\_SDA}$	Input low threshold level SDA	$V_{PULLUP}=VDD\_IO=3.3V$			0.7	V
$V_{IH\_SDA}$	Input high threshold level SDA	$V_{PULLUP}=VDD\_IO=3.3V$	2.6			V
$V_{IL\_SCL}$	Input low threshold level SCL	$V_{PULLUP}=VDD\_IO=3.3V$			0.7	V
$V_{IH\_SCL}$	Input high threshold level SCL	$V_{PULLUP}=VDD\_IO=3.3V$	2.6			V
$f_{SCL}$	SCL clock frequency				400	kHz
$t_{LOW}$	SCL clock low time		1.3			us
$t_{HIGH}$	SCL clock high time		0.6			us
$t_r$	Rise time of both SDA and SCL				0.3	us
$t_f$	Fall time of both SDA and SCL				0.3	us
$t_{SU,STA}$	Setup time for START condition		0.6			us
$t_{HD,STA}$	Hold time for START condition		0.6			us
$t_{SU,DAT}$	Data setup time		0.1			us
$t_{HD,DAT}$	Data hold time				0.9	us
$t_{SU,STO}$	Setup time for STOP condition		0.6			us
$t_{BF}$	Bus free time between STOP and START condition		1.3			us

Table 2. I<sup>2</sup>C Characteristics

## Revision History

Date	Version No.	Description
2018/10/03	0.1	Preliminary Release
2018/11/22	0.2	Initial Release
2018/12/24	1.0	Modified some-typo, officially released.

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