

CJ6101 Series

■ INTRODUCTION

The CJ6101 series are a group of positive voltage regulators manufactured by CMOS technologies with ultra low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small. The CJ6101 series can deliver 300mA output current and allow an input voltage as high as 8V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

■ APPLICATIONS

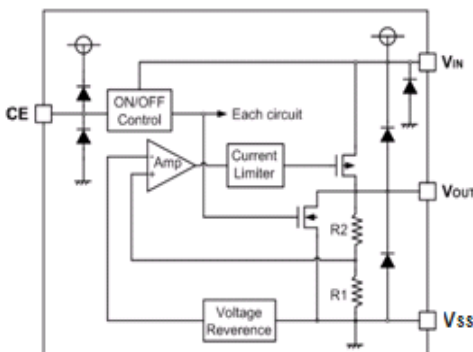
- Portable consumer equipments
- Radio control systems
- Laptop, Palmtops and PDAs

■ FEATURES

- Low Quiescent Current: 0.7 μ A
- Operating Voltage Range: 1.8V~8V
- Output Current: 300mA
- Low Dropout Voltage:
110mV@100mA($V_{OUT}=3.3V$)
- Output Voltage: 1.2~ 5.0V
- High Accuracy: $\pm 2\%/ \pm 1\%$ (Typ.)
- High Power Supply Rejection Ratio:
50dB@1kHz
- Low Output Noise:
27x V_{OUT} μ V_{RMS} (10Hz~100kHz)
- Excellent Line and Load Transient Response
- Built-in Current Limiter, Short-Circuit Protection

- Wireless Communication Equipments
- Portable Audio Video Equipments
- Ultra Low Power Microcontroller

■ BLOCK DIAGRAM



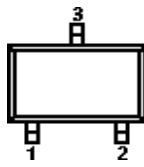
■ ORDER INFORMATION

CJ6101①②③④

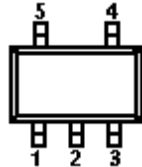
DESIGNATOR	SYMBOL	DESCRIPTION
①	A	Standard
	B	High Active, pull-down resistor built in, with C_{OUT} discharge resistor
	C	High Active, No pull-down resistor, No C_{OUT} discharge resistor
②③	Integer	Output Voltage e.g. 1.8V=②:1, ③:8
④	M	Package:SOT-23-3L/5L
	P	Package:SOT-89-3L
	F	Package:WFBFP-04C/DFNWB1x1-4

Pin Configuration

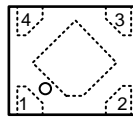
SOT-23-3L



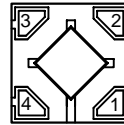
SOT-23-5L



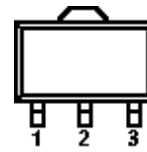
DFNWB1×1-4



WBFBP-04C



SOT-89-3L



PIN NUMBER		PIN NAME	FUNCTION
SOT-23-3L	SOT-89-3L		
M	P		
1	1	V_{SS}	Ground
2	3	V_{OUT}	Output
3	2	V_{IN}	Power input

SOT-23-5L

PIN NUMBER	SYMBOL	FUNCTION
1	V_{IN}	Power Input Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	NC	No Connection
5	V_{OUT}	Output Pin

DFNWB1×1-4/WBFBP-04C

PIN NUMBER	SYMBOL	FUNCTION
F		
1	V_{OUT}	Output Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	V_{IN}	Power Input Pin

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾ (Unless otherwise specified, $T_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage ⁽²⁾	V_{IN}	-0.3~9	V
Output Voltage ⁽²⁾	V_{OUT}	-0.3~ $V_{IN}+0.3$	V
Output Current	I_{OUT}	600	mA
Power Dissipation	SOT-23-3L/SOT-23-5L	0.3	W
	DFNWB1×1-4/WBFBP-04C	0.2	W
	SOT-89-3L	0.6	W
Operating Ambient Temperature Range	T_A	-40~+85	$^\circ\text{C}$
Operating Junction Temperature Range	T_j	-40~+125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40~+125	$^\circ\text{C}$
Soldering Temperature	T_{solder}	260, 10s	

Electrical Characteristics

Note:

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNITS
Supply voltage at V_{IN}	1.8		8	V
Operating junction temperature range, T_j	-40		125	°C
Operating free air temperature range, T_A	-40		85	°C

ELECTRICAL CHARACTERISTICS

($V_{IN}=V_{OUT}+1V$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP. ⁽³⁾	MAX.	UNITS	
Input Voltage	V_{IN}		1.8	—	8	V	
Output Voltage Range	V_{OUT}		1.2	—	5	V	
DC Output Accuracy		$I_{OUT}=1mA$	-2	—	2	%	
			-1	—	1	%	
Dropout Voltage	$V_{dif}^{(4)}$	$I_{OUT}=100mA, V_{OUT}=3.3V$	—	110	—	mV	
Supply Current	I_{SS}	I_{OUT}	0.6	0.7	1.3	μA	
		$=0$					
Standby Current	I_{STBY}	$CE=V_{SS}$			0.1	μA	
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	$I_{OUT}=10mA$ $V_{OUT}+1V \leq V_{IN} \leq 8V$	—	0.05	0.3	%/V	
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	$V_{IN}=V_{OUT}+1V$, $1mA \leq I_{OUT} \leq 100mA$	—	10	—	mV	
Temperature Coefficient	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	$I_{OUT}=10mA$, $-40^\circ C < T_A < 125^\circ C$		100		ppm	
Output Current Limit	I_{LIM}	$V_{OUT}=0.5 \times V_{OUT(Normal)}$, $V_{IN}=5V$	550	700	850	mA	
Short Current	I_{SHORT}	$V_{OUT}=V_{SS}$	—	20	—	mA	
Power Supply Rejection Ratio	PSRR	$I_{OUT}=50mA$	100Hz		70		dB
			1kHz	—	50	—	
			10kHz	—	40	—	
			100kHz	—	35	—	
Output Noise Voltage	V_{ON}	BW=10Hz to 100kHz	—	$27 \times V_{OUT}$	—	μV_{RMS}	
CE "High" Voltage	$V_{CE"H"}$		1.5		V_{IN}	V	
CE "Low" Voltage	$V_{CE"L"}$				0.3	V	

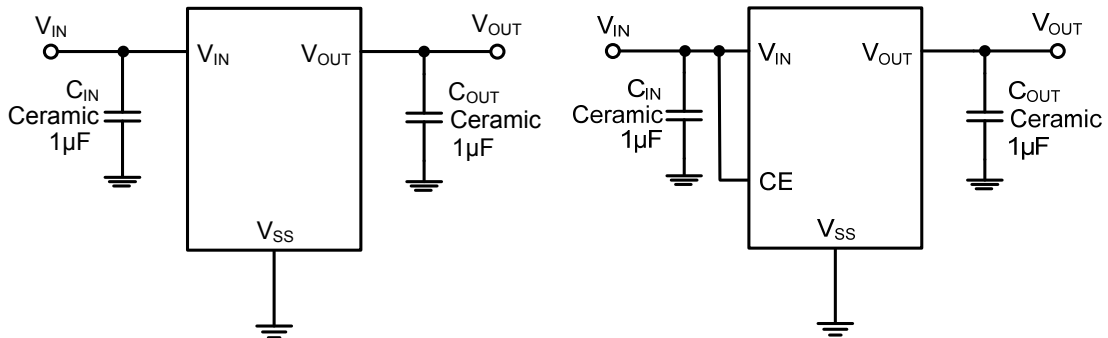
Typical Characteristics

Note:

(3) Typical numbers are at 25°C and represent the most likely norm.

(4) V_{dif} : The Difference Of Output Voltage And Input Voltage When Input Voltage Is Decreased Gradually Till Output Voltage Equals To 98% Of V_{OUT} (E).

■ TYPICAL APPLICATION CIRCUIT



■ APPLICATION INFORMATION

Selection of Input/ Output Capacitors

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current.

A recent trend in the design of portable devices has been to use ceramic capacitors to filter DC-DC converter inputs. Ceramic capacitors are often chosen because of their small size, low equivalent series resistance (ESR) and high RMS current capability. Also, recently, designers have been looking to ceramic capacitors due to shortages of tantalum capacitors.

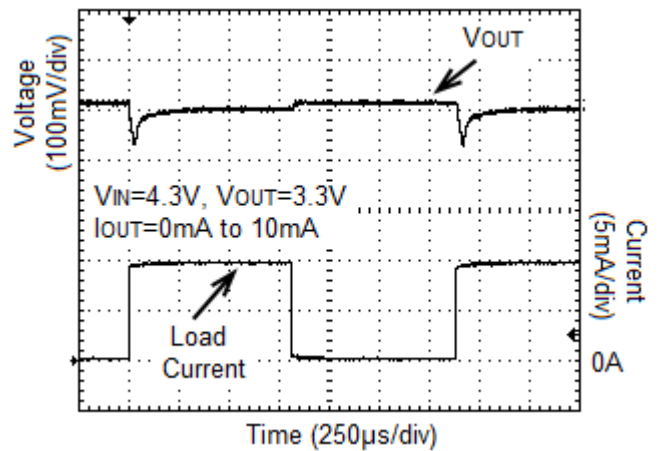
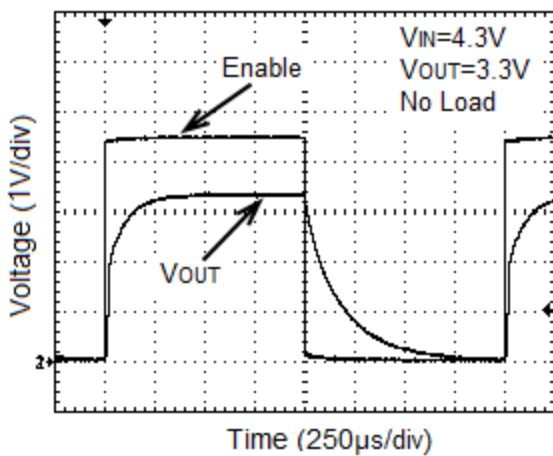
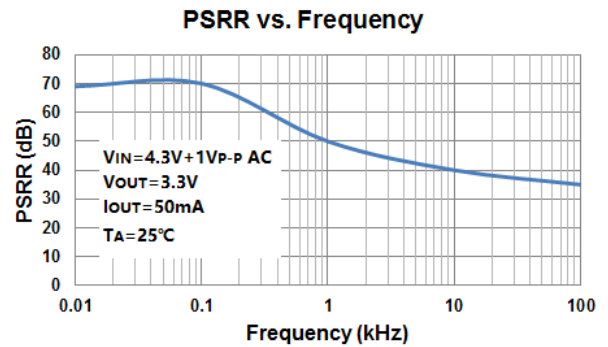
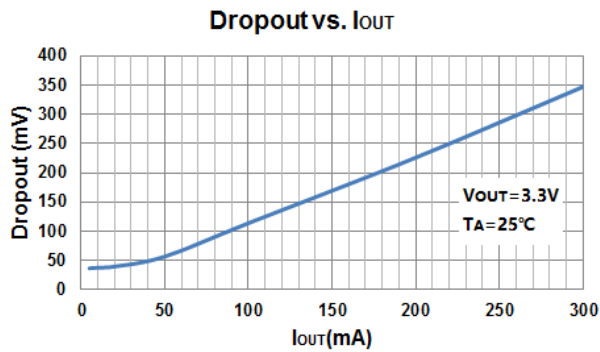
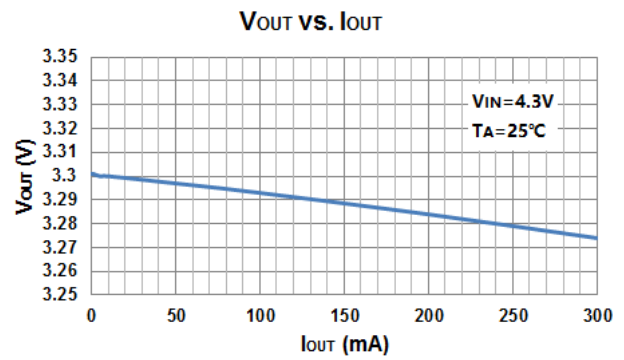
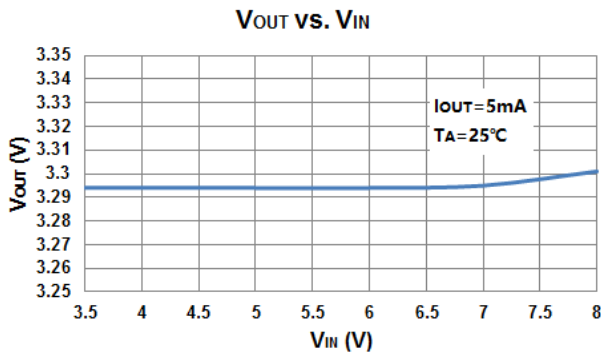
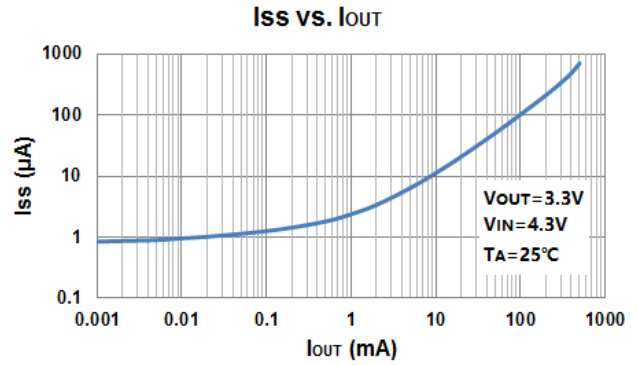
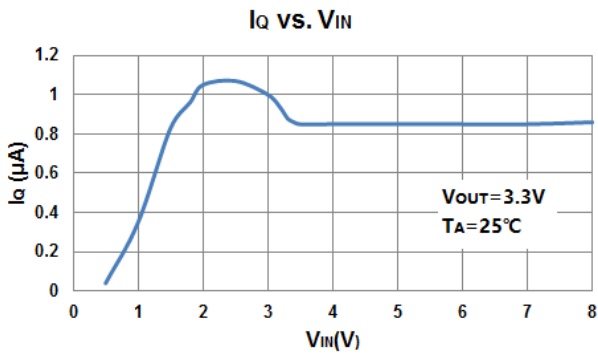
Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying a voltage step to a ceramic capacitor causes a large current surge that stores energy in the inductances of the power leads. A large voltage spike is created when the stored energy is transferred from these inductances into the ceramic capacitor. These voltage spikes can easily be twice the amplitude of the input voltage step.

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors (MLCC). Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the LDO input to a live power source. Adding a 3Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

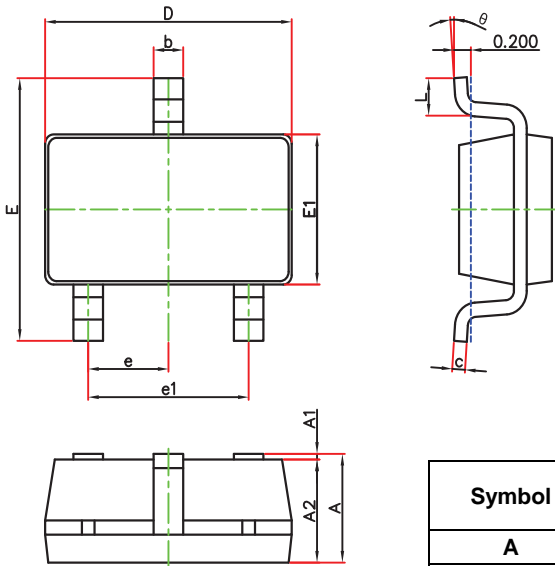
The LDO also requires an output capacitor for loop stability. Connect a 1µF tantalum capacitor from OUT to GND close to the pins. For improved transient response, this output capacitor may be ceramic.

Typical Characteristics

($V_{IN}=V_{OUT}+1V$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, unless otherwise specified)

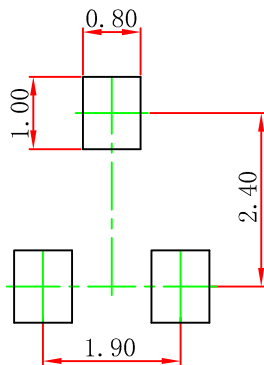


SOT-23-3L Package Outline Dimensions



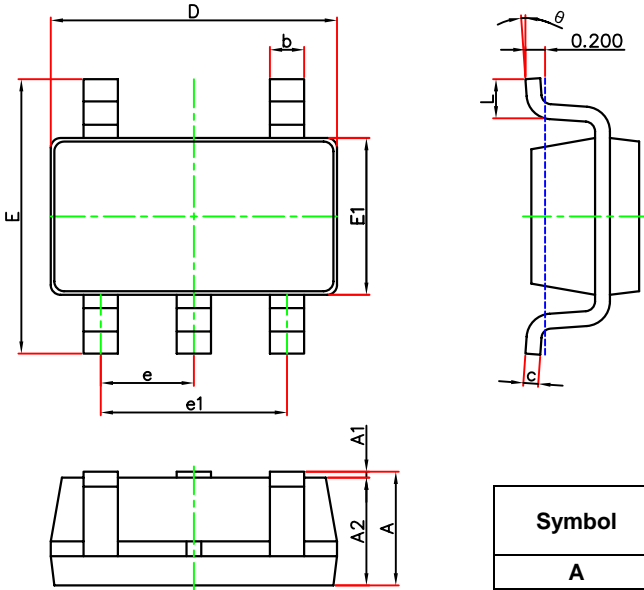
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-3L Suggested Pad Layout



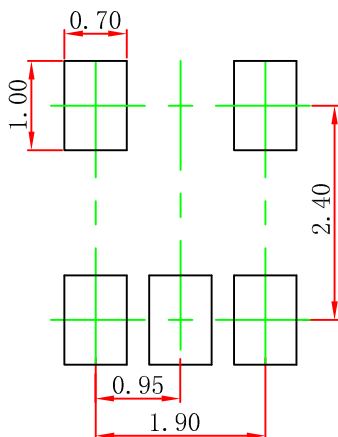
- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.

SOT-23-5L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

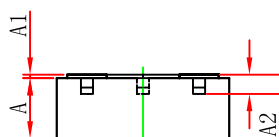
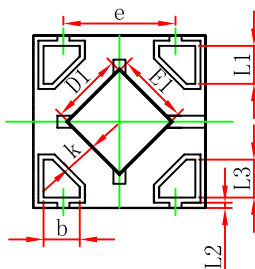
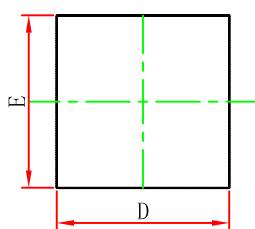
SOT-23-5L Suggested Pad Layout



Note:

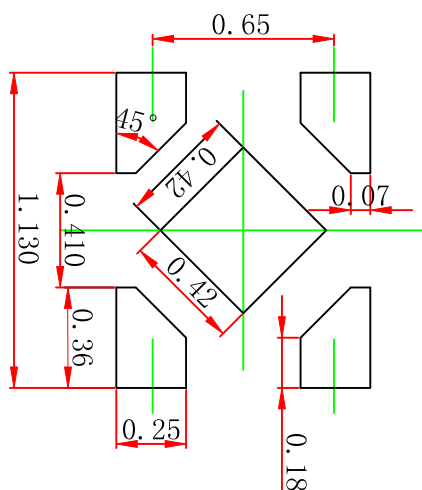
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

WBFBP-04C Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.335	0.405	0.013	0.016
D	0.950	1.050	0.037	0.041
E	0.950	1.050	0.037	0.041
D1	0.370	0.470	0.015	0.019
E1	0.370	0.470	0.015	0.019
k	0.17MIN.		0.007MIN.	
b	0.160	0.260	0.006	0.010
c	0.010	0.090	0.000	0.004
e	0.600	0.700	0.024	0.028
L1	0.185	0.255	0.007	0.010
L2	0.030 REF.		0.001 REF.	
L3	0.185	0.255	0.007	0.010

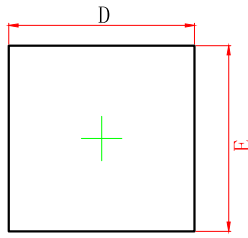
WBFBP-04C Suggested Pad Layout



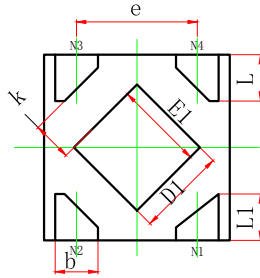
Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

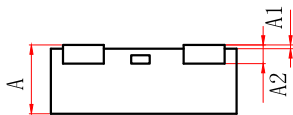
DFNWB1*1-4L Package Outline Dimensions



TOP VIEW



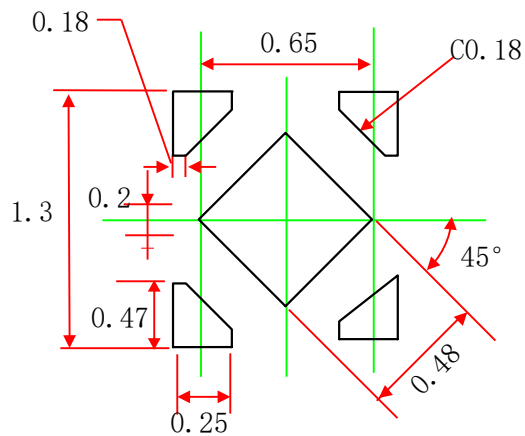
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.320	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.100 REF.		0.004 REF.	
D	0.950	1.050	0.037	0.041
E	0.950	1.050	0.037	0.041
D1	0.430	0.530	0.017	0.021
E1	0.430	0.530	0.017	0.021
k	0.150MIN.		0.006MIN.	
b	0.180	0.280	0.007	0.011
e	0.650TYP.		0.026TYP.	
L	0.200	0.300	0.008	0.012
L1	0.200	0.300	0.008	0.012

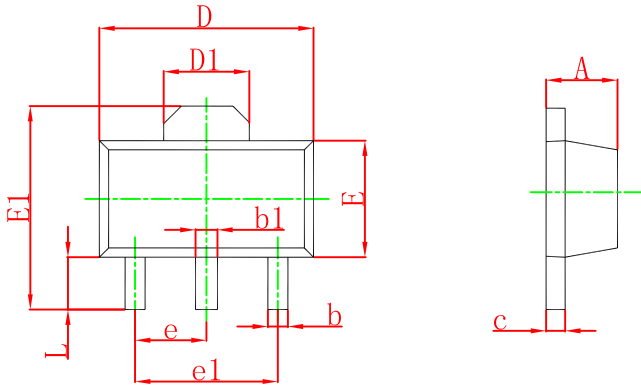
DFNWB1*1-4L Suggested Pad Layout



Note:

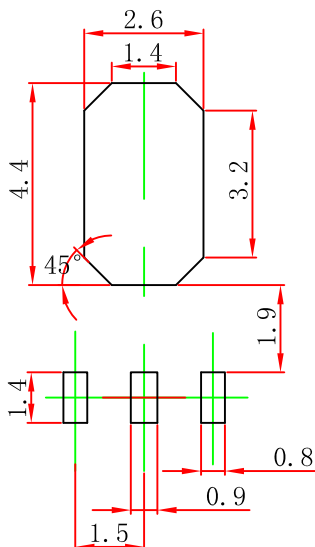
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

SOT-89-3L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF		0.061 REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP		0.060 TYP	
e1	3.000 TYP		0.118 TYP	
L	0.900	1.200	0.035	0.047

SOT-89-3L Suggested Pad Layout



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.05 mm.
 3. The pad layout is for reference purposes only.

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