ULN2003A Darlington Transistor (NPN)

1 Introduction

ULN2003A is a high voltage, high current Darlington transistor array. Each device consists of seven NPN Darlington pairs that can be output independently. These Darlington pairs have common emitter poles that support high voltage output with a common cathode clamp diode for switching inductive loads. The input and output of the clamp diode are relatively fixed to simplify the layout of the printed circuit board. The collector current of a single Darlington pair is rated at 500mA, and parallel Darlington pairs provide a higher current.

Each Darlington pair of ULN2003A devices has a 2.7kΩ series base resistance that works directly with TTL or CMOS devices. This device is often used to drive a variety of loads, such as DC engine, LED display light, high power cache and general logic circuits such as TTL, 5V CMOS, etc.

2 Available Package

PART NUMBER	PACKAGE
ULN2003A	SOP16

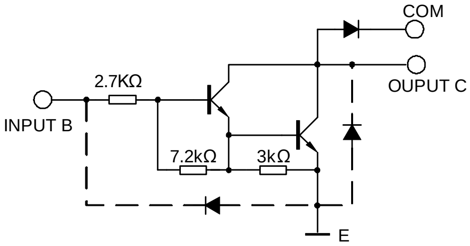


Figure 2-1. Functional Block Diagram

3 Features

- 500mA rated collector current (single output)
- High voltage output: 50V
- Output clamp diode
- Compatible with all kinds of logic input
- Relay driver application

4 Applications

- Relay Drivers
- Hammer Drivers
- Lamp Drivers
- Line Drivers
- Logic Buffers
- Stepper Motors
- IP Camera
- HVAC Valve and LED Dot Matrix

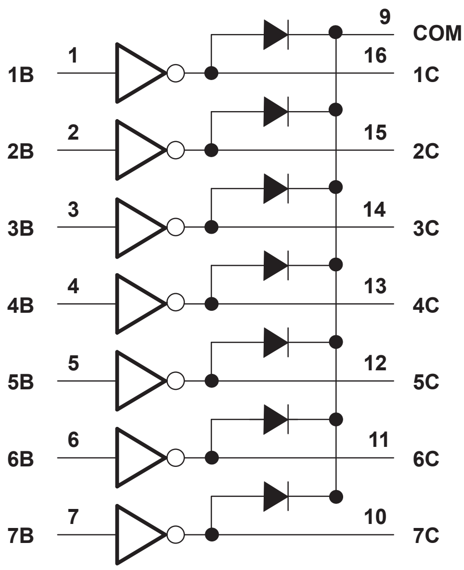


Figure 2-2. Simplified Block Diagram

5 Orderable Information

MODEL	DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
-	ULN2003A	SOP16	-40 ~ 85°C	RoHS & Green	Level 3 168 HR	Tape and Reel 2500 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

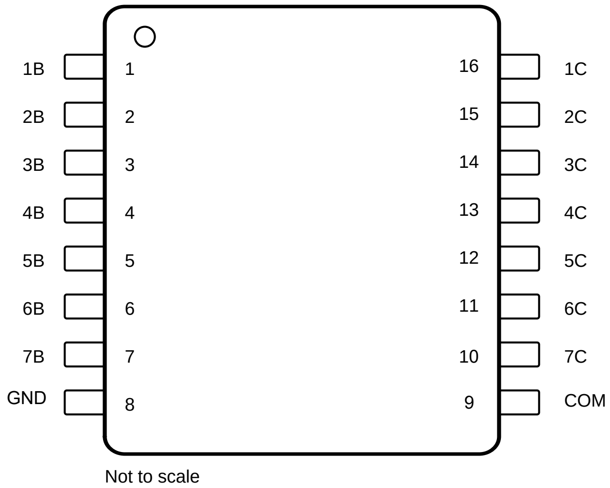
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration and Function

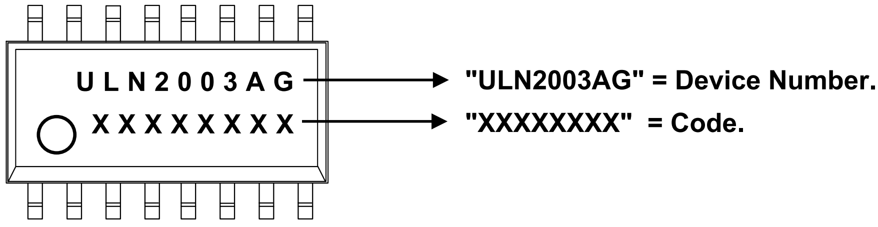
Figure 6-1. SOP16 Package Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 through 7 Darlington base input
2B	2		
3B	3		
4B	4		
5B	5		
6B	6		
7B	7		
1C	16	O	Channel 1 through 7 Darlington collector output
2C	15		
3C	14		
4C	13		
5C	12		
6C	11		
7C	10		
GND	8	—	Common emitter shared by all channels (typically tied to ground)
COM	9	I/O	Common cathode node for flyback diodes (required for inductive loads)

6.2 Marking Information



7 Specifications

7.1 Absolute Maximum Ratings(1)

at 25°C free-air temperature (unless otherwise noted)

CHARACTERISTIC		SYMBOL	VALUE	UNIT
Output voltage(2)		V_{OUT}	50	V
Input voltage(2)		V_{IN}	30	V
Collector current (peak)		I_C	500	mA
Base-terminal current		I_B	25	mA
Maximum power dissipation	SOP-18	$P_{D\ MAX}$	Internally Limited(3)	W
Maximum junction temperature		$T_{J\ MAX}$	150	°C
Storage Temperature		T_{stg}	-55 ~ 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Refer to *Thermal Information* for details.

7.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	NOM.	MAX.	UNIT
Operating junction temperature	T_J	-	-	125	°C
Operating ambient temperature	T_A	-40	-	85	°C

7.3 Thermal Information(4)

THERMAL METRIC	SYMBOL	ULN2003A SOP16 Package	UNIT
Junction-to-ambient thermal resistance	$R_{\Theta JA}$	75.2	°C/W
Reference maximum power dissipation for continuous operation	$P_{D\ Ref}$	1.33	W

(4) Test in T_A = 25°C, see *Notes* for more details.

7 Specifications

7.4 Electrical Characteristics

at 25°C free-air temperature (unless otherwise specified)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	FIGURES(5)	MIN.	TYP.(6)	MAX.	UNIT
Collector cutoff current	I_{CEX}	V_{CE} = 50V	1a	-	-	50.0	μA
Collector-emitter saturation voltage	$V_{CE (SAT)}$	I_C = 100mA, I_B = 250μA	2	-	0.9	1.1	V
		I_C = 200mA, I_B = 350μA		-	1.1	1.3	
		I_C = 350mA, I_B = 500μA		-	1.3	1.6	
Input current (ON)	$I_{IN (ON)}$	V_{IN} = 3.85V	3	-	0.93	1.35	mA
Input voltage (ON)	$V_{IN (ON)}$	V_{CE} = 2.0V, I_C = 200mA	5	-	-	2.4	V
		V_{CE} = 2.0V, I_C = 250mA		-	-	2.7	
		V_{CE} = 2.0V, I_C = 300mA		-	-	3.0	
Clamp reverse current	I_R	V_R = 50V	6	-4.0	-	50	μA
Clamp forward voltage	V_F	I_F = 350mA	7	-	1.7	2.0	V
Output leakage current	I_{CEX-1V}	V_{CE} = 50V, V_{IN} = 1.0V	1b	-5.0	-	80	μA

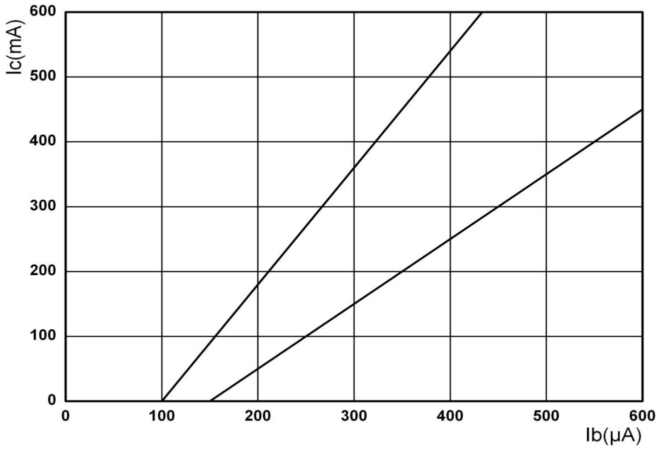
Note:

(5) Test figures. See *Parameter Measurement Information* for details.

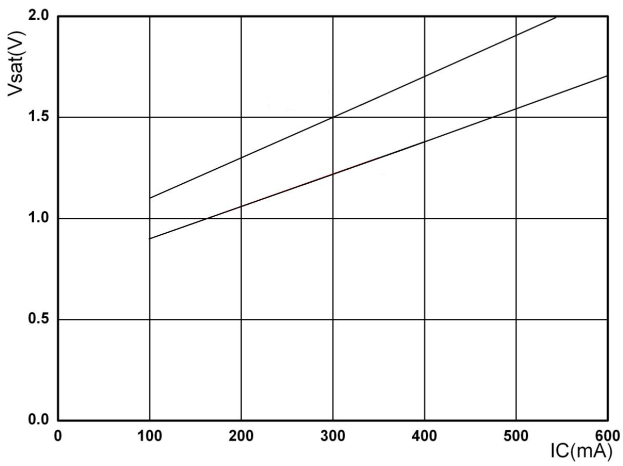
(6) Typical numbers are at 25°C and represent the most likely norm.

7.5 Typical Characteristics

Output Voltage vs. Input Current



Saturation Voltage vs. Output Voltage



8 Parameter Measurement Information

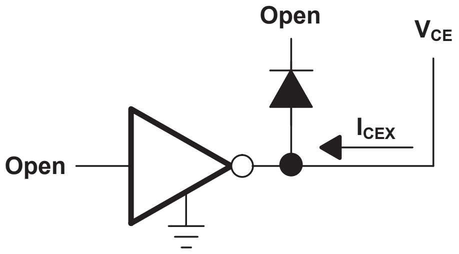


Figure 1a. I_{CEX} Test Circuit

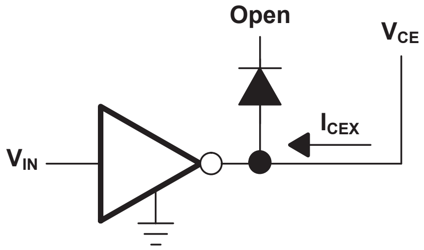


Figure 1b. I_{CEX} Test Circuit

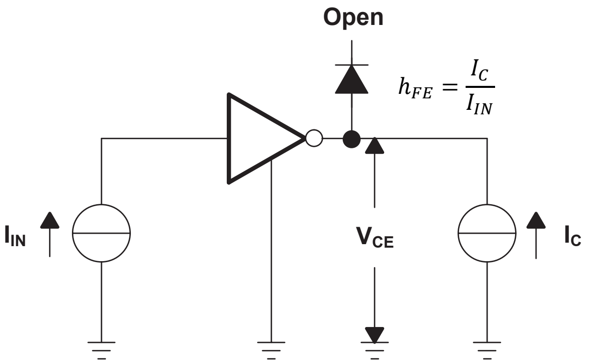


Figure 2. h_{FE}, $V_{CE\ (SAT)}$ Test Circuit

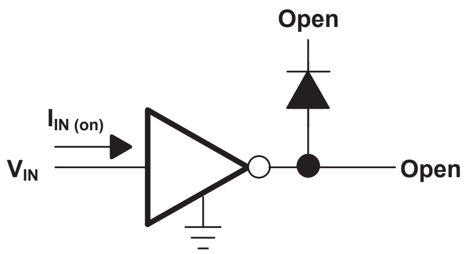
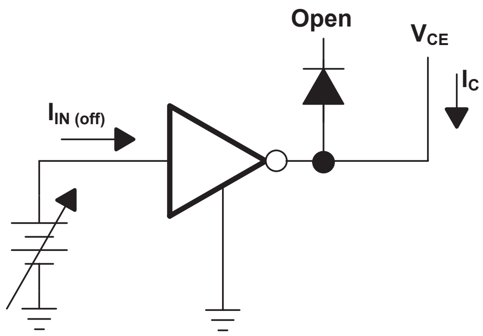


Figure 3. I_{IN} Test Circuit



I_{IN} is fixed when used to measure V_{CE} and variable when used to measure h_{FE}

Figure 4. $I_{IN\ (off)}$ Test Circuit

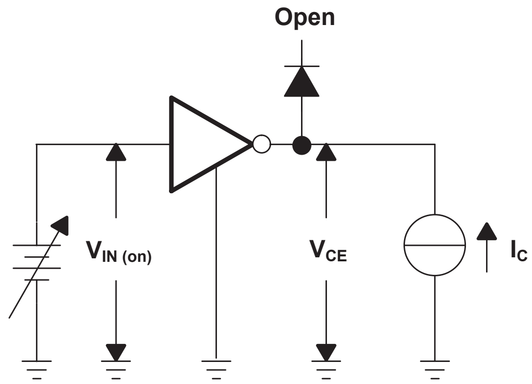


Figure 5. $V_{IN\ (on)}$ Test Circuit

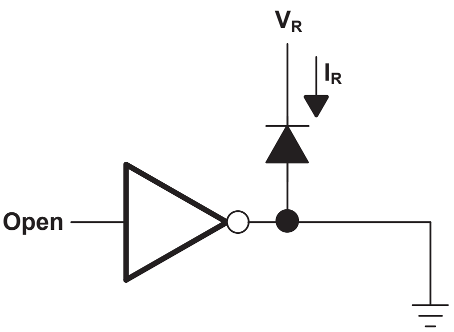


Figure 6. I_R Test Circuit

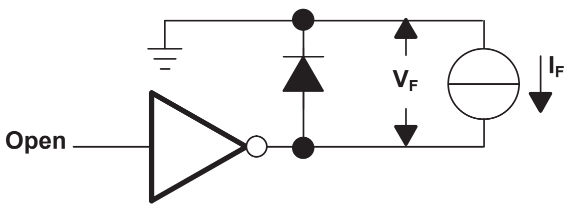
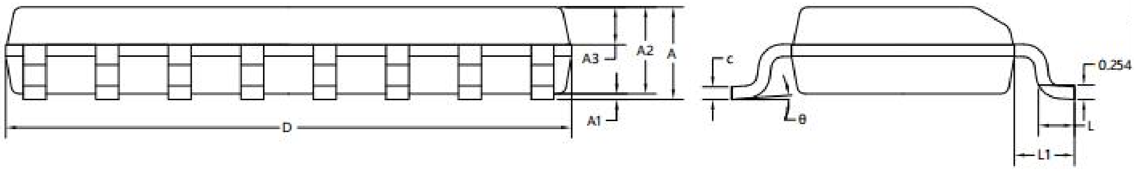
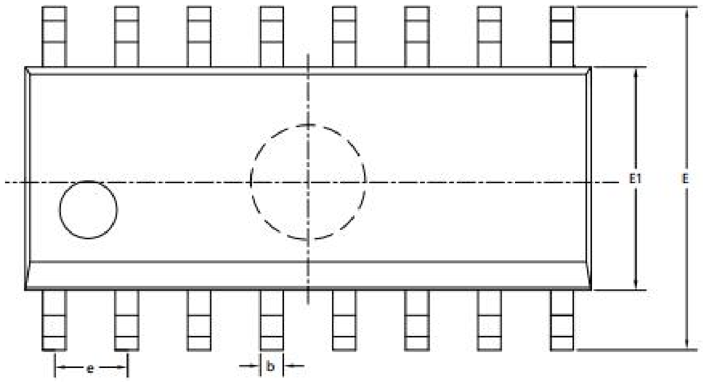


Figure 7. V_F Test Circuit

9 Mechanical Information

SOP16 Package





SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.500	1.600	1.700	0.059	0.063	0.068
A1	0.100	0.150	0.250	0.004	0.006	0.010
A2	1.400	1.450	1.500	0.055	0.057	0.059
A3	0.600	0.650	0.700	0.024	0.026	0.028
b	0.300	0.400	0.500	0.012	0.016	0.020
c	0.150	0.200	0.250	0.006	0.008	0.010
D	9.800	9.900	10.000	0.386	0.390	0.394
E	5.800	6.000	6.200	0.228	0.236	0.244
E1	3.850	3.900	3.950	0.152	0.154	0.156
e	1.270 Bsc.			0.050 Bsc.		
L	0.500	0.600	0.700	0.020	0.024	0.028
L1	1.050 Bsc.			0.041 Bsc.		
Θ	0°	4°	8°	0°	4°	8°

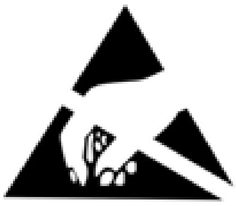
10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, please click the official website of JSCJ -- ***https: www.jscj-elec.com*** for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

Junction-to-ambient Thermal Resistance $R_{\Theta JA}$

Definition: The junction to ambient thermal resistance $R_{\Theta JA}$ is a metric of the thermal performance of the device's packages. By comparing the metric of different companies on the same product package, the thermal performance of the product can be roughly estimated in a relative sense. $R_{\Theta JA}$ is measured under the conditions specified in the corresponding specifications. If the measurement of $R_{\Theta JA}$ of two products follows different specifications and standards, or although the same specifications and standards are adopted, it is not tested in strict accordance with the specifications, then the RΘJA of two products will lose the meaning of comparison. This product follows the test specified by JEDEC in the EIA/JESD51-x series documents. $R_{\Theta JA}$ is measured in still air with T_A = 25°C and installed on a 1 in 2 FR-4 board covered with 2 ounces of copper.
Usage: Junction to ambient thermal resistance $R_{\Theta JA}$ is a parameter defined at the system level rather than on a single device or chip. In the test of $R_{\Theta JA}$ provided in the data sheet, most of the heat generated by the operation of the device is dissipated through the test board rather than the packaging surface of the device. In fact, the design and layout of PCB (such as chip or pad size, internal package geometry, etc.) will significantly affect $R_{\Theta JA}$. At this time, any calculation of the junction temperature or thermal power consumption of the device by applying $R_{\Theta JA}$ in the data sheet will have a very large error, so that it does not match the real performance of the device. Therefore, $R_{\Theta JA}$ should be used as the relative comparison of product packaging thermal performance between different companies, rather than directly using RΘJA in the data sheet in the actual calculation.

Reference Maximum Power Dissipation for Continuous Operation $P_{D\ Ref}$

The reference maximum power dissipation for continuous operation $P_{D\ Ref}$ is not an accurate value obtained from the actual test. It is a theoretical value obtained according to the heat dissipation capacity of packaging combined with practical application. It is used to compare the differences of heat dissipation capacity more intuitively between products of different companies. This value is only for estimation reference and cannot be used as an index of the actual performance of the device for circuit design.

10 Notes and Revision History

10.3 Revision History

April, 2023: changed from rev - 1.1 to rev - 1.2:

- Page 2, Orderable Inofrmation, "OP TEMP" changed from "-20 ~ 85°C" to "-40 ~ 85°C";
- Page 4, Recommend Operating Condition, "T_A" changed from "-20 ~ 85°C" to "-40 ~ 85°C".

January, 2023: changed from rev-1.0 to rev -1.1:

- Added the part "Orderable Information".
- Page 4, Absolute Maximum Ratings, Collector current changed from "(continuous)" to "(peak)".

August, 2022: released ULN2003A rev - 1.0.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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