CA-IS373x High-Speed Triple-Channel Digital Isolators

1. Key Features

- Signal Rate: DC to 150Mbps
- Wide Operating Supply Voltage: 2.5V to 5.5V
- Wide Operating Temperature Range: -40°C to 125°C
- No Start-Up Initialization Required
- Default Output High and Low Options
- High Electromagnetic Immunity
- High CMTI: ±100kV/μs (Typical)
- Low Power Consumption (Typical):
  - 1.5mA per Channel at 1Mbps with 3.3V Supply
  - 5.5mA per Channel at 100Mbps with 3.3V Supply
- Precise Timing (Typical)
  - 8ns Propagation Delay
  - 1ns Pulse Width Distortion
  - 2ns Propagation Delay Skew
  - 5ns Minimum Pulse Width
- Isolation Rating up to 5kVrms
- Isolation Barrier Life: >40 Years at Rated Working Voltage
- Tri-state Outputs with ENABLE
- Schmitt Trigger Inputs
- RoHS-Compliant Packages
  - SOIC-16 Narrow Body
  - SOIC-16 Wide Body

2. Applications

- Industrial Automation Systems
- Motor Control
- Medical Electronics
- Isolated Switch Mode Supplies
- Solar Inverters
- Isolated ADC, DAC

3. Description

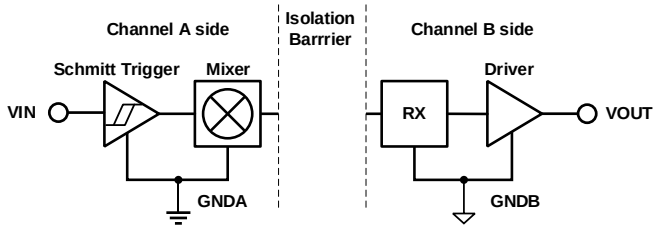
The CA-IS373x devices are high-performance triple-channel digital isolators with precise timing characteristics and low power consumption. The CA-IS373x devices provide high electromagnetic immunity and low emissions, while isolating CMOS digital I/Os. All device versions have Schmitt trigger input for high noise immunity. Each isolation channel consists of a transmitter and a receiver separated by silicon dioxide (SiO_2) insulation barrier. The CA-IS3730 device has all three channels in the same direction with output enable on output side, the CA-IS3731 device has two forward and one reverse-direction channels with output enable on both sides, and the CA-IS3735 device has the same channel configuration as CA-IS3730 without output enable. All devices have fail-safe mode option. If the input power or signal is lost, default output is low for devices with suffix L and high for devices with suffix H.

CA-IS373x devices has high insulation capability to handle noise and surge on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. High CMTI ability promises the correct transmission of digital signal. The CA-IS373x devices are available in 16-pin narrow body SOIC and 16-pin wide body SOIC packages. All products have > 2.5kVrms isolation rating, and products in wide-body packages support insulation withstanding up to 5kVrms.

Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
CA-IS3730, CA-IS3731, CA-IS3735	SOIC16-NB (N)	9.90 mm × 3.90 mm
	SOIC16-WB(W)	10.30 mm × 7.50 mm

Simplified Channel Structure



Channel A side and B side are separated by isolation capacitors. GNDA and GNDB are the isolated ground for signals and supplies of A side and B side respectively.

4. Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV)	Output Enable	Package
CA-IS3730LN	3	0	Low	2.5	Yes	NB SOIC-16
CA-IS3730LW	3	0	Low	5	Yes	WB SOIC-16
CA-IS3730HN	3	0	High	2.5	Yes	NB SOIC-16
CA-IS3730HW	3	0	High	5	Yes	WB SOIC-16
CA-IS3731LN	2	1	Low	2.5	Yes	NB SOIC-16
CA-IS3731LW	2	1	Low	5	Yes	WB SOIC-16
CA-IS3731HN	2	1	High	2.5	Yes	NB SOIC-16
CA-IS3731HW	2	1	High	5	Yes	WB SOIC-16
CA-IS3735LN	3	0	Low	2.5	No	NB SOIC-16
CA-IS3735LW	3	0	Low	5	No	WB SOIC-16
CA-IS3735HN	3	0	High	2.5	No	NB SOIC-16
CA-IS3735HW	3	0	High	5	No	WB SOIC-16

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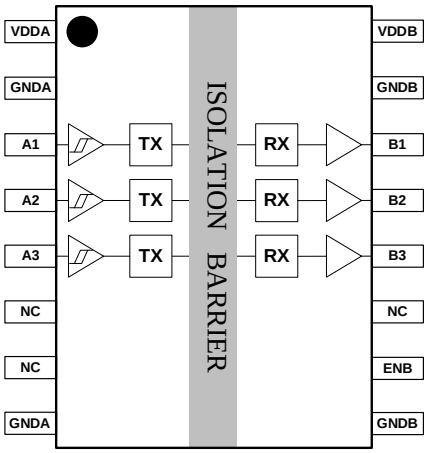
5. Revision History

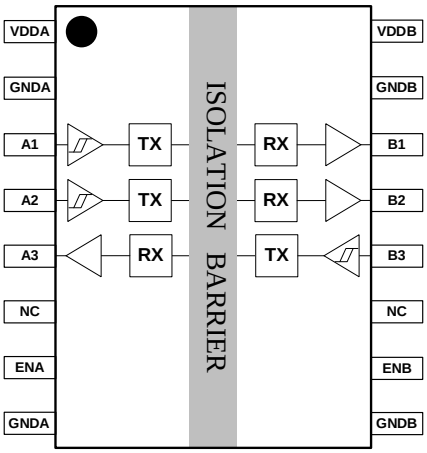
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
This is a preview version, initialized on July 23rd 2018.

6. PIN Descriptions and Functions

CA-IS3730 16-Pin SOIC NB/WB Top View



CA-IS3731 16-Pin SOIC NB/WB Top View



CA-IS3735 16-Pin SOIC NB/WB Top View

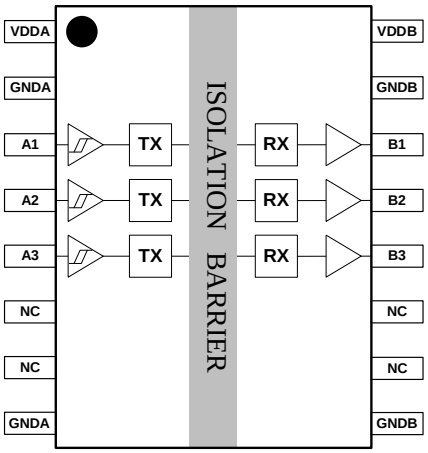


Figure 6-1 CA-IS373x Top View

Table 6-1 CA-IS373x Pin Description and Functions

Name	SOIC-16 Pin#	Type	Description
VDDA	1	Supply	Side A Power Supply
GNDA	2	Ground	Side A Ground
A1	3	Digital Input	Side A Digital Input
A2	4	Digital Input	Side A Digital Input
A3	5	Digital I/O	Side A Digital Input for CA-IS3730/35 or Output for CA-IS3731
NC	6	No Connect	No Connect
NC[1]/ENA	7	Digital Input	Side A Active High Enable. NC for CA-IS3730/35
GNDA	8	Ground	Side A Ground
GNDB	9	Ground	Side B Ground
NC[1]/ENB	10	Digital Input	Side B Active High Enable. NC for CA-IS3735
NC	11	No Connect	No Connect
B3	12	Digital I/O	Side B Digital Input for CA-IS3731 or Output for CA-IS3730/35
B2	13	Digital Output	Side B Digital Output
B1	14	Digital Output	Side B Digital Output
GNDB	15	Ground	Side B Ground
VDDB	16	Supply	Side B Power Supply

Note:

1. No Connect. These pins are not internally connected. They can be left floating, tied to VDD or tied to GND

7. Specifications

7.1. Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Supply Voltage[2]	-0.5	6.0	V
V_{in}	Voltage at Ax, Bx, ENx	-0.5	V_{DDA}+0.5[3]	V
I_O	Output Current	15	15	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 6 V.

7.2. ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	200	

NOTE:

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3. Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{DDA}, V_{DDB}	Supply Voltage		2.375	3.3	5.5	V
$V_{DD\ (UVLO+)}$	VDD Undervoltage Threshold When Supply Voltage is Rising		1.95	2.24	2.375	V
$V_{DD\ (UVLO-)}$	VDD Undervoltage Threshold When Supply Voltage is Falling		1.88	2.16	2.325	V
$V_{HYS\ (UVLO)}$	VDD Undervoltage Threshold Hysteresis		50	70	95	mV
I_{OH}	High-level Output Current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO} = 3.3V	-2			
		V_{DDO} = 2.5V	-1			
I_{OL}	Low-level Output Current	V_{DDO} = 5V			4	mA
		V_{DDO} = 3.3V			2	
		V_{DDO} = 2.5V			2	
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
DR	Data Rate		0		150	Mbps
T_A	Ambient Temperature		-40	27	125	°C

NOTE:

1. V_{DDO} = Output-side V_{DD}

7.4. Thermal Information

THERMAL METRIC[1]		CA-IS373x		UNIT
		N (SOIC)	W (SOIC)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance			°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance			°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance			°C/W
ψ_{JT}	Junction-to-top characterization parameter			°C/W
ψ_{JB}	Junction-to-board characterization parameter			°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance			°C/W

7.5. Power Rating

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CA-IS3730/35						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave			150	mW
P_{DA}	Maximum Power Dissipation on Side-A				25	mW
P_{DB}	Maximum Power Dissipation on Side-B				125	mW
CA-IS3731						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75-MHz 50% duty cycle square wave			150	mW
P_{DA}	Maximum Power Dissipation on Side-A				50	mW
P_{DB}	Maximum Power Dissipation on Side-B				100	mW

7.6. Electrical Characteristics

7.6.1. V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; *See Figure 8-2*	V_{DDO}[1]-0.4	4.8		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; *See Figure 8-2*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.38	0.44	0.5	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at Ax or Bx or ENx			10	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-10			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; *See Figure 8-4*	85	100		kV/µS
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 5 V		2		pF

NOTE:

1. V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%.
3. Measured from pin to Ground.

7.6.2. V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; *See Figure 8-2*	V_{DDO}[1]-0.4	3.1		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; *See Figure 8-2*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.38	0.44	0.5	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at Ax or Bx or ENx			10	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-10			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; *See Figure 8-4*	85	100		kV/µs
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 3.3 V		2		pF

NOTE:

1. V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%.
3. Measured from pin to Ground.

7.6.3. V_{DDA} = V_{DDB} = 2.5 V ± 5%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level Output Voltage	I_{OH} = -4mA; *See Figure 8-2*	V_{DDO}[1]-0.4	2.3		V
V_{OL}	Low-level Output Voltage	I_{OL} = 4mA; *See Figure 8-2*		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going Input Threshold		1.4	1.67	1.9	V
$V_{IT-(IN)}$	Negative-going Input Threshold		1.0	1.23	1.4	V
$V_{I(HYS)}$	Input Threshold Hysteresis		0.38	0.44	0.5	V
I_{IH}	High-Level Input Leakage Current	V_{IH} = V_{DDA} at Ax or Bx or ENx			10	µA
I_{IL}	Low-Level Input Leakage Current	V_{IL} = 0 V at Ax or Bx	-10			µA
Z_O	Output Impedance[2]			50		Ω
CMTI	Common-mode Transient Immunity	V_I = V_{DDI}[1] or 0 V, V_{CM} = 1200 V; *See Figure 8-4*	85	100		kV/µS
C_I	Input Capacitance[3]	V_I = V_{DD}/ 2 + 0.4×sin(2πft), f = 1 MHz, V_{DD} = 2.5 V		2		pF

NOTE:

1. V_{DDI} = Input-side V_{DD}, V_{DDO} = Output-side V_{DD}
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%.
3. Measured from pin to Ground.

7.7. Supply Current Characteristics

7.7.1. V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3730/35							
Supply Current – Disable[1]	ENB[2] = 0 V; V_{IN} = 0V (CA-IS3730L); V_{IN} = V_{DDA} (CA-IS3730H)		I_{DDA}		0.9	1.6	mA
			I_{DDB}		1.9	3.0	
	ENB = 0 V; V_{IN} = V_{DDA} (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		4.6	7.4	
			I_{DDB}		1.9	3.0	
Supply Current – DC Signal	ENB = V_{DDB}; V_{IN} = 0V (CA-IS3730/45L); V_{IN} = V_{DDA} (CA-IS3730/45H)		I_{DDA}		0.9	1.6	
			I_{DDB}		1.9	3.0	
	ENB = V_{DDB}; V_{IN} = V_{DDA} (CA-IS3730/45L); V_{IN} = 0V(CA-IS3730/45H)		I_{DDA}		4.6	7.4	
			I_{DDB}		1.9	3.0	
Supply Current – AC Signal	ENB = V_{DDB}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		2.2	3.1	
		10Mbps (5MHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		3.1	4.3	
		100Mbps (50MHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		13.2	17.8	
CA-IS3731							
Supply Current – Disable	ENA = ENB = 0 V; V_{IN} = 0V (CA-IS3731L); V_{IN} = V_{DDI}[1] (CA-IS3731H)		I_{DDA}		1.3	2.1	mA
			I_{DDB}		1.7	2.7	
	ENA = ENB = 0 V; V_{IN} = V_{DDI} (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		3.9	5.9	
			I_{DDB}		3.0	4.5	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3731L); V_{IN} = V_{DDI} (CA-IS3731H)		I_{DDA}		1.3	2.1	
			I_{DDB}		1.7	2.7	
	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI} (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		3.9	5.9	
			I_{DDB}		3.0	4.5	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		2.7	3.8	
			I_{DDB}		2.6	3.6	
		10Mbps (5MHz)	I_{DDA}		3.0	4.2	
			I_{DDB}		3.1	4.4	
		100Mbps (50MHz)	I_{DDA}		6.6	8.8	
			I_{DDB}		9.9	13.4	

Note:

1. CA-IS3735 device has no disable state.
2. CA-IS3735 device doesn't have ENB pin but NC pin instead.
3. V_{DDI} = Input-side V_{DD}

7.7.2. $V_{DDA} = V_{DDB} = 3.3\ V \pm 10\%$, T_A = -40 to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3730/35							
Supply Current – Disable[1]	ENB[2] = 0 V; V_{IN} = 0V (CA-IS3730L); $V_{IN} = V_{DDA}$ (CA-IS3730H)		I_{DDA}		0.9	1.6	mA
			I_{DDB}		1.9	3.0	
	ENB = 0 V; $V_{IN} = V_{DDA}$ (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		4.6	7.4	
			I_{DDB}		1.9	3.0	
Supply Current – DC Signal	ENB = V_{DDB}; V_{IN} = 0V (CA-IS3730/45L); $V_{IN} = V_{DDA}$ (CA-IS3730/45H)		I_{DDA}		0.9	1.6	
			I_{DDB}		1.9	3.0	
	ENB = V_{DDB}; $V_{IN} = V_{DDA}$ (CA-IS3730/45L); V_{IN} = 0V(CA-IS3730/45H)		I_{DDA}		4.6	7.4	
			I_{DDB}		1.9	3.0	
Supply Current – AC Signal	ENB = V_{DDB}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		2.2	3.1	
		10Mbps (5MHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		2.6	3.6	
		100Mbps (50MHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		9.3	12.5	
CA-IS3731							
Supply Current – Disable	ENA = ENB = 0 V; V_{IN} = 0V (CA-IS3731L); $V_{IN} = V_{DDI}$[1] (CA-IS3731H)		I_{DDA}		1.3	2.1	mA
			I_{DDB}		1.7	2.7	
	ENA = ENB = 0 V; $V_{IN} = V_{DDI}$ (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		3.9	5.9	
			I_{DDB}		3.0	4.5	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3731L); $V_{IN} = V_{DDI}$ (CA-IS3731H)		I_{DDA}		1.3	2.1	
			I_{DDB}		1.7	2.7	
	ENA = ENB = V_{DDI}; $V_{IN} = V_{DDI}$ (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		3.9	5.9	
			I_{DDB}		3.0	4.5	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		2.7	3.8	
			I_{DDB}		2.6	3.6	
		10Mbps (5MHz)	I_{DDA}		2.8	4.0	
			I_{DDB}		2.6	3.9	
		100Mbps (50MHz)	I_{DDA}		5.0	7.0	
			I_{DDB}		7.3	9.8	

Note:

1. CA-IS3735 device has no disable state.
2. CA-IS3735 device doesn't have ENB pin but NC pin instead.
3. V_{DDI} = Input-side V_{DD}

7.7.3. V_{DDA} = V_{DDB} = 2.5 V ± 5%, T_A = -40 to 125°C

PARAMETER	TEST CONDITION		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
CA-IS3730/35							
Supply Current – Disable[1]	ENB[2] = 0 V; V_{IN} = 0V (CA-IS3730L); V_{IN} = V_{DDA} (CA-IS3730H)		I_{DDA}		0.9	1.6	mA
			I_{DDB}		1.9	3.0	
	ENB = 0 V; V_{IN} = V_{DDA} (CA-IS3730L); V_{IN} = 0V(CA-IS3730H)		I_{DDA}		4.6	7.4	
			I_{DDB}		1.9	3.0	
Supply Current – DC Signal	ENB = V_{DDB}; V_{IN} = 0V (CA-IS3730/45L); V_{IN} = V_{DDA} (CA-IS3730/45H)		I_{DDA}		0.9	1.6	
			I_{DDB}		1.9	3.0	
	ENB = V_{DDB}; V_{IN} = V_{DDA} (CA-IS3730/45L); V_{IN} = 0V(CA-IS3730/45H)		I_{DDA}		4.6	7.4	
			I_{DDB}		1.9	3.0	
Supply Current – AC Signal	ENB = V_{DDB}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		2.2	3.1	
		10Mbps (5MHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		2.4	3.3	
		100Mbps (50MHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		7.5	10.1	
CA-IS3731							
Supply Current – Disable	ENA = ENB = 0 V; V_{IN} = 0V (CA-IS3731L); V_{IN} = V_{DDI}[1] (CA-IS3731H)		I_{DDA}		1.3	2.1	mA
			I_{DDB}		1.7	2.7	
	ENA = ENB = 0 V; V_{IN} = V_{DDI} (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		3.9	5.9	
			I_{DDB}		3.0	4.5	
Supply Current – DC Signal	ENA = ENB = V_{DDI}; V_{IN} = 0V (CA-IS3731L); V_{IN} = V_{DDI} (CA-IS3731H)		I_{DDA}		1.3	2.1	
			I_{DDB}		1.7	2.7	
	ENA = ENB = V_{DDI}; V_{IN} = V_{DDI} (CA-IS3731L); V_{IN} = 0V(CA-IS3731H)		I_{DDA}		3.9	5.9	
			I_{DDB}		3.0	4.5	
Supply Current – AC Signal	ENA = ENB = V_{DDI}; All Channels Switching with 50% Duty Cycle Square Wave Clock Input with 5V Amplitude; C_L = 15 pF for Each Channel	1Mbps (500kHz)	I_{DDA}		2.7	3.8	
			I_{DDB}		2.6	3.6	
		10Mbps (5MHz)	I_{DDA}		2.8	3.9	
			I_{DDB}		2.7	3.7	
		100Mbps (50MHz)	I_{DDA}		4.5	6.1	
			I_{DDB}		6.1	8.2	

Note:

1. CA-IS3735 device has no disable state.
2. CA-IS3735 device doesn't have ENB pin but NC pin instead.
3. V_{DDI} = Input-side V_{DD}

7.8. Timing Characteristics

7.8.1. V_{DDA} = V_{DDB} = 5 V ± 10%, T_A = -40 to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate			0		150	Mbps
PW_{min}	Minimum Pulse Width					5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time		*See Figure 8-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$		*See Figure 8-1*		0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]		Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]		*See Figure 8-1*		2.0	4.5	ns
t_r	Output Signal Rise Time		*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time		*See Figure 8-1*		2.5	4.0	ns
$t_{JIT(PK)}$	Peak Eye Diagram Jitter				350		ps
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output		*See Figure 8-2*		8	12	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output		*See Figure 8-2*		8	12	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output	CA-IS373xL	*See Figure 8-2*		6	11	ns
		CA-IS373xH	*See Figure 8-2*				ns
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output	CA-IS373xL	*See Figure 8-2*				ns
		CA-IS373xH	*See Figure 8-2*		6	11	ns
t_{DO}	Default Output Delay Time from Input Power Loss		*See Figure 8-3*		8	12	ns
t_{ie}	Time interval error		2^{16} – 1 PRBS 100Mbps data		0.7		ns
t_{SU}	Start-up Time				15	40	µs

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.8.2. V_{DDA} = V_{DDB} = 3.3 V ± 10%, T_A = -40 to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate			0		150	Mbps
PW_{min}	Minimum Pulse Width					5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time		*See Figure 8-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$		*See Figure 8-1*		0.2	4.5	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]		Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]		*See Figure 8-1*		2.0	4.5	ns
t_r	Output Signal Rise Time		*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time		*See Figure 8-1*		2.5	4.0	ns
$t_{JIT(PK)}$	Peak Eye Diagram Jitter				350		ps
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output		*See Figure 8-2*		8	12	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output		*See Figure 8-2*		8	12	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output	CA-IS373xL	*See Figure 8-2*		6	11	ns
		CA-IS373xH	*See Figure 8-2*				ns
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output	CA-IS373xL	*See Figure 8-2*				ns
		CA-IS373xH	*See Figure 8-2*		6	11	ns
t_{DO}	Default Output Delay Time from Input Power Loss		*See Figure 8-3*		8	12	ns
t_{ie}	Time interval error		2^{16} – 1 PRBS 100Mbps data		0.7		ns
t_{SU}	Start-up Time				15	40	µs

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

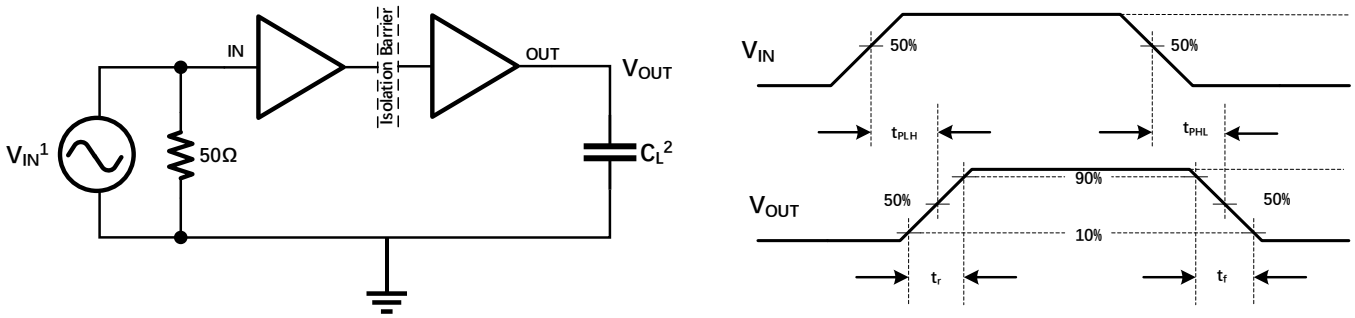
7.8.3. V_{DDA} = V_{DDB} = 2.5 V ± 5%, T_A = -40 to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data Rate			0		150	Mbps
PW_{min}	Minimum Pulse Width					5.0	ns
t_{PLH}, t_{PHL}	Propagation Delay Time		*See Figure 8-1*	5.0	8.0	13.0	ns
PWD	Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$				0.2	5.0	ns
$t_{sk(o)}$	Channel-to-channel Output Skew Time[1]		Same-direction channels		0.4	2.5	ns
$t_{sk(pp)}$	Part-to-part Skew Time[2]		*See Figure 8-1*		2.0	5.0	ns
t_r	Output Signal Rise Time		*See Figure 8-1*		2.5	4.0	ns
t_f	Output Signal Fall Time		*See Figure 8-1*		2.5	4.0	ns
$t_{JIT(PK)}$	Peak Eye Diagram Jitter				350		ps
t_{PHZ}	Disable Propagation Delay, High to High Impedance Output		*See Figure 8-2*		8	12	ns
t_{PLZ}	Disable Propagation Delay, Low to High Impedance Output				8	12	ns
t_{PZH}	Enable Propagation Delay, High Impedance to High Output	CA-IS373xL			6	11	ns
		CA-IS373xH					ns
t_{PZL}	Enable Propagation Delay, High Impedance to Low Output	CA-IS373xL					ns
		CA-IS373xH			6	11	ns
t_{DO}	Default Output Delay Time from Input Power Loss		*See Figure 8-3*		8	12	ns
t_{ie}	Time interval error		2^{16} – 1 PRBS 100Mbps data		0.7		ns
t_{SU}	Start-up Time				15	40	µs

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

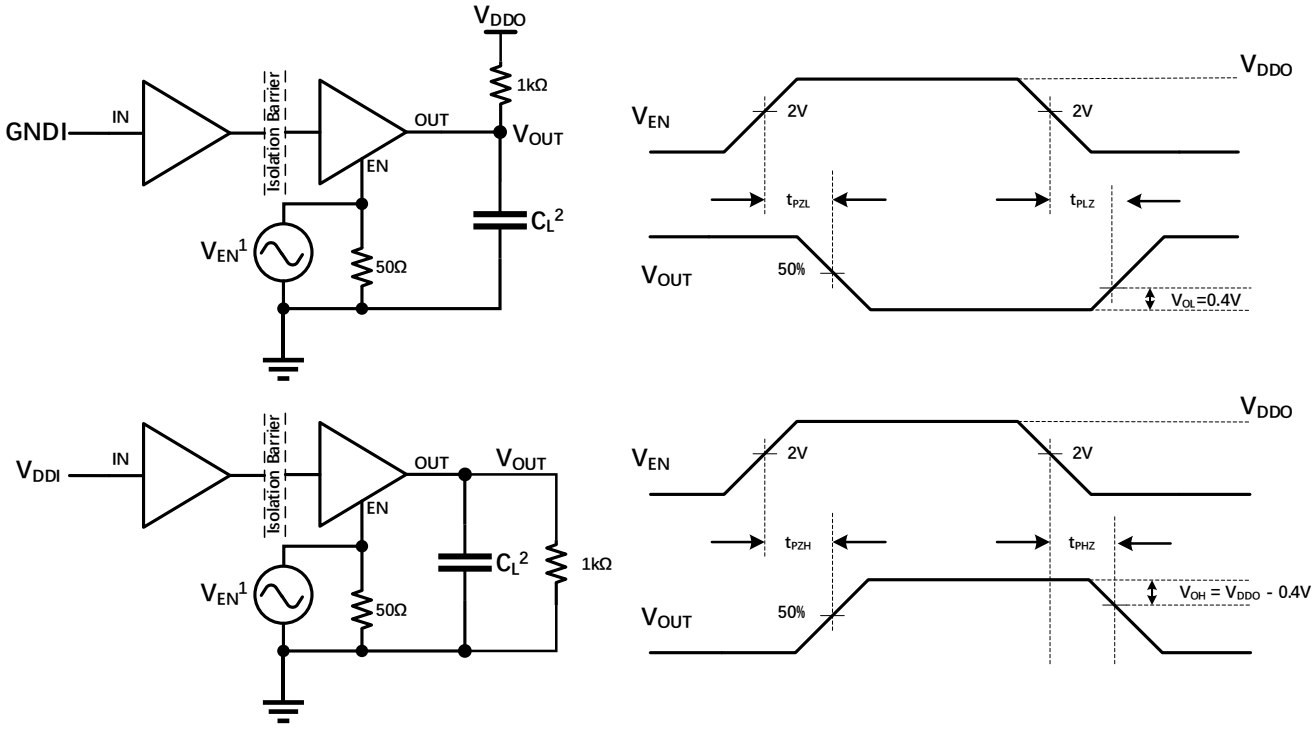
8. Parameter Measurement Information



NOTE:

1. A square wave generator generate the V_{IN} input signal with the following constraints: waveform frequency ⩽ 100kHz, 50% duty cycle, t_r⩽3ns, t_f⩽3ns. Since the waveform generator has an output impedance of Z_{out} = 50Ω, the 50Ω resistor in the figure is used for matching. There is no need in the actual application.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

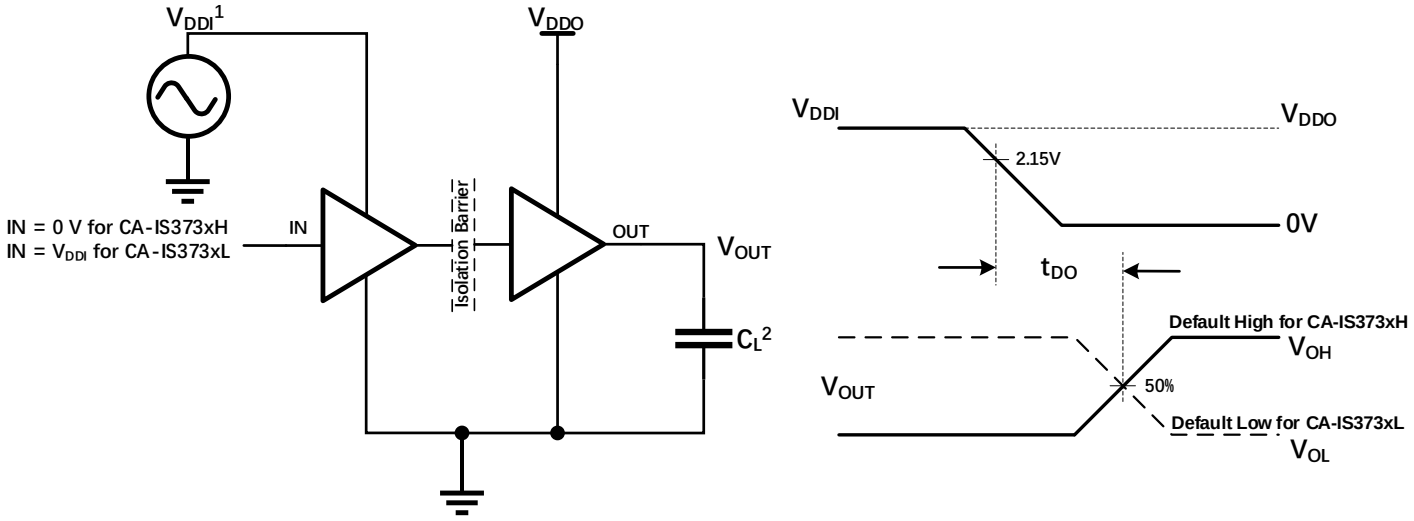
Figure 8-1 Timing Characteristics Test Circuit and Voltage Waveforms



NOTE:

1. A square wave generator generate the V_{EN} input signal with the following constraints: waveform frequency ⩽ 100kHz, 50% duty cycle, t_r⩽3ns, t_f⩽3ns. Since the waveform generator has an output impedance of Z_{out} = 50Ω, the 50Ω resistor in the figure is used for matching. There is no need in the actual application.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

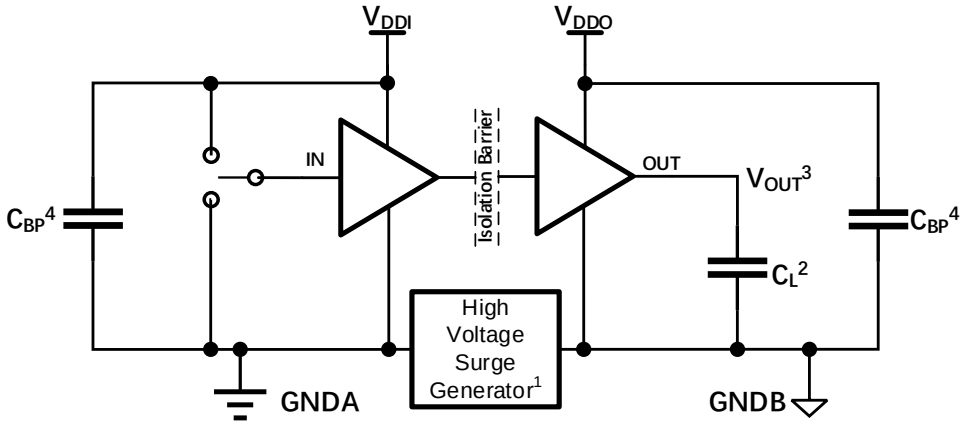
Figure 8-2 Enable/Disable Propagation Delay Time Test Circuit and Waveform



NOTE:

1. Power Supply Ramp Rate = 10 mV/ns. V_{DDI} should ramp over 2.15V but no higher than 5.5V.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-3 Default Output Delay Time Test Circuit and Voltage Waveforms



NOTE:

1. The High Voltage Surge Generator generates repetitive high voltage surges with > 1kV amplitude and <10ns rise time and fall time to reach common-mode transient noise with > 100kV/μs slew rate.
2. C_L is the load capacitance about 15pF together with the instrumentation capacitance.
3. Pass-fail criteria: The output must remain stable whenever the high voltage surges come.
4. C_{BP} is the 0.1 ~ 1uF bypass capacitance.

Figure 8-4 Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Theory of Operation

The CA-IS373x family of devices use a simple ON-OFF keying (OOK) modulation scheme to transmit signal across the SiO_2 isolation capacitors that provide a robust insulation between two different voltage domain and act as a high frequency signal path between the input and the output. The transmitter (TX) modulates the input signal onto the carrier frequency, that is, TX delivers high frequency signal across the isolation barrier in one input state and delivers no signal across the barrier in the other input state. Then the receiver rebuilds the input signal according to the detected in-band energy. If the ENx pin is low then the output goes to high impedance state and will be pulled up to V_{DDO} (CA-IS373xH) or pull down to the corresponding GND (CA-IS373xL). This simple architecture offers a robust isolated data path and requires no special considerations or initialization at start-up. The capacitor-based signal path is fully differential to maximize noise immunity, which is also known as common-mode transient immunity. Advanced circuitry techniques are applied for better EMI introduced by the carrier signal and IO switching. The capacitively-coupled architecture provides much higher electromagnetic immunity compared to the inductively-coupled one. And OOK modulation scheme eliminates the missing-pulse error that occurs in the pulse modulation method. A simplified functional block diagram and conceptual operation waveforms of a single channel is shown in Figure 9-1 and Figure 9-2.

9.2. Functional Block Diagram

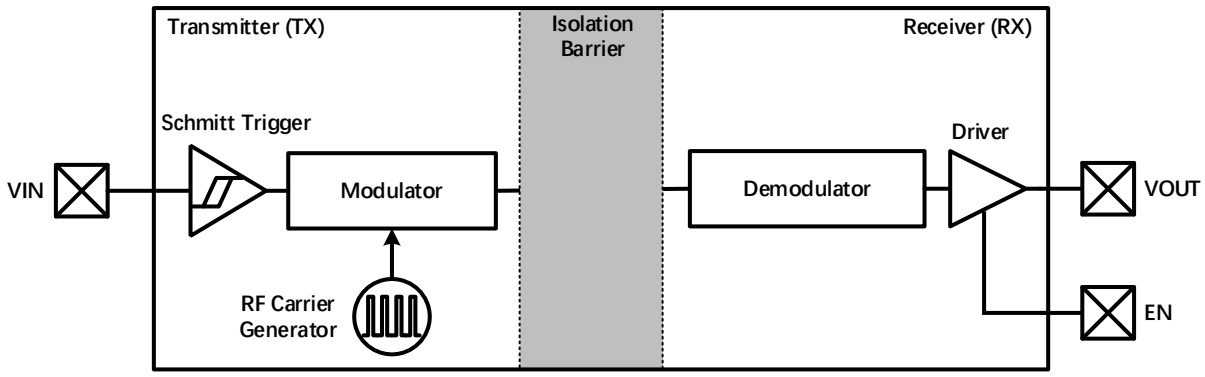


Figure 9-1 Functional Block Diagram of a Single Channel

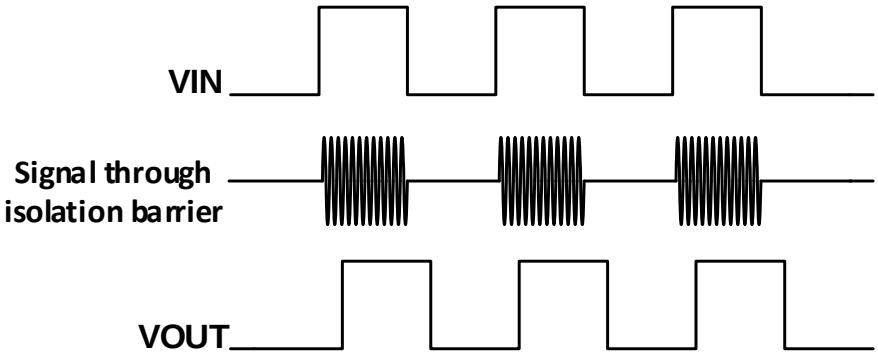


Figure 9-2 Conceptual Operation Waveforms of a Single Channel

9.3. Device Operation Modes

Table 9-1 provides the operation modes for the CA-IS373x devices.

Table 9-1 Operation Mode Table[1]

V_{DDI}	V_{DDO}	INPUT(Ax/Bx)[2]	OUTPUT ENABLE(ENx)[3,4]	OUTPUT (Ax/Bx)	OPERATION
PU	PU	H	H or Open	H	Normal operation mode: A channel's output follows the input state
		L	H or Open	L	
		Open	H or Open	Default	Default output fail-safe mode: If a channel's input is left open, its output goes to the default value (Low for CA-IS373xL and High for CA-IS373xH).
X	PU	X	L	Z	High impedance mode: If Enable pin is tied to low, the output will be in high-Z mode
PD	PU	X	H or Open	Default	Default output fail-safe mode: If the input side VDD is unpowered, the outputs go in to the default output fail-safe mode (Low for CA-IS373xL and High for CA-IS373xH)
X	PD	X	X	Undetermined	If the output side VDD is unpowered, the outputs' states are undetermined.[5]

NOTE:

1. V_{DDI} = Input-side V_{DD}; V_{DDO} = Output-side V_{DD}; PU = Powered up (VCC ⩾ 2.375 V); PD = Powered down (VCC ⩽ 2.25 V); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.
2. A strongly driven input signal can weakly power the floating V_{DD} through an internal protection diode and cause undetermined output.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the CA-IS373x is operating in noisy environments.
4. No Connect (NC) replaces ENA on CA-IS3730/45. No Connect replaces EN2 on the CA-IS3735. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. The outputs are in undetermined state when 2.25V < V_{DDI}, V_{DDO} < 2.375 V.

Table 9-2 provides the Enable input truth table for the CA-IS373x devices.

Table 9-2 Enable Input Truth Table

PART NUMBER	ENA[1,2]	ENB[1,2]	OPERATION
CA-IS3730	—	H	Outputs B1, B2, B3, B4 are enabled and follow the input state.
	—	L	Outputs B1, B2, B3, B4 are disabled and in high impedance state.
CA-IS3731	H	X	Output A4 enabled and follows the input state.
	L	X	Output A4 disabled and in high impedance state.
	X	H	Outputs B1, B2, B3 are enabled and follow the input state.
	X	L	Outputs B1, B2, B3 are disabled and in high impedance state.
CA-IS3735	—	—	Outputs B1, B2, B3, B4 are enabled and follow the input state.

NOTE:

1. Enable inputs ENA and ENB can be used for multiplexing, for clock sync, or other output control. ENA, ENB logic operation is summarized for each isolator product in Table 9-2. These inputs are internally pulled-up to local VDD allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to ENA or ENB if they are left floating. If ENA, ENB are unused, it is recommended they be connected to an external logic level, especially if the CA-IS373x is operating in a noisy environment.
2. X = Irrelevant; H = High level; L = Low level.

10. Application and Implementation

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, the CA-IS373x family device CMOS digital isolator needs only two external VDD bypass capacitors (0.1µF to 1 µF) to operate. Its TTL level compatible input terminals draw only micro amps of leakage current, allowing them to be driven without external buffering circuits. The output terminals have a characteristic impedance of 50 Ω (rail-to-rail swing) and are available in both forward and reverse channel configurations. Figure 10-1 shows the typical application of CA-IS3731 device. And the circuit of Figure 10-2 is typical for most applications of CA-IS37xx series products and is as easy to use as a standard logic gate.

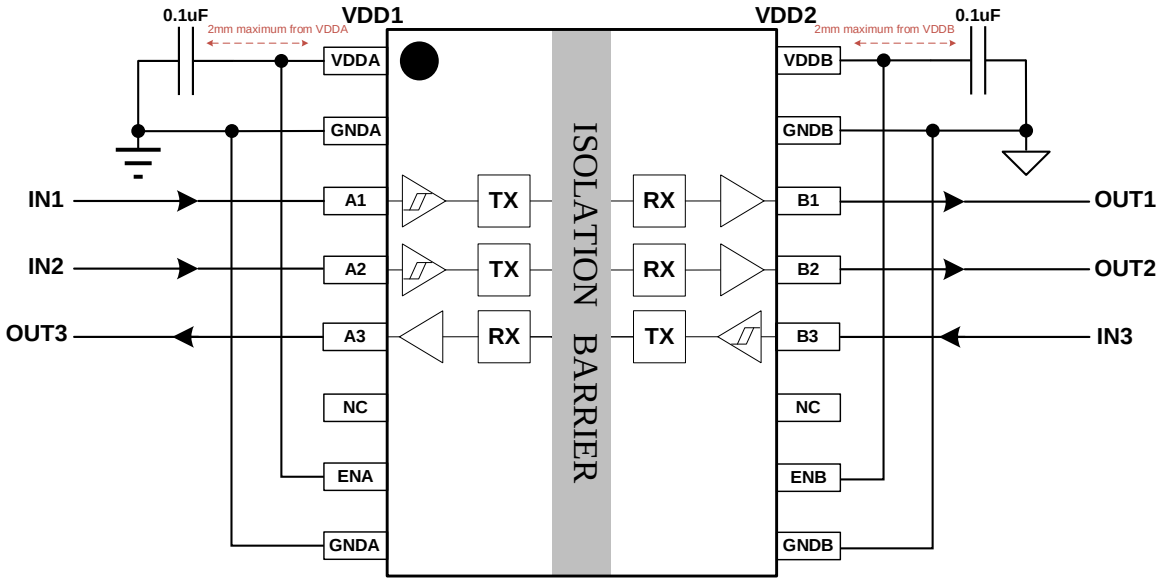


Figure 10-1 Typical Application Circuit of CA-IS3731

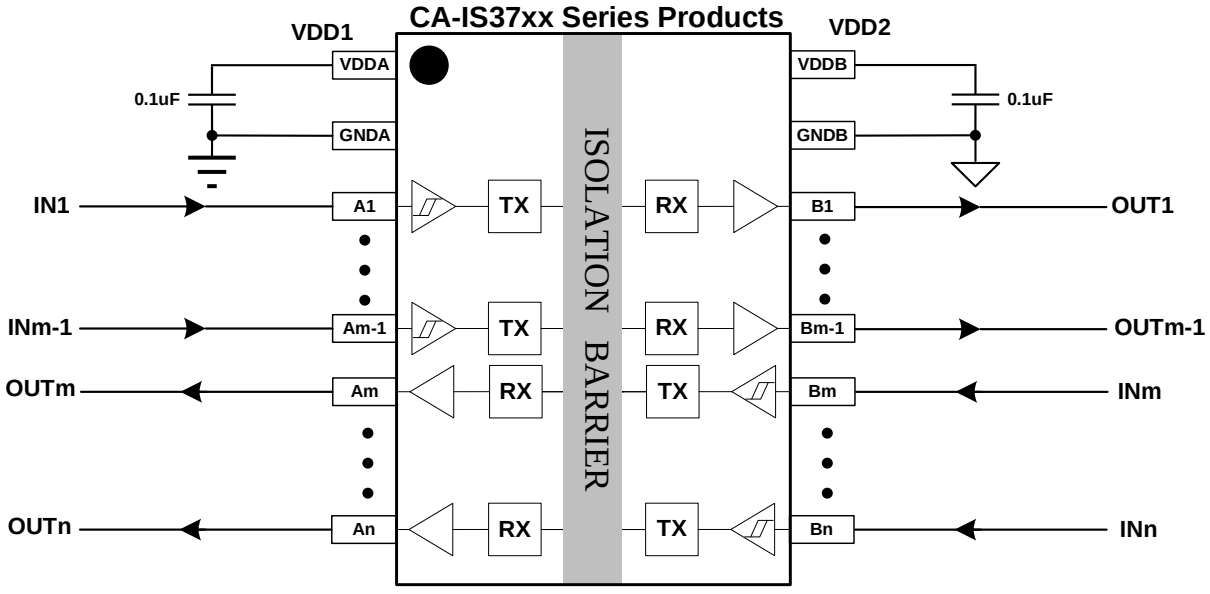
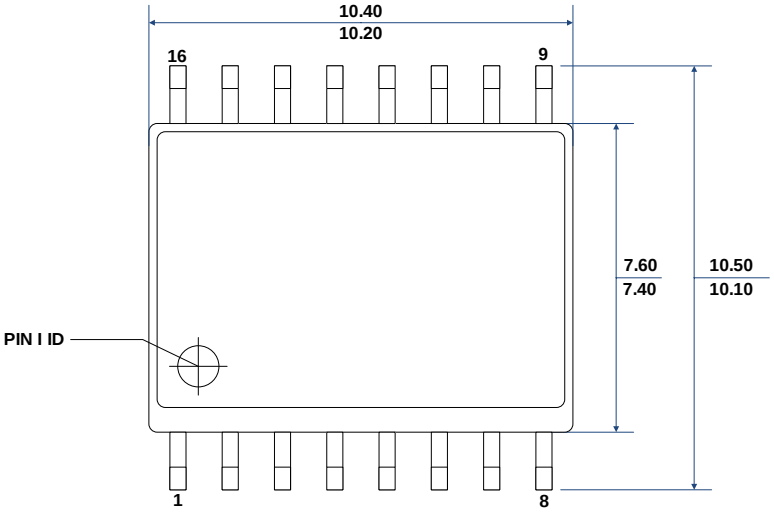


Figure 10-2 CA-IS37xx Series Digital Isolator Application Schematic

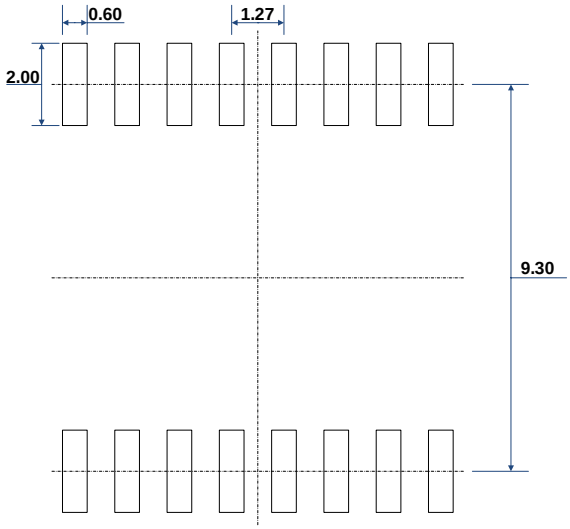
11. Package Information

11.1. 16-Pin Wide Body SOIC Package Outline and Recommended Land Pattern

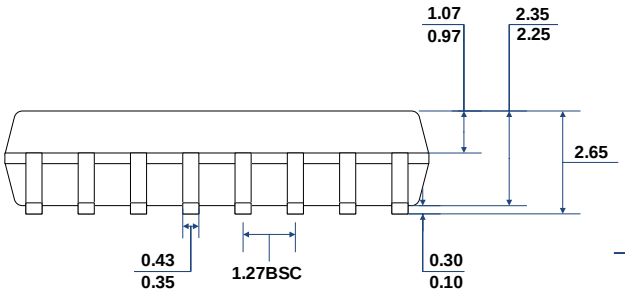
The figure below illustrates the package details and the recommended land pattern details for the CA-IS373x digital isolator in a 16-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



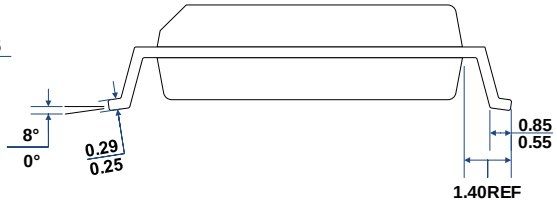
TOP VIEW



RECOMMENDED LAND PATTERN



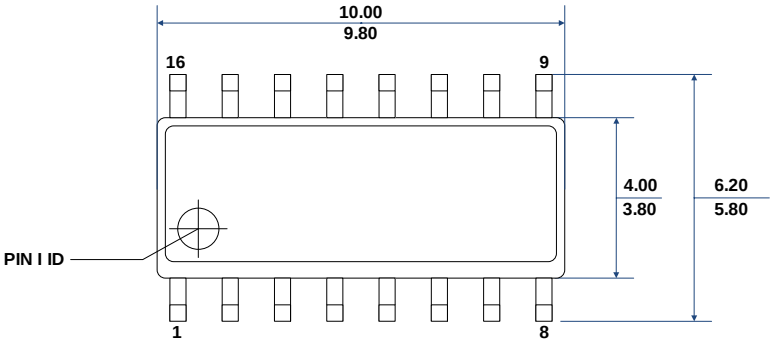
FRONT VIEW



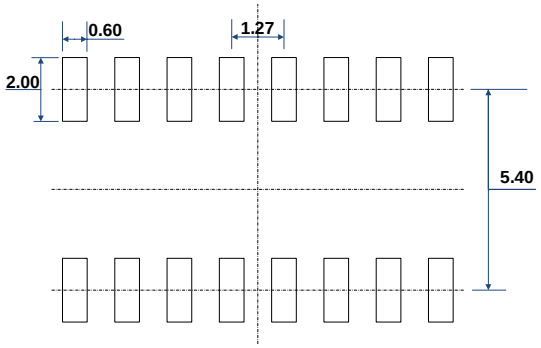
LEFT-SIDE VIEW

11.2. 16-Pin Narrow Body SOIC Package Outline

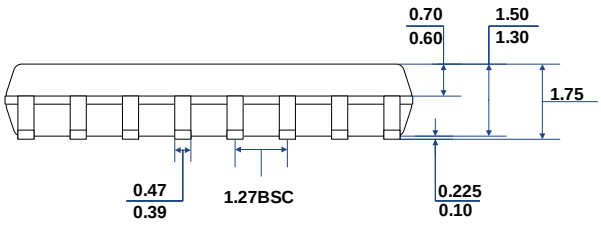
The figure below illustrates the package details and the recommended land pattern details for the CA-IS373x digital isolator in a 16-pin narrow-body SOIC package. The values for the dimensions are shown in millimeters.



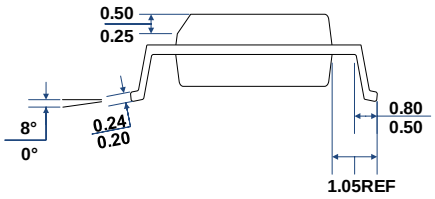
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT-SIDE VIEW

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