CA-IS398x Isolated Octal Industrial Digital Input

1. Features

- Accepts Industry Standard Input Types
  - Compliant to IEC 61131-2 Input Types 1, 2, and 3
- High Integration
  - Eight input channels with serializer (CA-IS3980S)
  - Eight input channels with parallel-output s (CA-IS398xP)
- Support up to 2Mbps Data Rates
- Integrated Digital Glitch and Debounce Filters with 0 to 100ms Selectable Delay Time
- High transient immunity:
  - ±300kV/µs CMTI for the low-speed channels
  - ±50kV/µs CMTI for the high-speed channels
- 2500V_{RMS} Integrated Isolation Reduces BOM and Footprint
- SPI-Compatible Serial Interface (CA-IS3980S only)
- 2.25V to 5.5V Single Supply , Eliminates the Need For Field-side Power Supply
- -40°C to 125°C Ambient Operating Temperature
- 8.66mm x 3.91mm 20-pin SSOP Package
- Safety Regulatory Approvals (pending)
  - DIN VVDE V 0884-10 Basic isolation
  - UL1577 certification, 2500 V_{RMS} insulation
  - CSA according to GB4943.1-2011 certification
  - TUV according to EN61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013 certifications

2. Applications

- Digital Input Modules for PLCs
- Industrial, Building, and Process Automation
- Motor Control
- CNC Control
- Industrial data acquisition

3. General Description

The CA-IS398x family of isolated octal digital inputs are optimized for industrial 24V digital input applications. All devices can be configured for Type 1, Type 2, or Type 3 inputs with a few external components and each channel can sink and source current. The isolation channels based on Chipanalog's advanced capacitive isolation technology feature up to 2.5kV_{RMS} isolation rating and ±300kV/µs typical CMTI (low-speed channels), provide high electromagnetic immunity, low propagation delay and low jitter.

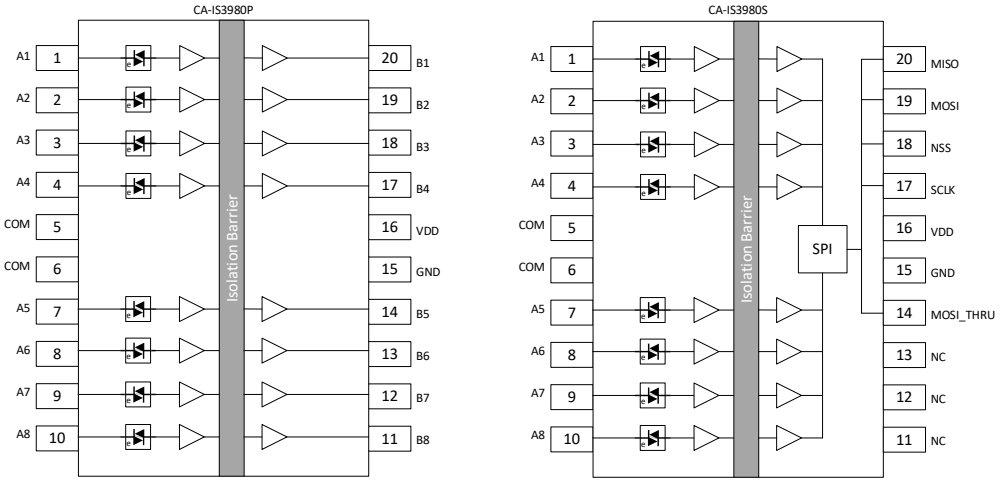
The CA-IS398x devices operate over the supply range of 2.25V to 5.5V on logic side, no power supply required on field side. The logic output level is set by supply voltage independently, easy to connect with 2.5V, 3.3V and 5V controller interface. The CA-IS3980S industrial interface serializer translates, conditions and serializes the eight 24V digital inputs to CMOS-compatible signals through the SPI port required by microcontrollers; While the CA-IS398xP devices translate eight 24V industrial digital inputs to eight CMOS-compatible parallel outputs. All devices provide isolated digital outputs and all digital inputs can be current-sinking or current sourcing industrial inputs (bidirectional inputs) from sensors and switches used in industrial, process, and building automation. For robust operation in industrial environments, each input of the CA-IS398x with parallel outputs includes a glitch and debounce filters with fixed delay time; The CA-IS3980S features programmable debounce filters, allow flexible debouncing and filtering of sensor outputs based on the application. Also, for systems with more than eight sensor inputs, CA-IS3980S is capable of daisy-chaining multiple devices and have up to 128 inputs sharing the same isolated SPI interface. A simplified block diagram for the CA-IS398x is shown in the figure below.

The CA-IS398x family of devices are specified over -40°C to +125°C operating temperature range and are available in 20-pin SSOP package. Also see the *Ordering Information* for suffixes associated output interface and filter delay time configuration options.

Device information

Part number	Package	Package size (NOM)
CA-IS3980 CA-IS3988	SSOP20(Y)	8.66mm x 3.91mm

Simplified Block Diagram



4. Ordering Information

Part Number	Output Interface	Number of High-speed Channels	Low-pass Filter Debounce Time	Package	Isolation Rating (kV_{RMS})
CA-IS3980S	Serial	0	0ms/10ms/30ms/100ms	SSOP20	2.5kV_{RMS}
CA-IS3980P	Parallel	0	0ms	SSOP20	2.5kV_{RMS}
CA-IS3988P	Parallel	8	0ms	SSOP20	2.5kV_{RMS}

Contents

5. Revision History

Revision Number	Description	Page Changed
Version 1.00	N/A	N/A
Version 1.01	N/A	N/A
Version 1.02	Updated “ESD Ratings” table, HBM ESD protection changed to ±5000V, CDM ESD protection changed to ±2000V.	Page 6
Version 1.03	Change POD and Type reel information	22,24
Version 1.04	Removed part number CA-IS3982x,CA-IS3984x	NA
Version 1.05	Updated SPI sync information Updated VDD UVLO information	24 8

6. Pin Configuration and Description

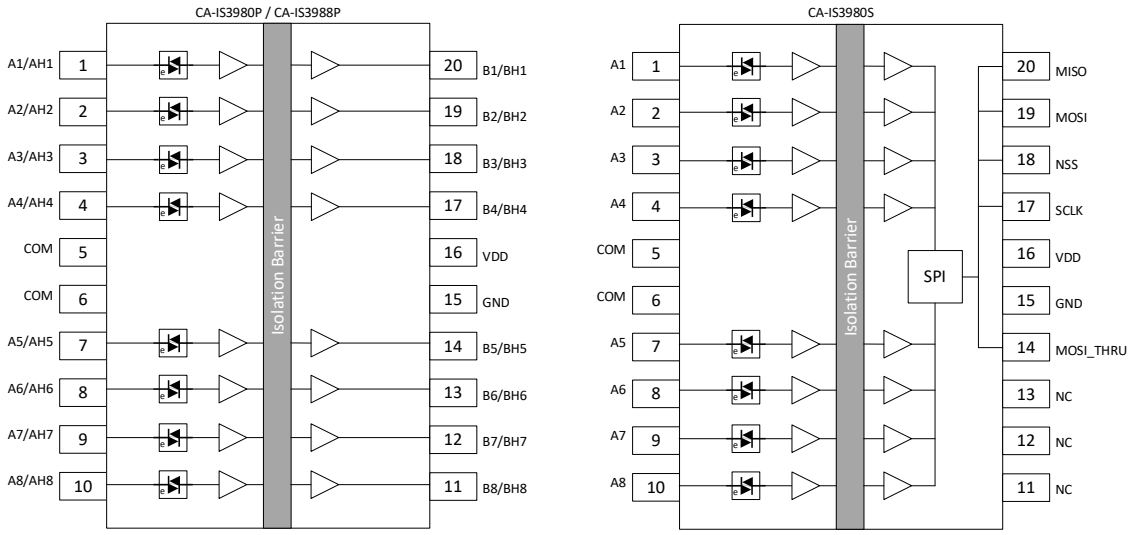


Figure 6-1. CA-IS398x Pin Configuration

Table 6-1. CA-IS3980P/CA-IS3982P/CA-IS3984P/CA-IS3988P pin description

Pin Number		Pin Name	Type	Description
CA-IS3980P	CA-IS3988P			
1,2,3,4,7,8,9,10	---	A1-A8	Input	Field input, low-speed channels.
---	1,2,3,4,7,8,9,10	AH1-AH8	Input	Field input, high-speed channels.
5, 6	5, 6	COM	COM	Common, can be connected to ground for sinking inputs or the field supply for sourcing inputs.
11,12,13,14, 17,18,19,20	---	B1-B8	Output	Logic Outputs, low-speed channels. Indicate the state (high or low) of A1-A8. If the input is open, output is Low.
---	11,12,13,14, 17,18,19,20	BH1-BH8	Output	Logic Outputs, high-speed channels. Indicate the state (high or low) of AH1-AH8. If the input is open, output is high-impedance.
16	16	VDD	Power	2.25V to 5.5V logic supply input.
15	15	GND	GND	Ground reference for logic side.

Table 6-2. CA-IS3980S pin description

Pin Number	Pin Name	Type	Description
CA-IS3980S			
1,2,3,4,7,8,9,10	A1-A8	Input	Field input, low-speed channels.
5, 6	COM	COM	Common, can be connected to ground for sinking inputs or the field supply for sourcing inputs.
11, 12, 13	NC	No Connect	Not internally connected.
16	VDD	Power	2.25V to 5.5V logic supply input.
15	GND	GND	Ground reference for logic side.
19	MOSI	Input	SPI serial data input.
17	SCLK	Input	SPI serial clock input.
18	NSS	Input	SPI chip-select input.
14	MOSI_THRU	Output	SPI serial data out for cascading multiple devices (up to 16).
20	MISO	Output	SPI serial data output.

7. Specifications

7.1. Absolute Maximum Ratings[1]

Parameters		Minimum value	Maximum value	Unit
V_{DD}	Power supply voltage	-0.3	6.0	V
$I_{F(AVG)}$	Ax/AHx Average Input Current		30	mA
$V_{F(AVG)}$	Ax/AHx Aerage Input Voltage @ 30mA Input Current		2.5	V
V_O	Bx/BHx, MISO Output Voltage	-0.5	V_{DD}+0.5	V
I_O	Bx/BHx Output Current	-10	10	mA
VI	MOSI、NSS、SCLK Input	-0.5	V_{DD}+0.5	V
T_J	Junction temperature		150	℃
T_{STG}	Storage temperature range	-65	150	℃

Note:

1. The stresses listed under "Absolute Maximum Ratings" are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.

7.2. ESD Ratings

		Value	Unit
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	±5000	V
	Charged device model (CDM), per JEDEC Specification JESD22-C101, all pins	±2000	V

Note:

1. Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.

7.3. Recommended Operating Conditions

Parameters		Min	Typ	Max	Unit
V_{DD}	Power supply voltage	2.3		5.5	V
DR	Maximum data rate[1], high-speed channel			2	Mbps
	Minimum data rate[2], high-speed channel			10	kbps
	Maximum data rate, low-speed channel (+0ms t_D)			250	kbps
	Minimum data rate, low-speed channel (+0ms t_D)			1	kbps
	Maximum data rate, low-speed channel (+10ms t_D)			100	bps
	Maximum data rate, low-speed channel (+30ms t_D)			33	bps
	Maximum data rate, low-speed channel (+100ms t_D)			10	bps
$I_{F(ON)}$	Input start-up current (sinking or sourcing inputs)	1.0		20	mA
T_A	Ambient Temperature[3]	-40		125	℃

Notes:

1. The maximum data rate corresponds to the input signals with 50% duty cycle. If the duty cycle of the input signal is greater than or less than 50%, the maximum data rate will decrease;
2. If the data rate is too low and the rising / falling edge of the input signal is slow, the output signals may have glitches;
3. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

7.4. Thermal Information

Thermal Metric		20-pin SSOP	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105	℃/W

7.5. Power Rating

Parameters		Test conditions	Maximum value	Unit
PD	Maximum Power Dissipation on input side	input current = 30mA/channel, T_J=150°C	540	mW
	Maximum Power Dissipation on output side	V_{DD}=5.5V, C_L=15pF, 1MHz 50% duty cycle input, T_J=150°C	450	mW
	Maximum Power Dissipation	V_{DD}=5.5V, input current = 30mA/channel, T_J=150°C	990	mW

7.6. Insulation Specifications

Parameters		Test conditions	Value SSOP	UNIT
CLR	External Clearance[1]	Shortest terminal-to-terminal distance through air	3.6 (minimum)	mm
CPG	External Creepage[1]	Shortest terminal-to-terminal distance across the package surface	3.6 (minimum)	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	8	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11)；IEC 60112	600	V
	Material group	Per IEC 60664-1	I	
Overvoltage category per IEC 60664-1		Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I- III	
DIN V VDE V 0884-11:2017-01				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	400	V_{RMS}
		DC voltage	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t=60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t=1 s (100% product test)	3600	V_{PK}
V_{IOSM}	Maximum surge isolation voltage [2]	Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (production test)	4000	V_{PK}
q_{pd}	Apparent charge [3]	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output [4]	V_{IO} = 0.4 × sin (2πft), f = 1MHz		pF
R_{IO}	Isolation resistance [4]	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	2500	V_{RMS}

Notes:

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
2. Devices are immersed in oil during surge characterization test.
3. The characterization charge is discharging charge (pd) caused by partial discharge.
4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.7. Safety-Related Certifications

VDE (pending)	UL
Certified according to DIN VDE V 0884-11:2017-01.	Certified according to UL 1577 Component Recognition Program.
Certification NO.:Pending	Certification NO.: E511334-20220727

7.8. Safety Limits[1]

Parameters		Test conditions	Min.	Typ.	Max.	Unit
I_S	Safety input/output current on logic side	$R_{\theta JA}$ = 120 °C/W, VI = 2.75V, T_J = 150°C, T_A=25°C.			80	mA
		$R_{\theta JA}$ = 120 °C/W, VI = 3.6V, T_J = 150°C, T_A=25°C.			100	
		$R_{\theta JA}$ = 120 °C/W, VI = 5.5V, T_J = 150°C, T_A=25°C.			240	
I_S	Safety input current on filed side	$R_{\theta JA}$ = 120 °C/W, T_J = 150°C, T_A=25°C.			240	mA
P_S	Total safety power dissipation	$R_{\theta JA}$ = 120 °C/W, T_J = 150°C, T_A=25°C.			1200	mW
T_S	Maximum safety temperature				150	°C

Note:

1. Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the CA-IS398x could dissipate an excessive amount of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. This table shows the safety limits for the CA-IS398x.

7.9. Electrical Characteristics

T_A = -40 to 125°C, over recommended operating conditions, unless otherwise specified.

Parameters		Test conditions	Min.	Typ.	Max.	Unit
Filed-side Inputs						
$I_{F(TH)}$	Input current threshold		460	606	950	μA
I_{HYS}	Input current hysteresis		30	76	200	μA
$V_{F(TH)}$	Field input threshold		1.0	1.38	1.7	V
V_{HYS}	Input voltage hysteresis		30	73	130	mV
C_I	Input capacitance	f=125kHz		105		pF
Logic-side Supply						
V_{ULVO+}	V_{DD} undervoltage threshold	V_{DD} rising	1.85	2.06	2.24	V
V_{UVLO-}	V_{DD} undervoltage threshold	V_{DD} falling	1.74	1.92	2.10	
$V_{HYS(UVLO)}$	UVLO hysteresis			0.14		
I_{DD}	Operating current	All inputs = “0”		4.7	7.7	mA
		All inputs = “1”		4.6	7.6	
		60kHz, all inputs switching with 50% duty cycle.		4.7	7.7	
		1MHz, all inputs switching with 50% duty cycle.		4.7	7.7	
Logic-side Inputs						
V_{IL}	Input logic-low voltage	SCLK，NSS，MOSI			0.8	V
V_{IH}	Input logic-high voltage	SCLK，NSS，MOSI	2.0			V
V_{OL}	Output logic-low voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output logic-high voltage	I_{OH} = -4 mA	V_{DD}-0.4			V
I_{IH}	Input leakage current at logic-low	SCLK，NSS，MOSI	-1		1	μA
I_{IL}	Input leakage current at logic-high	SCLK，NSS，MOSI	-1		1	μA

7.10. Timing Characteristics

T_A = -40 to 125°C, over recommended operating conditions, unless otherwise specified.

Parameters		Test conditions	Min.	Typ.	Max.	Unit
Signal Channels						
t_P	Propagation delay time	Input current rise/fall time=10ns, input current=10mA, high-speed channels AHx		36	120	ns
		Input current rise/fall time=10ns, input current=10mA, low-speed channel Ax (+0ms t_D)		5.6	6.7	□ µs
		Input current rise/fall time=10ns, input current=10mA, low-speed channel Ax (+10ms t_D)		10		ms
		Input current rise/fall time=10ns, input current=10mA, low-speed channel Ax (+30ms t_D)		30		ms
		Input current rise/fall time=10ns, input current=10mA, low-speed channel Ax (+100ms t_D)		100		ms
PWD	Pulse width distortion	AHx high-speed channel		6	50	ns
		Ax channel		450		ns
$Tpsk_{(P-P)}$	Propagation delay skew Part-to-part	AHx high-speed channel	-30		+30	ns
		Ax channel	-250		+250	ns
Tpsk	Propagation delay skew Channel-to-channel	AHx high-speed channel	-30		+30	ns
		Ax channel	-250		+250	ns
tr, tf	Output rise and fall times	C_L=15pF		3.3		ns
t_{START}	Start-up time			46		µs
CMTI	Common mode transient immunity	AHx high-speed channel	25	50		kV/µs
		Ax channel	200	300		kV/µs
SPI Interface						
t_C	SCLK Clock period		100			ns
t_{DO1}	Delay time	SCLK falling to MISO valid			20	ns
t_{DO2}	Delay time	SCLK falling to MISO transition			20	ns
t_{DZ}	Delay time	NSS rising to MISO high-Z			20	ns
t_{SU1}	Setup time	Falling edge of NSS to falling edge of SCLK	25			ns
t_{H1}	Hold time	Rising edge of SCLK to rising edge of NSS	20			ns
t_{SU2}	Setup time	MOSI to SCLK rising	25			ns
t_{H2}	Hold time	SCLK rising to MOSI transition	20			ns
t_{NSS}	Delay time	NSS delay time	200			ns
t_{DTHRU}	Delay time	MOSI to MOSI_THRU delay time			15	ns

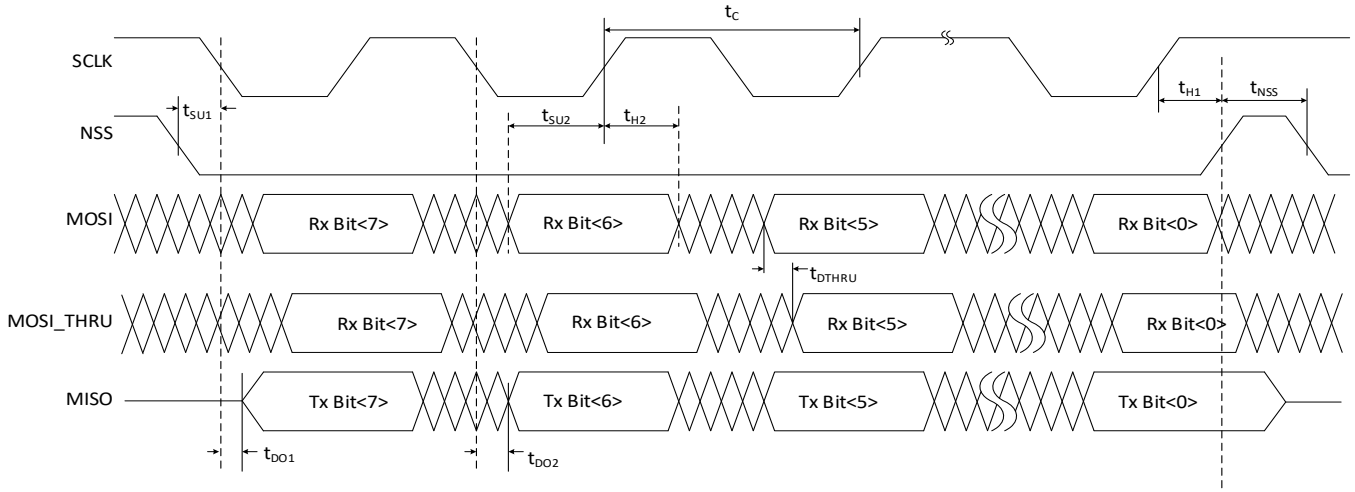


Figure 7-1. SPI Timing Diagram

Note: The timing specifications depicted in this figure apply to each byte of the three byte CA-IS3980S SPI communications packet.

7.11. Typical Operating Characteristics

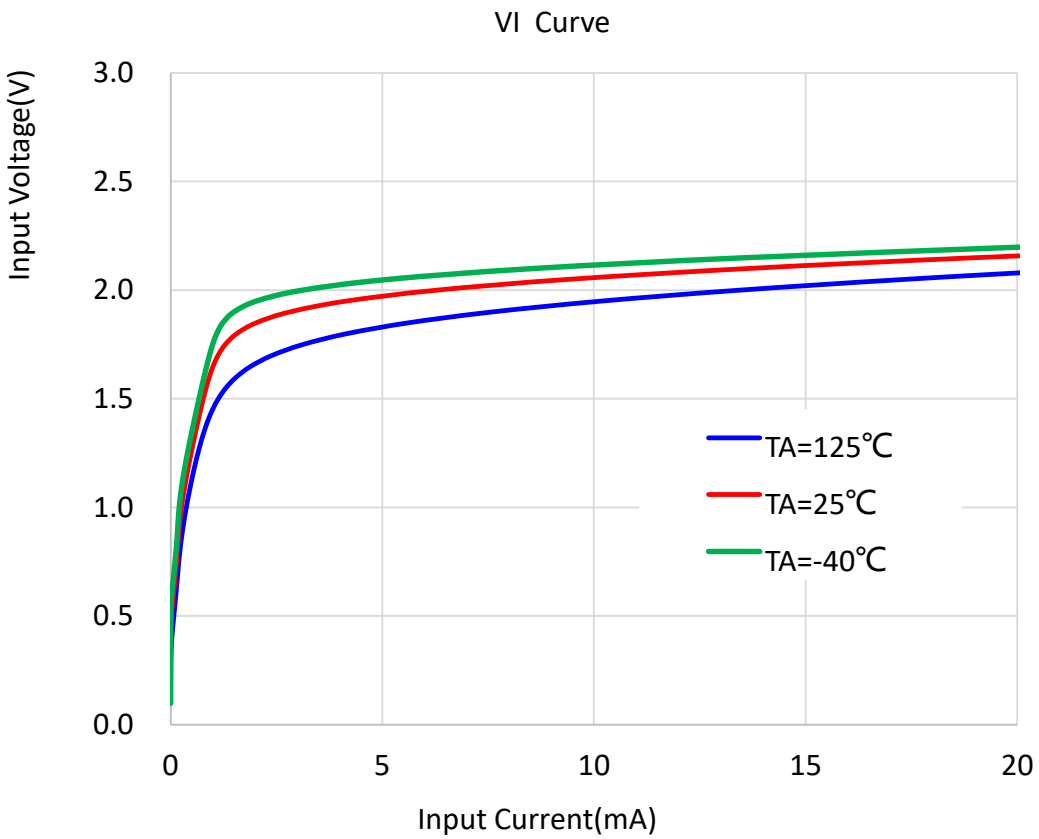


Figure 7-2. Input Voltage vs. Input Current Over Temperature

Note:
1. Input current and input voltages are absolute values and apply to both sourcing and sinking channel designs.

8. Parameter Measurement Information

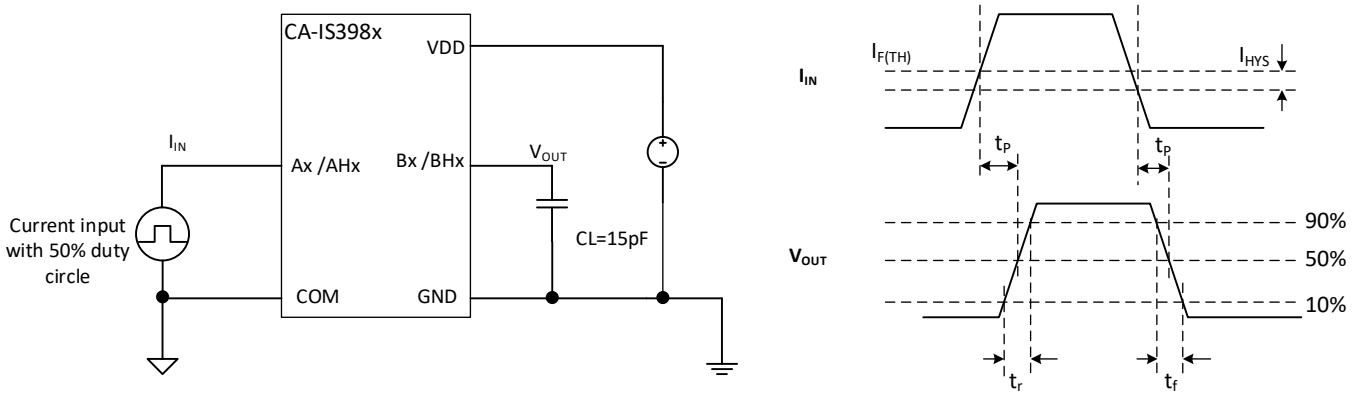


Figure 8-1. Switching Characteristics Test Circuit and Waveform

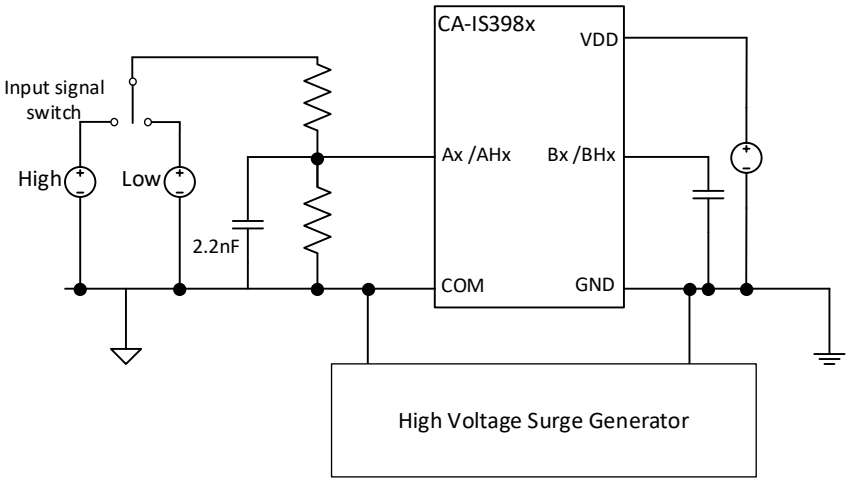


Figure 8-2. Common-Mode Transient Immunity Test Circuit

9. Detailed Description

9.1. Overview

The CA-IS398x family of devices is isolated octal digital inputs optimized for industrial 24V digital input applications. These devices are suitable for high-channel density, digital-input modules for programmable logic controllers and motor control digital input modules. The CA-IS398x devices provide compliance with IEC 61131-2 Types 1, 2, 3 inputs with a few external components and can be used to create a bidirectional input module that can sink and source current, see Figure 9-1 the simplified block diagram for a single CA-IS398x channel. There is a diode bridge and an LED emulator at the front end of each input channel, see Figure 7-2 *Input Voltage vs. Input Current* curve to find more details about input operating characteristics. The internal LED emulator output drives an ON-OFF keying (OOK) modulator, to transfer digital signals across the SiO2 based isolation barrier between circuits with different power domains. In many applications, this capacitive isolation technology is replacing optocoupler-based solution because it can reduce the power requirements and take up less board space while offering the same isolation capability.

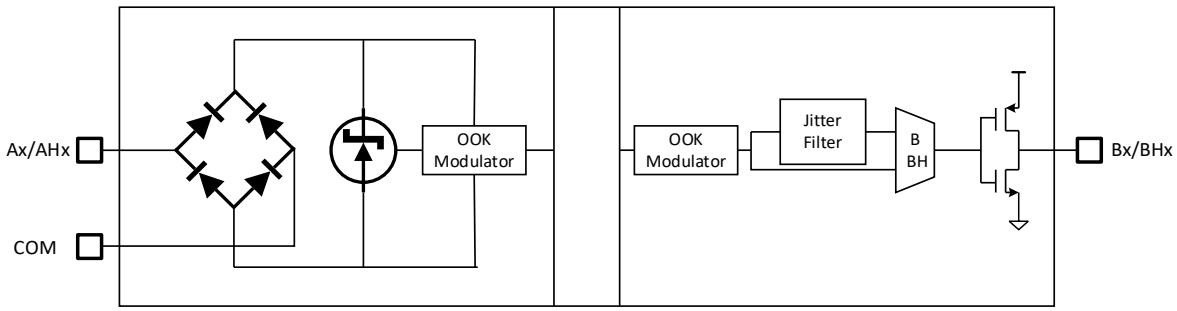


Figure 9-1. Simplified block diagram of a single CA-IS398x channel

On the output side, the signal is either passed directly to the output stage in the case of a high-speed channel (BHx), or the signal is routed through a debounce filter block in the case of a low-speed channel (Bx) for robust operation in industrial environments. For the CA-IS3980S, there are three debounce filter modes available: deglitch filter mode, low-pass filter mode, and blanking filter mode. For the parallel outputs devices, the CA-IS398xP, there are four debounce filter delay time options available: no delay, delays of 10ms, 30ms, or 100 ms, see the *Ordering Information* for suffixes associated filter configuration options. Additionally, a built-in low-pass filter delay of 4µs is always present in low-speed channels, regardless of user configuration options.

The CA-IS398xP/PF/PM/PS devices translate eight 24V industrial digital inputs from sensors and switches used in industrial, process and building automation to eight CMOS-compatible parallel outputs; while the CA-IS3980S industrial interface serializer translates, conditions and serializes the eight 24V digital inputs to CMOS-compatible signals required by microcontrollers and communicate with controllers through the SPI interface. For systems with more than eight sensor inputs, the CA-IS3980S device is capable of daisy-chaining multiple devices and have up to 128 inputs (16 pieces of CA-IS3980S) sharing the same isolated SPI interface.

9.2. Device Operation Modes

The CA-IS398x digital input sense the state (on, high or off, low) of each input (Ax/AHx). The voltages at the Ax/AHx input pins are compared against internal references to determine whether the sensor is on (logic 1) or off (logic 0), then the devices translate the eight digital inputs to serial or parallel outputs, see Table 9-1 the truth table of the CA-IS398x.

The CA-IS398x devices include undervoltage lockout (UVLO) to prevent erroneous operation during device startup and shutdown or when V_{DD} is below its specified operating range. During UVLO, the outputs from the device do not track the inputs to the device, would be in an undetermined state.

Table 9-1. CA-IS398x Truth Table[1]

V_{DD}	Input (Ax/AHx)	Output(Bx/BHx)	Note
Powered up	H	H	Normal operation. The outputs track the digital inputs.
	L	L	
	Open	L	Output is logic-low if input open.
Powered down	X	Indeterminate[2]	If V_{DD} <$V_{UVLO\_}$, or power off, output is indeterminate.

Notes:
1. X = don't care; H = high level; L = low level; Hi-Z = high impedance; Power up: V_{DD} > 2.25V; Power down: V_{DD} < $V_{UVLO\_}$.
2. If V_{DD} < $V_{UVLO\_}$, the output is indeterminate, can be any value within the absolute maximum rating.

9.3. Input Filters

9.3.1. Debounce filter selection and delay configuration

The CA-IS398x family isolated digital inputs offer serial outputs and parallel outputs options. A digital glitch filter provides debouncing and filtering of noisy sensor signals on each low-speed digital input channel. The high-speed channels have no debounce filtering to reduce the propagation delay. The debounce filter can be configured either through part number selection for parallel output devices or through the SPI interface (CA-IS3980S only), see the *Ordering Information* for parallel outputs devices selection with different filter delay options. For the CA-IS3980S debounce filter delay configuration details, see Table 9-2. One of four filter delays (0ms, 10ms, 30ms, 100ms) can be independently selected for each channel.

Table 9-2. Debounce filter delay control

FLT_DLY[1:0]	Delay t_D(ms)	Description
00	0	No additional debounce filter delay.
01	10	Fast channel debounce filter delay.
10	30	Medium channel debounce filter delay.
11	100	Slow channel debounce filter delay.

Note:
1. All low-speed channels include a internal 4 µs low-pass debounce filter delay. Additional delay may be added based on the FLT_DLY0, FLT_DLY1 registers configuration.

9.3.2. Debounce filter operation modes

In addition to configuring filter delay time, the CA-IS3980S also provide selection between three filtering modes for each of the digital input channels: deglitch filter, low-pass filter and blanking filter, allow flexible debouncing and filtering of sensor outputs based on the application, see Table 9-3 for the debounce filter mode setting. All low-speed channels present on parallel output devices are configured with the low-pass filter mode only.

Table 9-3. Debounce filter mode control

FLT_MODEx[1:0]	Filter mode	Description
00	Deglitch filter	Trailing edge delay filter
01	Low-pass filter	Traditional low-pass filter
1x	Blanking filter	Leading edge delay filter

Deglitch filter

The deglitch filter mode corresponding to FLT_MODEx[1:0] = 00, employs only a simple trailing edge delay commonly used in digital deglitch filters. In this mode, the device checks that an input is stable for at least the amount of time specified in the corresponding channel's debounce delay setting t_D. Once the channel's input has been stable for t_D, the channel's output assumes the value of the channel's input. Consequently, if the input is not stable for at least t_D, the input change is not sent to the internal shift register.

Low-pass filter

The low-pass filter corresponding to FLT_MODEx[1:0] = 01, provides a low-pass filtering function on each low-speed input channel. This is also the mode of the built-in 4µs default filter in all low-speed channels. Under this filter mode, noise rejection is accomplished through a nonrollover up-down counter where the state of the field digital input controls the counting direction (up or down). When the channel input has assumed a new value, the counter begins counting up toward the debounce delay setting t_D. If before the count t_D is reached the channel's input returns to its previous value, it counts down. If the channel input again assumes the new value before the counter reaches 0 (i.e., noise pulse width is less than the time the channel input had previously assumed a new value), the counter counts up from a non-zero value. The filter output is updated and assumes the new value when the counter hits the upper limit t_D. Using low-pass filter mode, any noise pulse on the channel input with duration less than the channel's debounce filter delay setting t_D, will be suppressed.

Blanking filter

The blanking filter mode corresponding to FLT_MODEx[1:0] = 1X, provides a leading edge filtering function on each low-speed input channel. The internal counter is initialized to zero. When the channel input changes, the channel output immediately assumes the new value, and the counter is reset to the current delay setting t_D. Independent of what occurs on the channel input, the counter begins counting down after this change, leaving the channel blind to changes on the input. When the counter again reaches zero, the channel's current input is compared to the channel's current output. If they are different the channel output immediately assumes the new value. If they are the same, the channel output will immediately change on the next new value seen by the channel input. In any cases, a change on the channel input resets the counter to the current delay setting t_D.

Figure 9-2 shows the debounce filter modes timing diagram.

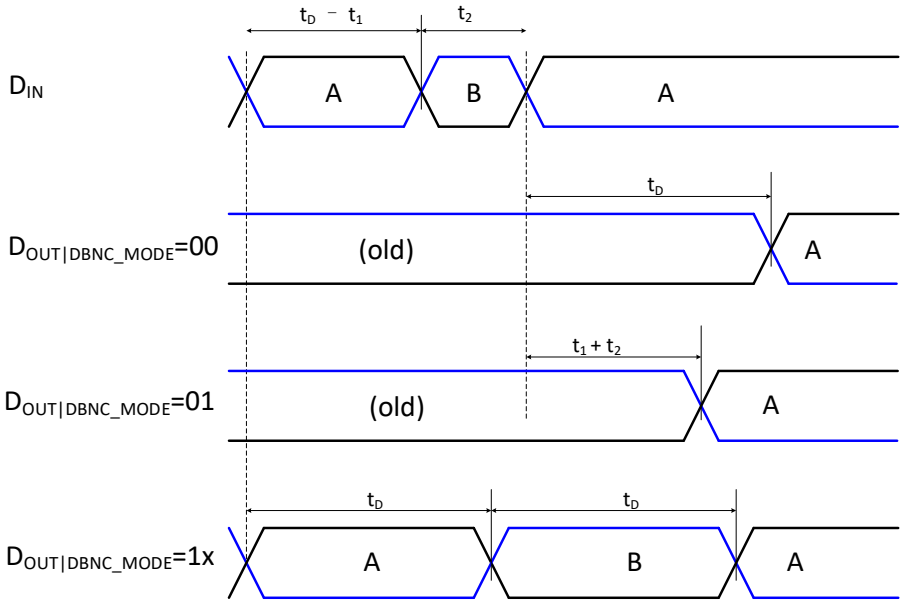


Figure 9-2. Debounce Filter Modes Timing Diagram

9.4. SPI Interface (CA-IS3980S)

The CA-IS3980S has an SPI compatible interface used to read digital inputs data and configure the filter delay, debounce mode registers. Each configuration register can be read back to ensure proper configuration. For systems with more than eight sensor inputs, the CA-IS3980S is capable of daisy-chaining multiple devices and have up to 128 inputs sharing the same isolated SPI interface.

9.4.1. Register Map and Description

The CA-IS3980S includes below addressable registers:

1. CHAN_STATUS: input data status register. The internal data serializer comprises a 8-bit shift register, containing 8 bits of data corresponding to the eight field inputs. The shift register contents are read only (no write capability exists) through the SPI-compatible interface.
2. FLT_MODE0, FLT_MODE1: the programmable filter mode control bits for A1 to A8, read and write registers, see *Table 9-4* for more details.
3. FLT_DLY0, FLT_DLY1: the filter delay configuration bits for A1 to A8, read and write. These registers are used to set one of four filter delays (0ms, 10ms, 30ms, 100ms) for each channel independently. See Table 9-4 for more details.

Table 9-4. Register Map

Register	Address	Type	Description
CHAN_STATUS	0x0	Read only	{STATUS[7:0]}, Digital input state, D[x] is the state of the corresponding input pin. 0: D[x] = 0, channel x is driven low. 1: D[x] = 1, channel x is driven high.
FLT_MODE0	0x1	Read and Write	Programmable filter mode control bits for A1 to A4, organized as: {md_ch3[1:0],md_ch2[1:0],md_ch1[1:0],md_ch0[1:0]} md_chx[1:0] = 00 = deglitch filter; md_chx = 01 = low-pass filter; md_chx = 1X = blanking filter
FLT_MODE1	0x2	Read and Write	Programmable filter mode control bits for A5 to A8, organized as: {md_ch7[1:0],md_ch6[1:0],md_ch5[1:0],md_ch4[1:0]} md_chx[1:0] = 00 = deglitch filter; md_chx = 01 = low-pass filter; md_chx = 1X = blanking filter
FLT_DLY0	0x3	Read and Write	Programmable filter delay values for A1 to A4, organized as: {dly_ch3[1:0], dly_ch2[1:0], dly_ch1[1:0], dly_ch0[1:0]} dly_chx[1:0] = 00 = 0ms; dly_chx[1:0] = 01 = 10ms; dly_chx[1:0] = 10 = 30ms, dly_chx[1:0] = 11 = 100ms.
FLT_DLY1	0x4	Read and Write	Programmable filter delay values for A5 to A8, organized as: {dly_ch7[1:0], dly_ch6[1:0], dly_ch5[1:0], dly_ch4[1:0]} dly_chx[1:0] = 00 = 0ms; dly_chx[1:0] = 01 = 10ms; dly_chx[1:0] = 10 = 30ms, dly_chx[1:0] = 11 = 100ms.

9.4.2. SPI Protocol

The CA-IS3980S communicates with microcontrollers through an SPI-compatible 4-wire serial interface. The interface has three inputs: clock (SCLK), chip select (NSS), and data in (MOSI), and one output, data out (MISO). An additional MOSI_THRU output is provided to facilitate the cascading of up to 16 CA-IS3980S devices. The CA-IS3980S devices are the slave device in an SPI communication with the microcontroller being the master. The NSS input is used to initiate and terminate a data transfer. SCLK is used to synchronize data movement between the master (microcontroller) and the slave devices. NSS must be low to clock data into or out of the device, and MOSI must be stable when sampled on the rising edge of SCLK. MISO and MOSI_THRU are stable on the rising edge of SCLK. The CA-IS3980S ignores all activity on SCLK and DIN except when NSS is low. Please see Figure 7-1 SPI timing diagram and Timing Characteristics to find more details.

The CA-IS3980S SPI communication packet is composed of three serial bytes, byte0, byte 1 and byte 2, see *Figure 9-3* for a SPI communication packet. In this sequence, byte 0 is the control byte, and specifies the operation to be performed as well as the device to be selected in a daisy-chain organization. The CID[3:0] is device ID for each CA-IS3980S in daisy chain. This field should be set to all zeros by the SPI master in non daisy-chained operation. Next, byte 1 specifies the address of the internal

CA-IS3980S SPI register to be accessed (read or write). If the write address provided does not correspond to a physically available internal register, no internal CA-IS3980S register update will occur in the SPI write operation; while if the read address provided does not correspond to a physically available internal register, all zeroes will be returned as the read value by the CA-IS3980S in the SPI read operation. The final byte, byte 2 in the packet consists of either the data to be written into the addressed CA-IS3980S SPI register (using MOSI), or the data read from the addressed CA-IS3980S SPI register (using MISO). Data is read from the status/configuration registers or written to the configuration registers MSB first for SPI communication. The serial clock (SCLK), which is generated by the microcontroller, is active only when NSS is low and during control byte, address and data transfer to any device on the SPI bus. Control byte, address and data bits are transferred in groups of eight, MSB first, this means each of the eight bits for this three byte communication packet is captured by the CA-IS3980S on eight adjacent rising edges of SCLK. If NSS goes high in the middle of a transmission (any time before the 8th bit), the sequence is aborted, the CA-IS3980S lost synchronization with host SPI and cause communication error. In this case, the target register value will not be changed. Every time NSS goes low, a new 8-bit stream is expected. (i.e., data does not get written to internal registers). However, if more than 8 bits data are clocked into the CA-IS3980S in the last byte, the target register data will be uncertain, need to rebuild synchronization with SPI host.

Take NSS high and SPI host issue clock signal to rebuild SPI communication. The SCLK rising edge during NSS high will reset the internal SPI state machine and build synchronization between the CA-IS3980S and SPI host. After rebuilding communication with host, NSS goes low and the host issues 8 bits as the first byte (byte0) of the three serial bytes to initiate communication. Note that, after the synchronization operation, the first byte of SPI (byte0) must be transmitted to initiate communication.

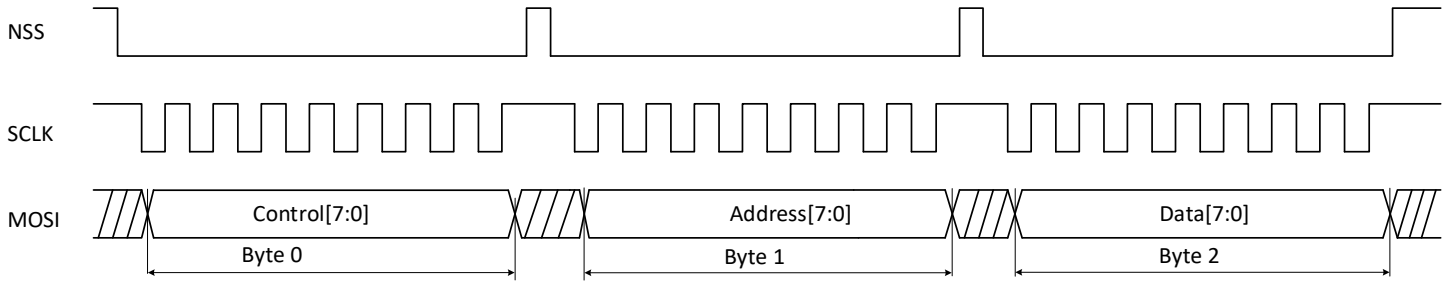


Figure 9-3. SPI Communication Protocol

Table 9-5. SPI communication packet

Control Byte							
7	6	5	4	3	2	1	0
BRCT	R/Wb	0	0	CID[0]	CID[1]	CID[2]	CID[3]
Address Byte							
7	6	5	4	3	2	1	0
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Data Byte							
7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 9-6. Bit descriptions for the control byte

Control Byte (byte 0)							
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
BRCT	R/Wb	0	0	CID[0]	CID[1]	CID[2]	CID[3]
1 - broadcast (write) 0 – Write the addressed part only **Note:** the status of this bit is ignored if in read operation.	1 - read 0 - write	Reserved Set to (0,0)		CID[**3:0**] is daisy-chained device ID CID[**3:0**] = 0000 (CID[**0:3**] = 0000) in non daisy-chained operation.			

Referring to Figure 9-3, in an SPI read operation the control byte will only have bit 6 set to a 1 in a single CA-S3980S device organization (no daisy chaining). Bit 7 (the broadcast bit) is ignored during a read operation since only one device may be read at a time in either a single or daisy-chained organization. The read data is provided during the final byte of the three byte read communication packet to the querying master SPI device through the MISO output, which remains tri-stated at all other times. In an SPI write operation, if the bit 7 (the broadcast bit) of control byte set to 1, during an SPI write operation, the broadcast bit forces all daisy-chained CA-IS3980S devices to update the designated internal SPI register with the supplied write data, regardless of the CA-IS3980S device being addressed using the CID[3:0] field of the control word. If the bit 7 of Byte 0 set to 0, only have the addressed CA-IS3980S device to update the internal register. The write data is provided by the SPI master during the final byte of the three byte write communication packet. The CA-IS3980S MISO output remains tri-stated during the entire SPI write operation.

9.4.3. SPI Daisy-Chaining

For systems with more than eight sensor inputs, multiple CA-IS3980S devices can be daisy-chained to allow access to all data inputs through a single serial port. When using a daisy-chain configuration, connect MOSI of SPI master to MOSI of the first device CA-IS3980S[0] in the chain. Connect SPI master MISO to MISO pin of all CA-IS3980S devices in the chain. For all middle links, connect MOSI to MOSI_THRU of the previous device and MOSI_THRU to MOSI of the next device. NSS and SCLK of all devices in the chain should be connected together in parallel, see Figure 9-4 which illustrates a 128-inputs application for daisy-chaining.

Each CA-IS3980S is assigned a device ID CID[3:0] which is corresponded bit 0 to bit 3 of the control byte, as the address in daisy chain, see Table 9-7 the device ID for each of CA-IS3980S device. All bits composing an SPI communication packet from the SPI master are passed directly through by the CA-IS3980S from the MOSI input to the MOSI_THRU output unchanged, except for the CID[3:0] field of the control byte. As this bit field is passed through the CA-IS3980S, it is decremented by one. When a given CA-IS3980S device in the daisy chain is presented with the CID[3:0] code of 0000, it is activated as the one to be addressed slave device, thereby enabling this device. After locking the addressed device, all remaining operations between the SPI master and the CA-IS3980S activated in this manner proceed as previously discussed in the SPI interface communication protocol above section for the case of a single CA-IS3980S slave. Please note that the SPI master placed the 4-bit device ID (CID [3:0]) in control word in reverse order, as shown in Table 9-7, CID[0] is placed at bit 3 and CID[3] placed at bit 0 of the control byte. When operating the addressing instruction, pay attention to the order of device ID code.

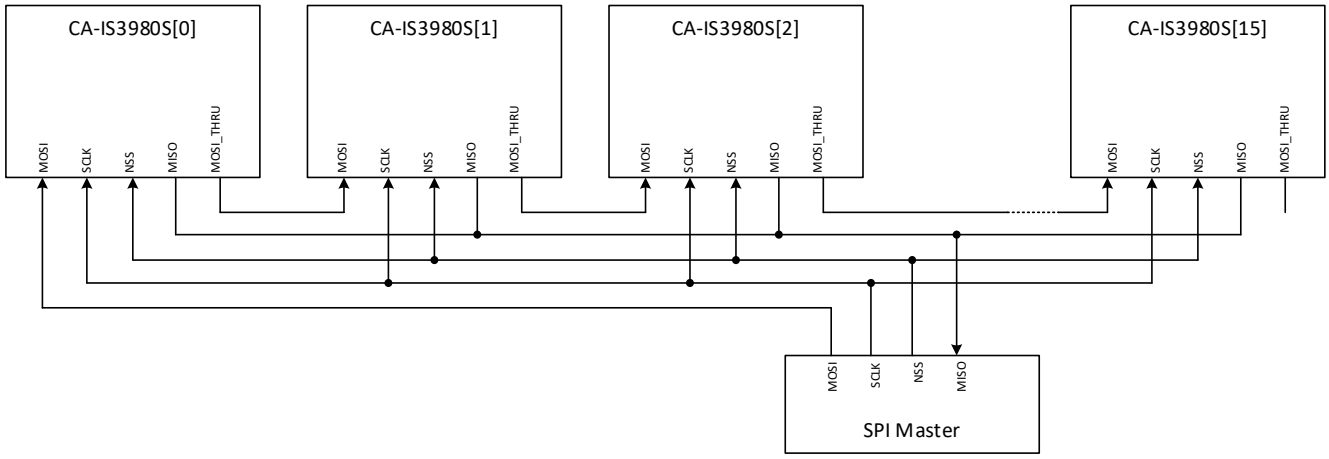


Figure 9-4. SPI Daisy-Chaining Organization

The CA-IS3980S device supports three kind of control command: broadcast write, only addressed part write, only addressed part read, see Table 9-8. During the daisy-chain write operation, if the broadcast bit is 0, only the CA-IS3980S device being addressed using the CID[3:0] field of the control byte in a daisy-chain will be updated. If the broadcast bit is 1 during a daisy-chain write operation, the CID[3:0] field is ignored, and all CA-IS3980S devices connected in a daisy chain will be updated. For example, in order to write to CA-IS3980S[12], the control byte would be: Control[7:0] = 00000011, here CID[3:0]=1100. Note that there is a delay time associated with passing the MOSI input pin of a given CA-IS3980S to the MOSI_THRU output pin. As a result, the maximum possible SCLK frequency will be reduced based on the number of devices connected in a daisy-chain.

Table 9-7. Device ID for each of CA-IS3980S in the daisy-chain

Device ID	CA-IS3980S[0]	CA-IS3980S[1]	CA-IS3980S[2]	CA-IS3980S[3]	CA-IS3980S[4]	CA-IS3980S[5]	CA-IS3980S[6]	CA-IS3980S[7]
CID[3:0]	0000	0001	0010	0011	0100	0101	0110	0111
CID[0:3][1]	0000	1000	0100	1100	0010	1010	0110	1110
Device ID	**CA-IS3980S[8]**	**CA-IS3980S[9]**	**CA-IS3980S[10]**	**CA-IS3980S[11]**	**CA-IS3980S[12]**	**CA-IS3980S[13]**	**CA-IS3980S[14]**	**CA-IS3980S[15]**
CID[3:0]	1000	1001	1010	1011	1100	1101	1110	1111
CID[0:3][1]	0001	1001	0101	1101	0011	1011	0111	1111

Note:
1. CID[3:0] are dedicated to addressing one of up to 16 CA-IS3980S devices connected in a daisy chain. This four bit field is placed in the control word by the SPI master in reverse order, CID[0] is placed at bit 3 and CID[3] placed at bit 0 of the control byte.

Table 9-8. Daisy-chain Operation Command

Command	Control Byte (Control[7:0])							
	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
	BRCT	R/Wb	0	0	CID[0]	CID[1]	CID[2]	CID[3]
Broadcast Write	1	0	0	0	0	0	0	0
Write CA-IS3980S[n]	0	0	0	0	CID[0:3] **Note:** CID[3:0] is the addressed device ID.			
Read CA-IS3980S[n]	0	1	0	0				

10. Application and Implementation

The CA-IS398x devices are complete, isolated digital-input receivers with IEC 61131-2 Type 1, Type 2, and Type 3 characteristics, Figure 10-1 provides the input channel switching characteristics. These devices enable 24 V bipolar digital inputs to be connected to its input through a resistor divider network, see Figure 10-2 and Figure 10-3 the typical application circuits for the current sinking inputs and current sourcing inputs respectively. The digital inputs On/Off voltage thresholds at the device pin are fixed to $V_{F(TH)}$ and ($V_{F(TH)}$ – V_{HYS}), see Electrical Characteristics for the typical threshold value. However the On/Off voltage thresholds of the field input are determined by the value of the resistor divider R1 and R2 placed between the field input and the device, and the input current I_{IN}. Please see *Table 10-1* for the recommended external resistors of Type 1, Type 2 and Type 3 sensors or switches based on 24 V DC PLC digital input types as defined by IEC 61131-2.

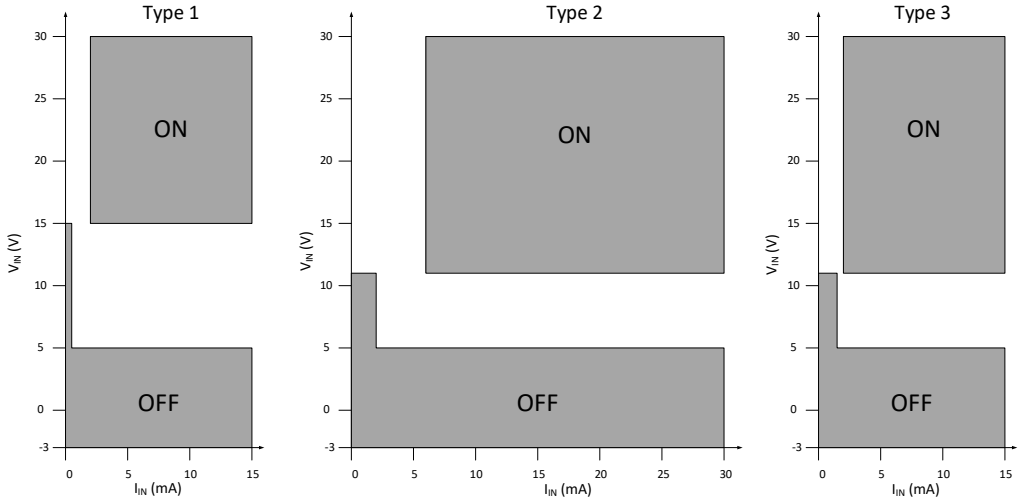


Figure 10-1. Switching Characteristics for IEC 61131-2 Type 1, 2, and 3 24VDC Digital Inputs

Other digital voltage levels and characteristics can be implemented with simple modifications to the resistor divider network. Note that, the 2.2nF capacitor in Figure 10-2 and Figure 10-3 is used to filter noise on the high-speed channels only. For the low-speed channels, we do not recommend to use external RC filter at inputs because the capacitor will cause very high transient voltage under surge condition. The built-in debounce filters can be used to filter noise on the low-speed channels.

Table 10-1. Recommended external components in the typical application circuit

Resistor network	Type 1	Type 2	Type 3
R1	2.4kΩ	390Ω	750Ω
R2	6.2kΩ	1.5kΩ	2.7kΩ
Note: These recommendations assume a resistor tolerance of 5%, it is highly recommended that a MELF resistor be used.			

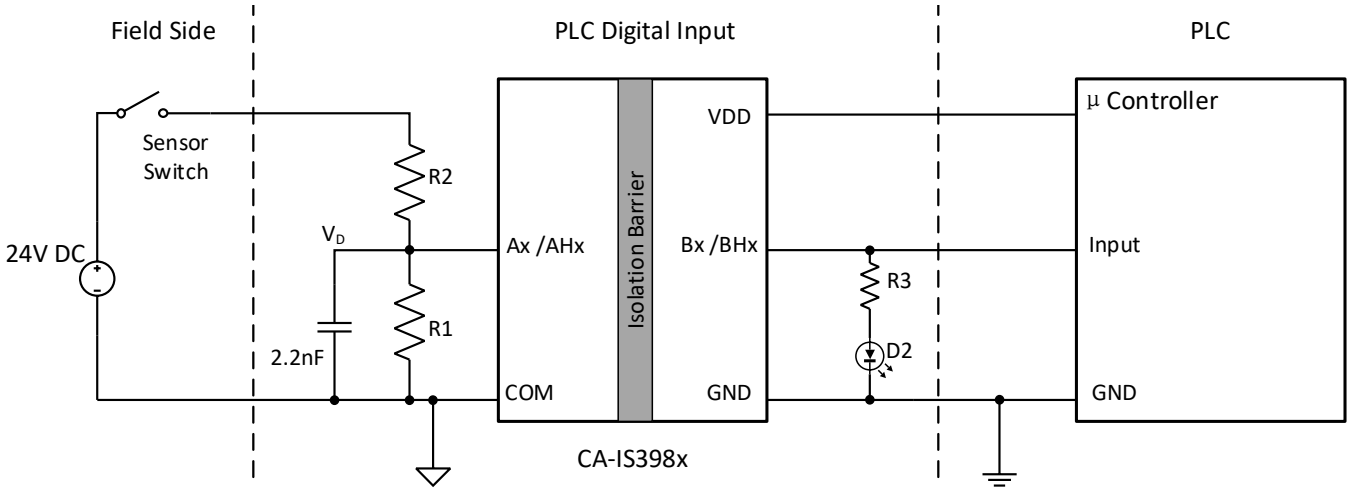


Figure 10-2. Typical Application Circuit with Sinking Inputs

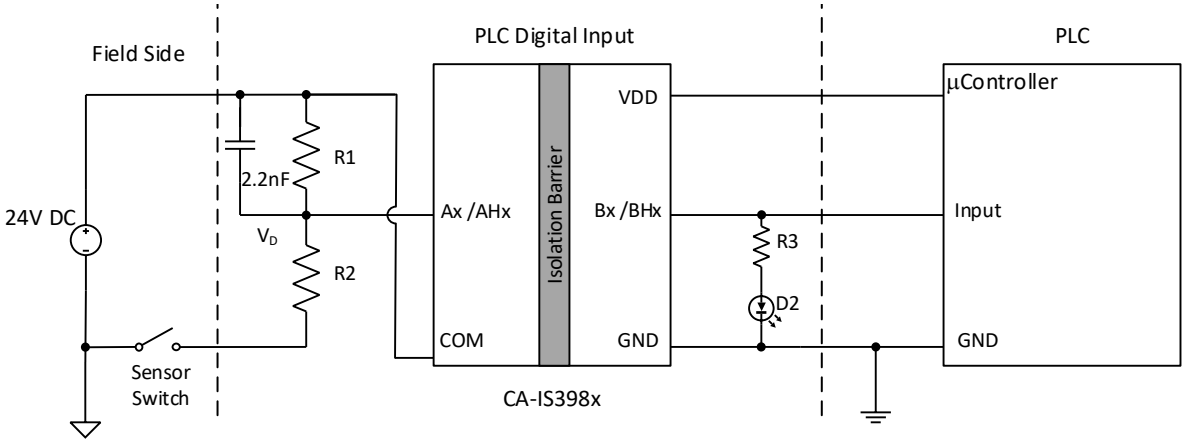


Figure 10-3. Typical Application Circuit with Sourcing Inputs

Designing high-channel count digital inputs modules require cascading multiple CA-IS3980S devices. Simply connect the serial output (MOSI_THRU) of a leading device with the serial input (MOSI) of a following device without changing the processor interface, see Figure 10-4 the typical application circuit, also refer SPI Daisy-Chaining section for more details about the daisy-chain operation.

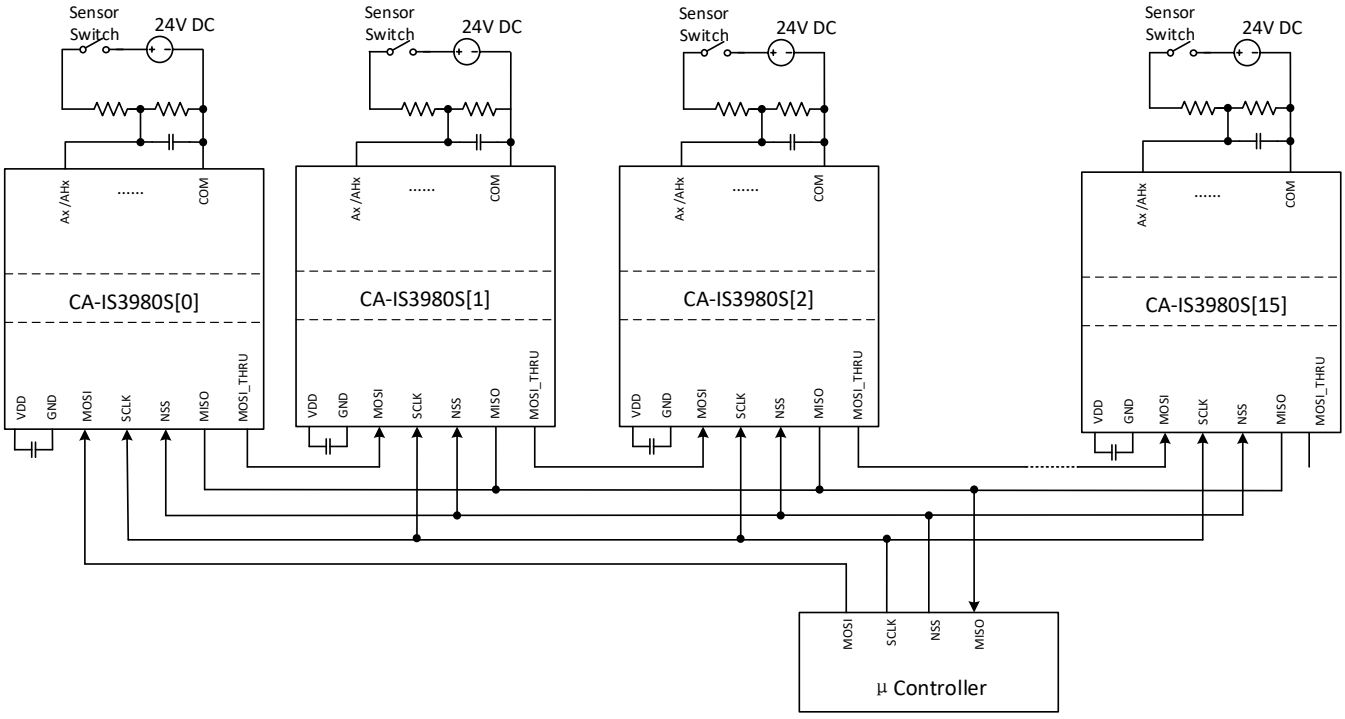
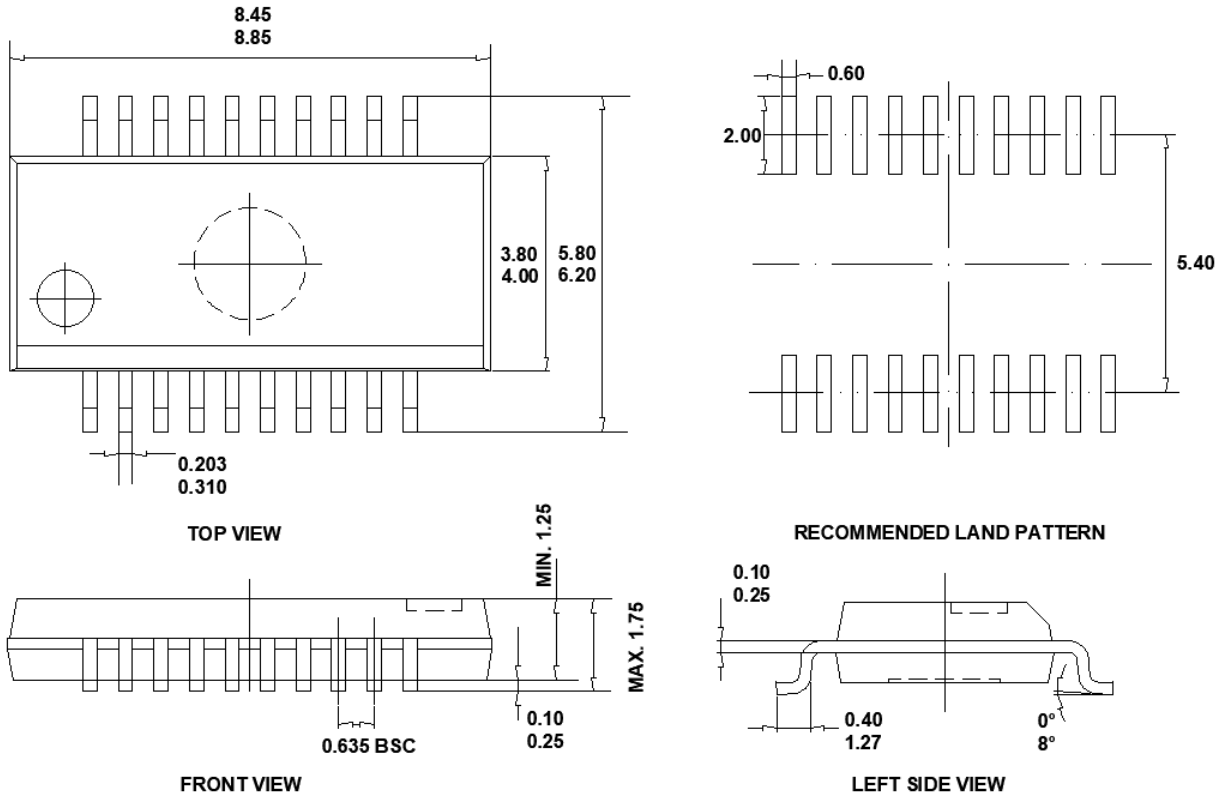


Figure 10-4. Typical Application Circuit with Daisy-Chaining

To reduce ripple and the chance of introducing data errors, bypass V_{DD} with at least 0.1µF low-ESR ceramic capacitors to GND. Place the bypass capacitor as close to the power supply input pin as possible. The PCB designer should keep the input/output traces as short as possible and keep signal paths low-inductance, avoid using vias. The area underneath the CA-IS398x isolation barrier should be free from ground and signal planes.

11. Package Information

SSOP20 Package Outline



12. Soldering Temperature (reflow) Profile

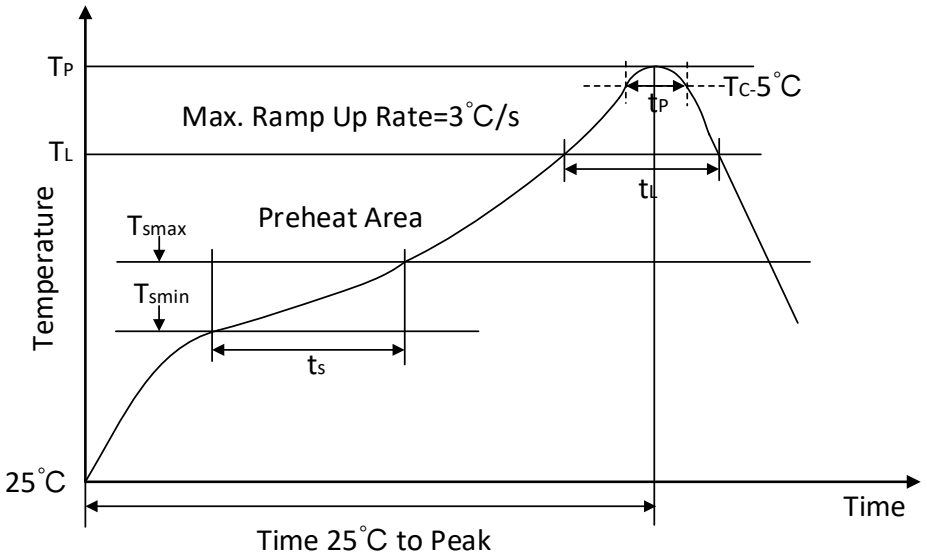


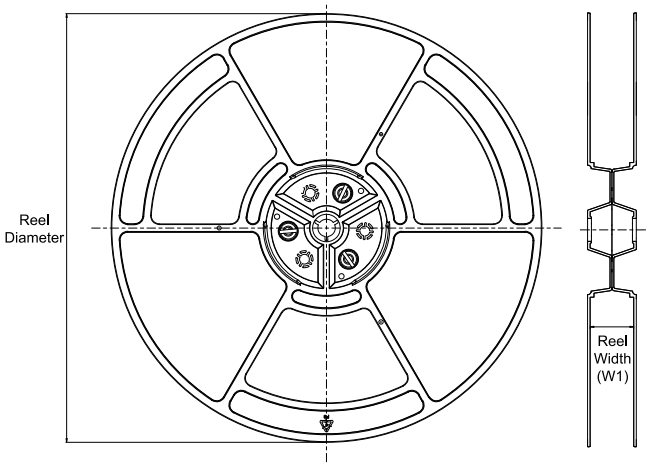
Figure 12-1. Soldering Temperature (reflow) Profile

Table 12-1. Soldering Temperature Parameter

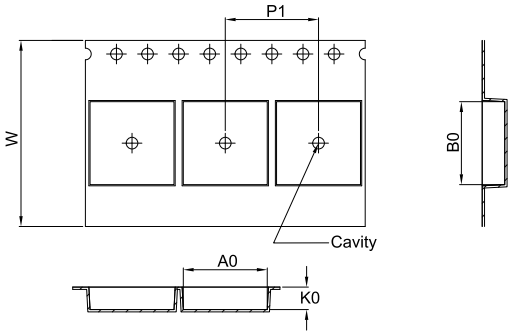
Profile Feature	Pb-Free Assembly
Average ramp-up rate(217˚C to Peak)	3˚C /second max
Time of Preheat temp(from 150˚C to 200 ˚C	60-120 second
Time to be maintained above 217˚C	60-150 second
Peak temperature	260 +5/-0 ˚C
Time within 5 ˚C of actual peak temp	30 second
Ramp-down rate	6 ˚C /second max.
Time from 25˚C to peak temp	8 minutes max

13. Tape and Reel Information

REEL DIMENSIONS

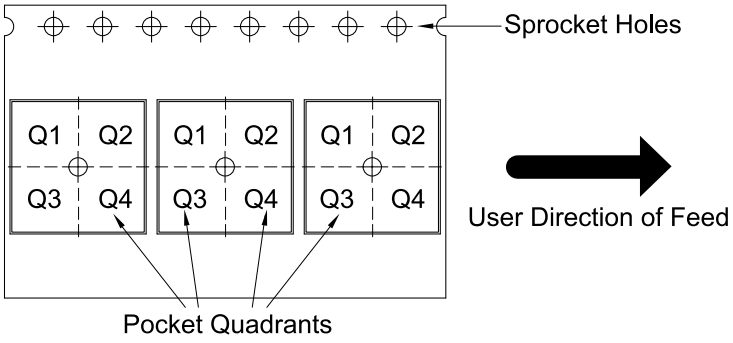


TAPE DIMENSIONS



Y0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal.

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3980S	SSOP	Y	20	2500	330	16.4	6.50	9.40	2.00	8.00	16.00	Q1
CA-IS3980P	SSOP	Y	20	2500	330	16.4	6.50	9.40	2.00	8.00	16.00	Q1
CA-IS3988P	SSOP	Y	20	2500	330	16.4	6.50	9.40	2.00	8.00	16.00	Q1

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