CS5451A

Six-channel, Delta-sigma Analog-to-digital Converter

Features

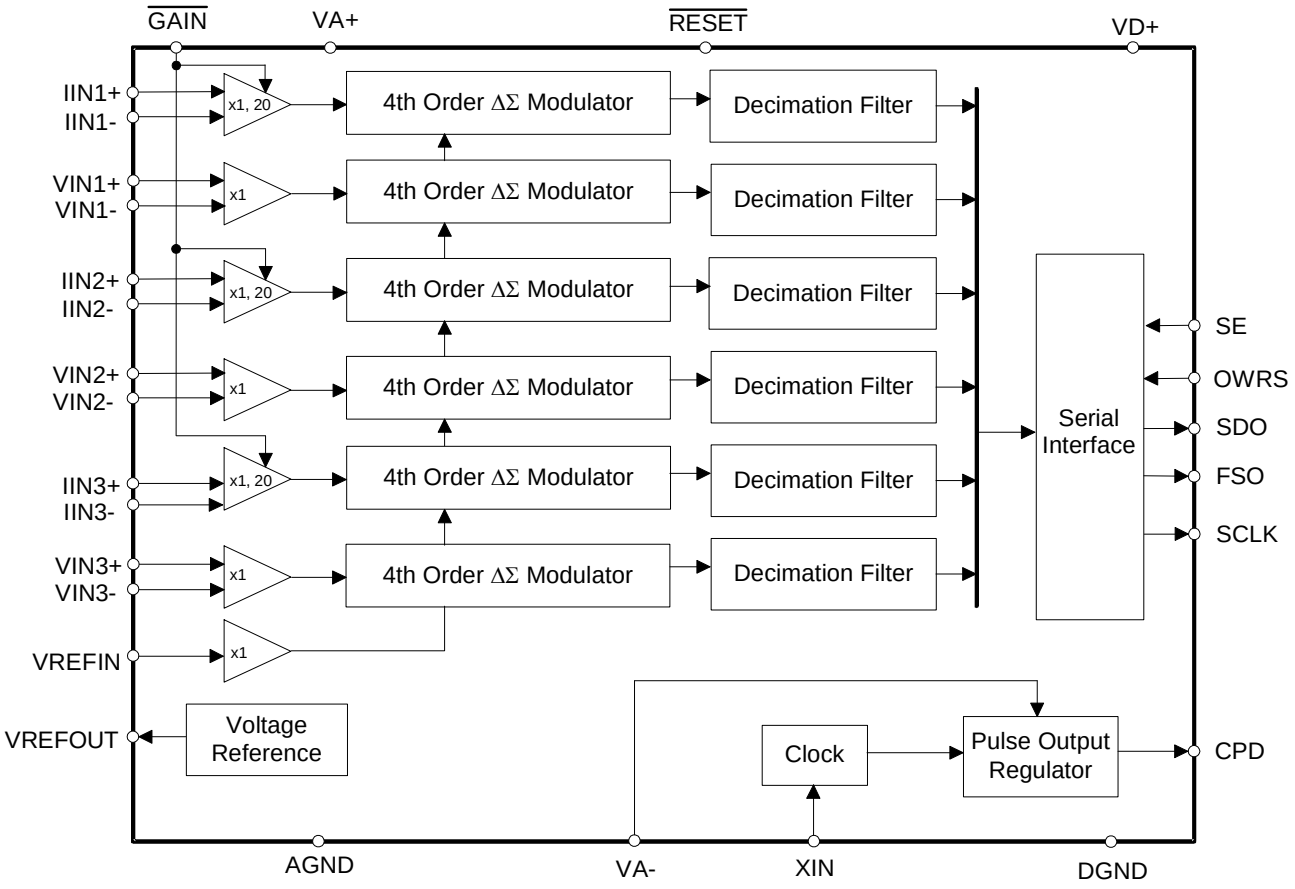
- Synchronous Sampling
- On-chip 1.2 V Reference (25 ppm/°C typ.)
- Power Supply Configurations:
  - VA+ = +3 V; VA- = -2 V; VD+ = +3 V
  - Supply Tolerances: ±10%
- Power Consumption
  - 23 mW Typical at VD+ = +3 V
- Simple Four-wire Serial Interface
- Charge pump driver output generates negative power supply.
- Ground-referenced Bipolar Inputs

Description

The CS5451A is a highly integrated delta-sigma (ΔΣ) analog-to-digital converter (ADC) developed for the power measurement industry. The CS5451A combines six ΔΣ ADCs, decimation filters, and a serial interface on a single chip. The CS5451A interfaces directly to a current transformer or shunt to measure current, and to a resistive divider or transformer to measure voltage. The product features a serial interface for communication with a microcontroller or DSP. The product is initialized and fully functional upon reset, and includes a voltage reference.

ORDERING INFORMATION:

See page 13.



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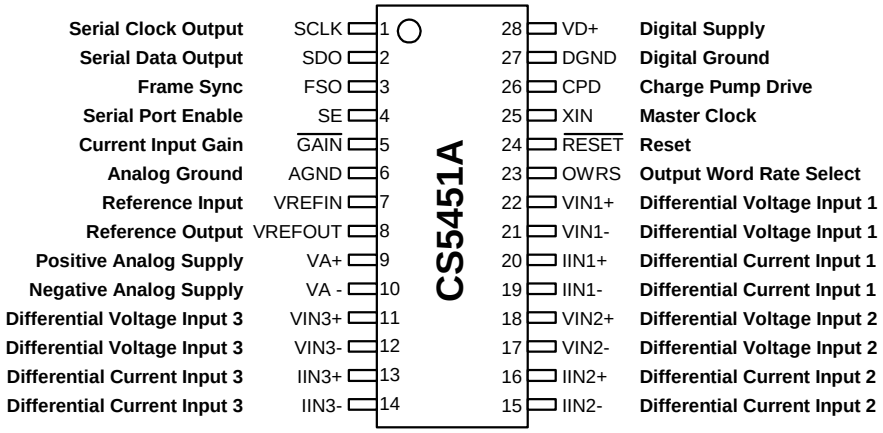


Clock Generator		
Master Clock Input	25	**XIN** - External clock signal or oscillator input.
Control Pins and Serial Data I/O		
Serial Clock Output	1	**SCLK** - Serial port clock signal that determines the output data rate for SDO pin. Rate of SCLK is dependent on the XIN frequency and state of OWRS pin.
Serial Data Output	2	**SDO** -Serial port data output pin. Data will be output at a rate defined by SCLK.
Frame Sync	3	**FSO** - Framing signal indicates when data samples are about to be transmitted on the SDO pin.
Serial Port Enable	4	**SE** - When SE is low, the output pins of the serial port are tri-stated.
Current Input Gain	5	**$\overline{\text{GAIN}}$** - A logic high sets current channel gain to 1, a logic low sets the gain to 20. If no connection is made to this pin, it will default to logic low level (through internal 200 kΩ resistor to DGND).
Output Word Rate Select	23	**OWRS** - A logic low sets the output word rate (OWR) to XIN/2048 (Hz). A logic high sets the OWR to XIN/1024 (Hz). If no connection is made to this pin, then OWRS will default to logic low level (through internal 200 kΩ resistor to DGND).
Reset	24	**$\overline{\text{RESET}}$** - Low activates Reset, all internal registers are set to their default states.
Analog Inputs/Outputs		
Voltage Reference Input	7	**VREFIN** - The input to this pin establishes the voltage reference for the on-chip modulator.
Voltage Reference Output	8	**VREFOUT** - The on-chip voltage reference output. The voltage reference has a nominal magnitude of 1.2 V and is referenced to the AGND pin on the converter.
Differential Voltage Inputs	11,12 18,17 22,21	**VIN3+, VIN3-** - Differential analog input pins for the voltage channel 3. **VIN2+, VIN2-** - Differential analog input pins for the voltage channel 2. **VIN1+, VIN1-** - Differential analog input pins for the voltage channel 1.
Differential Current Inputs	13,14 16,15 20,19	**IIN3+, IIN3-** - Differential analog input pins for the current channel 3. **IIN2+, IIN2-** - Differential analog input pins for the current channel 2. **IIN1+, IIN1-** - Differential analog input pins for the current channel 1.
Power Supply Connections		
Analog Ground	6	**AGND** - Analog ground.
Positive Analog Supply	9	**VA+** - The positive analog supply. Typical +3 V ±10% relative to AGND.
Negative Analog Supply	10	**VA-** - The negative analog supply. Typical -2 V ±10% relative to AGND.
Charge Pump Drive	26	**CPD** - Designed to drive external charge pump circuitry that will produce a negative analog supply (VA-)voltage.
Digital Ground	27	**DGND** - Digital Ground.
Positive Digital Supply	28	**VD+** - The positive digital supply. Typical +3 V ±10% relative to AGND.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Digital	VD+	2.7	3.0	3.3	V
	Positive Analog	VA+	2.7	3.0	3.3	V
	Negative Analog	VA-	-2.2	-2.0	-1.8	V
Voltage Reference Input		VREF+	-	1.2	-	V

ANALOG CHARACTERISTICS

- Min/Max characteristics and specifications are guaranteed over all Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 3 V ±10%; VA- = -2 V ±10%; AGND = DGND = 0 V; VREFIN = +1.2 V. All voltages with respect to 0 V.
- XIN = 4.096 MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (All Channels)						
Total Harmonic Distortion		THD	74	-	-	dB
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Common Mode + Signal on Input			VA-	-	VA+	V
Input Sampling Rate			-	XIN/8	-	Hz
Analog Inputs (Note 1)						
Differential Input Voltage Range	Gain=20	VIN	-	80	-	mV_{P-P}
$[(I_{IN+}) - (I_{IN-})]$ or $[(V_{IN+}) - (V_{IN-})]$	Gain=1	VIN	-	1.6	-	V_{P-P}
Bipolar Offset	Gain=20	VOS	-	±11.5	±20	mV
	Gain=1	VOS	-	±0.5	±4.0	mV
Crosstalk (Channel-to-channel)	(50, 60 Hz)		-	-105	-	dB
Input Capacitance	Gain = 20	IC	-	-	20	pF
	Gain = 1	IC	-	-	1	pF
Effective Input Impedance	Gain=20	EII	50	60	-	kΩ
	Gain=1	EII	500	600	-	kΩ
Noise (Referred to Input)						
0-60 Hz	Gain=20		-	-	1	μV_{rms}
	Gain=1		-	-	20	μV_{rms}
0-1 kHz	Gain=20		-	-	2.5	μV_{rms}
	Gain=1		-	-	50	μV_{rms}
0-2 kHz	Gain=20		-	-	3.75	μV_{rms}
	Gain=1		-	-	75	μV_{rms}
Reference Output						
Output Voltage		REFOUT	1.15	1.2	1.25	V
Temperature Coefficient			-	25	50	ppm/°C
Load Regulation	(Output Current 1 µA Source or Sink)	ΔV_R	-	6	10	mV
Power Supply Rejection		PSRR	60	-	-	dB
Reference Input						
Input Voltage Range		VREF+	1.15	1.2	1.25	V
Input Capacitance			-	-	10	pF
Input CVF Current			-	-	1	µA

ANALOG CHARACTERISTICS (continued)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies						
Power Supply Currents	I_{A+}	PSCA	-	4.0	5.3	mA
Typical VA+ = VD+ = +3 V; VA- = -2 V	I_{D+} with CPD	PSCD	-	5.0	6.3	mA
	I_{D+} without CPD	PSCD	-	1.0	1.5	mA
Power Consumption	With CPD	PC	-	27	35	mW
(Note 2)	Without CPD	PC	-	23	31	mW
Power Supply Rejection	(DC)	PSRR	50	-	-	dB
50, 60 Hz (Note 3)	Voltage Channel	PSRR	50	65	-	dB
50, 60 Hz (Note 3)	Current Channel	PSRR	60	90	-	dB

Notes:
1. Specifications for Gain = 20 apply only to Current Channels. Voltage Channels are fixed to Gain = 1
2. All outputs unloaded. All inputs CMOS level.
3. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 3 V, AGND = DGND = 0 V, VA- = -2 V (using charge-pump circuit with CPD). In addition, a 106.07 mV rms (60 Hz) sinewave is imposed onto the VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to VA-. 2048 instantaneous digital output data words are collected for the channel under test. The rms value of the digital sinusoidal output signal is calculated, and this rms value is converted into the rms value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log \left\{ \frac{106.07}{V_{eq}} \right\}$$

DIGITAL CHARACTERISTICS (See Note 4)

- Min/Max characteristics and specifications are guaranteed over all Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 3V ±10%; VA- = -2 V ±10%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- XIN = 4.096 MHz

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Characteristics						
Master Clock Frequency		XIN	3	4.096	5	MHz
Master Clock Duty Cycle			40	-	60	%
Filter Characteristics						
High Rate Filter Output Word Rate	OWRS = 0	OWR	-	XIN/2048	-	Hz
	OWRS = 1	OWR	-	XIN/1024	-	Hz
Input/Output Characteristics						
High-Level Input Voltage		V_{IH}	0.6 VD+	-	VD+	V
Low-Level Input Voltage		V_{IL}	0.0	-	0.8	V
High-Level Output Voltage	I_{out} = -5.0 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage	I_{out} = 5.0 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	(Note 5)	I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes:
4. All measurements performed under static conditions.
5. For OWRS and GAIN pins, input leakage current is 30 µA (Max).

SWITCHING CHARACTERISTICS

- Min/Max characteristics and specifications are guaranteed over all Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 3 V ±10%; VA- = -2 V ±10%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- Logic Levels: Logic 0 = 0 V, Logic 1 = VD+

Parameter		Symbol	Min	Typ	Max	Unit
Rise Times	Any Digital Input (except XIN)	t_{rise}	-	-	1.0	µs
(Note 6)	XIN only		-	-	10	ns
	Any Digital Output		-	50	-	ns
Fall Times	Any Digital Input (except XIN)	t_{fall}	-	-	1.0	µs
(Note 6)	XIN only		-	-	10	ns
	Any Digital Output		-	50	-	ns
Serial Port Timing						
Serial Clock Frequency	OWRS = "0"	SCLK	-	500	-	kHz
(Note 7)	OWRS = "1"	SCLK	-	1000	-	kHz
Serial Clock	Pulse Width High	t_1	-	0.5	-	SCLK
(Note 7 and 8)	Pulse Width Low	t_2	-	0.5	-	SCLK
SCLK falling to New Data Bit		t_3	-	-	50	ns
FSO Falling to SCLK Rising Delay	(Note 7 & 8)	t_4	-	0.5	-	SCLK
FSO Pulse Width	(Note 7 & 8)	t_5	-	1	-	SCLK
SE Rising to Output Enabled	(Note 9)	t_6	-	-	50	ns
SE Falling to Output in Tri-state		t_7	-	-	50	ns

Notes:
6. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.
7. Device parameters are specified with XIN = 4.096 MHz.
8. Device parameters are specified with OWRS = 1.
9. After SE is asserted, the states of SDO and SCLK are FSO is undefined.

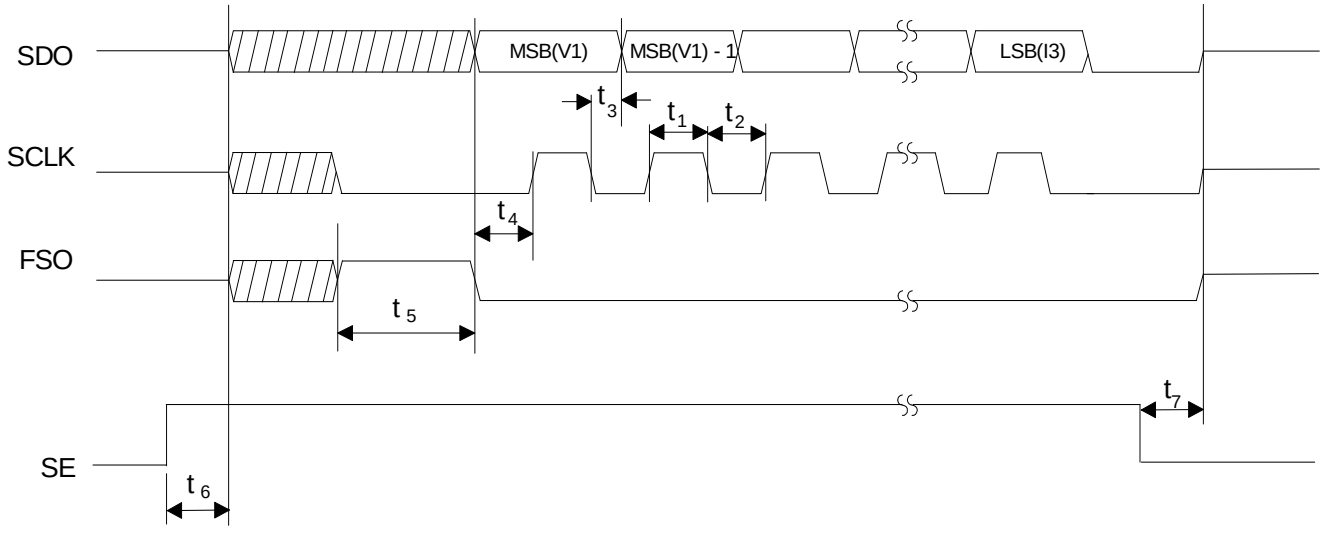


Figure 1. Serial Port Timing

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Digital Positive Analog Negative Analog	VD+ VA+ VA-	-0.3 -0.3 -2.5	- -	+3.5 +3.5 -0.3	V V V
Input Current, Any Pin Except Supplies	(Note 10 and 11)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 12)	PDN	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	(VA-) - 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes:
10. Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.
11. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.
12. Total power dissipation, including all input currents and output currents.

3. THEORY OF OPERATION

The CS5451A is a six-channel analog-to-digital converter (ADC) followed by a serial interface that allows communication with a target device. The analog inputs are structured for 3-phase power meter applications, with three dedicated voltage and current channels. Figure 2 illustrates the CS5451A typical inputs and power supply connections.

The voltage-sensing element introduces a voltage waveform on the voltage channel inputs VIN(1-3)± and is subject to a fixed 1x gain amplifier. A fourth-order delta-sigma modulator samples the amplified signal for digitization.

Simultaneously, the current-sensing element introduces a voltage waveform on the current channel input IIN(1-3)± and is subject to two selectable gains of the programmable gain amplifier (PGA). The amplified signal is sampled by a fourth-order delta-sigma modulator for digitization. Both converters sample at a rate of XIN/8, the over-sampling provides a wide dynamic range and simplified anti-alias filter design.

The decimating digital filters on all channels are $Sinc^3$ filters. The single bit data is passed to the low-pass decimation filter and output at a fixed word rate. The decimation rate is selectable for two output word rates.

The 16-bit output word is then transmitted via a master serial data port. The six-channel data is multiplexed on the serial data output and is preceded by a frame sync signal.

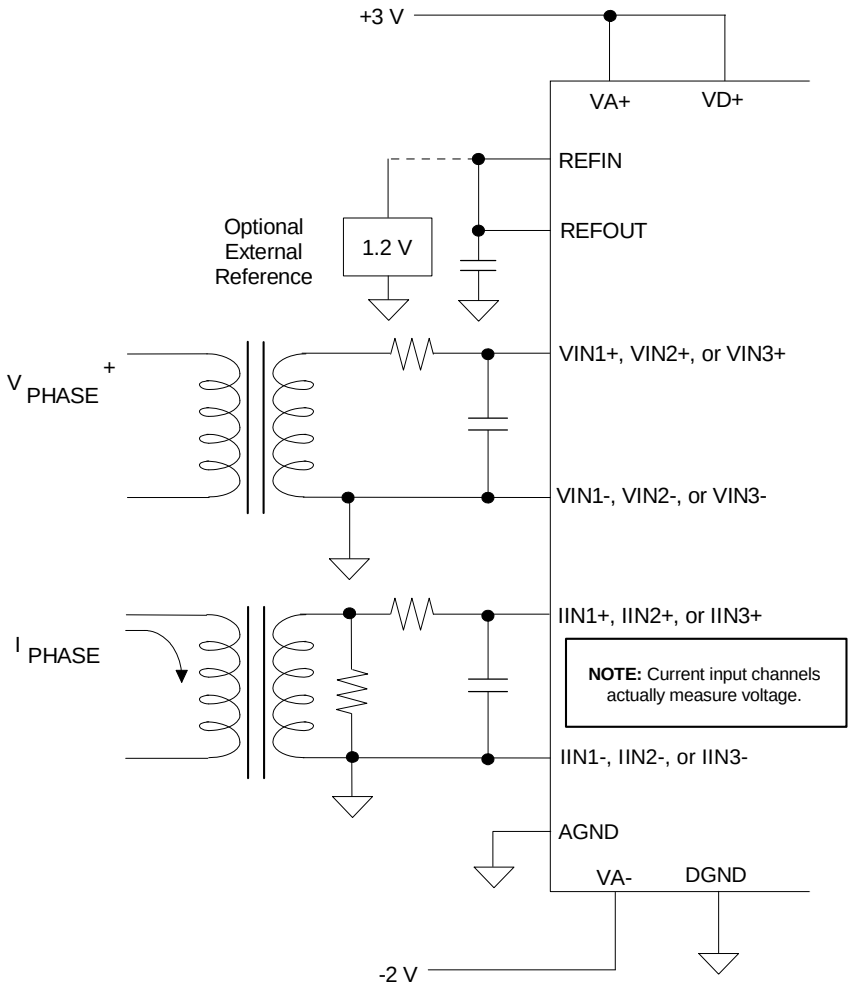


Figure 2. Typical Connection Diagram

4. FUNCTIONAL DESCRIPTION

4.1 Analog Inputs

The CS5451A is equipped with six fully differential input channels. The inputs VIN(1-3)± and IIN(1-3)± are designated as the voltage and current channel inputs, respectively. The full-scale differential input voltage for the current and voltage channel is ±800 mV_P (gain = 1x).

4.1.1 Voltage Channel

The output of the line voltage resistive divider or transformer is connected to the VIN(1-3)+ and VIN(1-3)- input pins of the CS5451A. The voltage channels are equipped with a 1x fixed gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±800 mV. If the input signal is a sine wave the maximum RMS voltage is:

$$\frac{800mV_P}{\sqrt{2}} \cong 565.69mV_{RMS}$$

which is approximately 70.7% of maximum peak voltage.

4.1.2 Current Channel

The output of the current sense resistor or transformer is connected to the IIN(1-3)+ and IIN(1-3)- input pins of the CS5451A. To accommodate different current-sensing devices the current channels incorporates a programmable gain amplifier (PGA) that can be set to one of two input ranges. Input pin $\overline{\text{GAIN}}$ (see Table 1) define the PGA's two gain selections and corresponding maximum input signal level.

$\overline{\text{GAIN}}$	Maximum Input Range	
0	±40mV	20x
1	±800mV	1x

Table 1. Current Channel PGA Setting

4.2 Digital Filters

The decimating digital filter samples the modulator bit stream at XIN/8 and produces a fixed output word rate. The digital filters are implemented as $sinc^3$ filters with the following transfer function:

$$H(z) = \left(\frac{1 - z^{-DR}}{1 - z^{-1}}\right)^3$$

The decimation rate is determined by the exponent DR (see Table 2).

The output word rate (OWR) is selected by the OWRS pin and defined by Table 2.

OWRS	DR	Output Word Rate
0	256	XIN/2048
1	128	XIN/1024

Table 2. Decimation Filter OWR

4.3 Performing Measurements

The ADC outputs are transferred in 16-bit, signed (two's complement) data formats. Table 3 defines the relationship between the differential voltage applied to any one of the input channels and the corresponding output code. Note that for the current channels, the state of the $\overline{\text{GAIN}}$ input pin is assumed to driven low such that the PGA gain on the current channels is 1x. If the PGA gain of the current channels is set to 20x, a +40 mV voltage is applied to any pair of IIN(1-3)± pins would cause an output code of 32767.

Differential Input Voltage (mV)	Output Code (hexadecimal)	Output Code (decimal)
+800	7FFF	32767
0.0122 to 0.0366	0001	1
-0.0122 to 0.0122	0000	0
-0.0122 to -0.0366	FFFF	-1
-800	8000	-32768
Notes: Assume PGA gain is set to 1x.		

Table 3. Differential Input Voltage vs. Output Code

4.4 Serial Interface

The CS5451A communicates with a target device via a master serial data output port. Output data is provided on the SDO output synchronous with the SCLK output. A third output, FSO, is a framing signal used to signal the start of output data. These three outputs will be driven as long as the SE (serial enable) input is held high. Otherwise, these outputs will be high-impedance.

Data out (SDO) changes as a result of SCLK falling, and always outputs valid data on the rising edge of SCLK. When data is being transferred the SCLK frequency is XIN/8 when OWRS is low or XIN/4 when OWRS is high.

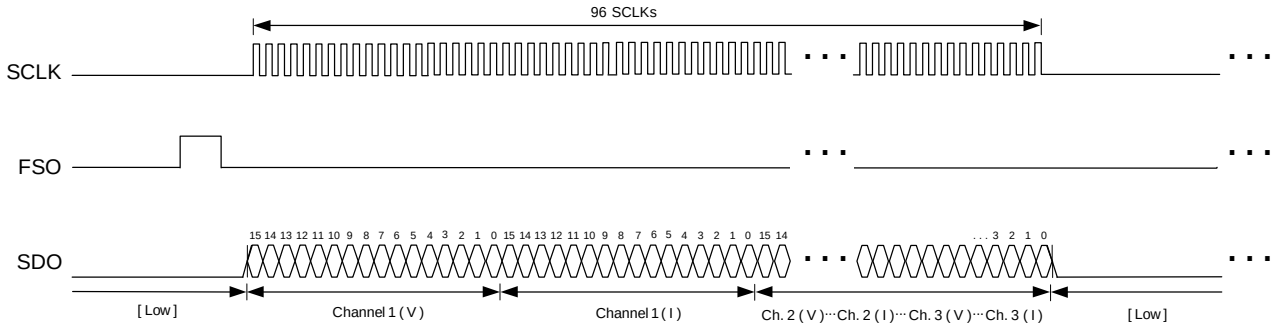


Figure 3. One Data Frame

When data is not being transferred SCLK is held low. (see Figure 3.)

The framing signal (FSO) output is normally low. FSO goes high, with a pulse width equal to one SCLK period, when the instantaneous voltage and current data samples are about to be transmitted out of the serial interface (after each A/D conversion cycle). SCLK is not active during FSO high.

For 96 SCLK periods after FSO falls, SCLK is active and SDO provides valid output. Six channels of 16-bit data are output, MSB first. Figure 4 illustrates how the voltage and current measurements are output for the three phases. SCLK will then be held low until the next sample period.

4.5 System Initialization

A hardware reset is initiated when the $\overline{\text{RESET}}$ pin is forced low with a minimum pulse width of 50 ns. When $\overline{\text{RESET}}$ is activated, all internal registers are set to a default state.

Upon powering up, the $\overline{\text{RESET}}$ pin must be held low (active) until after the power stabilizes.

4.6 Voltage Reference

The CS5451A is specified for operation with a +1.2 V reference between the VREFIN and AGND pins. The converter includes an internal 1.2 V reference that can be used by connecting the VREFOUT pin to the VREFIN pin of the device. The VREFIN can be used to connect external filtering and/or references.

4.7 Power Supply

The low, stable analog power consumption and superior supply rejection of the CS5451A allow for the use of a simple charge-pump negative supply generator. The use of a negative supply alleviates the need for level

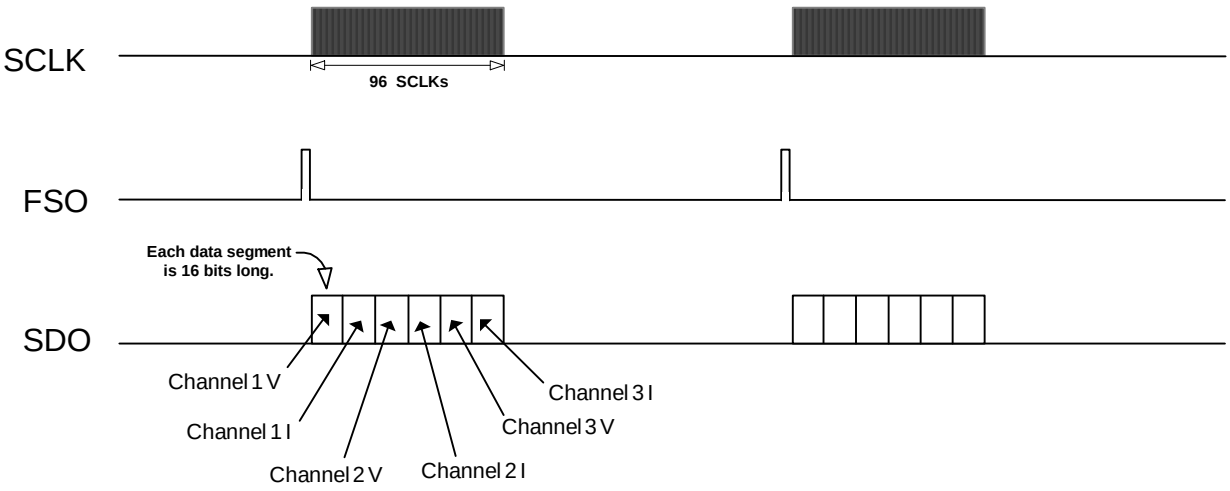


Figure 4. Serial Port Data Transfer

shifting of the analog inputs. The CPD pin and capacitor C1 provide the necessary analog supply current as shown in Figure 5. The Schottky diodes D1 and D2 are chosen for their low forward voltages and high-speed capabilities. The capacitor C2 provides the required charge storage and bypassing of the negative supply. The CPD output signal provides the charge pump driver signal. The frequency of the charge pump driver signal is synchronous to XIN. The nominal average frequency is 1 MHz. The level on the VA- pin is fed back internally so that the CPD output will regulate the VA- level to -2/3 of VA+ level.

The value of capacitor C1 (see Figure 5) is dependent on the XIN clock frequency. The 39 nF value for C1 was selected for a XIN clock frequency equal to 4.096 MHz. For more information about the operation of this type of charge pump circuit, the reader can refer to Cirrus Logic, Inc.'s application note *AN152: Using the CS5521/24/28, and CS5525/26 Charge Pump Drive for External Loads.*

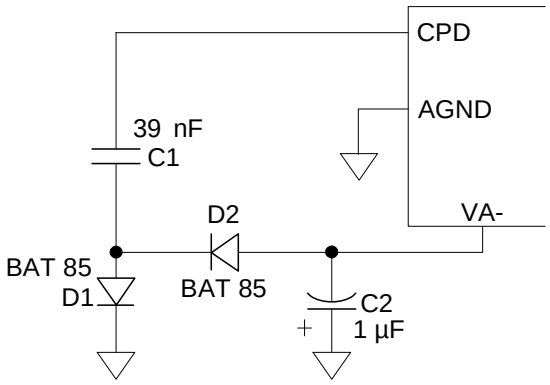
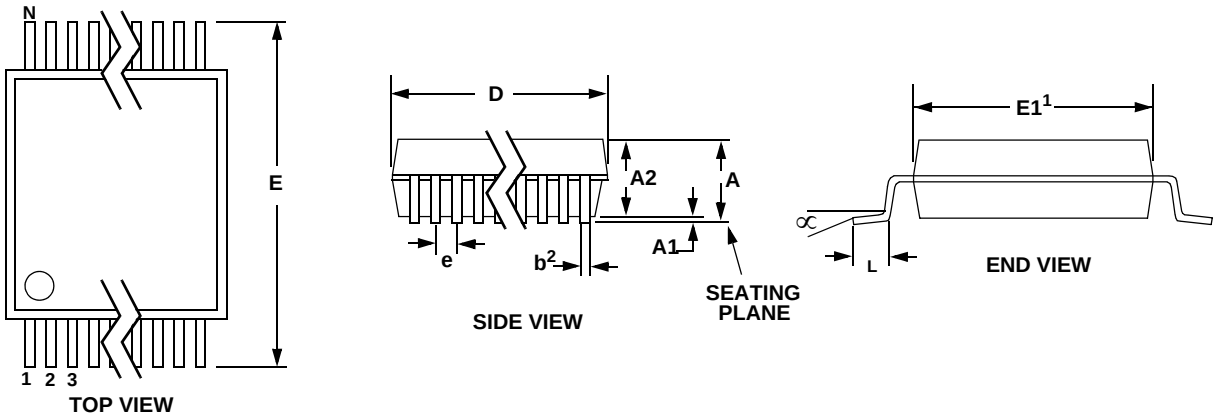


Figure 5. Generating VA- with a Charge Pump

5. PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

6. ORDERING INFORMATION

Model	Temperature	Package
CS5451A-ISZ (lead free)	-40 to +85 °C	28-pin SSOP

7. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5451A-ISZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8. REVISION HISTORY

Revision	Date	Changes
A1	JUL 2003	Initial Release
PP1	OCT 2003	Initial release for Preliminary Product Information
F1	FEB 2005	Update electrical specifications w/ most-current characterization data.
F2	AUG 2005	Update electrical specifications w/ most-current characterization data. Added MSL data.
F3	FEB 2010	Corrected typical input sampling rate from XIN/4 to XIN/8 (Hz).
F4	APR 2011	Removed lead-containing (Pb) device ordering information.

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