CDB35L00-X4

2.7 W x 4 CS35L00 Amplifier Demonstration Board

Features

- Contains 4 CS35L00 Hybrid Class-D Amplifiers
- Selectable +6 dB or +12 dB Gain
- Selectable Operational Modes
- Device Shutdown Control
- Delivers 2.7 W/Ch into 4 Ω at 10 % THD+N
- Delivers 1.6 W/Ch into 8 Ω at 10 % THD+N
- Differential Mono Analog Inputs for each CS35L00 Amplifier
- Demonstrates Recommended 4-Layer Layout and Grounding Arrangements
  - Optional Output Filter Connections
  - Optional Gain Adjustment Resistors
- Powered by Single +2.5-5.5 V Power Supply

Description

The CDB35L00-X4 demonstrates the CS35L00 high-efficiency Hybrid Class-D audio amplifier. This demonstration board implements a four-channel, quad amplifier system that delivers 2.7 W per full-bridge channel into 4-Ω loads using a single +5 V supply.

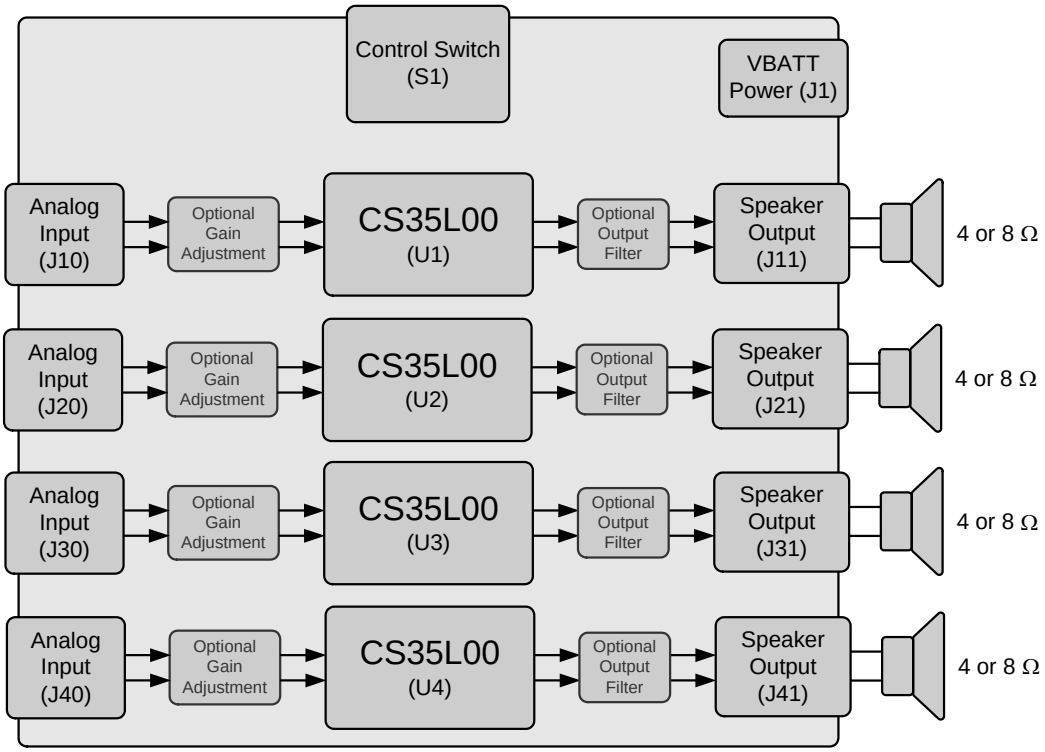
Differential audio inputs can easily be connected through the J10, J20, J30, and J40 headers. If desired, the gain can be adjusted through the optional input resistors.

Component landings are available for an optional EMI output filter.

The CDB35L00-X4 can be configured to evaluate the four operational modes and two gain settings of the CS35L00 amplifier. Mode, Gain, and Shutdown control is available through the S1 switch. Hybrid control is available through the R13, R23, R33, and R43 resistors.

ORDERING INFORMATION

CDB35L00	CS35L00-X4 Demo Board



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1. SYSTEM OVERVIEW

The CDB35L00-X4 demonstration board is an practical means for evaluating the CS35L00 2.7 W Hybrid Class-D amplifier with low idle current consumption. A differential mono analog input signal interface is provided for each device. Optional input gain and output filtering component placeholders are provided for easy modification to custom tune the CS35L00 for the user's specific system requirements.

1.1 CS35L00 Hybrid Class-D Amplifier

The CS35L00 Hybrid Class-D amplifier is a 2.7 W mono, full-bridge, closed-loop, audio amplifier available in a 10-pin, 3 mm x 3 mm, DFN package. A complete description of the CS35L00 is included in the CS35L00 product data sheet.

1.2 Power Supply

A single +2.5 to +5.5 VDC power supply is required to power the CDB35L00-X4. The supply must be capable of delivering sufficient current for the intended power output. The supply provides power to each of the four CS35L00 amplifiers. The power supply connection to the board is provided by the header J1. The positive terminal is labeled VBATT. The ground terminal is labeled GND.

1.3 Operational Modes

The CS35L00 device has 4 different operational modes. Each of the 4 operational modes requires different board configuration as described in Section 1.3.1 and Section 1.3.1.1. The operational modes of the CS35L00 are listed below. More information on the specifics of each operational mode can be found in the CS35L00 product datasheet.

- SD: Standard Class-D Mode
- FSD: Reduced Frequency Standard Class-D Mode
- HD: Hybrid Class-D Mode
- FHD: Reduced Frequency Hybrid Class-D Mode

The CDB35L00-X4 demonstration board schematic is shown in Figure 4 on page 9.

1.3.1 Operational Mode Control

Using a combination of the S1 switch and the hybrid control resistors, as described in Section 1.3.1.1, allows the CDB35L00-X4 to be configured in all 4 of the operational modes listed in Section 1.3.

Each CS35L00's MODE pin on the CDB35L00-X4 board is connected to the S1 switch labeled MODE as shown in Figure 4 on page 9. The MODE pin controls whether all four of the CS35L00 devices on the CDB35L00-X4 board are operating in one of the reduced frequency modes (FSD or FHD) or in one of the higher frequency modes (SD or HD).

	GAIN	MODE
LOW	+12 dB	FSD / FHD
HIGH	+6 dB	SD / HD

Table 1. S1 Switch GAIN & MODE Configurations

Table 1 on page 3 and Table 3 on page 5 show the S1 switch-controlled configuration options on the CDB35L00-X4 board. More configuration options are available by removing or repopulating 0 Ω resistors as described in Section 1.4.

Note: In order to avoid transient audio signals, the CS35L00 devices should be shutdown either via the S1 switch or by removing power when the operational mode is being changed.

1.3.1.1 Hybrid Control Resistor Configuration

Each CS35L00 device has a hybrid control resistor. When the hybrid control resistor for each CS35L00 is populated, it connects the LFILT+ pin to VBATT and enables the Standard Class-D functionality (SD or FSD modes) for the corresponding device. When the hybrid control resistor for each CS35L00 is not populated, LFILT+ is floating, and the Hybrid Class-D functionality (HD or FHD modes) is enabled.

The hybrid control resistors (R13, R23, R33, R43) are located on the bottom side of the board adjacent to the LFILT+ decoupling capacitor and are highlighted in blue in Figure 1.

A combination of the hybrid control resistors and the S1 MODE switch allow the CS35L00 devices (U1-U4) on the CDB35L00-X4 board to be configured in all 4 of the operational modes. There is no requirement to have the all four of the CS35L00 devices configured in the same mode. Each device can be configured to the user's requirements. Table 2 lists the configuration options available using the hybrid control resistors and the S1 MODE switch.

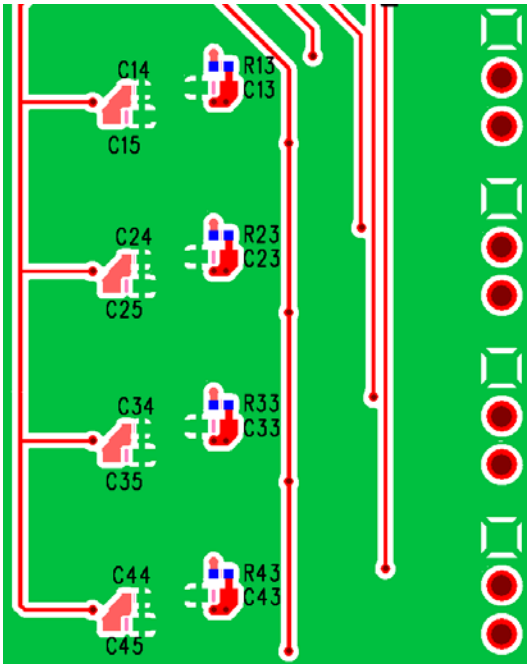

Figure 1. Hybrid Control Resistors

		S1 MODE Switch:	
		GND	**VBATT**
Hybrid Control Resistor	**R13: VBATT**	U1 = FSD	U1 = SD
	R13: Removed	U1 = FHD	U1 = HD
	R23: VBATT	U2 = FSD	U2 = SD
	R23: Removed	U2 = FHD	U2 = HD
	R33: VBATT	U3 = FSD	U3 = SD
	R33: Removed	U3 = FHD	U3 = HD
	R43: VBATT	U4 = FSD	U4 = SD
	R43: Removed	U4 = FHD	U4 = HD

Table 2. Hybrid Control Resistor & S1 Switch MODE Configurations

1.4 Shutdown Control

The S1 switch implements shutdown control for the four CS35L00 devices on the CDB35L00-X4. $\overline{\text{SD1-2}}$ controls the shutdown for U1 and U2. $\overline{\text{SD3-4}}$ controls the shutdown for U3 and U4 as shown in Table 3 and on the schematic in Figure 4 on page 9.

1.4.1 Shutdown Control Resistors

The CDB35L00-X4 contains 0 ohm resistors (R1-R4) which allow the individual CS35L00 shutdown pins to be disconnected from the S1 switch or connected to an external control device. These resistors are located on the back side of the CDB35L00-X4 board near S1, as shown highlighted in blue in Figure 2.

R1-R4 are connected to $\overline{SD}$ on U1-U4, respectively. It is recommended that the individual shutdown line pull-up resistors for U1-U4 (R10, R20, R30, R40) be left populated to help prevent the individual $\overline{SD}$ control lines from floating.

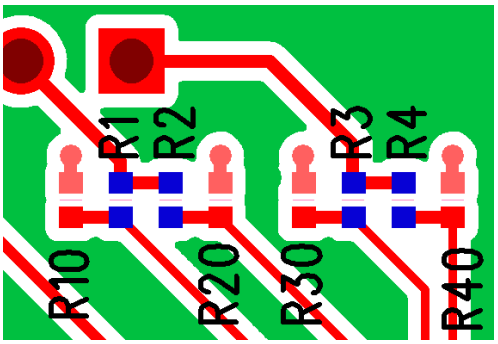

Figure 2. Shutdown Control Resistors

	SD1-2	SD3-4
LOW	U1 & U2 OFF	U3 & U4 OFF
HIGH	U1 & U2 ON	U3 & U4 ON

Table 3. S1 Switch Default Shutdown Configurations

1.5 Gain Control

The amplifier gain of the CS35L00 can be configured to operate with either a +6 dB gain or a +12 dB gain as shown in Table 1 on page 3. The amplifier gain is selectable through the GAIN setting on the S1 switch. This is connected to the GAIN_SEL pins on the four CS35L00 devices as shown in Figure 4 on page 9.

Note: The CS35L00 devices should be placed into shutdown via either the S1 switch or by removing power before changing the GAIN setting.

1.5.1 Optional Gain Adjustment Resistors

The CDB35L00-X4 contains optional gain adjustment resistor placeholders for each CS35L00 device (R11, R12, R21, R22, R31, R32, R41, R42). By default these are not populated and the CS35L00 operates at its gain control setting as set by the S1 switch. See Table 1. The gain adjustment resistors are only necessary when a gain of +6 dB or a gain of +12 dB is not desired. By adding series resistance to the input, the signal amplitude to the CS35L00 will be reduced, and will reduce the overall system gain. The typical input impedance values of the CS35L00 as well as how to calculate the resistor values for a desired gain can be found in the device datasheet.

In order to use the optional gain adjustment resistors for U1, the traces between the R11 pads and the traces between the R12 pads must be cut in order to break the bypass circuit before populating R11 and R12 with the desired resistance values. The location of these required cuts are shown in Figure 3 on page 6. After the trace between the pads has been broken, the gain adjustment resistors can be added to the board.

The gain adjustment resistors for U2, U3, and U4 can be added in the same manner as is described for U1 (above).

1.6 Differential Analog Inputs

The differential audio inputs into the four CS35L00 devices are provided by the 3-pin headers (J10, J20, J30, and J40) through DC blocking capacitors (C11, C12, C21, C22, C31, C32, C41, C42). The DC blocking capacitors allow for an analog source to connect directly to the CS35L00, regardless of any DC bias that may be present between the analog audio source's outputs and the CS35L00 inputs.

1.7 Speaker Outputs

The four CS35L00 power outputs pairs are each configured for a single, full-bridge, audio channel. The outputs are routed through an optional EMI output filter and then presented at the J11, J21, J31, and J41 headers. The CS35L00 is intended to be used with a 4 to 8 Ω load.

1.7.1 Optional Speaker Output EMI Filter Components

The CDB35L00-X4 contains optional placeholders for a series ferrite bead (FB11, FB12, FB21, FB22, FB31, FB32, FB41, FB42) and shunt capacitor (C16, C17, C26, C27, C36, C37, C46, C47) output filter. For most applications with very short speaker leads between the CS35L00 and the speaker, use of these components will not be necessary. However, for systems with long signal paths between the CS35L00 and the speaker or if the system requires connecting to cables off the PCB, it is suggested that the ferrite bead and capacitor are populated with the recommended values shown in Table 6 on page 10. These optional output filters will reduce EMI between the CS35L00 speaker outputs and the load.

In order to use the optional output filter ferrite beads for U1, the traces between the FB11 pads and the traces between the FB12 pads must be cut to break the bypass circuit, before populating FB11 and FB12 with the desired component values. The location of these required cuts are shown in below in Figure 3.

The optional output filter ferrite beads for U2, U3, and U4 can be added in the same manner as described for U1 (above). The optional output filter capacitors can be populated with or without the addition of the ferrite beads and require no board modifications.

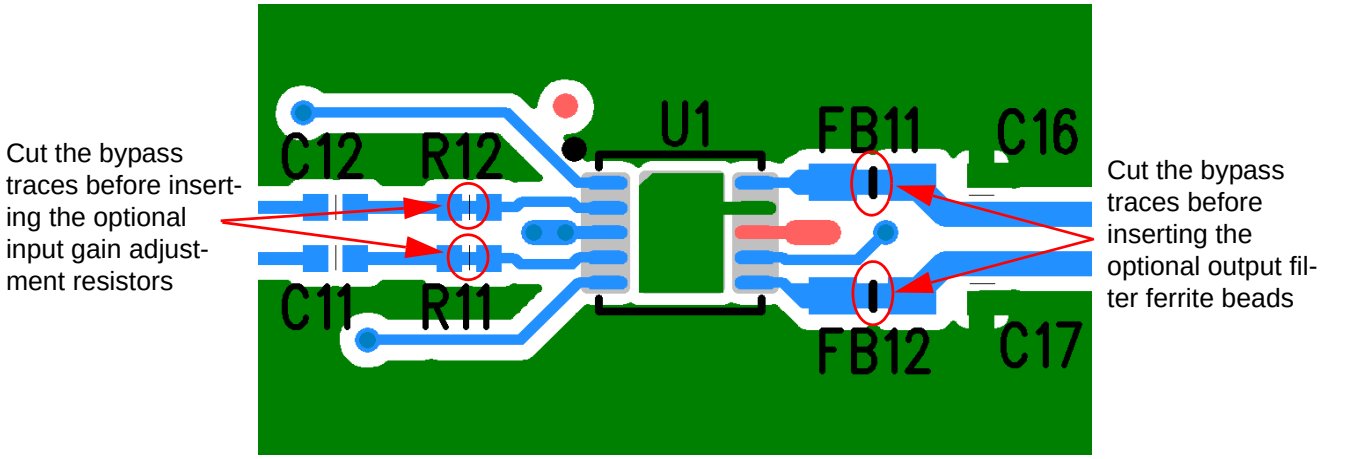

Figure 3. Optional Bypass Trace Cut Locations for U1

2. GROUNDING AND POWER SUPPLY DECOUPLING

The CS35L00 requires careful attention to power supply and grounding arrangements to optimize performance and minimize radiated emissions. The device decoupling capacitors should be located as close to the CS35L00 as possible. This can be optimized by using both top and bottom side component population as demonstrated by the CDB35L00-X4 board.

2.1 Power Supply Decoupling

Proper power supply decoupling is one key to maximizing the performance of a Class-D amplifier. Figure 5 and Figure 6 on page 11 show the component placement for the CDB35L00-X4 board. Note the addition of the C13, C23, C33, and C43 capacitors connected to the LFILT+ pin. This pin is used as decoupling for the internal LDO regulator when operating in HD or FHD modes.

The small value decoupling capacitors are placed as close as possible to the power pins of the CS35L00 on the CDB35L00-X4 board. It is recommended that the power supply decoupling capacitors reside on the opposite side of the board from which the CS35L00 is populated on. This allows for very close placement of the decoupling capacitors to the power supply pins of the CS35L00 without interfering with the differential audio inputs or differential audio outputs. This placement keeps the high-frequency current loop small to minimize EMI.

2.2 Electromagnetic Interference (EMI)

This reference design is a board-level solution that is meant to control emissions by minimizing and suppressing them at the source, in contrast to containing them in an enclosure.

2.2.1 Suppression of EMI at the Source

Several techniques are used in the circuit design and board layout to minimize high-frequency fields in the immediate vicinity of the high-power components. Specific techniques include the following:

- As mentioned in Section 2.1, effective power supply decoupling of high-frequency currents and minimizing the loop area of the decoupling loop is one aspect of minimizing EMI.
- Differential input and output signals should be routed differentially whenever possible.
- A solid ground plane on the adjacent PCB layer underneath all high-frequency traces to minimize the loop area of the return path.
- Optional output EMI filter component landings are available as described in Section 1.7.1, if emissions need to be further reduced.
- Keeping the switching output filter components as close to the amplifier as possible.

3. SYSTEM CONNECTORS AND JUMPERS

Connector Name	Reference Designator	Pin	Signal Direction	Connector Function
VBATT	J1	1	Input	Positive connection from power supply, +2.5 to +5.5 VDC
GND	J1	2	Input	GND connection from power supply.
GND	J10	1	GND	GND reference connection
IN1-	J10	2	Input	Differential analog input (-) to CS35L00, U1
IN1+	J10	3	Input	Differential analog input (+) to CS35L00, U1.
OUT1-	J11	1	Output	Analog output (-) from CS35L00, U1
OUT1+	J11	2	Output	Analog output (+) from CS35L00, U1.
GND	J20	1	GND	GND reference connection
IN2-	J20	2	Input	Differential analog input (-) to CS35L00, U2
IN2+	J20	3	Input	Differential analog input (+) to CS35L00, U2.
OUT2-	J21	1	Output	Analog output (-) from CS35L00, U2
OUT2+	J21	2	Output	Analog output (+) from CS35L00, U2.
GND	J30	1	GND	GND reference connection
IN3-	J30	2	Input	Differential analog input (-) to CS35L00, U3
IN3+	J30	3	Input	Differential analog input (+) to CS35L00, U3.
OUT3-	J31	1	Output	Analog output (-) from CS35L00, U3
OUT3+	J31	2	Output	Analog output (+) from CS35L00, U3.
GND	J40	1	GND	GND reference connection
IN4-	J40	2	Input	Differential analog input (-) to CS35L00, U4
IN4+	J40	3	Input	Differential analog input (+) to CS35L00, U4.
OUT4-	J41	1	Output	Analog output (-) from CS35L00, U4
OUT4+	J41	2	Output	Analog output (+) from CS35L00, U4.

Table 4. System Input and Output Connections

S1 Control Name	Function	Function Selected
GAIN	Gain U1-U4	Low = CS35L00 gain set to +12 dB High = CS35L00 gain set to +6 dB
MODE	Mode U1-U4	Low = CS35L00 frequency reduced operational mode (FSD or FHD) High = CS35L00 non-frequency reduced operational mode (SD or HD)
$\overline{\text{SD1-2}}$	Shutdown U1 & U2	Low = CS35L00 shutdown enabled High = CS35L00 shutdown disabled
$\overline{\text{SD3-4}}$	Shutdown U3 & U4	Low = CS35L00 shutdown enabled High = CS35L00 shutdown disabled

Table 5. S1 Switch Settings

4. CDB SCHEMATIC

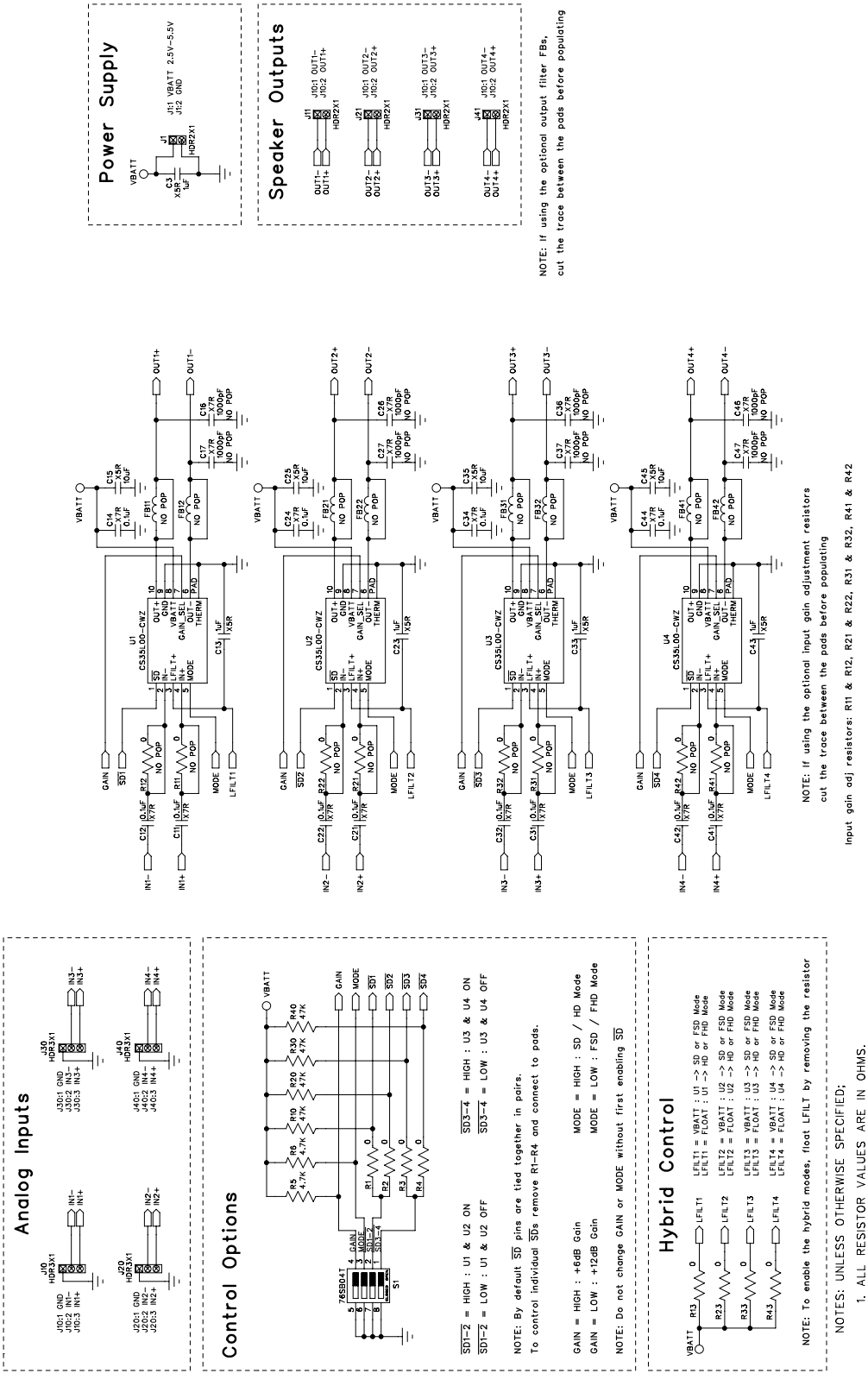

Figure 4. CDB35L00-X4 Schematic

4.1 Bill of Materials

The component listing below is shown for the CDB35L00-X4 board. Unpopulated (DNP) components are listed with recommended components for reference purposes.

Qty	Reference Designator(s)	Description	MFG / Part Number
1	C3	Capacitor, 1 µF, X5R, 10V	Kemet / C0603C105K8PAC
8	C11, C12, C21, C22, C31, C32, C41, C42	Capacitor, 0.1 µF, X7R, 16V	Kemet / C0402C104K4RAC
4	C13, C23, C33, C43	Capacitor, 1 µF, X5R, 10V	Kemet / C0603C105K8PAC
4	C15, C25, C35, C45	Capacitor, 10 µF, X5R, 6.3 V	Kemet / C0603C106M9PAC
4	C14, C24, C34, C44	Capacitor, 0.1 µF, X7R, 16V	Kemet / C0402C104K4RAC
2	R5, R6	Resistor, 4.7 kΩ, 1/10W	Dale / CRCW06034K70JNEA
8	R1, R2, R3, R4, R13, R23, R33, R43	Resistor, 0 Ω, 1/16W	Yageo / RC0402JR-070RL
4	R10, R20, R30, R40	Resistor, 47 kΩ, 1/16W	Dale / CRCW040247K0JNED
4	U1, U2, U3, U4	Hybrid Class-D DFN Amp	Cirrus Logic / CS35L00-CWZ
1	S1	Switch, 4 POS, DIP	Grayhill / 76SB04T
(DNP)	C16, C17, C26, C27, C36, C37, C46, C47	Capacitor, 1 nF, X7R, 50V	Murata / GRM155R71H102KA01D
(DNP)	FB11, FB12, FB21, FB22, FB31, FB32, FB41, FB42	Ferrite Bead, 220 Ω @ 100MHz	TDK / MPZ1608S221A
(DNP)	R11, R12, R21, R22, R31, R32, R41, R42	Resistor, 0 Ω, 1/16W	Yageo / RC0402JR-070RL

Table 6. Bill of Materials Listing

5. CDB LAYOUT

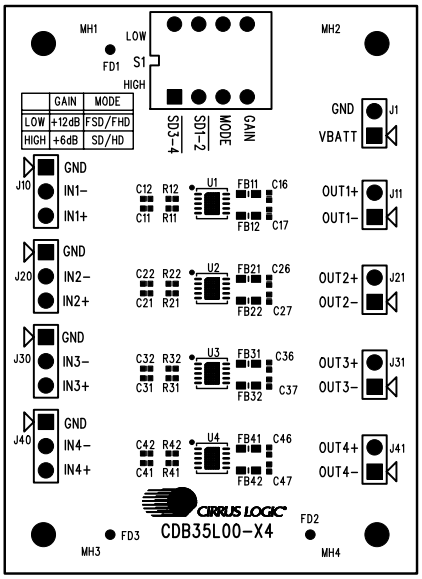

Figure 5. CDB35L00-X4 Top Side Component Placement

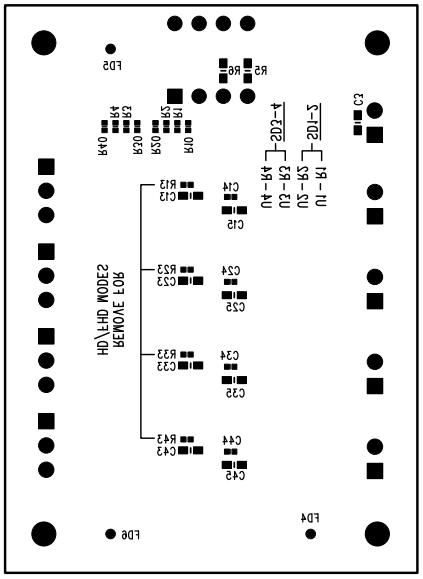

Figure 6. CDB35L00-X4 Bottom Side Component Placement

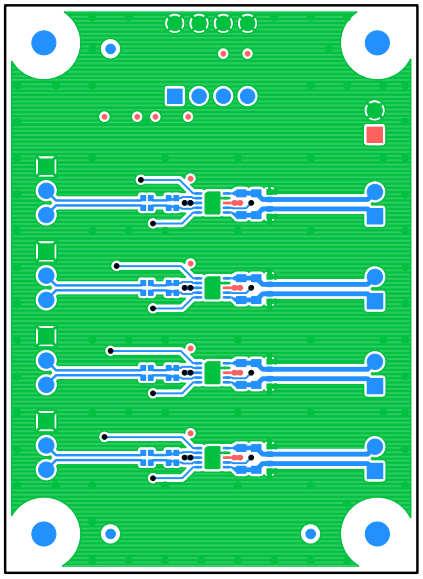

Figure 7. CDB35L00-X4 Layer 1 Copper

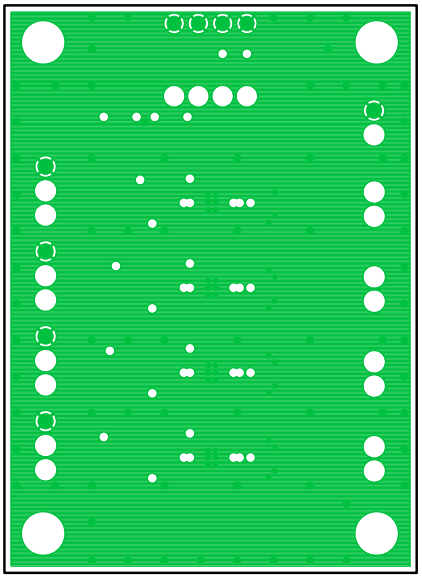

Figure 8. CDB35L00-X4 Layer 2 Copper

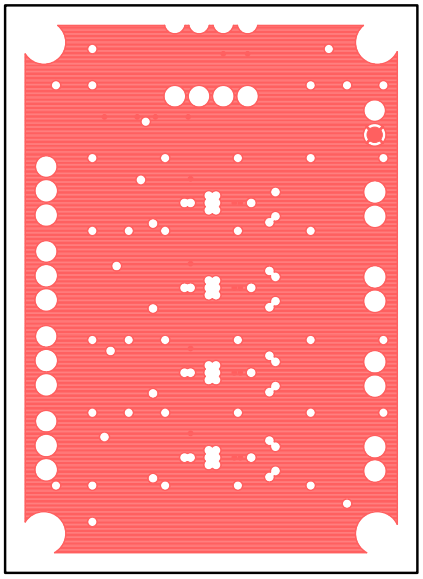

Figure 9. CDB35L00-X4 Layer 3 Copper

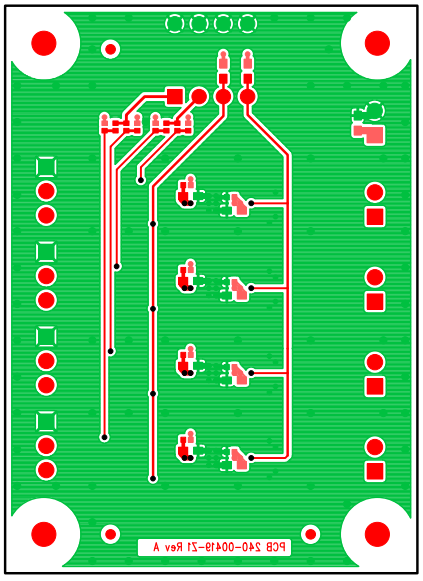

Figure 10. CDB35L00-X4 Layer 4 Copper

6. REVISION HISTORY

Release	Changes
DB1	– Initial Release
DB2	– Updated 10% output power numbers on the front page to match DS906A2 device datasheet. – Updated Figure 4 on page 9 to match the updated CDB35L00-X4 Rev A1 schematic. – Updated BOM values for C6 & C7 in Table 6 on page 10 to match the udpated Rev A1 schematics and the typical connection diagram in the DS906A2 device datasheet. All CDB35L00-X4 boards with an assembly date of 02/15/10 or earlier contain components from the Rev A0 BOM.

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