WM8214

40MSPS 16-bit CCD Digitiser

DESCRIPTION

The WM8214 is a 16-bit analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 40MSPS.

The device includes three analogue signal processing channels each of which contains Reset Level Clamping, Correlated Double Sampling and Programmable Gain and Offset adjust functions. Three multiplexers allow single channel processing. The output from each of these channels is time multiplexed into a single high-speed 16-bit Analogue to Digital Converter. The digital output data is available in 8-bit wide multiplexed format and there is also an optional single byte output mode, or 4-bit multiplexed LEGACY mode.

An internal 4-bit DAC is supplied for internal reference level generation. This may be used during CDS to reference CIS signals or during Reset Level Clamping to clamp CCD signals. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

Using an analogue supply voltage of 3.3V and a digital interface supply of 3.3V, the WM8214 typically only consumes 390mW.

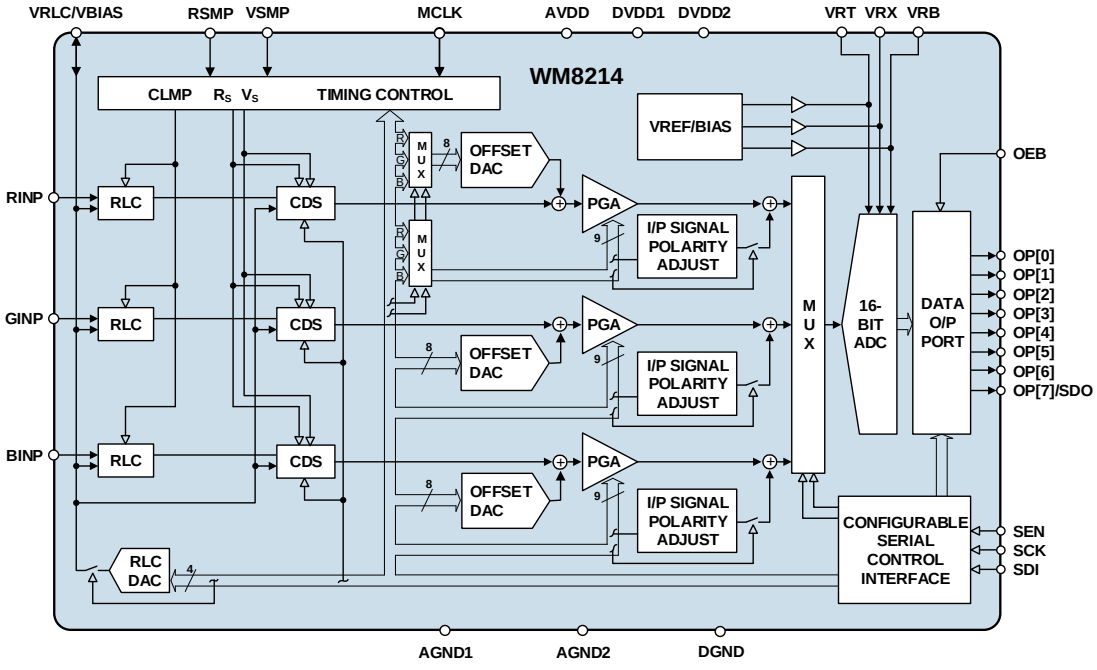
FEATURES

- 16-bit ADC
- 40MSPS conversion rate
- Low power – 390mW typical
- 3.3V single supply operation
- Single, 2 or 3 channel operation
- Correlated double sampling
- Programmable gain (9-bit resolution)
- Programmable offset adjust (8-bit resolution)
- Flexible clamp control with programmable clamp voltage
- Flexible timing, can be made compatible with WM819X and WM815X parts.
- 8-bit wide multiplexed data output format
- 8-bit only output mode
- 4-bit LEGACY multiplexed nibble mode
- Internally generated voltage references
- 28-lead SSOP package, pin compatible with WM8199
- Serial control interface

APPLICATIONS

- High speed USB2.0 compatible scanners
- Multi-function peripherals
- High-performance CCD sensor interface
- Digital Copiers

BLOCK DIAGRAM



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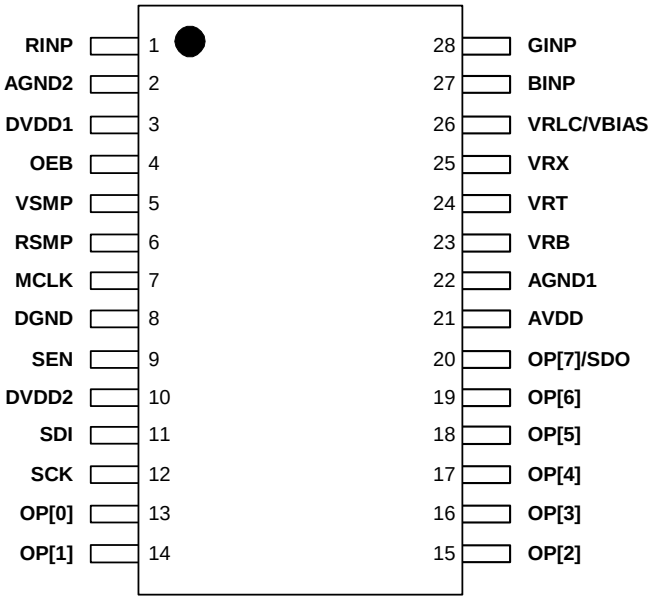
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE	PEAK SOLDERING TEMPERATURE
WM8214SCDS/V	0 to 70°C	28-lead SSOP (Pb-free)	260°C
WM8214SCDS/RV	0 to 70°C	28-lead SSOP (Pb-free, tape and reel)	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION	
1	RINP	Analogue input	Red channel input video.	
2	AGND2	Supply	Analogue ground reference.	
3	DVDD1	Supply	Digital supply for logic and clock generator. This must be operated at the same potential as AVDD.	
4	OEB	Digital input	Output Hi-Z control, all digital outputs disabled when register bit OEB = 1 or register bit OPD = 1.	
5	VSMP	Digital input	Video sample timing pulse.	
6	RSMP	Digital input	Reset sample timing pulse (also used for RLC control).	
7	MCLK	Digital input	Master (ADC) clock. This determines the ADC conversion rate.	
8	DGND	Supply	Digital ground reference.	
9	SEN	Digital input	Enables the serial interface when high.	
10	DVDD2	Supply	Digital supply, all digital I/O pins.	
11	SDI	Digital input	Serial data input.	
12	SCK	Digital input	Serial clock.	
			Digital multiplexed output data bus. ADC output data (d15:d0) is available in multiplexed format as shown. See 'Output Formats' description in Device Description section for details of other output modes.	
			A	**B**
13	OP[0]	Digital output	d8	d0
14	OP[1]	Digital output	d9	d1
15	OP[2]	Digital output	d10	d2
16	OP[3]	Digital output	d11	d3
17	OP[4]	Digital output	d12	d4
18	OP[5]	Digital output	d13	d5
19	OP[6]	Digital output	d14	d6
20	OP[7]/SDO	Digital output	d15	d7
			Alternatively, pin OP[7]/SDO may be used to output register read-back data when register bit OEB = 0, OPD = 0 and SEN has been pulsed high. See Serial Interface description in Device Description section for further details.	
21	AVDD	Supply	Analogue supply. This must be operated at the same potential as DVDD1.	
22	AGND1	Supply	Analogue ground reference.	
23	VRB	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.	
24	VRT	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.	
25	VRX	Analogue output	Input return bias voltage. This pin must be connected to AGND via a decoupling capacitor.	
26	VRLC/VBIAS	Analogue I/O	Selectable analogue output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. VRLC can be externally driven if programmed Hi-Z.	
27	BINP	Analogue input	Blue channel input video.	
28	GINP	Analogue input	Green channel input video.	

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD	GND - 0.3V	GND + 5V
Digital supply voltages: DVDD1 – 2	GND - 0.3V	GND + 5V
Digital ground: DGND	GND - 0.3V	GND + 0.3V
Analogue grounds: AGND1 – 2	GND - 0.3V	GND + 0.3V
Digital inputs, digital outputs and digital I/O pins	GND - 0.3V	DVDD2 + 0.3V
Analogue inputs (RINP, GINP, BINP)	GND - 0.3V	AVDD + 0.3V
Other pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	0°C	+70°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. GND denotes the voltage of any ground pin.
2. AGND1, AGND2 and DGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range	T_A	0		70	°C
Analogue supply voltage	AVDD	2.97	3.3	3.63	V
Digital core supply voltage	DVDD1	2.97	3.3	3.63	V
Digital I/O supply voltage	DVDD2	2.97	3.3	3.63	V

Notes:

1. DVDD2 should be operated at the same potential as DVDD1 ± 0.3V.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Performance						
Thermal resistance – junction to case	$R_{\theta JC}$	$T_{ambient}$ = 25°C		23.9		°C/W
Thermal resistance – junction to ambient	$R_{\theta JA}$			67.1		°C/W

Notes:

1. Figures given are for package mounted on 4-layer FR4 according to JESD51-5 and JESD51-7.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = DVDD1 = DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 40MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 16-bit ADC, PGA, Offset and CDS functions)						
Conversion rate				40		MSPS
Full-scale input voltage range (see Note 1)		LOWREFS=0, Max Gain LOWREFS=0, Min Gain		0.25 3.03		Vp-p Vp-p
		LOWREFS=1, Max Gain LOWREFS=1, Min Gain		0.15 1.82		Vp-p Vp-p
Input signal limits (see Note 2)	V_{IN}		AGND-0.3		AVDD+0.3	V
Input Capacitance				10		pF
Input Impedance				50		Ω
Full-scale transition error		Gain = 0dB; PGA[8:0] = 18(hex)		20		mV
Zero-scale transition error		Gain = 0dB; PGA[8:0] = 18(hex)		20		mV
Differential non-linearity	DNL			1		LSB
Integral non-linearity	INL			25		LSB
Channel to channel gain matching				1%		%
Total output noise		Min Gain Max Gain		15 140		LSB rms LSB rms
References						
Upper reference voltage	VRT	LOWREFS=0 LOWREFS=1	1.95	2.05 1.85	2.25	V
Lower reference voltage	VRB	LOWREFS=0 LOWREFS=1	0.95	1.05 1.25	1.25	V
Input return bias voltage	VRX			1.25		V
Diff. reference voltage (VRT-VRB)	V_{RTB}	LOWREFS=0 LOWREFS=1	0.90	1.0 0.6	1.10	V
Output resistance VRT, VRB, VRX				1		Ω
Reset-Level Clamp (RLC) circuit/ Reference Level DAC						
RLC switching impedance				50		Ω
VRLC short-circuit current				2		mA
VRLC output resistance				2		Ω
VRLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
Reference RLCDAC resolution				4		bits
Reference RLCDAC step size	$V_{RLCSTEP}$	AVDD=3.3V RLCDACRNG=0		0.173		V/step
Reference RLCDAC step size	$V_{RLCSTEP}$	RLCDACRNG=1		0.11		V/step
Reference RLCDAC output voltage at code 0(hex)	V_{RLCBOT}	AVDD=3.3V, RLCDACRNG=0		0.4		V
Reference RLCDAC output voltage at code 0(hex)	V_{RLCBOT}	RLCDACRNG=1		0.4		V
Reference RLCLDAC output voltage at code F(hex)	V_{RLCTOP}	AVDD=3.3V, RLCDACRNG=0		3.0		V
Reference RLCDAC output voltage at code F(hex)	V_{RLCTOP}	RLCDACRNG = 1		2.05		V
RLCDAC	DNL		-0.5		+0.5	LSB
RLCDAC	INL			+/-1		LSB

Notes:

1. **Full-scale input voltage** denotes the peak input signal amplitude that can be gained to match the ADC full-scale input range.
2. **Input signal limits** are the limits within which the full-scale input voltage signal must lie.

Test Conditions

AVDD = DVDD1 = DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 40MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.1	0.5	LSB
Integral non-linearity	INL			0.25	1	LSB
Step size				2.04		mV/step
Output voltage		Code 00(hex) Code FF(hex)		-260 +260		mV mV
Programmable Gain Amplifier						
Resolution				9		bits
Gain equation			$0.66 + \frac{7.34}{511} * PGA[8:0]$			V/V
Max gain, each channel	G_{MAX}			7.8		V/V
Min gain, each channel	G_{MIN}			0.68		V/V
Channel Matching				1	5	%
Analogue to Digital Converter						
Resolution				16		bits
Speed					40	MSPS
Full-scale input range (2*(VRT-VRB))		LOWREFS=0 LOWREFS=1		2 1.2		V V
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.7 * DVDD2			V
Low level input voltage	V_{IL}				0.2 * DVDD2	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF
Digital Outputs						
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZ}				1	µA
Digital IO Pins						
Applied high level input voltage	V_{IH}		0.7 * DVDD2			V
Applied low level input voltage	V_{IL}				0.2 * DVDD2	V
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Low level input current	I_{IL}				1	µA
High level input current	I_{IH}				1	µA
Input capacitance	C_I			5		pF
High impedance output current	I_{OZ}				1	µA
Supply Currents						
Total supply current – active (Analogue and Digital) (Three channel mode)				118		mA
Analogue supply current -active (three channel mode)				105		mA
Digital supply current - active (three channel mode)				13		mA
Supply current – full power down mode				20		µA

INPUT VIDEO SAMPLING

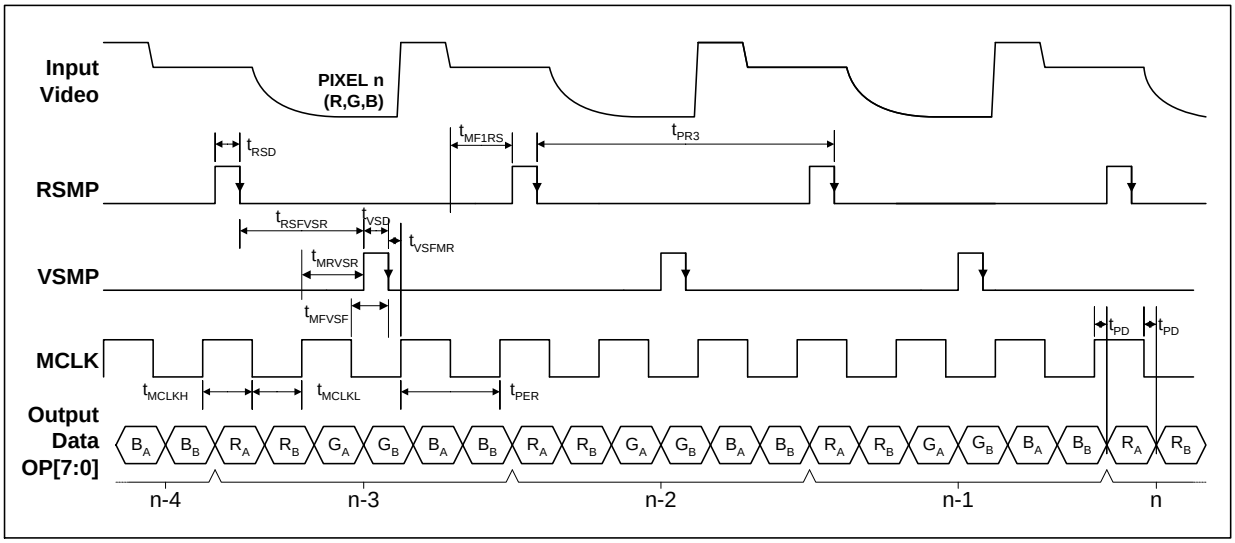


Figure 1 Three-channel CDS Input Video Timing

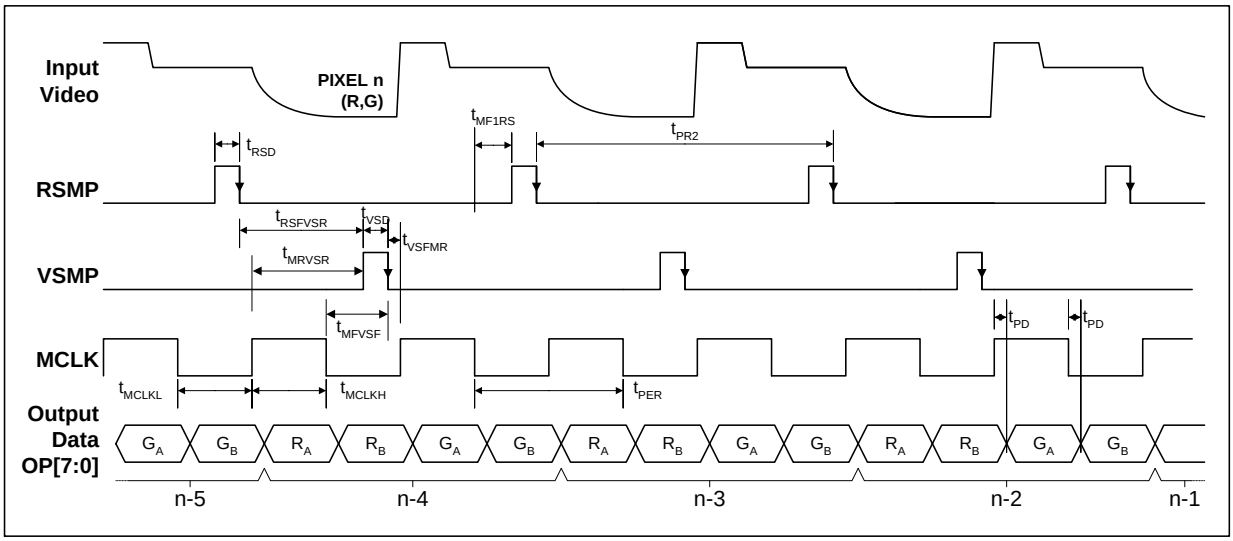


Figure 2 Two-channel CDS Input Video Timing

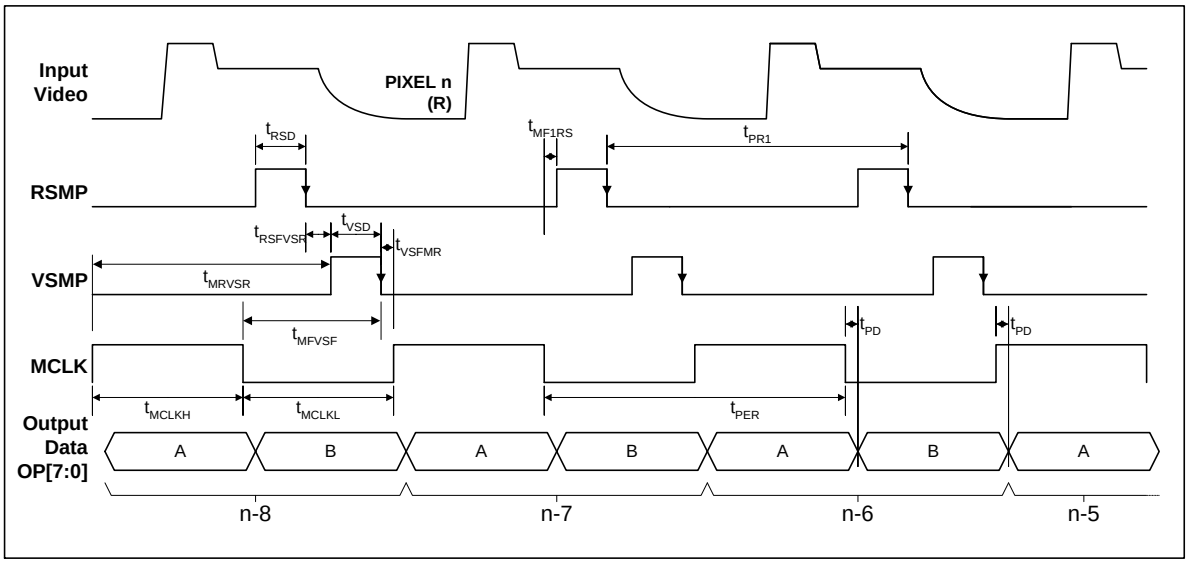


Figure 3 Single-channel CDS Input Video Timing

Notes:

1. The relationship between input video and sampling is controlled by VSMP and RSMP.
2. When VSMP is high the input video signal is connected to the Video sampling capacitors.
3. When RSMP is high the input video signal is connected to the Reset sampling capacitors.
4. RSMP must not go high before the first falling edge of MCLK after VSMP goes low.
5. It is required that the falling edge of VSMP should occur before the rising edge of MCLK.
6. In 1-channel CDS mode it is not possible to have a equally spaced Video and Reset sample points with a 40MHz MCLK
7. Non-CDS operation is also possible; RSMP is not required in this mode.

Test Conditions

AVDD = DVDD1 = DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 40MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period	t_{PER}		25			ns
MCLK high period	t_{MCLKH}		11.3	12.5		ns
MCLK low period	t_{MCLKL}		11.3	12.5		ns
RSMP pulse high time	t_{RSD}		5			ns
VSMP pulse high time	t_{VSD}		5			ns
RSMP falling to VSMP rising time	t_{RSFVSR}		0			ns
MCLK rising to VSMP rising time	t_{MRVSR}		3			ns
MCLK falling to VSMP falling time	t_{MFVSF}		5			ns
VSMP falling to MCLK rising time [2]	t_{VSFMR}		1			ns
1st MCLK falling edge after VSMP falling to RSMP rising time	t_{MF1RS}		1			ns
3-channel mode pixel rate	t_{PR3}		75			ns
2-channel mode pixel rate	t_{PR2}		50			ns
1-channel mode pixel rate	t_{PR1}		25			ns
Output propagation delay	t_{PD}			5	10	ns
Output latency. From 1st rising edge of MCLK after VSMP falling to data output	LAT			7		MCLK periods

Notes:

1. Parameters are measured at 50% of the rising/falling edge.
2. In Single-Channel mode, if the VSMP falling edge is placed more than 3ns before the rising edge of MCLK the output amplitude of the WM8214 will decrease.

SERIAL INTERFACE

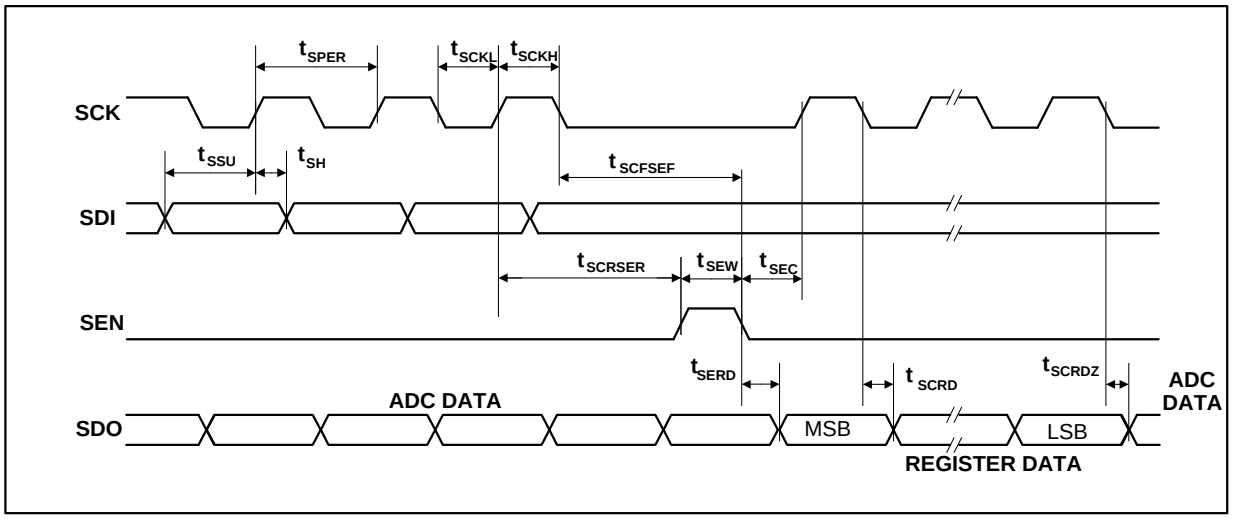


Figure 4 Serial Interface Timing

Test Conditions

AVDD = DVDD1 = DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 40MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCK period	t_{SPER}		83.3			ns
SCK high	t_{SCKH}		37.5			ns
SCK low	t_{SCKL}		37.5			ns
SDI set-up time	t_{SSU}		6			ns
SDI hold time	t_{SH}		6			ns
SCK Rising to SEN Rising	t_{SCRSER}		37.5			ns
SCK Falling to SEN Falling	t_{SCFSEF}		12			ns
SEN to SCK set-up time	t_{SEC}		12			ns
SEN pulse width	t_{SEW}		60			ns
SEN low to SDO = Register data	t_{SERD}				30	ns
SCK low to SDO = Register data	t_{SCRD}				30	ns
SCK low to SDO = ADC data	t_{SCRDZ}				30	ns

Note:

1. Parameters are measured at 50% of the rising/falling edge

INTERNAL POWER ON RESET CIRCUIT

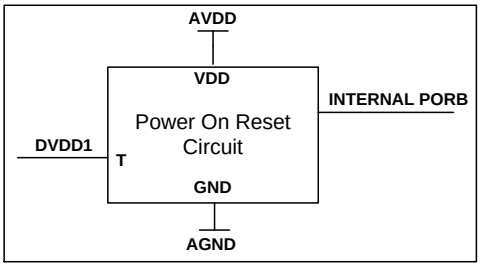


Figure 5 Internal Power On Reset Circuit Schematic

The WM8214 includes an internal Power-On-Reset Circuit, as shown in Figure 5, which is used reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DVDD1. It asserts PORB low if AVDD or DVDD1 is below a minimum threshold.

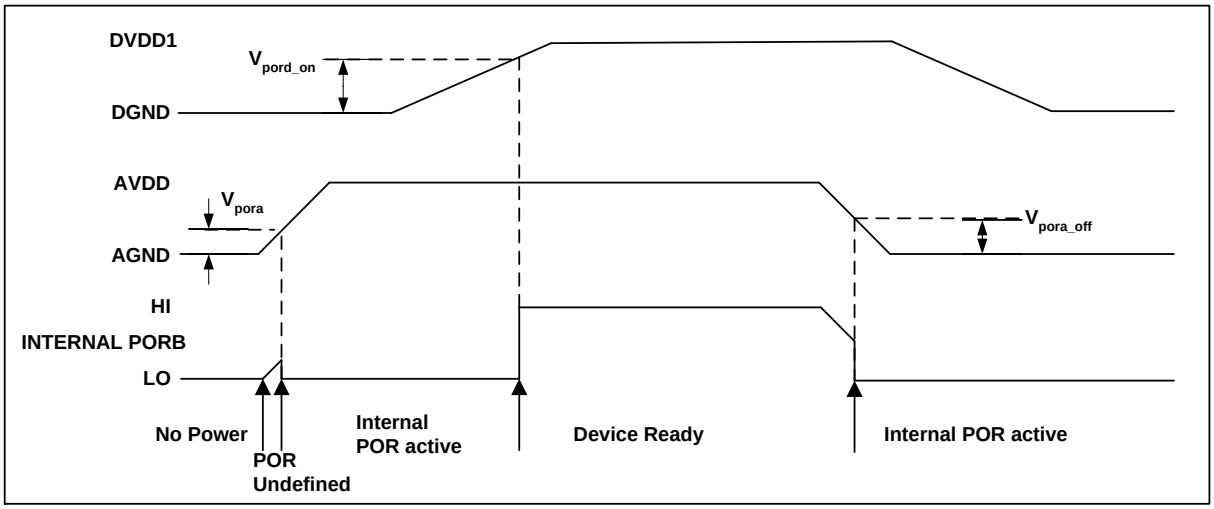


Figure 6 Typical Power up Sequence where AVDD is Powered before DVDD1

Figure 6 shows a typical power-up sequence where AVDD is powered up first. When AVDD rises above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DVDD1 rises to Vpord_on and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold Vpora_off.

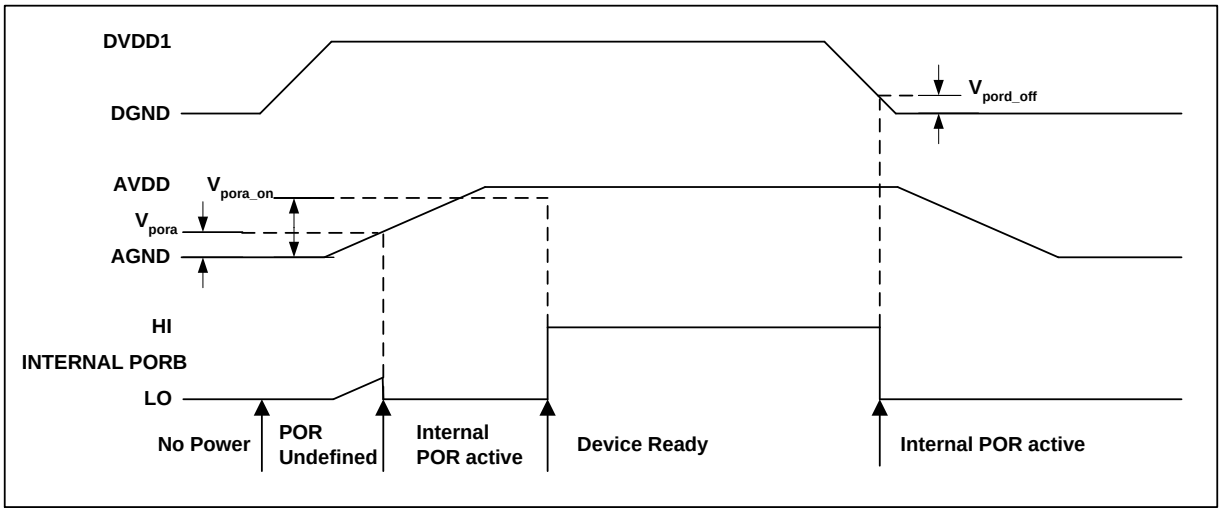


Figure 7 Typical Power up Sequence where DVDD1 is Powered before AVDD

Figure 7 shows a typical power-up sequence where DVDD1 is powered up first. It is assumed that DVDD1 is already up to specified operating voltage. When AVDD goes above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to Vpora_on, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DVDD1 falls first, PORB is asserted low whenever DVDD1 drops below the minimum threshold Vpord_off.

SYMBOL	TYP	UNIT
V_{pora}	0.6	V
V_{pora_on}	1.2	V
V_{pora_off}	0.6	V
V_{pord_on}	0.7	V
V_{pord_off}	0.6	V

Table 1 Typical POR Operation (typical values, not tested)

Note: It is recommended that every time power is cycled to the WM8214 a software reset is written to the software register to ensure that the contents of the control registers are at their default values before carrying out any other register writes.

DEVICE DESCRIPTION

INTRODUCTION

A block diagram of the device showing the signal path is presented on the front page of this datasheet.

The WM8214 samples up to three inputs (RINP, GINP and BINP) simultaneously. The device then processes the sampled video signal with respect to the video reset level or an internally/externally generated reference level using between one and three processing channels.

Each processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and a 9-bit Programmable Gain Amplifier (PGA).

The ADC then converts each resulting analogue signal to a 16-bit digital word. The digital output from the ADC is presented on an 8-bit wide bus.

On-chip control registers determine the configuration of the device, including the offsets and gains applied to each channel. These registers are programmable via a serial interface.

The WM8214 has been designed to have a high degree of compatibility with previous generations of Cirrus Logic AFEs. By setting the LEGACY register bit the device adopts the same timing as the WM819x and WM815x families of AFEs. The control interface is also compatible.

INPUT SAMPLING

The WM8214 can sample and process one to three inputs through one to three processing channels as follows:

Colour Pixel-by-Pixel: The three inputs (RINP, GINP and BINP) are simultaneously sampled for each pixel and a separate channel processes each input. The signals are then multiplexed into the ADC, which converts all three inputs within the pixel period.

Two Channel Pixel-by-pixel: Two input channels (RINP and GINP) are simultaneously sampled for each pixel and a separate channel processes each input. The signals are then multiplexed into the ADC, which converts both inputs within the pixel period. The unused Blue channel is powered down when this mode is selected.

Monochrome: A single chosen input (RINP, GINP, or BINP) is sampled, processed by the corresponding channel, and converted by the ADC. The choice of input and channel can be changed via the control interface, e.g. on a line-by-line basis if required. The unused channels are powered down when this mode is selected.

Colour Line-by-Line: A single input (RINP) is sampled and multiplexed into the red channel for processing before being converted by the ADC. The registers which are applied to the PGA and Offset DAC can be switched in turn (RINP → GINP → BINP → RINP…) by applying pulses to the RSMP pin. This is known as auto-cycling. Alternatively, other sequences can be generated via the control registers. This mode causes the unused blue and green channels to be powered down. Refer to the Line-by-Line Operation section for more details.

RESET LEVEL CLAMPING (RLC)

To ensure that the signal applied to the WM8214 lies within the supply voltage range (0V to AVDD) the output signal from a CCD is usually level shifted by coupling through a capacitor, $C_{IN.}$ The RLC circuit clamps the WM8214 side of this capacitor to a suitable voltage through a CMOS switch during the CCD reset period. In order for clamping to produce sensible results the input voltage during the clamping must be a consistent value.

The WM8214 allows the user to control the RLC switch in a variety of ways as illustrated in Figure 8. This figure shows a single channel, however all 3 channels are identical, each with its own clamp switch controlled by the common CLMP signal.

The method of control chosen depends upon the characteristics of the input video. The RLCEN register bit must be set to 1 to enable clamping, otherwise the RLC switch cannot be closed (by default RLCEN=1).

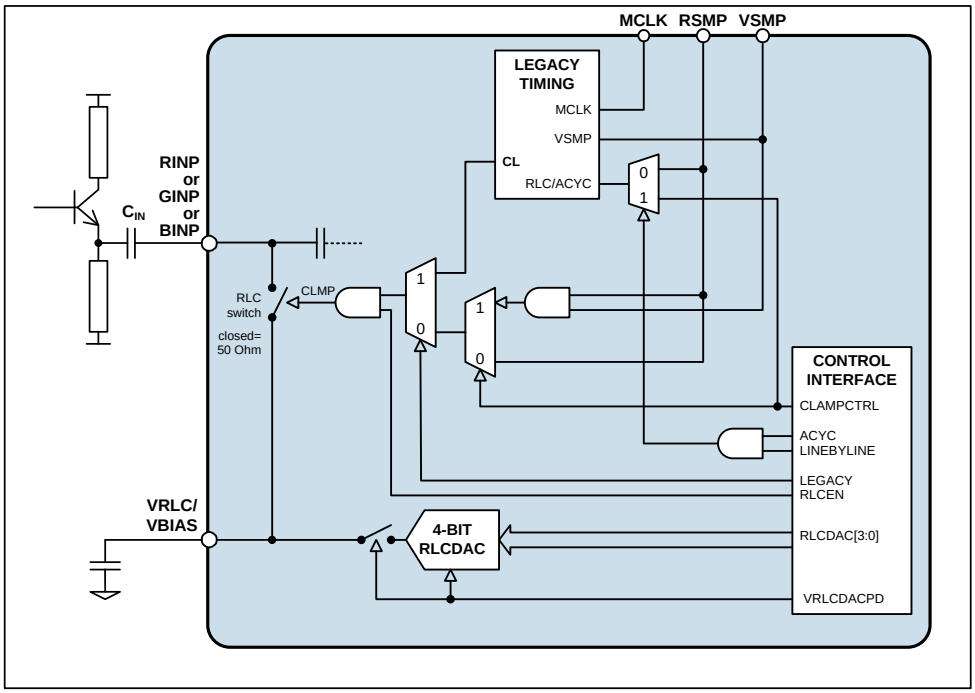


Figure 8 RLC Clamp Control Options

When an input waveform has a stable reference level on every pixel it may be desirable to clamp every pixel during this period. Setting CLAMPCTRL=0 means that the RLC switch is closed whenever the RSMP input pin is high, as shown in Figure 9.

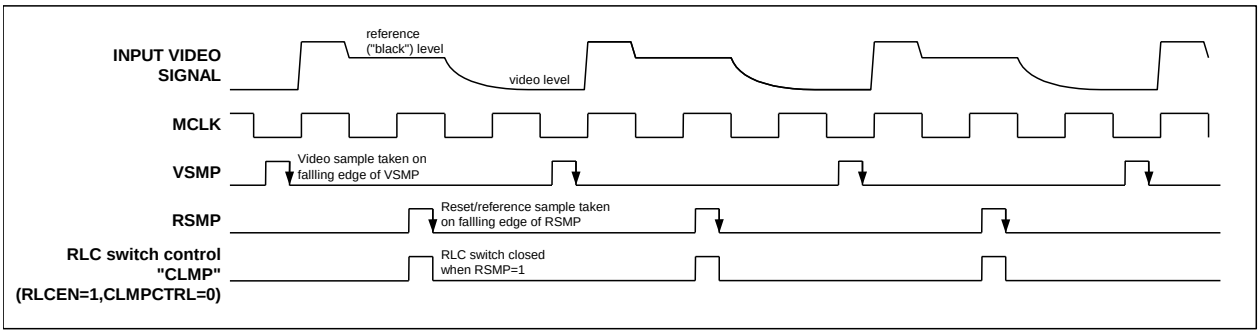


Figure 9 Reset Level Clamp Operation (CLAMPCTRL=0), CDS operation shown, non-CDS also possible

In situations where the input video signal does not have a stable reference level it may be necessary to clamp only during those pixels which have a known state (e.g. the dummy, or “black” pixels at the start or end of a line of most image sensors). This is known as line-clamping and relies on the input capacitor to hold the DC level between clamp intervals. In non-CDS mode (CDS=0) this can be done directly by controlling the RSMP input pin to go high during the black pixels only.

Alternatively it is possible to use RSMP to identify the black pixels and enable the clamp at the same time as the input is being sampled (i.e. when VSMP is high and RSMP is high). This mode is enabled by setting CLAMPCTRL=1 and the operation is shown in

Figure **10**.

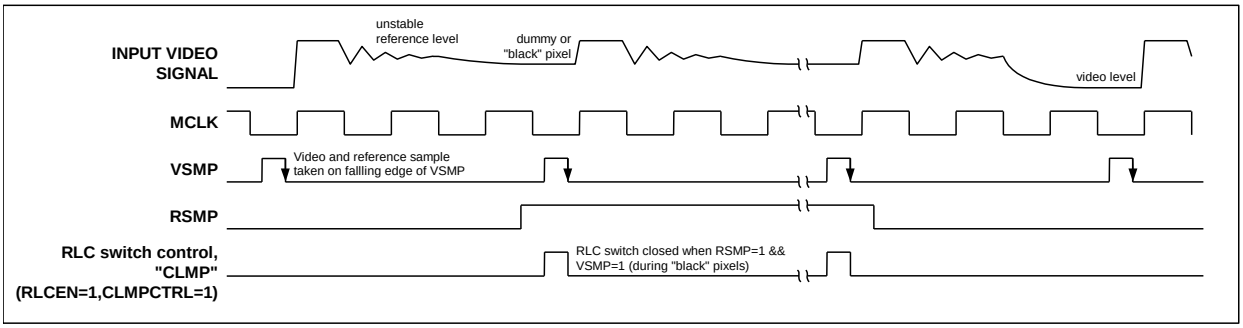


Figure 10 Reset Level Clamp Operation (CLAMPCTRL=1), non-CDS mode only

When in LEGACY mode all timing, including the RLC switch timing, is derived from MCLK and VSMP. MCLK operates at double the ADC conversion rate and VSMP determines the sample rate of the device.

Reset Level Clamping in LEGACY mode is only possible in CDS mode and the time at which the clamp switch is closed is concurrent with the reset sample period, RS, as shown in Figure 11. RLC can be enabled on a pixel by pixel basis under control of the RSMP input pin. If RSMP is high when VSMP is high and is sampled by MCLK then clamping will be enabled for that input sample at the time determined by CDSREF[1:0]. If RSMP is low at this point then the RLC switch will not be closed for that input sample. If RLC is required on every pixel then the RSMP pin can be constantly held high in LEGACY mode.

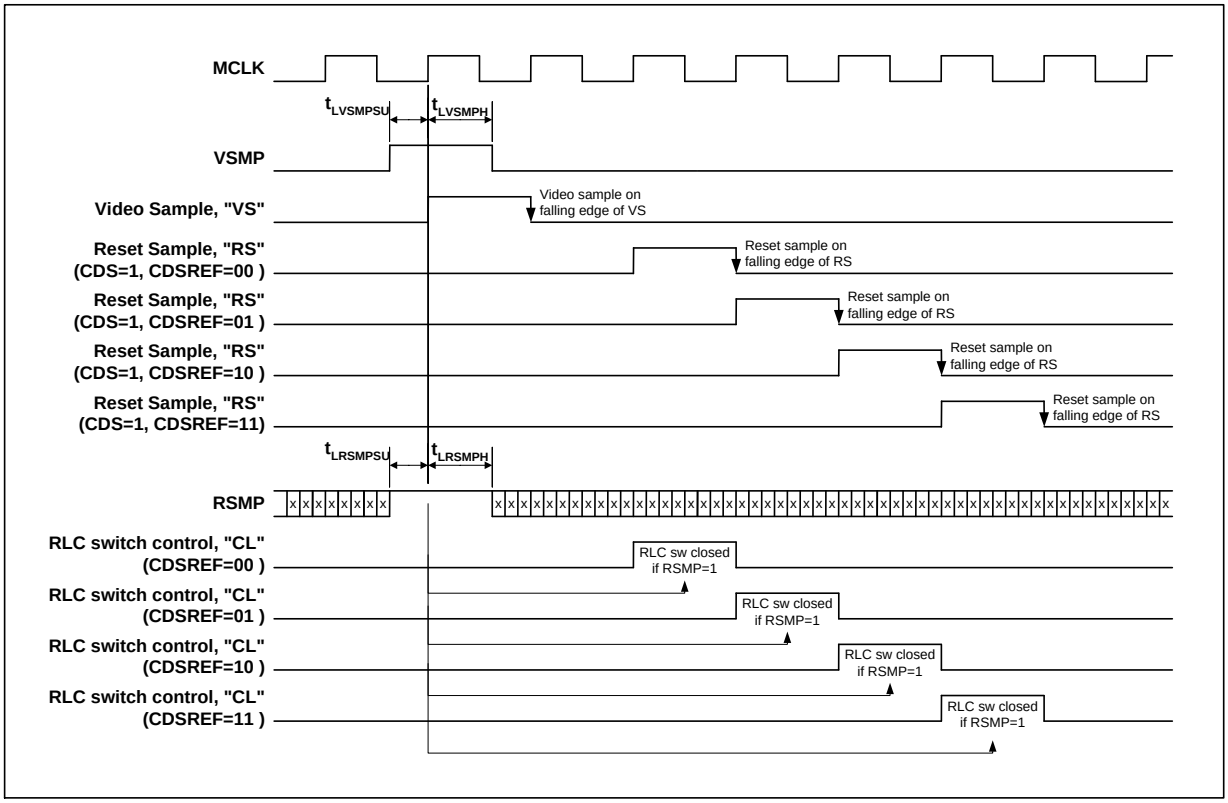


Figure 11 LEGACY Mode RLC and Sampling (LEGACY=1)

Table 2 summarises the various options for control of the Reset Level Clamp switch.

RLCEN	LEGACY	CLAMPCTRL	LINEBYLINE &&ACYC	OUTCOME	USE
0	**X**	**X**	**X**	RLC is not enabled. RLC switch is always open.	When input is DC coupled and within supply rails.
1	**0**	**0**	**X**	RLC switch is controlled directly from RSMP input pin: RSMP=0: switch is open RMSP=1: switch is closed	When user explicitly provides a reset sample signal and the input video waveform has a suitable reset level.
1	**0**	**1**	**X**	VSMP applied as normal, RSMP is used to indicate the location of black pixels RLC switch is controlled by logical combination of RSMP and VSMP: RSMP && VSMP = 0: switch is open RSMP && VSMP = 1: switch is closed	When you wish to clamp during the video period of black pixels or there is no stable per-pixel reference level.
1	**1**	**X**	**X**	LEGACY mode RLC works in the same fashion as the WM819x series, where the RSMP pin is equivalent to the RLC/ACYC pin on those devices. The reset sample clock which is generated by the LEGACY internal timing generator is gated with the RSMP pin to produce the RLC control signal CL (see Figure 11) : CL=0: clamp switch open CL=1: clamp switch closed	When using the LEGACY timing mode.
X	**1**	**0** **1**	**1**	In this mode the RSMP pin is used to control auto-cycling so can't be used for clamp control. Register bit CLAMPCTRL controls whether RLC is enabled or not. CLAMPCTRL=0, RLC is disabled CLAMPCTRL=1, RLC is enabled and every pixel will be clamped during the control signal CL (see Figure 11).	When auto-cycling in LEGACY mode.

Table 2 Reset Level Clamp Control Summary

CDS/NON-CDS PROCESSING

For CCD type input signals, containing a fixed reference/reset level, the signal may be processed using Correlated Double Sampling (CDS), which will remove pixel-by-pixel common mode noise. With CDS processing the input waveform is sampled at two different points in time for each pixel, once during the reference/reset level and once during the video level. To sample using CDS, register bit CDS must be set to 1 (default). This causes the signal reference to come from the video reference level as shown in Figure 12.

The video sample is always taken on the falling edge of the input VSMP signal (VS). In CDS-mode the reset level is sampled on the falling edge of the RSMP input signal (RS).

For input signals that do not contain a reference/reset level (e.g. CIS sensor signals), non-CDS processing is used (CDS=0). In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS. The VRLC/VBIAS voltage is sampled at the same time as VSMP samples the video level in this mode.

In LEGACY mode the input video signal is always sampled on the 1st rising edge of MCLK after VSMP has gone low (VS) regardless of the operating mode. If in non-CDS mode (CDS=0) the voltage on the VRLC/VBIAS pin is also sampled at this point. In CDS-mode (CDS=1) the position of the reset sample (RS) can be varied, under control of the CDSREF[1:0] register bits, as shown in Figure 11.

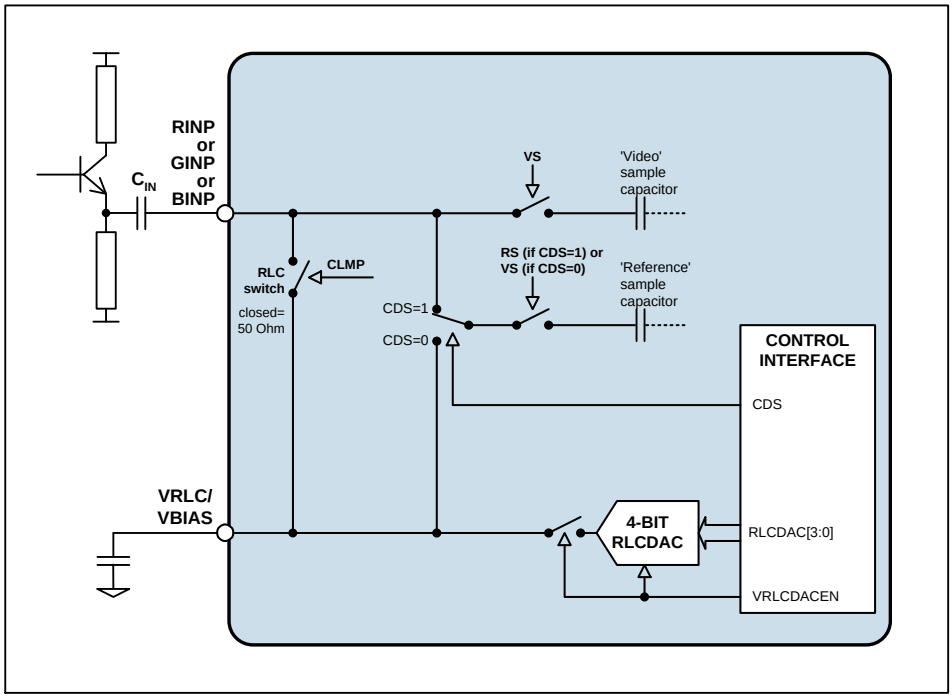


Figure 12 CDS/non-CDS Input Configuration

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by a 9-bit PGA. The gain and offset for each channel are independently programmable by writing to control bits DAC[7:0] and PGA[7:0].

The gain characteristic of the WM8214 PGA is shown in Figure 13. Figure 14 shows the maximum device input voltage that can be gained up to match the ADC full-scale input range (default=2V).

In colour line-by-line mode the gain and offset coefficients for each colour can be multiplexed in order (Red → Green → Blue → Red…) by pulsing the RSMP pin, or controlled via the ACYC and INTM[1:0] bits. Refer to the Line-by-Line Operation section for more details.

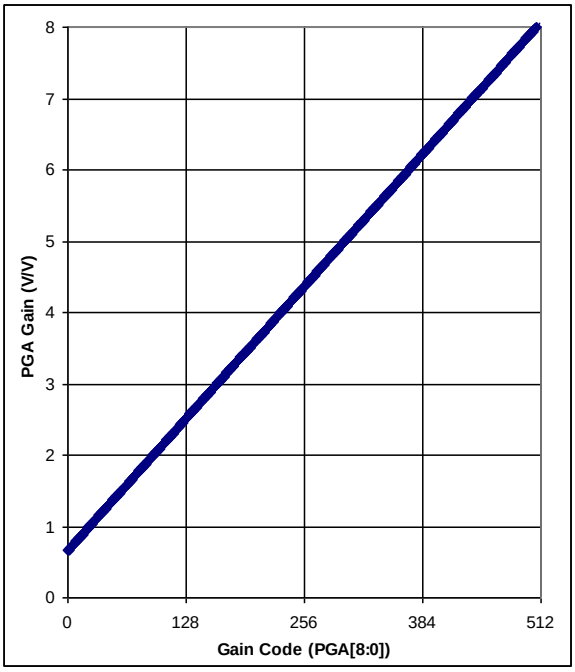


Figure 13 PGA Gain Characteristic

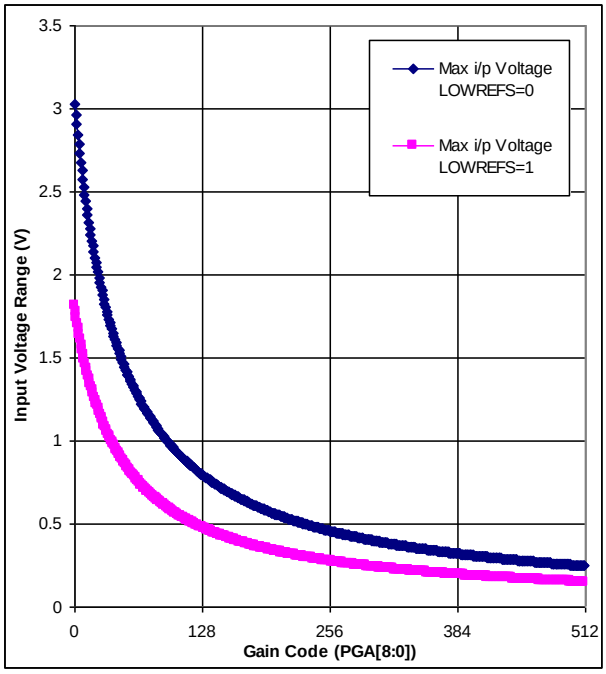


Figure 14 Peak Input Voltage to Match ADC Full-scale Range

ADC INPUT BLACK LEVEL ADJUST

The output from the PGA can be offset to match the full-scale range of the differential ADC (2*[VRT-VRB]).

For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS[1:0]=10. This will give an output code of FFFF (hex) from the WM8214 for zero input. If code zero is required for zero differential input then the INVOP bit should be set.

For positive going input signals the black level should be offset to the bottom of the ADC range by setting PGAFS[1:0]=11. This will give an output code of 0000 (hex) from the WM8214 for zero input.

Bipolar input video is accommodated by setting PGAFS[1:0]=00 or PGAFS[1:0]=01. Zero differential input voltage gives mid-range ADC output, 7FFF (hex).

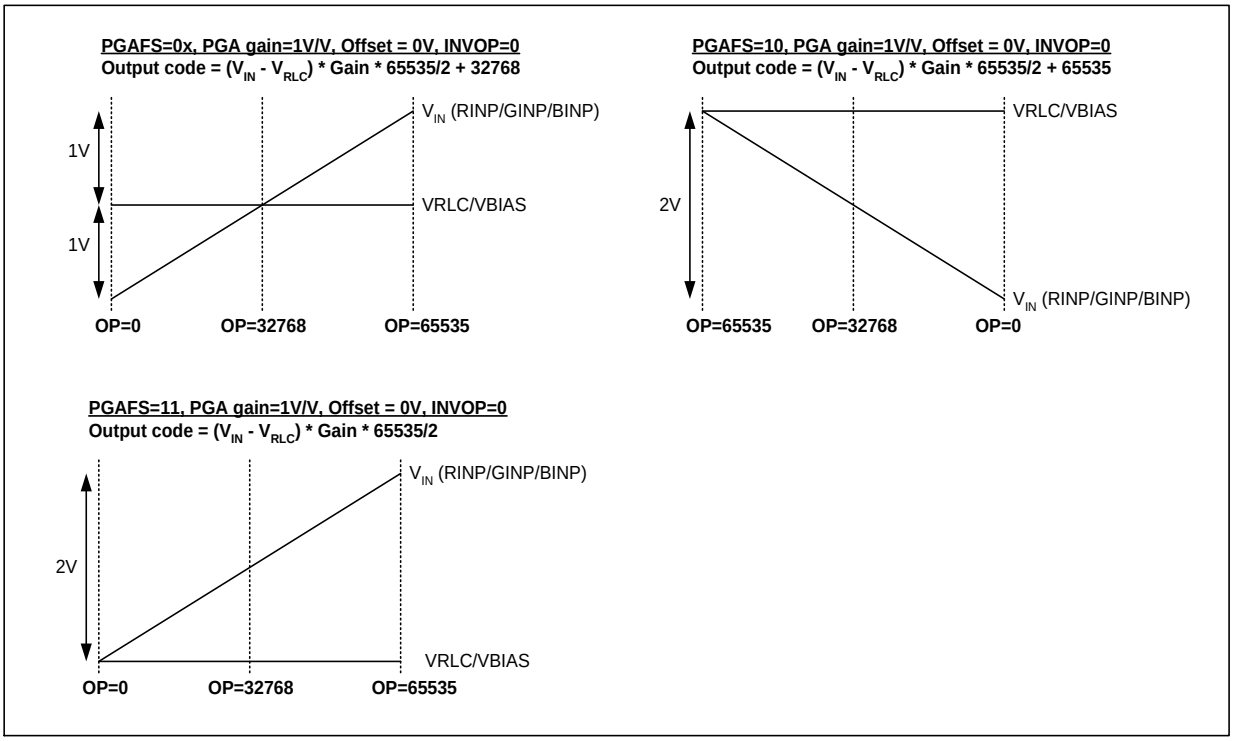


Figure 15 ADC Input Black Level Adjust Settings

OVERALL SIGNAL FLOW SUMMARY

Figure 16 represents the processing of the video signal through the WM8214.

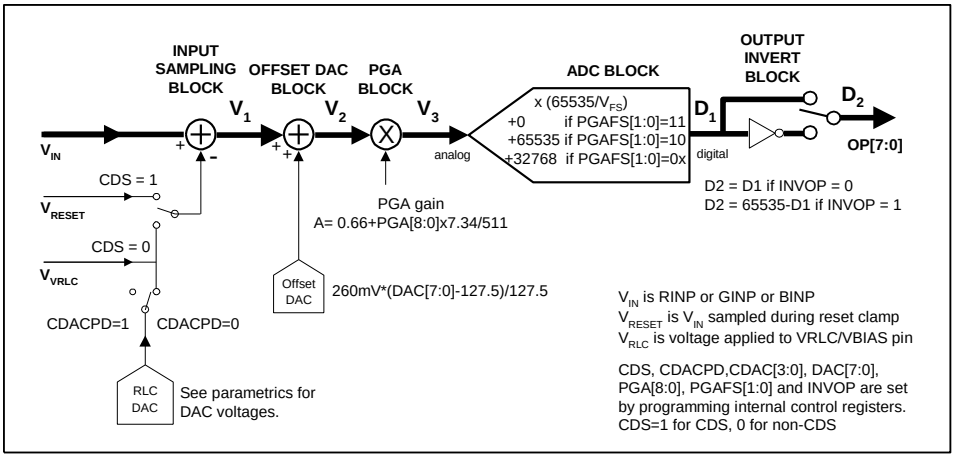


Figure 16 Overall Signal Flow

The **INPUT SAMPLING BLOCK** produces an effective input voltage $\mathbf{V_1}$. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC/VBIAS pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing $\mathbf{V_2}$.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage $\mathbf{V_3}$.

The **ADC BLOCK** then converts the analogue signal, $\mathbf{V_3}$, to a 16-bit unsigned digital output, $\mathbf{D_1}$.

The digital output is then inverted, if required, through the **OUTPUT INVERT BLOCK** to produce $\mathbf{D_2}$.

CALCULATING THE OUTPUT CODE FOR A GIVEN INPUT

The following equations describe the processing of the video and reset level signals through the WM8214. The values of V_1, V_2 and V_3 are often calculated in reverse order during device setup. The PGA value is written first to set the input Voltage range, the Offset DAC is then adjusted to compensate for any Black/Reset level offsets and finally the RLC DAC value is set to position the reset level correctly during operation.

Note: Refer to Applications Note WAN0123 for detailed information on device calibration procedures.

INPUT SAMPLING BLOCK: INPUT SAMPLING AND REFERENCING

If CDS = 1, (i.e. CDS operation) the previously sampled reset level, V_{RESET}, is subtracted from the input video.

$$\mathbf{V_1} = V_{IN} - V_{RESET} \quad \text{Eqn. 1}$$

If CDS = 0, (non-CDS operation) the simultaneously sampled voltage on pin VRLC is subtracted instead.

$$\mathbf{V_1} = V_{IN} - V_{VRLC} \quad \text{Eqn. 2}$$

If VRLCDACPD = 1, V_{VRLC} is an externally applied voltage on pin VRLC/VBIAS.

If VRLCDACPD = 0, V_{VRLC} is the output from the internal RLC DAC.

$$V_{VRLC} = (V_{RLCSTEP} * \text{RLC DAC[3:0]}) + V_{RLCBOT} \quad \text{Eqn. 3}$$

$V_{RLCSTEP}$ is the step size of the RLC DAC and V_{RLCBOT} is the minimum output of the RLC DAC.

OFFSET DAC BLOCK: OFFSET (BLACK LEVEL) ADJUST

The resultant signal $\mathbf{V_1}$ is added to the Offset DAC output.

$$\mathbf{V_2} = \mathbf{V_1} + \{260\text{mV} * (\text{DAC[7:0]}-127.5)\} / 127.5 \quad \text{Eqn. 4}$$

PGA NODE: GAIN ADJUST

The signal is then multiplied by the PGA gain.

$$\mathbf{V_3} = \mathbf{V_2} * (0.66 + \text{PGA[8:0]}x7.34/511) \quad \text{Eqn. 5}$$

ADC BLOCK: ANALOGUE-DIGITAL CONVERSION

The analogue signal is then converted to a 16-bit unsigned number, with input range configured by PGAFS[1:0].

$$\mathbf{D_1}[15:0] = \text{INT}\{ (\mathbf{V_3}/V_{FS}) * 65535\} + 32767 \quad \text{PGAFS[1:0] = 00 or 01} \quad \text{Eqn. 6}$$

$$\mathbf{D_1}[15:0] = \text{INT}\{ (\mathbf{V_3}/V_{FS}) * 65535\} \quad \text{PGAFS[1:0] = 11} \quad \text{Eqn. 7}$$

$$\mathbf{D_1}[15:0] = \text{INT}\{ (\mathbf{V_3}/V_{FS}) * 65535\} + 65535 \quad \text{PGAFS[1:0] = 10} \quad \text{Eqn. 8}$$

where the ADC full-scale range, V_{FS} = 2V when LOWREFS=0 and V_{FS} = 1.2V when LOWREFS=1.

OUTPUT INVERT BLOCK: POLARITY ADJUST

The polarity of the digital output may be inverted by control bit INVOP.

$$\mathbf{D_2}[15:0] = \mathbf{D_1}[15:0] \quad \text{(INVOP = 0)} \quad \text{Eqn. 9}$$

$$\mathbf{D_2}[15:0] = 65535 - \mathbf{D_1}[15:0] \quad \text{(INVOP = 1)} \quad \text{Eqn. 10}$$

OUTPUT FORMATS

The output from the WM8214 can be presented in several different formats under control of the OPFORM[1:0] register bits as shown in

Figure 17.

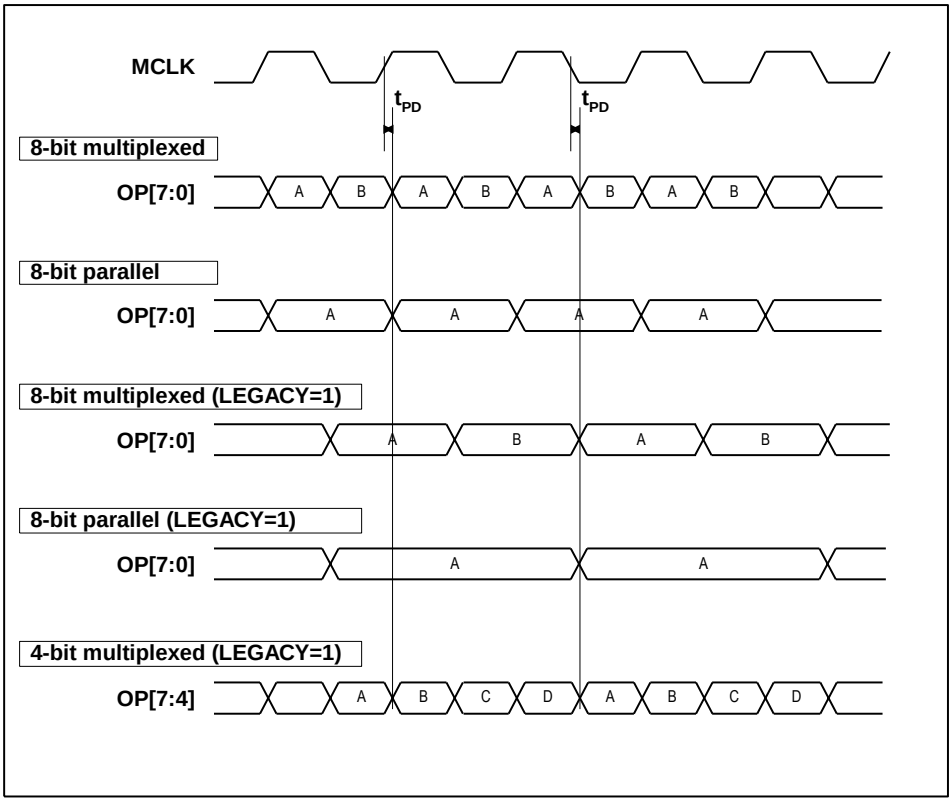


Figure 17 Output Data Formats

OUTPUT FORMAT	OPFORM[1:0]	LEGACY	OUTPUT PINS	OUTPUT
8+8-bit multiplexed	00, 10	X	OP[7:0]	A = d15, d14, d13, d12, d11, d10, d9, d8 B = d7, d6, d5, d4, d3, d2, d1,d0
8-bit parallel	01	X	OP[7:0]	A = d15, d14, d13, d12, d11, d10, d9, d8
4+4+4+4-bit (nibble)	11	1	OP[7:4]	A = d15, d14, d13, d12 B = d11, d10, d9, d8 C = d7, d6, d5, d4 D = d3, d2, d1, d0

Table 3 Details of Output Data Formats (as shown in

Figure 17).

REFERENCES

The ADC reference voltages are derived from an internal bandgap reference, and buffered to pins VRT and VRB, where they must be decoupled to ground. Pin VRX is driven by a similar buffer, and also requires decoupling. The output buffer from the RLCDAC also requires decoupling at pin VRLC/VBIAS.

POWER MANAGEMENT

Power management for the device is performed via the Control Interface. By default the device is fully enabled. The EN bit allows the device to be fully powered down when set low. Individual blocks can be powered down using the bits in Setup Register 5. When in MONO or TWOCHAN mode the unused input channels are automatically disabled to reduce power consumption.

LINE-BY-LINE OPERATION

Certain linear sensors give colour output on a line-by-line basis. i.e. a full line of red pixels followed by a line of green pixels followed by a line of blue pixels. Often the sensor will have only a single output onto which these outputs are time multiplexed.

The WM8214 can accommodate this type of input by setting the LINEBYLINE register bit high. When in this mode the green and blue input PGAs are disabled to save power. The analogue input signal should be connected to the RINP pin. The offset and gain values that are applied to the Red input channel can be selected, by internal multiplexers, to come from the Red, Green or Blue offset and gain registers. This allows the gain and offset values for each of the input colours to be setup individually at the start of a scan.

When register bit ACYC=0 the gain and offset multiplexers are controlled via the INTM[1:0] register bits. When INTM=00 the red offset and gain control registers are used to control the Red input channel, INTM=01 selects the green offset and gain registers and INTM=10 selects the blue offset and gain registers to control the Red input channel.

When register bit ACYC=1, 'auto-cycling' is enabled, and the input channel switches to the next offset and gain registers in the sequence when a pulse is applied to the RSMP input pin. The sequence is Red → Green → Blue → Red… offset and gain registers applied to the single input channel. A write to the Auto-cycle reset register (address 05h) will reset the sequence to a known state (Red registers selected).

When auto-cycling is enabled, the RSMP pin cannot be used to control reset level clamping. The CLMPCTRL bit may be used instead (enabled when high, disabled when low).

NB, when auto-cycling is enabled, the RSMP pin cannot be used for reset sampling (i.e. CDS must be set to 0).

CONTROL INTERFACE

The internal control registers are programmable via the serial digital control interface. The register contents can be read back via the serial interface on pin OP[7]/SDO.

Note: It is recommended that a software reset is carried out after the power-up sequence, before writing to any other register. This ensures that all registers are set to their default values (as shown in Table 7).

SERIAL INTERFACE: REGISTER WRITE

Figure 18 shows register writing in serial mode. Three pins, SCK, SDI and SEN are used. A six-bit address (a5, 0, a3, a2, a1, a0) is clocked in through SDI, MSB first, followed by an eight-bit data word (b7, b6, b5, b4, b3, b2, b1, b0), also MSB first. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register. Note all valid registers have address bit a4 equal to 0 in write mode.

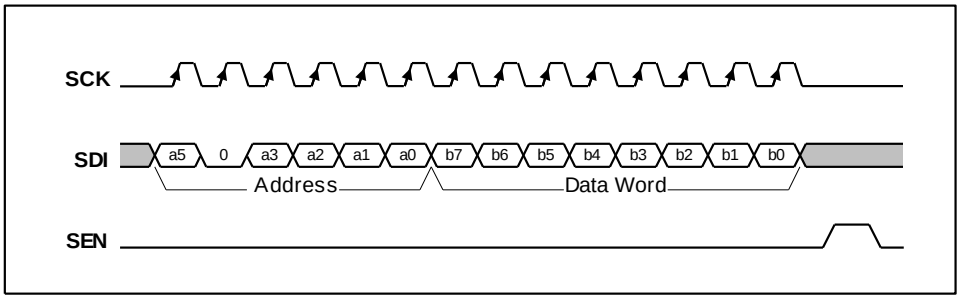


Figure 18 Serial Interface Register Write

A software reset is carried out by writing to Address “000100” with any value of data, (i.e. Data Word = XXXXXXXX).

SERIAL INTERFACE: REGISTER READ-BACK

Figure 19 shows register read-back in serial mode. Read-back is initiated by writing to the serial bus as described above but with address bit a4 set to 1, followed by an 8-bit dummy data word. Writing address (a5, 1, a3, a2, a1, a0) will cause the contents (d7, d6, d5, d4, d3, d2, d1, d0) of corresponding register (a5, 0, a3, a2, a1, a0) to be output MSB first on pin SDO (on the falling edge of SCK). Note that pin SDO is shared with an output pin, OP[7], therefore OEB should always be held low and the OPD register bit should be set low when register read-back data is expected on this pin. The next word may be read in to SDI while the previous word is still being output on SDO.

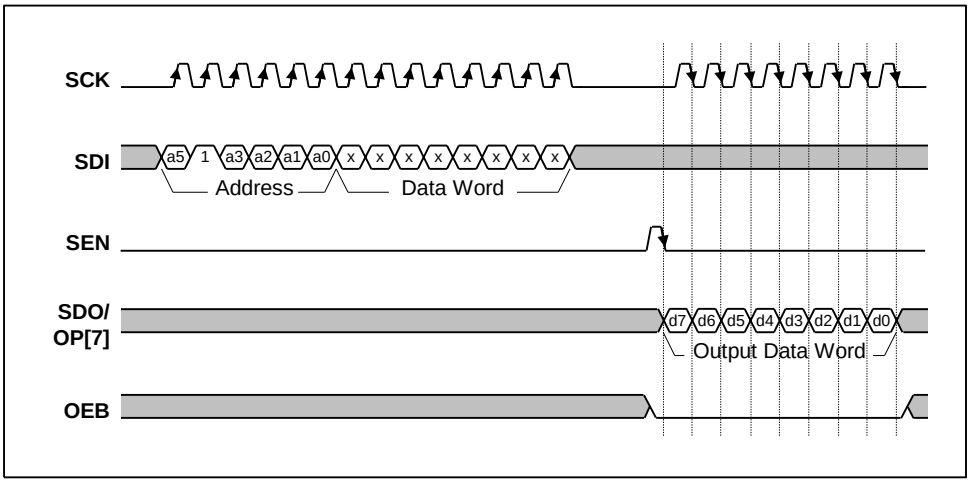


Figure 19 Serial Interface Register Read-back

NORMAL OPERATING MODES

Table 4 below shows the normal operating modes of the device. The MCLK speed can be specified along with the MCLK:VSMP ratio to achieve the desired sample rate.

NUMBER OF CHANNELS	DESCRIPTION	CDS AVAILABLE	MAXIMUM SAMPLE RATE	TIMING REQUIREMENTS	CHANNEL MODE SETTINGS
3	Three channel Pixel-by-Pixel	YES	13.33 MSPS	MCLK max = 40Mhz Minimum MCLK:VSMP ratio = 3:1	MONO = 0 TWOCHAN = 0
2	Two channel Pixel-by-Pixel	YES	20 MSPS	MCLK max = 40Mhz Minimum MCLK:VSMP ratio = 2:1	MONO = 0 TWOCHAN = 1
1	One channel Pixel-by-Pixel	YES	40 MSPS	MCLK max = 40Mhz Minimum MCLK:VSMP ratio = 1:1	MONO = 1 TWOCHAN = 0

Table 4 WM8214 Normal Operating Modes

Table 5 below shows the different channel mode register settings required to operate the 8214 in 1, 2 and 3 channel modes.

MONO	TWOCHAN	CHAN[1:0]	MODE DESCRIPTION
0	0	XX	3-channel (colour mode)
0	1	XX	2-channel (Blue PGA disabled)
1	0	00	1-channel (monochrome) mode. Red channel selected, Green and Blue PGAs disabled.
1	0	01	1-channel (monochrome) mode. Green channel selected, Red and Blue PGAs disabled.
1	0	10	1-channel (monochrome) mode. Blue channel selected, Red and Green PGAs disabled.
1	0	11	Invalid mode
1	1	XX	Invalid mode

Table 5 Sampling Mode Summary

Note: Unused input pins should be connected to AGND.

LEGACY MODE INFORMATION

The WM8214 has been designed to have a high degree of compatibility with previous generations of Cirrus Logic AFEs. By setting the LEGACY register bit the input timing is made compatible with the WM819x and WM815x series of devices. Additional features such as the VSMP detect mode are also retained in LEGACY mode.

LEGACY: PROGRAMMABLE VSMP DETECT CIRCUIT

The VSMP input is used to determine the sampling point and frequency of the WM8214. Under normal operation a pulse of 1 MCLK period should be applied to VSMP at the desired sampling frequency (as shown in the LEGACY Mode Timing Diagrams) and the input sample will be taken on the first rising MCLK edge after VSMP has gone low. However, in certain applications such a signal may not be readily available. The programmable VSMP detect circuit in the WM8214 allows the sampling point to be derived from any signal of the correct frequency, such as a CCD shift register clock, when applied to the VSMP pin.

When enabled, by setting the VSMPDET control bit, the circuit detects either a rising or falling edge (determined by POSNNEG control bit) on the VSMP input pin and generates an internal VSMP pulse, INTVSMP. When POSNNEG = 1, a positive edge transition is detected and when POSNNEG = 0, a falling edge transition is detected. INTVSMP can optionally be delayed by a number of MCLK periods, specified by the VDEL[2:0] bits.

Figure **20** shows the internal VSMP pulses that can be generated by this circuit for a typical clock input signal. The internal VSMP pulse is then applied to the timing control block in place of the normal VSMP pulse provided from the input pin.

The sampling point occurs on the first rising MCLK edge after this internal VSMP pulse, as shown in the LEGACY Mode Timing Diagrams.

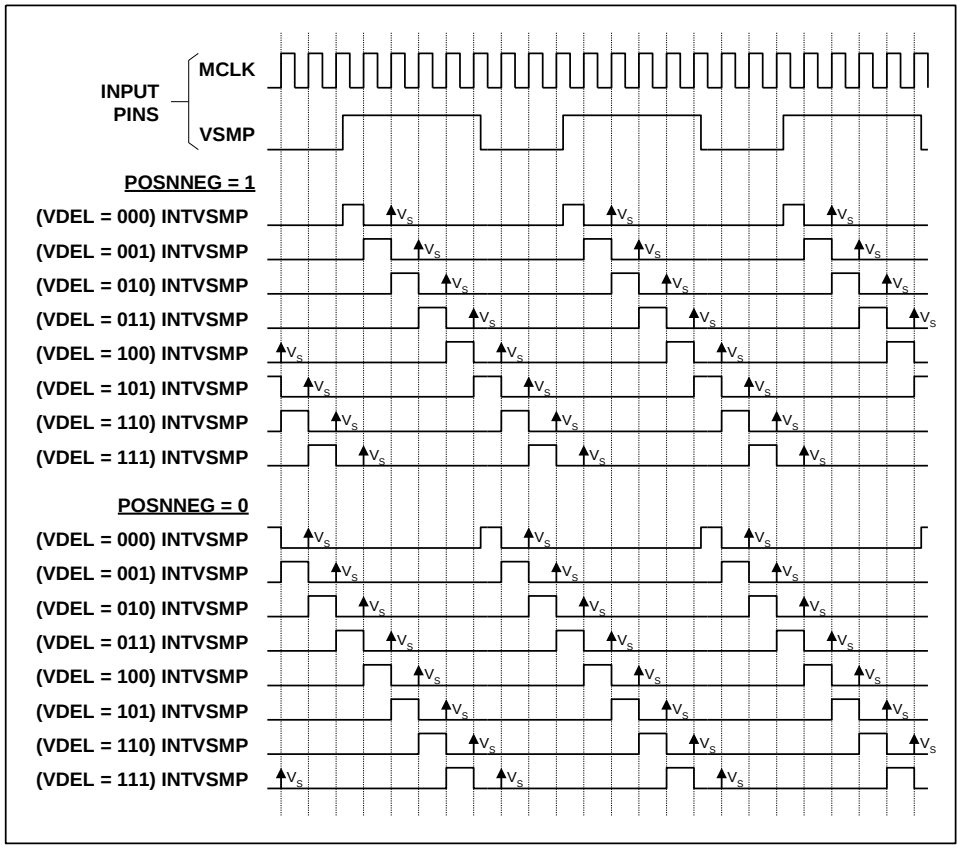


Figure 20 **Internal VSMP Pulses Generated by Programmable VSMP Detect Circuit**

LEGACY OPERATING MODES

Table 6 summarises the most commonly used modes, the clock waveforms required and the register contents required for CDS and non-CDS operation.

MODE	DESCRIPTION	CDS AVAILABLE	MAX SAMPLE RATE	SENSOR INTERFACE DESCRIPTION	TIMING REQUIRE-MENTS	REGISTER CONTENTS WITH CDS	REGISTER CONTENTS WITHOUT CDS
1	Colour Pixel-by-Pixel	Yes	6.67MSPS	The 3 input channels are sampled in parallel. The signal is then gain and offset adjusted before being multiplexed into a single data stream and converted by the ADC, giving an output data rate of 20MSPS max.	MCLK max = 40MHz MCLK: VSMP ratio is 2n:1 , n≥ 3	SetReg1: 83(hex)	SetReg1: 81(hex)
2	Monochrome/ Colour Line-by-Line	Yes	6.67MSPS	As mode 1 except: Only one input channel at a time is continuously sampled.	MCLK max = 40MHz MCLK: VSMP ratio is 2n:1 , n≥ 3	SetReg1: 87(hex)	SetReg1: 85(hex)
3	Fast Monochrome/ Colour Line-by-Line	Yes	13.33MSPS	Identical to mode 2	MCLK max = 40MHz MCLK: VSMP ratio is 3:1	Identical to mode 2 plus SetReg3: bits 5:4 must be set to 0(hex)	Identical to mode 2
4	Maximum speed Monochrome/ Colour Line-by-Line	No	20MSPS	Identical to mode 2	MCLK max = 40MHz MCLK: VSMP ratio is 2:1	CDS not possible	SetReg1: C5(hex)

Table 6 WM8214 Legacy Operating Modes

Notes:

1. In Monochrome mode, SetReg3 bits 7:6 determine which input is to be sampled.
2. For Colour Line-by-Line, set control bit LINEBYLINE. For input selection, refer to Table 4, Colour Selection Description in Line-by-Line Mode.

LEGACY MODE TIMING DIAGRAMS

The following diagrams show 8-bit multiplexed output data and MCLK, VSMP and input video requirements for operation of the most commonly used modes as shown in Table 6. The diagrams are identical for both CDS and non-CDS operation. Outputs from RINP, GINP and BINP are shown as R, G and B respectively. X denotes invalid data.

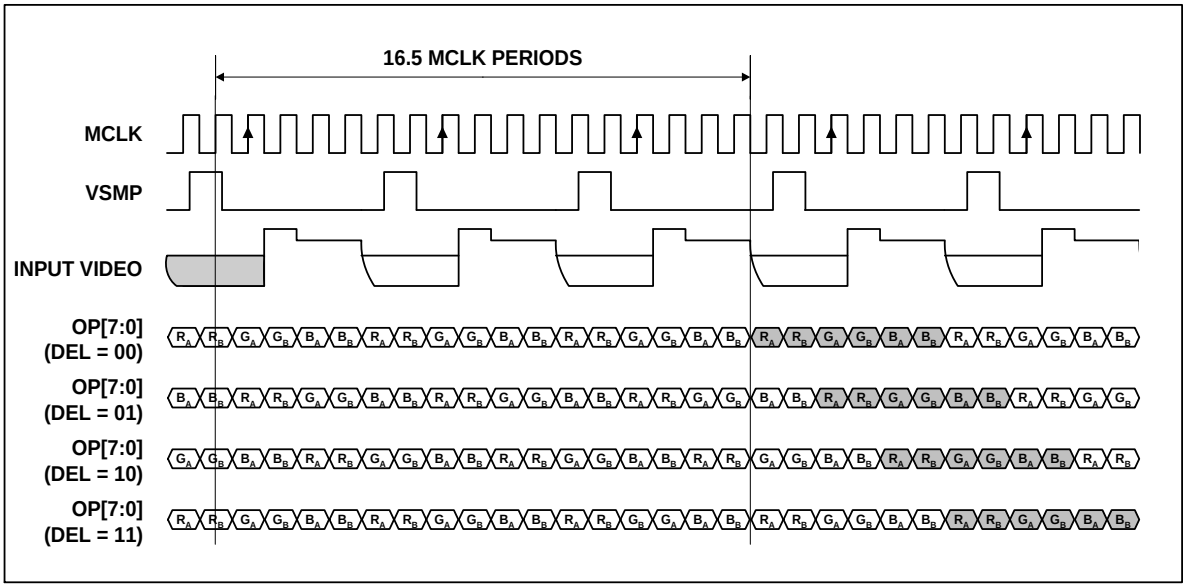


Figure 21 Mode 1 Operation

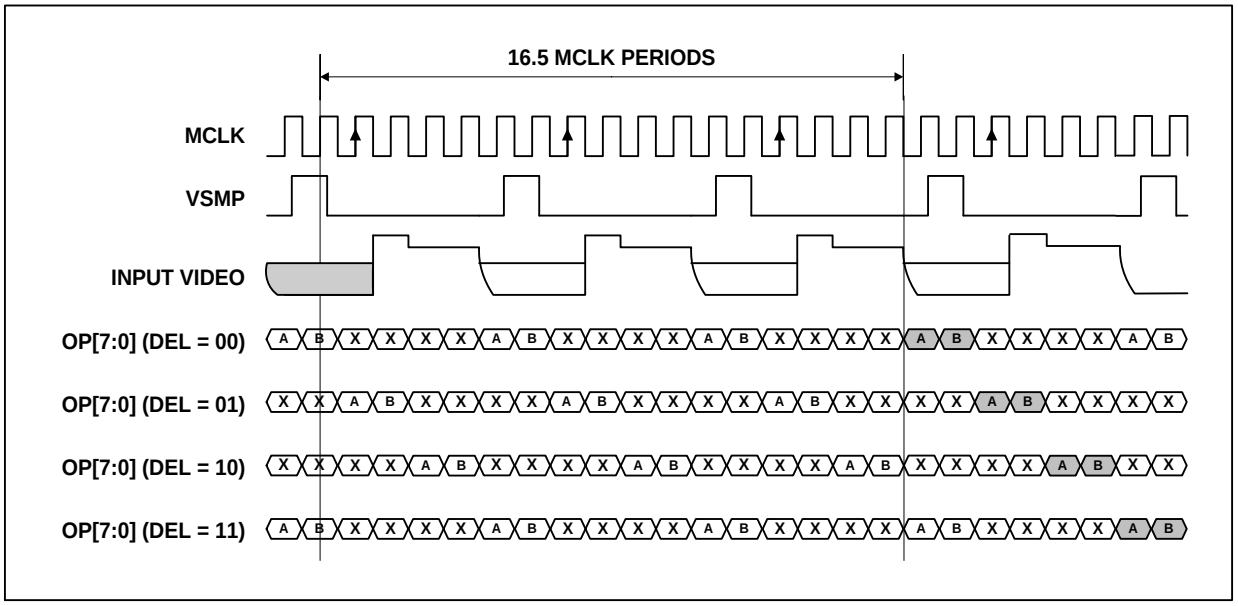


Figure 22 Mode 2 Operation

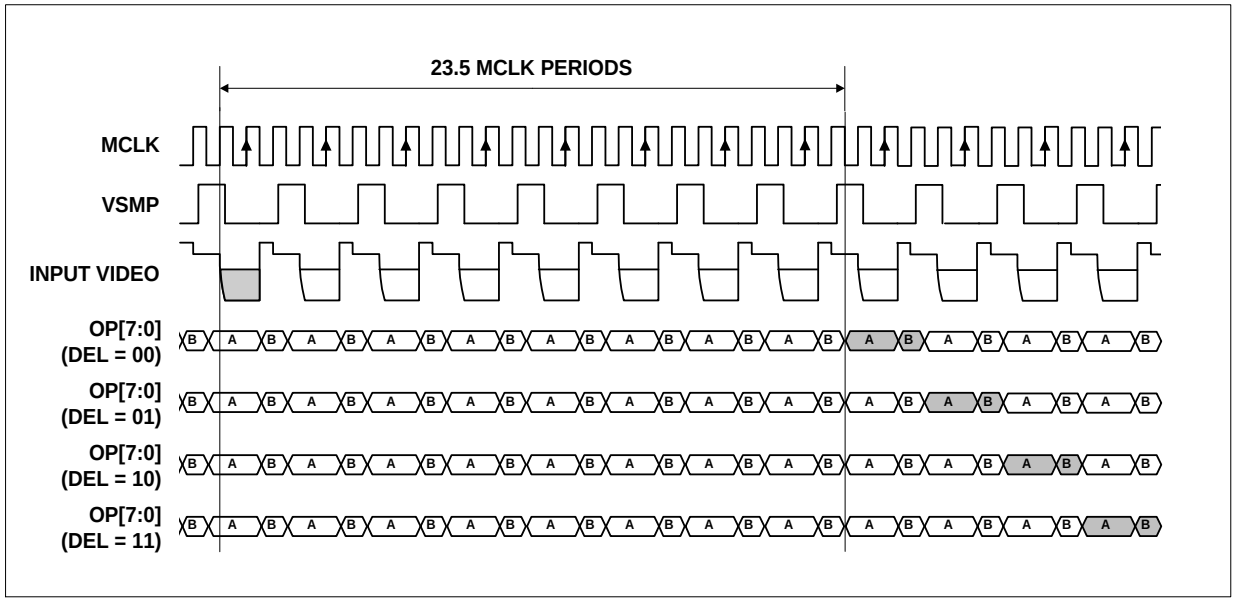


Figure 23 Mode 3 Operation

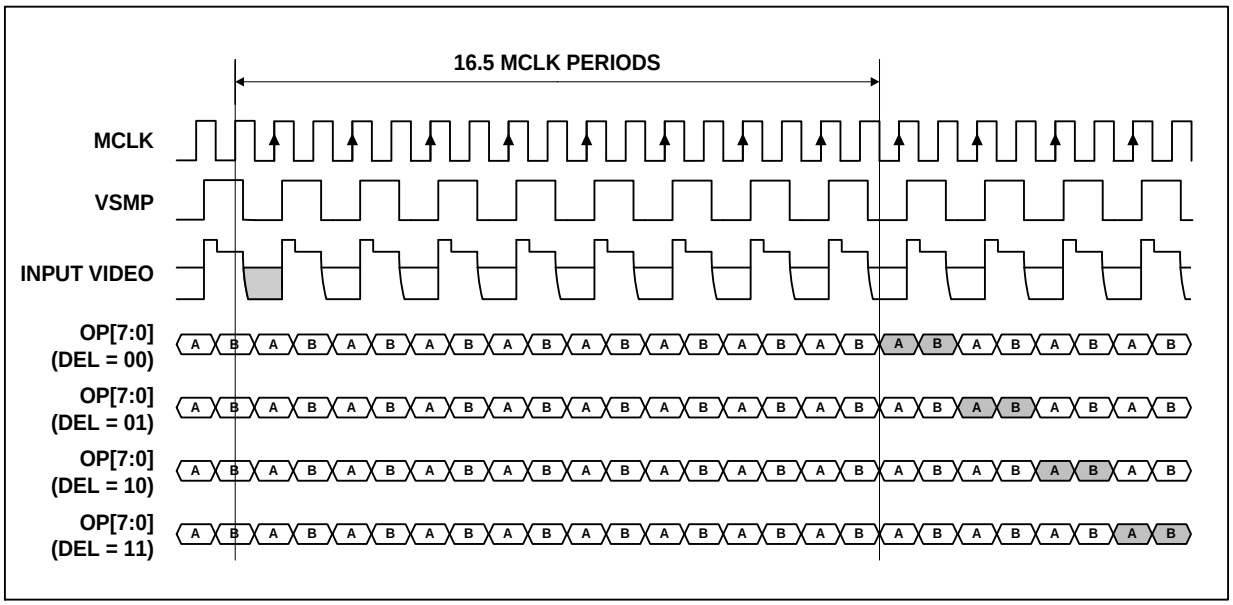


Figure 24 Mode 4 Operation

DEVICE CONFIGURATION

REGISTER MAP

The following table describes the location of each control bit used to determine the operation of the WM8214.

ADDRESS <a5:a0>	DESCRIPTION	DEF (hex)	RW	BIT							
				b7	b6	b5	b4	b3	b2	b1	b0
000001 (01h)	Setup Reg 1	03	RW	LEGACY	MODE4LEG	PGAFS[1]	PGAFS[0]	TWOCHAN	MONO	CDS	EN
000010 (02h)	Setup Reg 2	20	RW	DEL[1]	DEL[0]	RLCDACRNG	LOWREFS	OPD	INVOP	OPFORM[1]	OPFORM[0]
000011 (03h)	Setup Reg 3	1F	RW	CHAN[1]	CHAN[0]	CDSREF [1]	CDSREF [0]	RLCDAC[3]	RLCDAC[2]	RLCDAC[1]	RLCDAC[0]
000100 (04h)	Software Reset	00	W								
000101 (05h)	Auto-cycle Reset	00	W								
000110 (06h)	Setup Reg 4	00	RW	0	0	0	0	INTM[1]	INTM[0]	ACYC	LINEBYLINE
000111 (07h)	Setup Reg 5	00	RW	0	VRXPD	ADCREFPD	VRLCDACPD	ADCPD	BLUPD	GRNPD	REDPD
001000 (08h)	Setup Reg 6	20	RW	0	CLAMPCTRL	RLCEN	POSNNEG	VDEL[2]	VDEL[1]	VDEL[0]	VSMPDET
001001 (09h)	Reserved	00	RW	0	0	0	0	0	0	0	0
001010 (0Ah)	Reserved	00	RW	0	0	0	0	0	0	0	0
001011 (0Bh)	Reserved	00	RW	0	0	0	0	0	0	0	0
001100 (0Ch)	Reserved	00	RW	0	0	0	0	0	0	0	0
100000 (20h)	DAC Value (Red)	80	RW	DACR[7]	DACR[6]	DACR[5]	DACR[4]	DACR[3]	DACR[2]	DACR[1]	DACR[0]
100001 (21h)	DAC Value (Green)	80	RW	DACG[7]	DACG[6]	DACG[5]	DACG[4]	DACG[3]	DACG[2]	DACG[1]	DACG[0]
100010 (22h)	DAC Value (Blue)	80	RW	DACB[7]	DACB[6]	DACB[5]	DACB[4]	DACB[3]	DACB[2]	DACB[1]	DACB[0]
100011 (23h)	DAC Value (RGB)	00	W	DACRGB[7]	DACRGB[6]	DACRGB[5]	DACRGB[4]	DACRGB[3]	DACRGB[2]	DACRGB[1]	DACRGB[0]
100100 (24h)	PGA Gain LSB (Red)	00	RW	0	0	0	0	0	0	0	PGAR[0]
100101 (25h)	PGA Gain LSB (Green)	00	RW	0	0	0	0	0	0	0	PGAG[0]
100110 (26h)	PGA Gain LSB (Blue)	00	RW	0	0	0	0	0	0	0	PGAB[0]
100111 (27h)	PGA Gain LSB (RGB)	00	W	0	0	0	0	0	0	0	PGARGB[0]
101000 (28h)	PGA Gain MSBs (Red)	0C	RW	PGAR[8]	PGAR[7]	PGAR[6]	PGAR[5]	PGAR[4]	PGAR[3]	PGAR[2]	PGAR[1]
101001 (29h)	PGA Gain MSBs (Green)	0C	RW	PGAG[8]	PGAG[7]	PGAG[6]	PGAG[5]	PGAG[4]	PGAG[3]	PGAG[2]	PGAG[1]
101010 (2Ah)	PGA Gain MSBs (Blue)	0C	RW	PGAB[8]	PGAB[7]	PGAB[6]	PGAB[5]	PGAB[4]	PGAB[3]	PGAB[2]	PGAB[1]
101011 (2Bh)	PGA Gain MSBs (RGB)	00	W	PGARGB[8]	PGARGB[7]	PGARGB[6]	PGARGB[5]	PGARGB[4]	PGARGB[3]	PGARGB[2]	PGARGB[1]

Table 7 Register Map

REGISTER MAP DESCRIPTION

The following table describes the function of each of the control bits shown in Table 7.

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Setup Register 1	0	EN	1	Global Enable 0 = complete power down, 1 = fully active (individual blocks can be disabled using individual power down bits – see setup register 5).
	1	CDS	1	Select correlated double sampling mode: 0 = single ended mode, 1 = CDS mode.
	2	MONO	0	Sampling mode select (see Table 5 for further details): 0 = other mode (2 or 3-channel) 1 = Monochrome (1-channel) mode. Input channel selected by CHAN[1:0] register bits, unused channels are powered down.
	3	TWOCHAN	0	Sampling mode select (see Table 5 for further details): 0 = other mode (1 or 3-channel) 1 = 2-channel mode. Inputs channels are Red and Green, Blue channel is powered down.
	5:4	PGAFS[1:0]	00	Offsets PGA output to optimise the ADC range for different polarity sensor output signals. Zero differential PGA input signal gives: 0x = Zero output from the PGA (Output code=32767) 10 = Full-scale positive output (OP=65535) - use for negative going video. NB, Set INVOP=1 if zero differential input should give a zero output code with negative going video. 11 = Full-scale negative output (OP=0) - use for positive going video
	6	MODE4LEG	0	This bit has no effect when LEGACY=0. Set this bit when operating in LEGACY MODE4: 0 = other modes, 1 = LEGACY MODE4.
	7	LEGACY	0	Makes the WM8214 timing compatible with the WM819x and WM815x AFE families. 0 = Normal timing 1 = Enable LEGACY timing. Requires double rate MCLK and pixel rate VSMP input. RSMP pin performs same function as RLC/ACYC pin on WM819x devices.

<table>
<tr><th>REGISTER</th><th>BIT NO</th><th>BIT NAME(S)</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="8">Setup Register 2</td><td>1:0</td><td>OPFORM[1:0]</td><td>0</td><td>Determines the output data format.
x0 = 8-bit multiplexed (8+8 bits)
01 = 8-bit parallel (8-MSBs only)
11 = 4-bit multiplexed mode (4+4+4+4 bits). This mode is only valid when LEGACY=1.</td></tr>
<tr><td>2</td><td>INVOP</td><td>0</td><td>Digitally inverts the polarity of output data.
0 = negative going video gives negative going output,
1 = negative-going video gives positive going output data.</td></tr>
<tr><td>3</td><td>OPD</td><td>0</td><td>Output Disable. This works with the OEB pin to control the output pins.
0=Digital outputs enabled, 1=Digital outputs high impedance
<table>
<tr><th>OEB (pin)</th><th>OPD</th><th>OP pins</th></tr>
<tr><td>0</td><td>0</td><td>Enabled</td></tr>
<tr><td>0</td><td>1</td><td>High Impedance</td></tr>
<tr><td>1</td><td>0</td><td>High Impedance</td></tr>
<tr><td>1</td><td>1</td><td>High impedance</td></tr>
</table></td></tr>
<tr><td>4</td><td>LOWREFS</td><td>0</td><td>Reduces the ADC reference range (2*[VRT-VRB]), thus changing the max/min input voltages.
0= ADC reference range = 2.0V
1= ADC reference range = 1.2V</td></tr>
<tr><td>5</td><td>RLCDACRNG</td><td>1</td><td>Sets the output range of the RLCDAC.
0 = RLCDAC ranges from 0 to AVDD (approximately),
1 = RLCDAC ranges from 0 to VRT (approximately).</td></tr>
<tr><td>7:6</td><td>DEL[1:0]</td><td>00</td><td>Controls the latency from sample to data appearing on output pins
<table>
<tr><th></th><th colspan="3">Latency</th></tr>
<tr><th>DEL</th><th>LEGACY=0
All timing modes</th><th>LEGACY=1
timing modes 1-2,4-6</th><th>LEGACY=1
timing mode 3</th></tr>
<tr><td>00</td><td>7 MCLK periods</td><td>16.5 MCLK periods</td><td>23.5 MCLK periods</td></tr>
<tr><td>01</td><td>8 MCLK periods</td><td>18.5 MCLK periods</td><td>26.5 MCLK periods</td></tr>
<tr><td>10</td><td>9 MCLK periods</td><td>20.5 MCLK periods</td><td>29.5 MCLK periods</td></tr>
<tr><td>11</td><td>10 MCLK periods</td><td>22.5 MCLK periods</td><td>31.5 MCLK periods</td></tr>
</table></td></tr>
</table>

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Setup Register 3	3:0	RLCDAC[3:0]	1111	Controls RLCDAC driving VRLC/VBIAS pin to define single ended signal reference voltage or Reset Level Clamp voltage. See Electrical Characteristics section for ranges.
	5:4	CDSREF[1:0]	01	When LEGACY=0 these register bits have no effect. CDS mode reset timing adjust. 00 = Advance reset sample by 1 MCLK period (relative to default). 01 = Default reset sample position. 10 = Delay reset sample by 1 MCLK period (relative to default) 11 = Delay reset sample by 2 MCLK periods (relative to default)
	7:6	CHAN[1:0]	00	When MONO=0 these register bits have no effect Monochrome mode channel select. 00 = Red channel select 10 = Blue channel select 01 = Green channel select 11 = Reserved
Software Reset				Any write to Software Reset causes all cells to be reset. It is recommended that a software reset be performed after a power-up before any other register writes.
Auto-cycle Reset				Any write to Auto-cycle Reset causes the auto-cycle counter to reset to RINP. This function is only required when LINEBYLINE = 1.
Setup Register 4	0	LINEBYLINE	0	Selects line by line operation. Line by line operation is intended for use with systems which operate one line at a time but with up to three colours shared on that one output. 0 = normal operation, 1 = line by line operation. When line by line operation is selected MONO is forced to 1 and CHAN[1:0] to 00 internally, ensuring that the correct internal timing signals are produced. Green and Blue PGAs are also disabled to save power.
	1	ACYC	0	When LINEBYLINE = 0 this bit has no effect. When LINEBYLINE = 1 this bit determines the function of the RSMP input pin and the offset/gain register controls. 0 = RSMP pin enabled for either reset sampling (CDS) or Reset Level Clamp control. Internal selection of gain/offset multiplexers using INTM[1:0] register bits. 1 = Auto-cycling enabled by pulsing the RSMP input pin. This means that each time a pulse is applied to this pin the single input channel will switch to the next offset register and gain register in the sequence. The sequence is Red->Green->Blue->Red… offset and gain registers applied to the red input channel. When auto-cycling is enabled, the RSMP pin cannot be used to control reset level clamping. The CLMPCTRL bit may be used instead (enabled when high, disabled when low). NB, when auto-cycling is enabled, the RSMP pin cannot be used for reset sampling (i.e. CDS must be set to 0).
	3:2	INTM[1:0]	00	When LINEBYLINE=0 or ACYC=1 this bit has no effect. When LINEBYLINE=1 and ACYC=0: Controls the PGA/offset mux selector: 00 = Red PGA/Offset registers applied to input channel 01 = Green PGA/Offset registers applied to input channel 10 = Blue PGA/Offset registers applied to input channel 11 = Reserved.
	7:4	Reserved	0000	Must be set to 0

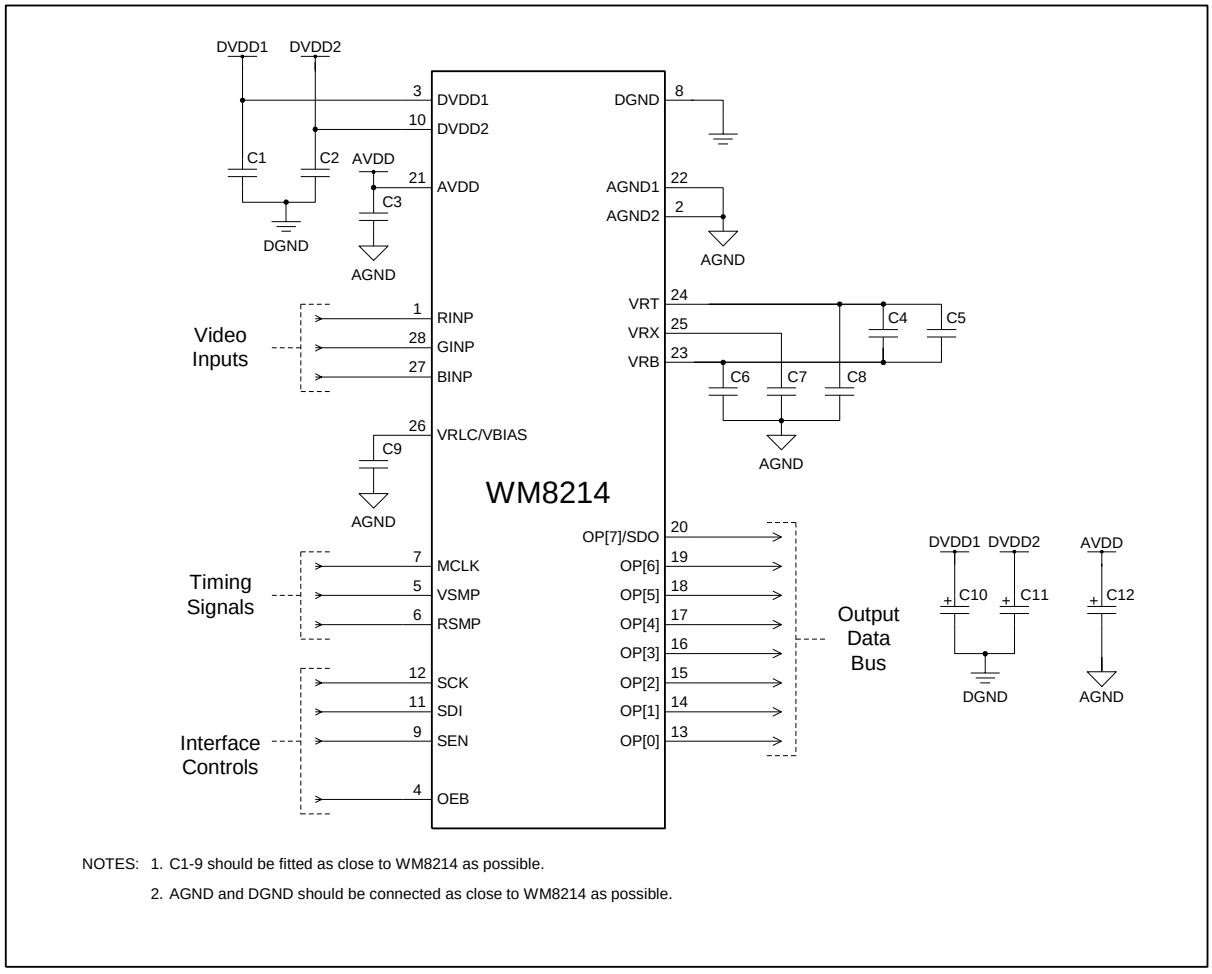
REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Setup Register 5	0	REDPD	0	When set powers down red S/H, PGA
	1	GRNPD	0	When set powers down green S/H, PGA
	2	BLUPD	0	When set powers down blue S/H, PGA
	3	ADCPD	0	When set powers down ADC. Allows reduced power consumption without powering down the references which have a long time constant when switching on/off due to the external decoupling capacitors.
	4	VRLCDACPD	0	When set powers down 4-bit RLCDAC, setting the output to a high impedance state and allowing an external reference to be driven in on the VRLC/VBIAS pin.
	5	ADCREFPD	0	When set disables VRT, VRB buffers to allow external references to be used.
	6	VRXPD	0	When set disables VRX buffer to allow an external reference to be used.
	7	Reserved	0	Must be set to 0
Setup Register 6	0	VSMPDET	0	When LEGACY=0 this register bit has no effect. When LEGACY=1: 0 = Normal operation, signal on VSMP input pin is applied directly to Timing Control block. 1 = Programmable VSMP detect circuit is enabled. An internal synchronisation pulse is generated from signal applied to VSMP input pin and is applied to Timing Control block in place of VSMP.
	3:1	VDEL[2:0]	000	When LEGACY=0 or VSMPDET=0 these bits have no effect. The VDEL bits set a programmable delay from the detected edge of the signal applied to the VSMP pin. The internally generated pulse is delayed by VDEL MCLK periods from the detected edge. See Figure **20**, Internal VSMP Pulses Generated for details.
	4	POSNNEG	0	When LEGACY=0 or VSMPDET=0 this bit has no effect. When LEGACY=1 and VSMPDET=1 this bit controls whether positive or negative edges on the VSMP input pin are detected: 0 = Negative edge on VSMP pin is detected and used to generate internal timing pulse. 1 = Positive edge on VSMP pin is detected and used to generate internal timing pulse. See Figure **20** for further details.
	5	RLCEN	1	Reset Level Clamp Enable. When set Reset Level Clamping is enabled. The method of clamping is determined by CLAMPCTRL and LEGACY. In LEGACY mode clamping will still occur on every pixel at a time defined by the CDSREF[1:0] bits.
	6	CLAMPCTRL	0	This bit has no effect if LEGACY=1. See Table 2 for more information. 0 = RLC switch is controlled directly from RSMP input pin: RSMP = 0: switch is open RMSP = 1: switch is closed 1 = RLC switch is controlled by logical combination of RSMP and VSMP. RSMP && VSMP = 0: switch is open RSMP && VSMP = 1: switch is closed
	7	Reserved	0	Must be set to 0

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Offset DAC (Red)	7:0	DACR[7:0]	10000000	Red channel 8-bit offset DAC value (mV) = 260*(DACR[7:0]-127.5)/127.5
Offset DAC (Green)	7:0	DACG[7:0]	10000000	Green channel 8-bit offset DAC value (mV) = 260*(DACG[7:0]-127.5)/127.5
Offset DAC (Blue)	7:0	DACB[7:0]	10000000	Blue channel 8-bit offset DAC value (mV) = 260*(DACB[7:0]-127.5)/127.5
Offset DAC (RGB)	7:0	DACRGB[7:0]	0	A write to this register location causes the red, green and blue offset DAC registers to be overwritten by the new value
PGA Gain LSB (Red)	0	PGAR[0]	0	This register bit forms the LSB of the red channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 28 hex.
PGA Gain LSB (Green)	0	PGAG[0]	0	This register bit forms the LSB of the green channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 29 hex.
PGA Gain LSB (Blue)	0	PGAB[0]	0	This register bit forms the LSB of the blue channel PGA gain code. PGA gain is determined by combining this register bit and the 8 MSBs contained in register address 2A hex.
PGA Gain LSB (RGB)	0	PGARGB[0]	0	Writing a value to this location causes red, green and blue PGA LSB gain values to be overwritten by the new value.
PGA gain MSBs (Red)	7:0	PGAR[8:1]	00001100	Bits 8 to 1 of red PGA gain. Combined with red LSB register bit to form complete PGA gain code. This determines the gain of the red channel PGA according to the equation: Red channel PGA gain (V/V) = 0.66 + PGAR[8:0]x7.34/511
PGA gain MSBs (Green)	7:0	PGAG[8:1]	00001100	Bits 8 to 1 of green PGA gain. Combined with green LSB register bit to form complete PGA gain code. This determines the gain of the green channel PGA according to the equation: Green channel PGA gain (V/V) = 0.66 + PGAG[8:0]x7.34/511
PGA gain MSBs (Blue)	7:0	PGAB[8:1]	00001100	Bits 8 to 1 of blue PGA gain. Combined with blue LSB register bit to form complete PGA gain code. This determines the gain of the blue channel PGA according to the equation: Blue channel PGA gain (V/V) = 0.66 + PGAB[8:0]x7.34/511
PGA gain MSBs(RGB)	7:0	PGARGB[8:1]	0	A write to this register location causes the red, green and blue PGA MSB gain registers to be overwritten by the new value.

Table 8 Register Control Bits

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



NOTES: 1. C1-9 should be fitted as close to WM8214 as possible.

2. AGND and DGND should be connected as close to WM8214 as possible.

Figure 25 External Components Diagram

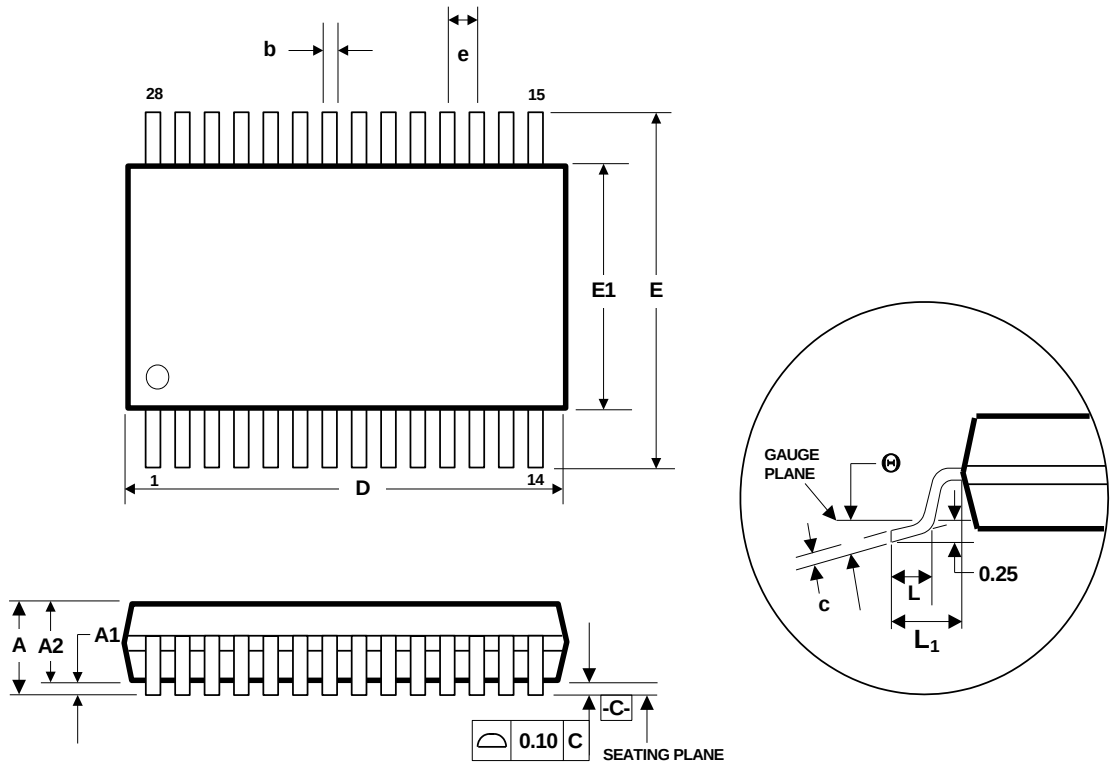
RECOMMENDED EXTERNAL COMPONENT VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	100nF	De-coupling for DVDD1.
C2	100nF	De-coupling for DVDD2.
C3	100nF	De-coupling for AVDD.
C4	10nF	High frequency de-coupling between VRT and VRB.
C5	1µF	Low frequency de-coupling between VRT and VRB (non-polarised).
C6	100nF	De-coupling for VRB.
C7	100nF	De-coupling for VRX.
C8	100nF	De-coupling for VRT.
C9	100nF	De-coupling for VRLC.
C10	10µF	Reservoir capacitor for DVDD1.
C11	10µF	Reservoir capacitor for DVDD2.
C12	10µF	Reservoir capacitor for AVDD.

Table 9 External Components Descriptions

PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.E**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	0.25
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		1.25 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES	CHANGED BY
23/02/07	4.0	Updated all references throughout doc from VRLCDACEN to VRLCDACPD Added Note in POR section to recommend a software reset is written to the software Register after power is cycled to the device, p12.	JB
16/03/07	4.1	Input Video Sampling, Note 2 Removed: In Three-Channel mode, if the VSMP falling edge is placed more than 4ns before the rising edge of MCLK the output amplitude of the WM8214 will increase, p 9.	JB
24/04/08	4.2	Changed Serial Control Interface Timing to remove tSCE and replace with tSCRSER and tSCFSEF, p10. Updated Serial Control Interface Timing Table to match diagram, p10. Corrected Default PGA MSB values from '0D' to '0C' in register tables, p29 and p33	NB
17/6/8	4.3	Register Map: Default 23h changed from 80 to 00, p29	JMacD
		DACR[7:0], DACG[7:0] and DACB[7:0] default changed to 10000000 PGAR[8:1], PGAG[8:1] and PGAB[8:1] default changed to 00001100, p33	
07/06/08	4.4	Order Info: /V and /RV added to part numbers. MSL changed from MSL1 to MSL2, p3	JMacD
16/01/20	4.5	Ordering Information and Absolute Maximum Ratings updated – MSL information removed	PH

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