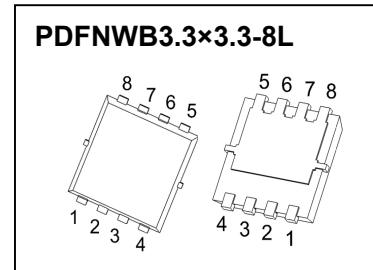


CJAB25P03 P-Channel Power MOSFET

V_{(BR)DSS}	R_{DS(on)MAX}	I_D
-30V	20mΩ@-10V	-25A



DESCRIPTION

The CJAB25P03 uses advanced trench technology and design to provide excellent R_{DS(ON)} with low gate charge. It can be used in a wide variety of applications

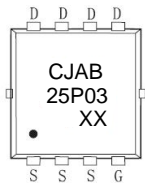
FEATURES

- High density cell design for ultra low R_{DS(ON)}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

APPLICATIONS

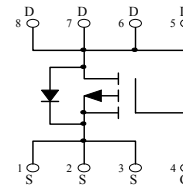
- Battery and loading switching

MARKING



CJAB25P03 = Part No.
 Solid dot=Pin1 indicator
 XX=Date Code

EQUIVALENT CIRCUIT



MAXIMUM RATINGS (T_a=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-30	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D ⁽¹⁾	-25	A
Pulsed Drain Current	I _{DM}	-100	A
Single Pulsed Avalanche Energy	E _{AS} ⁽¹⁾	150	mJ
Power Dissipation	P _D	3	W
Thermal Resistance from Junction to Ambient	R _{θJA} ⁽²⁾	41.67	°C/W
Junction Temperature	T _J	150	°C
Storage Temperature Range	T _{stg}	-55 ~+150	°C
Lead Temperature for Soldering Purposes(1/8" from case for 10s)	T _L	260	°C

(1).EAS condition: VDD=15V,L=0.1mH, RG=25Ω, Starting T_J = 25°C

(2).Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

MOSFET ELECTRICAL CHARACTERISTICS

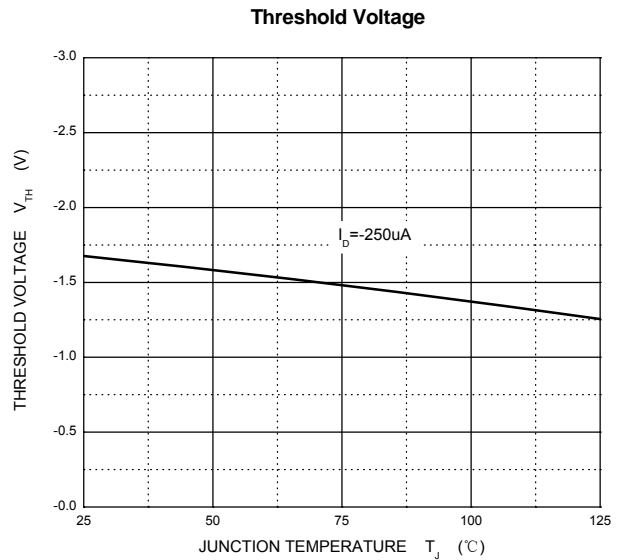
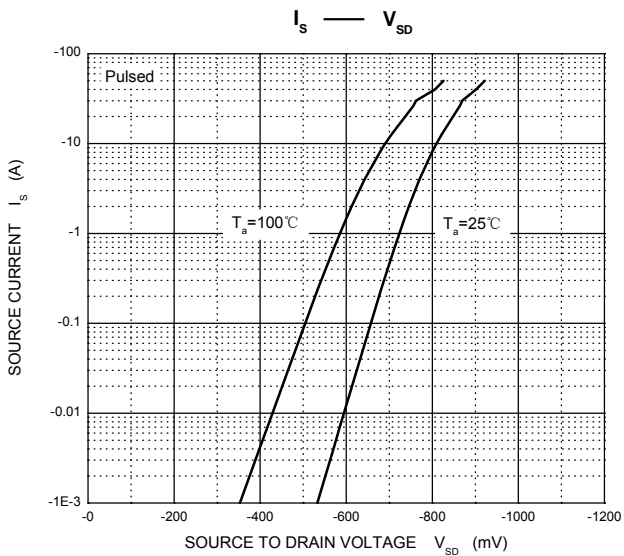
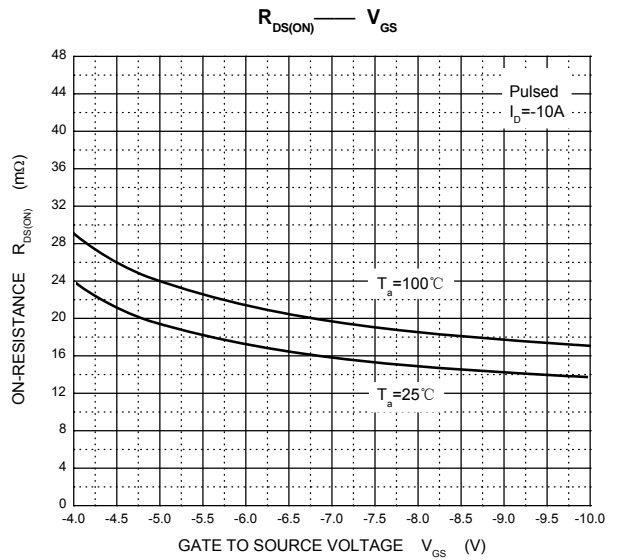
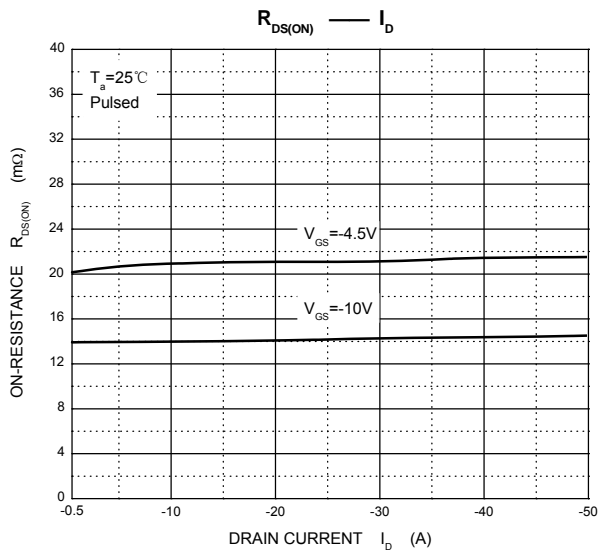
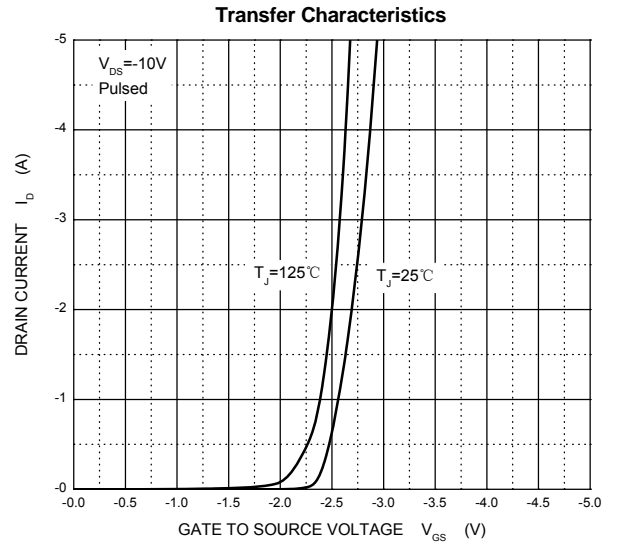
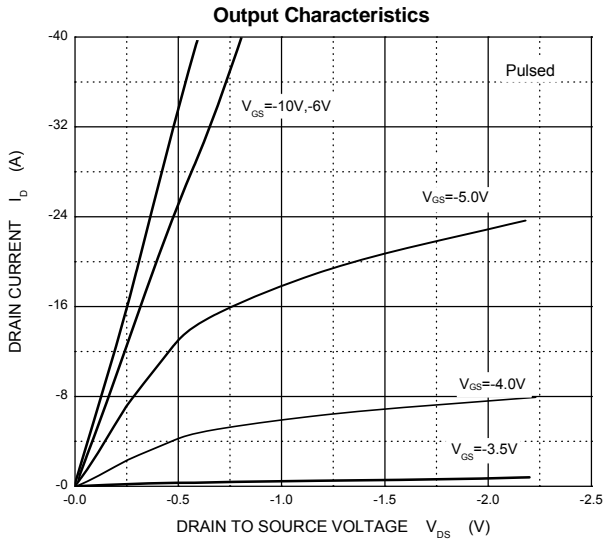
$T_a=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
Gate-body leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
On characteristics (note1)						
Gate-threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.6	-3	V
Static drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -10A$		14	20	$m\Omega$
		$V_{GS} = -4.5V, I_D = -10A$		21	34	$m\Omega$
Forward transconductance	g_{fs}	$V_{DS} = -10V, I_D = -10A$		22		S
Dynamic characteristics (note 2)						
Input capacitance	C_{iss}	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1MHz$		1700		μF
Output capacitance	C_{oss}			296		
Reverse transfer capacitance	C_{rss}			205		
Switching characteristics (note 2)						
Total gate charge	Q_g	$V_{DS} = -15V, I_D = -10A,$ $V_{GS} = -10V$		30		nC
Gate-source charge	Q_{gs}			6		
Gate-drain charge	Q_{gd}			9		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15V, I_D = -1A, R_L = 15\Omega$ $V_{GS} = -10V, R_G = 2.5\Omega$		10		ns
Turn-on rise time	t_r			26		
Turn-off delay time	$t_{d(off)}$			35		
Turn-off fall time	t_f			8		
Drain-Source Diode Characteristics						
Drain-source diode forward voltage(note1)	V_{SD}	$V_{GS} = 0V, I_S = -10A$		-0.8	-1.2	V
Continuous drain-source diode forward current(note3)	I_S				-25	A
Pulsed drain-source diode forward current	I_{SM}				-100	A

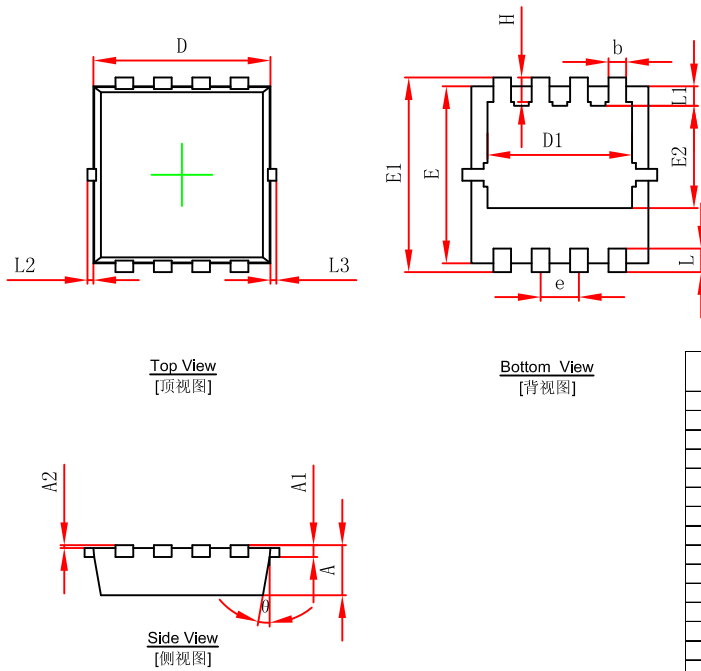
Notes:

1. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production.
3. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Typical Characteristics

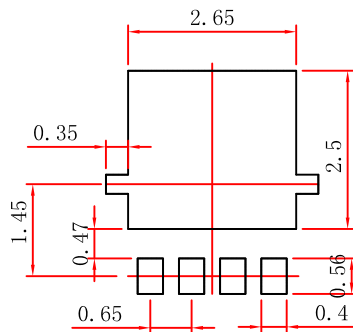


PDFNWB3.3x3.3-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3.3x3.3-8L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.05 mm.
3. The pad layout is for reference purposes only.

NOTICE

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