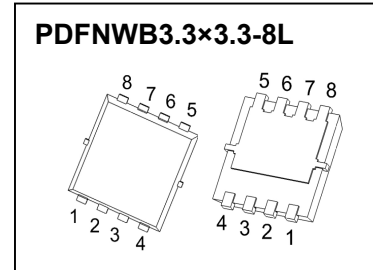


CJAB40SN10 N-Channel Power MOSFET

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
100V	8.5mΩ@10V	40A
	11mΩ@4.5V	



DESCRIPTION

The CJAB40SN10 uses SGT technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

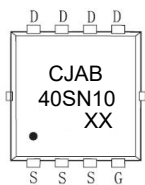
FEATURES

- Load switch
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

APPLICATIONS

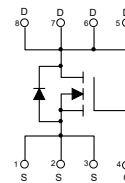
- SMPS and general purpose applications
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

MARKING



CJAB40SN10 = Part No.
 Solid dot=Pin1 indicator
 XX=Code

EQUIVALENT CIRCUIT



MAXIMUM RATINGS ($T_a=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_D^{①}$	40	A
Pulsed Drain Current	$I_{DM}^{②}$	160	A
Single Pulsed Avalanche Energy	$E_{AS}^{③}$	80	mJ
Power Dissipation	$P_D^{①}$	1.5	W
Thermal Resistance from Junction to Ambient	$R_{\theta JA}^{⑥}$	83.3	$^{\circ}C/W$
Junction Temperature	T_J	150	$^{\circ}C$
Storage Temperature Range	T_{stg}	-55 ~+150	$^{\circ}C$
Lead Temperature for Soldering Purposes(1/8" from case for 10s)	T_L	260	$^{\circ}C$

MOSFET ELECTRICAL CHARACTERISTICS

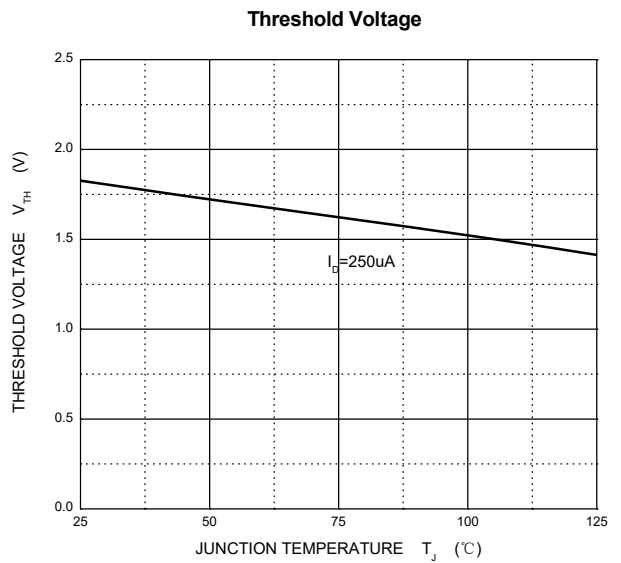
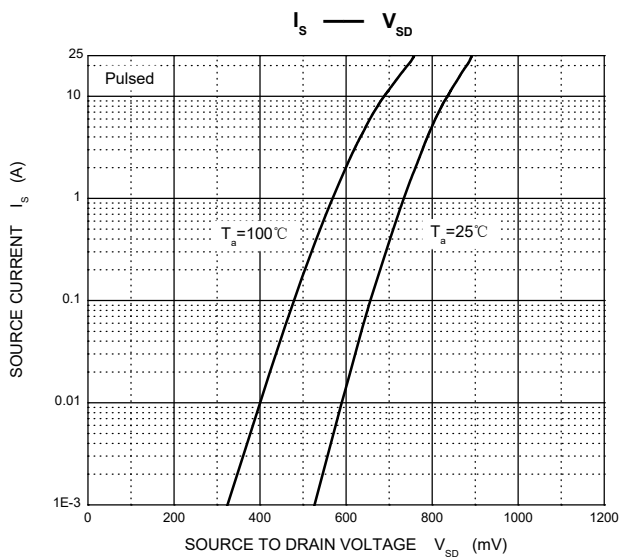
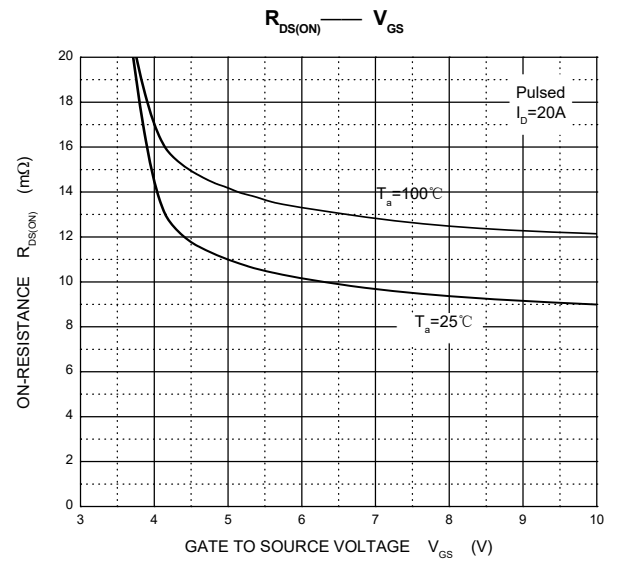
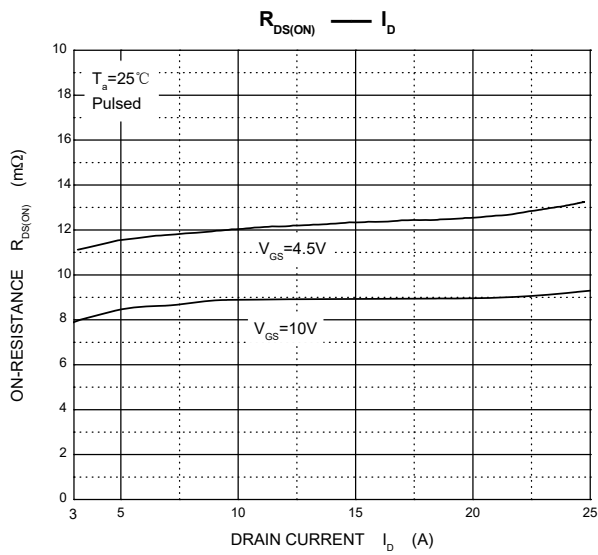
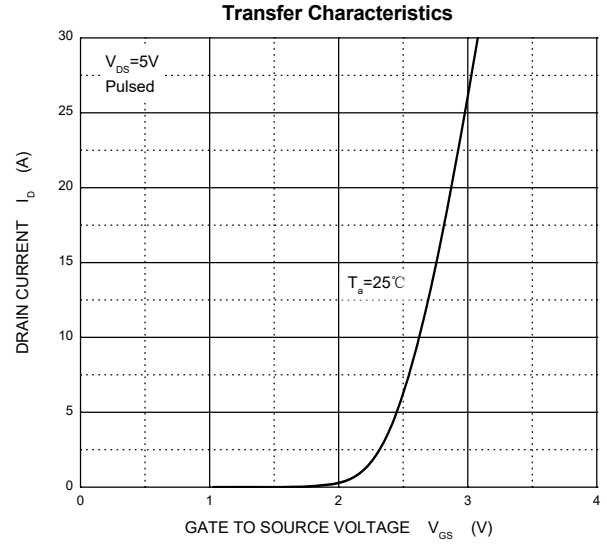
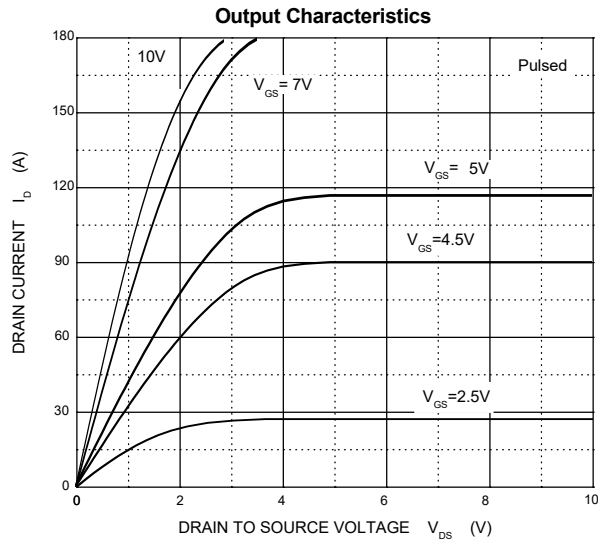
$T_a=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V$			1	μA
Gate-body leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
On characteristics ^④						
Gate-threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.4	1.8	2.2	V
Static drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 12A$		8.5	13	$m\Omega$
		$V_{GS} = 4.5V, I_D = 9A$		11	17	$m\Omega$
Dynamic characteristics ^{④ ⑤}						
Input capacitance	C_{iss}	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1MHz$		1460	2920	μF
Output capacitance	C_{oss}			280	560	
Reverse transfer capacitance	C_{rss}			5.2	11	
Gate resistance	R_g	$f = 1MHz$		1.4		Ω
Switching characteristics ^{④ ⑤}						
Total gate charge	Q_g	$V_{DS} = 50V,$ $V_{GS} = 10V, I_D = 20A$		25	50	nC
Gate-source charge	Q_{gs}			5.0	10	
Gate-drain charge	Q_{gd}			6.5	13	
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 50V, I_D = 20A,$ $V_{GS} = 10V, R_G = 10\Omega$		6.5	13	ns
Turn-on rise time	t_r			4.5	9.0	
Turn-off delay time	$t_{d(off)}$			19	38	
Turn-off fall time	t_f			3.5	7.0	
Drain-Source Diode Characteristics						
Drain-source diode forward voltage	V_{SD} ^④	$V_{GS} = 0V, I_S = 12A$			1.2	V
Continuous drain-source diode forward current	I_S ^①				40	A
Pulsed drain-source diode forward current	I_{SM} ^②				160	A
Reverse Recovery Time	t_{rr} ^④	$V_R = 50V, I_F = 20A,$ $dI_F/dt = 500A/\mu s$		42		ns
Reverse Recovery Charge	Q_{rr} ^④				160	

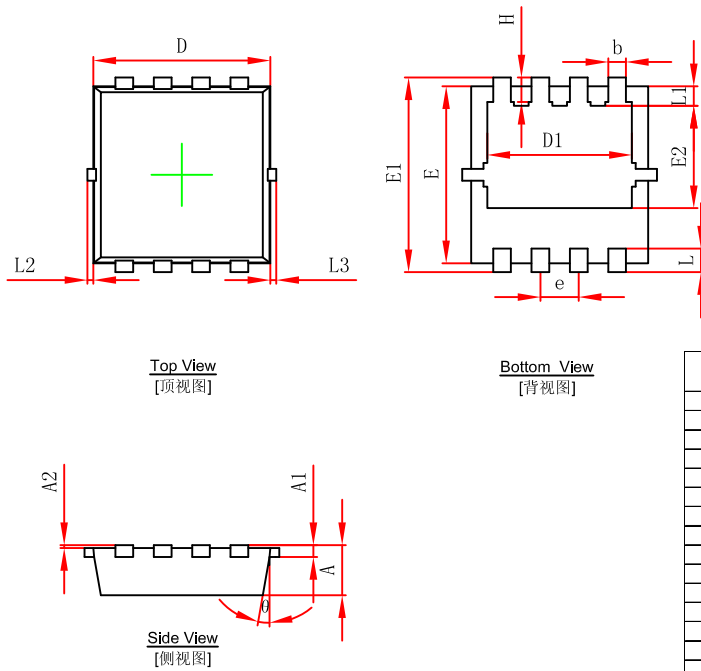
Notes:

1. $T_C = 25^\circ\text{C}$ Limited only by maximum temperature allowed.
2. $PW \leq 10\mu s$, Duty cycle $\leq 1\%$.
3. EAS condition: $V_{DD} = 50V, V_{GS} = 10V, L = 0.1mH, R_g = 25\Omega$ Starting $T_J = 25^\circ\text{C}$.
4. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. Guaranteed by design, not subject to production.
6. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a = 25^\circ\text{C}$.

Typical Characteristics

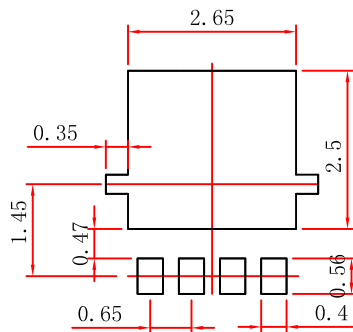


PDFNWB3.3x3.3-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3.3x3.3-8L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.05 mm.
3. The pad layout is for reference purposes only.

NOTICE

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