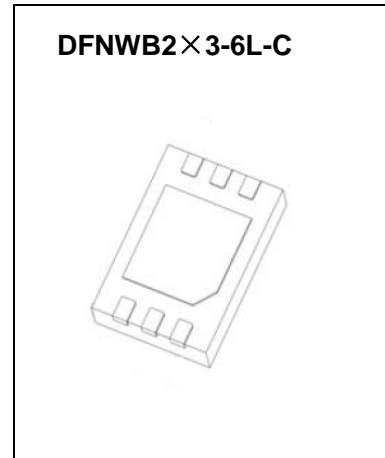


CJCD2005 Dual N-Channel MOSFET

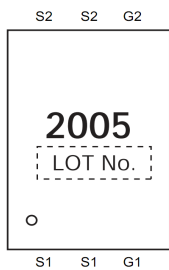
$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
20V	9 mΩ@4.5V	8A
	9.5mΩ@4.0V	
	9.7mΩ@3.8V	
	10.6mΩ@3.1V	
	12.5mΩ@2.5V	



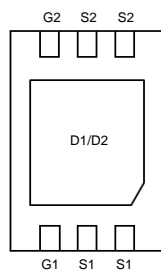
DESCRIPTION

The CJCD2005 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.

MARKING:

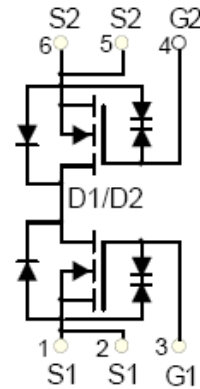


Top



Back

Equivalent Circuit



MAXIMUM RATINGS ($T_a=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	8	A
Pulsed Drain Current	I_{DM}^*	50	A
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	83.3	$^{\circ}C/W$
Junction Temperature	T_j	150	$^{\circ}C$
Storage Temperature	T_{stg}	-55~+150	$^{\circ}C$
Lead Temperature for Soldering Purposes(1/8" from case for 10 s)	T_L	260	$^{\circ}C$

MOSFET ELECTRICAL CHARACTERISTICS

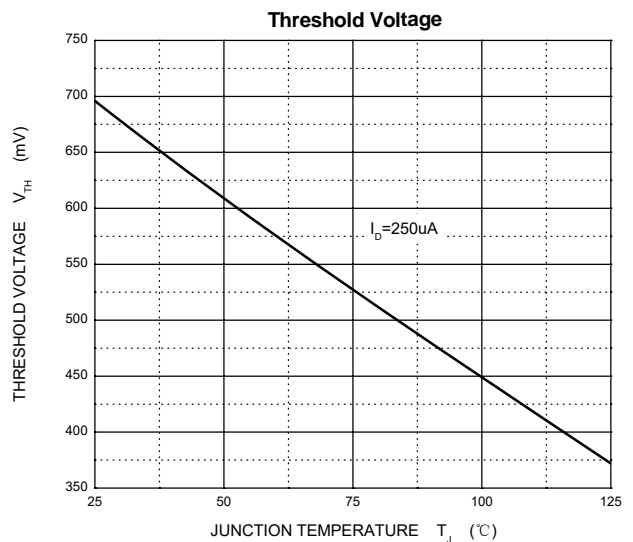
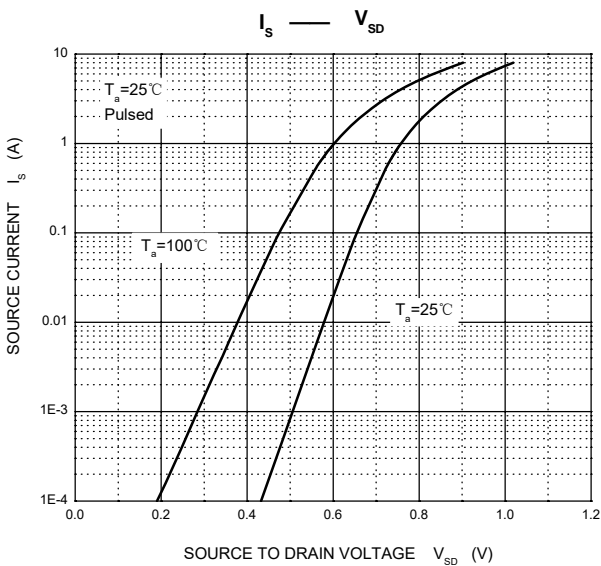
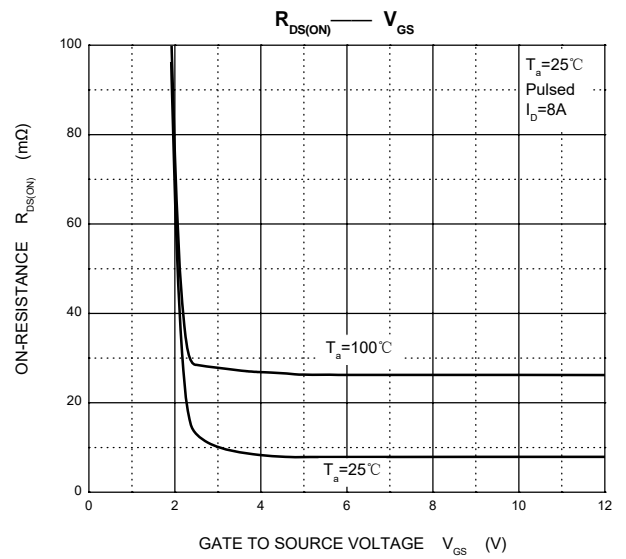
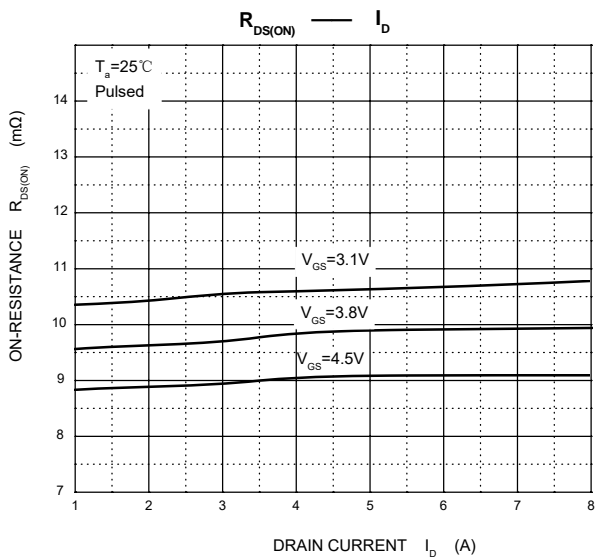
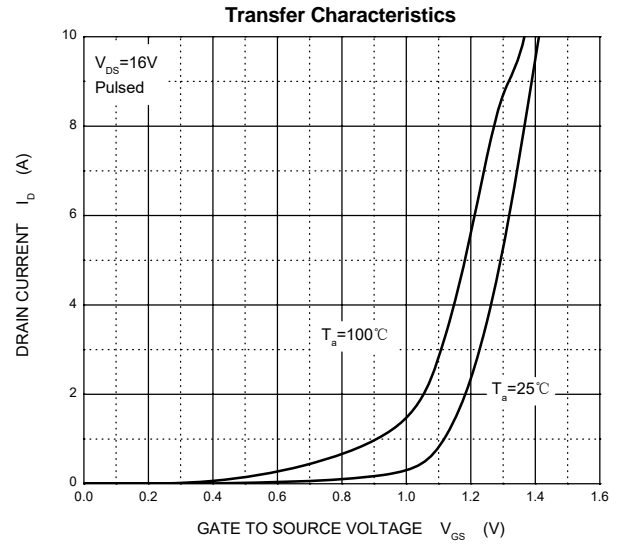
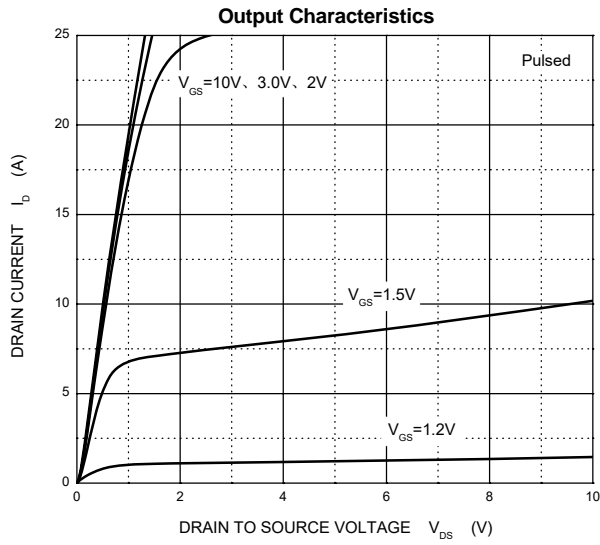
$T_a=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 16V, V_{GS} = 0V$			1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 4.5V, V_{DS} = 0V$			± 1	μA
		$V_{GS} = \pm 8V, V_{DS} = 0V$			± 10	μA
Gate threshold voltage (note 1)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.4		1	V
Drain-source on-resistance (note 1)	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 3A$	7	9	12.0	m Ω
		$V_{GS} = 4.0V, I_D = 3A$	7.3	9.5	12.5	m Ω
		$V_{GS} = 3.8V, I_D = 3A$	7.5	9.7	13.0	m Ω
		$V_{GS} = 3.1V, I_D = 3A$	8.0	10.6	14.0	m Ω
		$V_{GS} = 2.5V, I_D = 3A$	9.5	12.5	15.0	m Ω
Forward transconductance (note 1)	g_{FS}	$V_{DS} = 5V, I_D = 7A$	9	36		S
Diode forward voltage(note 1)	V_{SD}	$I_S = 1A, V_{GS} = 0V$			1	V
DYNAMIC PARAMETERS (note 2)						
Input Capacitance	C_{iss}	$V_{DS} = 10V, V_{GS} = 0V, f = 1MHz$		1800		pF
Output Capacitance	C_{oss}			230		pF
Reverse Transfer Capacitance	C_{rss}			200		pF
Total gate charge	Q_g	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 7A$		17		nC
Gate-source charge	Q_{gs}			1.5		nC
Gate-drain charge	Q_{gd}			4.7		nC
SWITCHING PARAMETERS (note 2)						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = 5V, V_{DD} = 10V,$ $R_L = 1.35\Omega, R_{GEN} = 3\Omega$		2.5		ns
Turn-on rise time	t_r			7.2		ns
Turn-off delay time	$t_{d(off)}$			49		ns
Turn-off fall time	t_f			108		ns
Drain-Source Diode Characteristics						
Diode Forward Current	I_S		-	-	6.0	A

Notes :

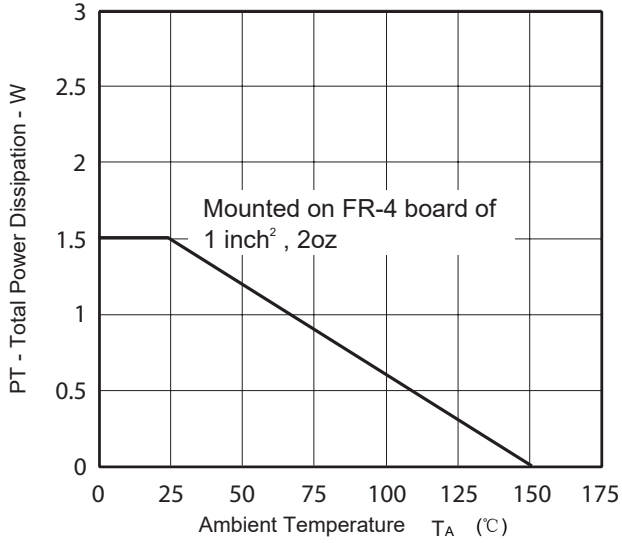
1. Pulse Test : Pulse width $\leq 300\mu s$, duty cycle $\leq 0.5\%$.
2. Guaranteed by design, not subject to production testing.

Typical Characteristics

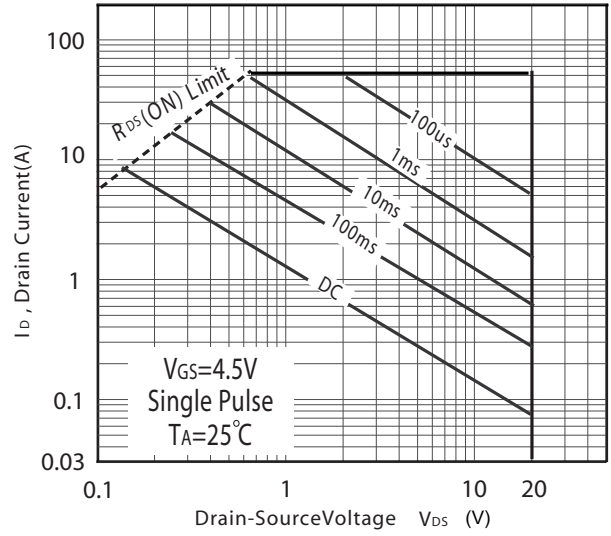


Typical Characteristics

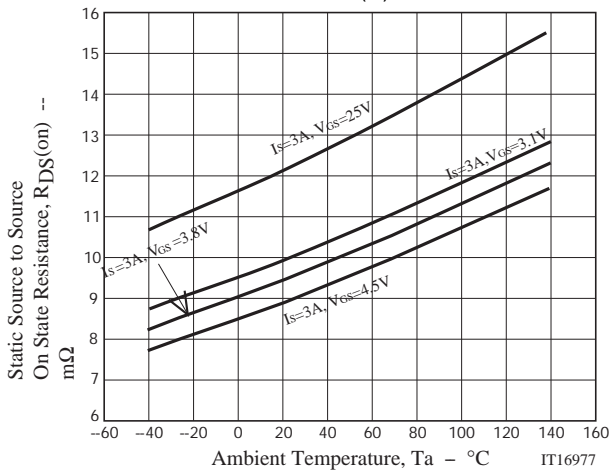
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



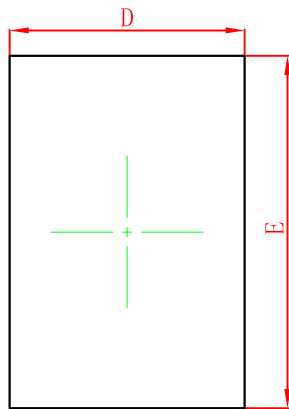
Maximum Safe Operating Area



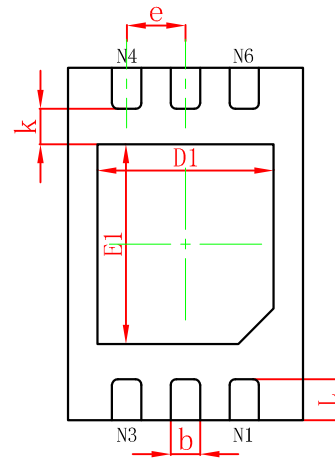
CJCD2005 $R_{DS(ON)}$ vs. T_A



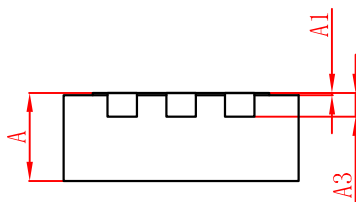
DFNWB2×3-6L Package Outline Dimensions(Unit:mm)



TOP VIEW



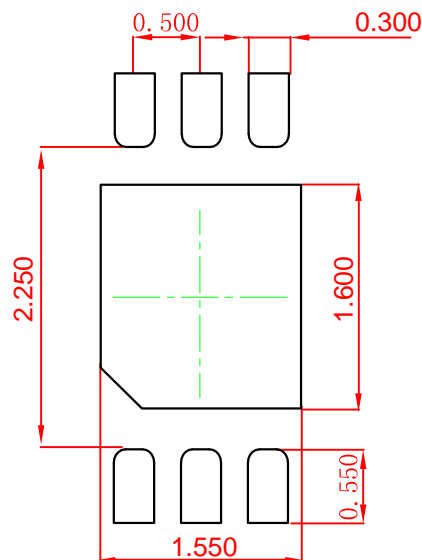
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.950	2.050	0.077	0.081
E	2.950	3.050	0.116	0.120
D1	1.450	1.550	0.057	0.061
E1	1.650	1.750	0.065	0.069
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.400	0.012	0.016

DFNWB2×3-6L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.050 mm.
3. The pad layout is for reference purposes only.

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