



JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD

TO-263K Plastic-Encapsulate Thyristors

CT312Q 3Q TRIACs

MAIN CHARACTERISTICS

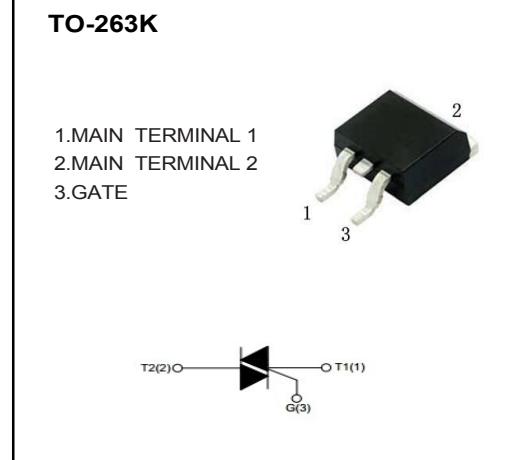
$I_{T(RMS)}$		12A
V_{DRM}/V_{RRM}	CT312Q-600S/C/B	600V
	CT312Q-800S/C/B	800V
V_{TM}		1.55V

FEATURES

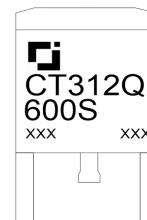
- NPNPN 5-layer Structure TRIACs
- Mesa Glass Passivated Technology
- Multi Layers Metal Electrodes
- High Junction Temperature
- Good Commutation Performance
- High dV/dt and dl/dt

APPLICATIONS

- Heater Control
- Motor Speed Controller
- Mixer



MARKING



CT312Q:Series Code
600S:Depends on V_{DRM} and IGT
XXX:Internal Code

ABSOLUTE RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test condition		Value	Unit
V_{DRM}/ V_{RRM}	Repetitive peak off-state voltage	$T_j=25^\circ\text{C}$	CT312Q-600S/C/B	600	V
			CT312Q-800S/C/B	800	V
$I_{T(RMS)}$	RMS on-state current	TO-263K($T_c \leq 105^\circ\text{C}$), Fig. 1,2		12	A
I_{TSM}	Non repetitive surge peak on-state current	Full sine wave , $T_j(\text{init})=25^\circ\text{C}$, tp=20ms; Fig. 3,5		120	A
I^2t	I^2t value	tp=10ms		78	A^2s
dl_t/dt	Critical rate of rise of on-state current	$I_G=2*I_{GT}$, $tr \leq 10\text{ns}$, $F=120\text{Hz}$, $T_j=125^\circ\text{C}$	I - II - III	50	$\text{A}/\mu\text{s}$
			IV	n/a	
I_{GM}	Peak gate current	tp=20 μs , $T_j=125^\circ\text{C}$		4	A
$P_{G(AV)}$	Average gate power	$T_j=125^\circ\text{C}$		1	W
T_{STG}	Storage temperature			-40~+150	$^\circ\text{C}$
T_j	Operating junction temperature			-40~+125	

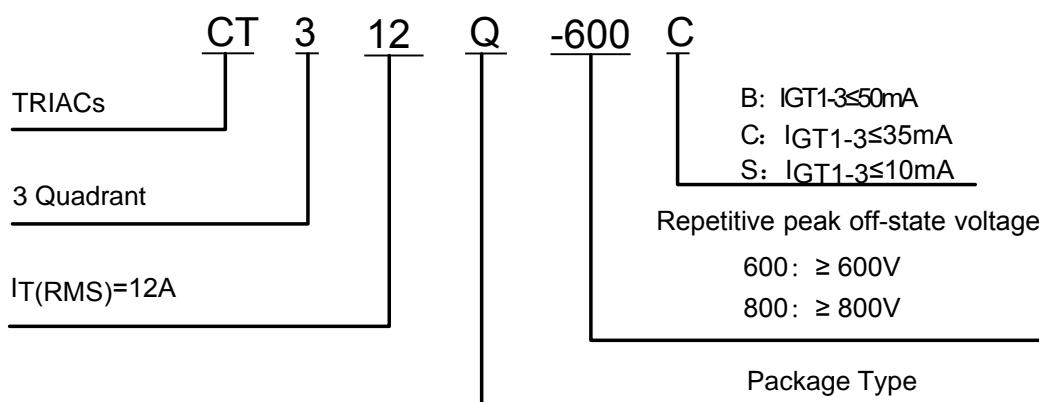
ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test condition	Value			Unit
			S	C	B	
I_{GT}	Gate trigger current	$V_D=12\text{V}$, $R_L=30\Omega$, $T_j=25^\circ\text{C}$, Fig. 6	≤ 10 IV	≤ 35 n/a	≤ 50 n/a	mA
V_{GT}	Gate trigger voltage		I - II - III	≤ 1.3		
V_{GD}	Non-triggering gate voltage	$V_D=V_{DRM}$, $R_L=3.3\text{k}\Omega$, $T_j=125^\circ\text{C}$	≥ 0.2			V
I_H	Holding current	$I_T=500\text{mA}$, Fig. 6	≤ 15	≤ 35	≤ 50	mA
I_L	Latching current	$I_G=1.2I_{GT}$, Fig. 6	≤ 25 II	≤ 50 ≤ 60	≤ 70 ≤ 80	mA
dV_D/dt	Critical rate of rise of off-state	$V_D=67\%V_{DRM}$, Gate Open $T_j=125^\circ\text{C}$	≥ 40	≥ 500	≥ 1000	V/ μs
V_{TM}	On-state Voltage	$I_{TM}=17\text{A}$, $t_p=380\mu\text{s}$, Fig. 4	≤ 1.55			V
I_{DRM} / I_{RRM}	Repetitive peak off-state current	$V_D=V_{DRM}/V_{RRM}$, $T_j=25^\circ\text{C}$	≤ 5	≤ 5	≤ 5	μA
		$V_D=V_{DRM}/V_{RRM}$, $T_j=125^\circ\text{C}$	≤ 1	≤ 1	≤ 1	mA

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th} (j-c)$	Junction to case (AC)	1.4	$^\circ\text{C/W}$
$R_{th} (j-a)$	Junction to ambient	45	$^\circ\text{C/W}$

PART NUMBER



CHARACTERISTICS CURVES

FIG.1: Maximum power dissipation versus RMS on-state current (full cycle)

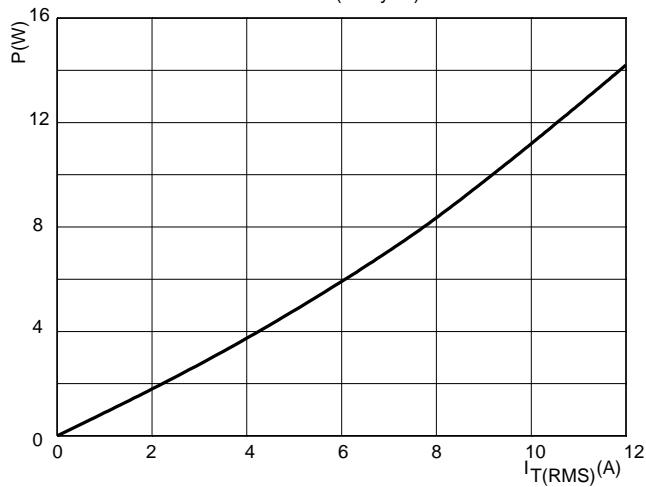


FIG.2: RMS on-state current versus case temperature (full cycle)

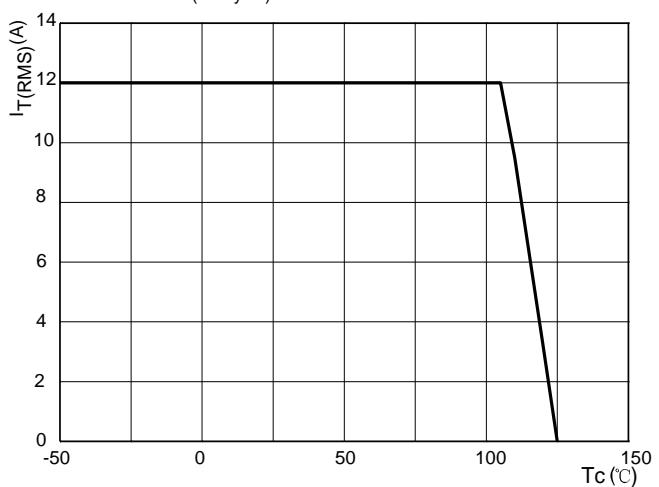


FIG.3: Surge peak on-state current versus number of cycles

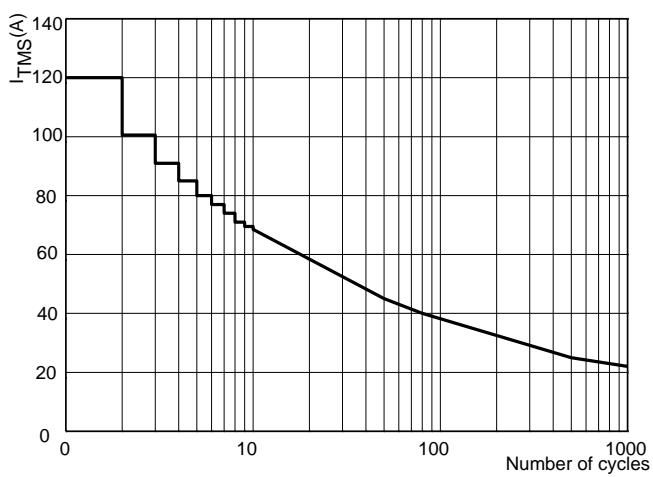


FIG.4: On-state characteristics (maximum values)

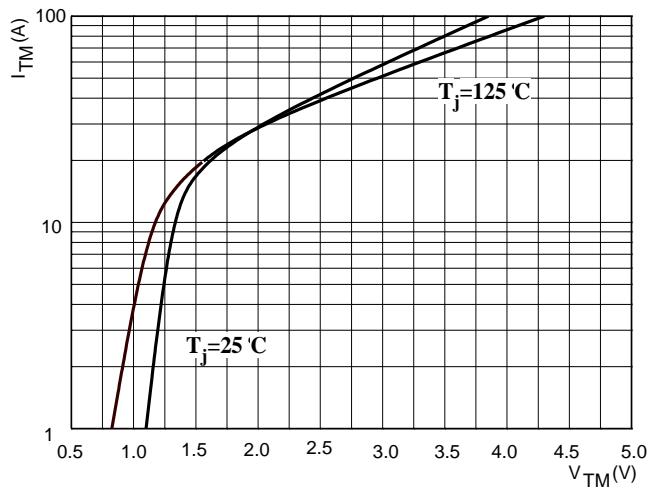


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ms}$

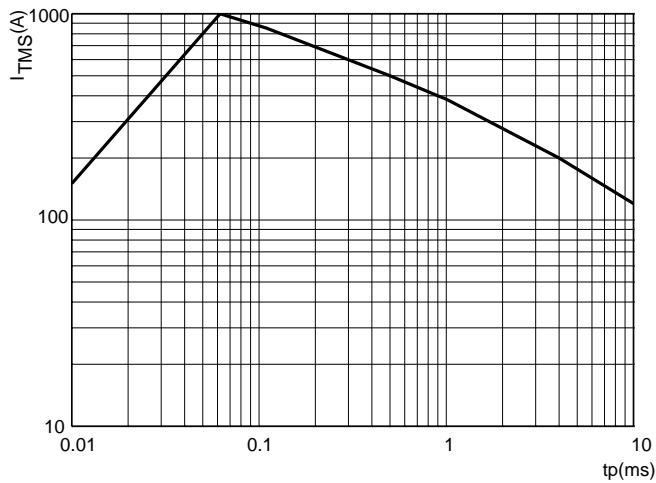
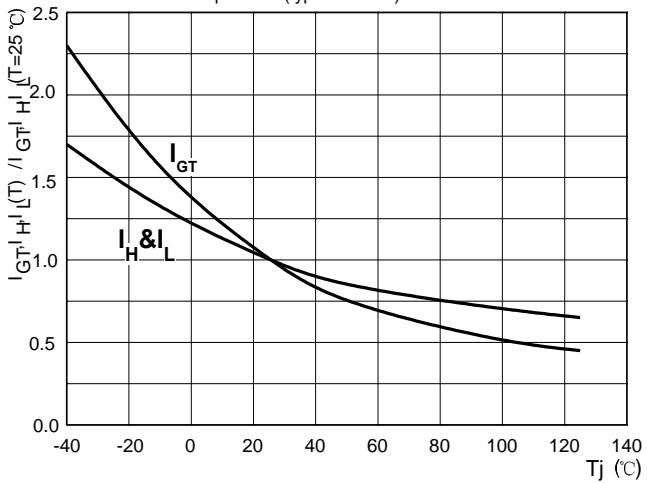
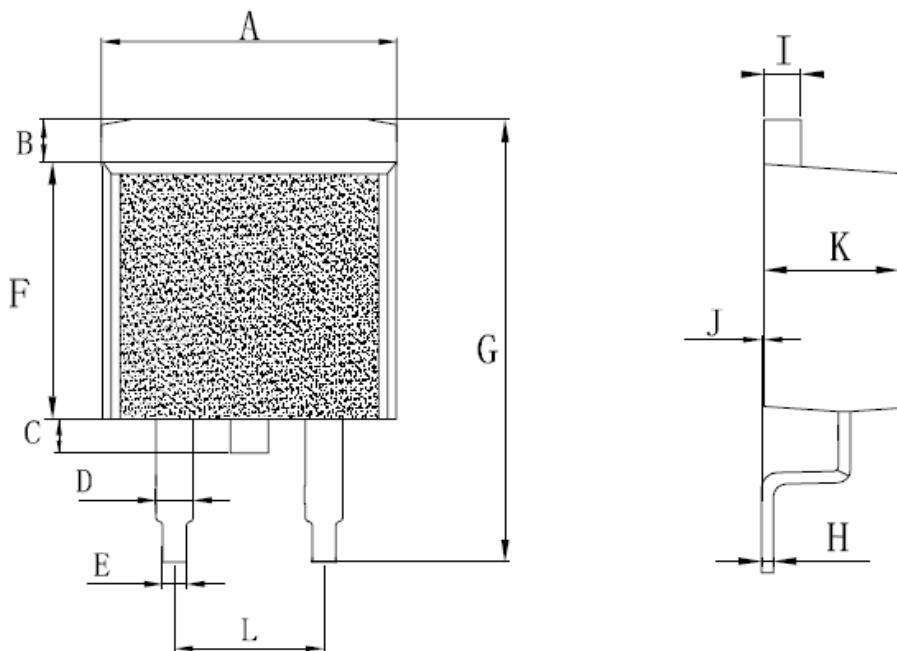


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature (typical values)



TO-263K PACKAGE OUTLINE DIMENSIONS



DIM.	Unit(mm)		Unit(inch)	
	Min	Max	Min	Max
A	9.7	10.4	0.381	0.409
B	1.31	1.62	0.051	0.063
C	0.65	1.22	0.025	0.048
D	1.15	1.36	0.045	0.053
E	0.62	0.95	0.024	0.037
F	8.75	9.32	0.344	0.366
G	14.75	15.8	0.580	0.622
H	0.32	0.48	0.012	0.018
I	1.18	1.36	0.046	0.053
J	0	0.15	0	0.005
K	4.38	4.86	0.172	0.191
L	4.85	5.23	0.190	0.205

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