

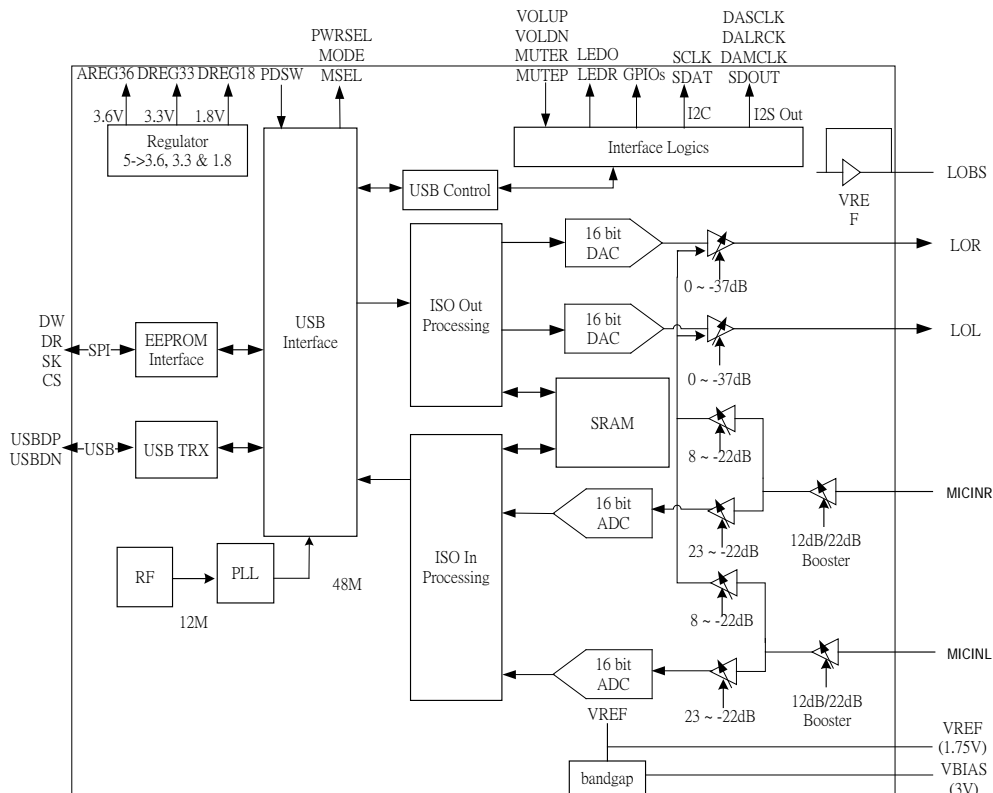
### DESCRIPTION

The CM118B is a highly integrated, crystal-less USB audio single chip solution optimized for USB headset, headphone, dongle, microphone and application such as VoIP (voice over Internet protocol). All essential analog modules are embedded in the CM118B, including dual DAC and ADC, earphone driver, microphone booster, PLL, regulator, and USB transceiver. It also supports 3 GPIO pins. In addition, audio adjustment can be easily controlled via specific HID compliant volume control pins. Many features such as headset, headphone and microphone only topologies are programmable with jumper pins. Vender can customize unique USB VID / PID / Product String / Manufacture String and min/max/initial volumes to the external EEPROM. The CM118B also offers anti-pop noise circuits design and internal oscillator which can operate without an external crystal oscillator.

### FEATURES

- Compliant with USB 2.0 Full Speed Operation
- Compliant with USB Audio Device Class v1.0
- Supports USB Suspend/Resume Mode and Remote Wakeup with Volume Control pins
- On-chip oscillator to provide reference sources for PLL and embedded USB transceiver
- Jumper pin for Headset Mode (Playback + Recording), Microphone Mode (Stereo and Mono Recording), or Speaker/Headphone Mode (Playback Only)
- Jumper pin for Mixer Unit enable/disable under Headset Mod, and Power Mode setting
- I2C interface to access internal registers, and I2S Output for external DAC
- In Headset Mode, USB audio function topology has 2 Input Terminals, 2 Output Terminals, 1 Mixer Unit, 1 Selector Unit, and 3 Feature Units
- In Speaker Mode, USB audio function topology has 1 Input Terminal, 1 Output Terminal, and 1 Feature Unit.
- In Microphone Mode, USB audio function topology has 1 Input Terminal, 1 Output Terminal, 1 Selector Unit and 1 Feature Unit.
- Anti-pop noise design for plug and unplug.

### BLOCK DIAGRAM



**RELEASE NOTES**

Revision	Date	Description
1.00	23 May 2014	- First release

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## 1. Ordering Information

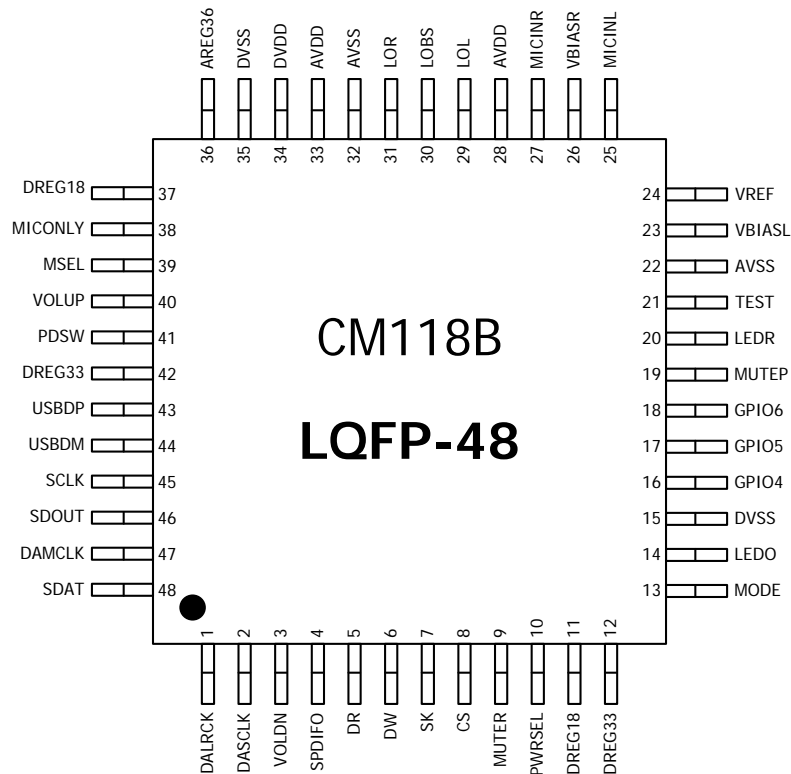
Product	Package Marking	Package Type	Transport Media	Storage Temperature
CM118B	CM118B	LQFP-48 (7 x 7mm) Green Package	Tray	-45 to 120°C

## 2. Pin Descriptions

### 2.1 Pin Assignment by Pin Number

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	DALRCK	13	MODE	25	MICINL	37	DREG18
2	DASCLK	14	LEDO	26	VBIASR	38	MICONLY
3	VOLDN	15	DVSS	27	MICINR	39	MSEL
4	SPDIFO	16	GPIO4	28	AVDD	40	VOLUP
5	DW	17	GPIO5	29	LOL	41	PDSW
6	DR	18	GPIO6	30	LOBS	42	DREG33
7	SK	19	MUTEP	31	LOR	43	USBDP
8	CS	20	LEDR	32	AVSS	44	USBDM
9	MUTER	21	TEST	33	AVDD	45	SCLK
10	PWRSEL	22	AVSS	34	DVDD	46	SDOUT
11	DREG18	23	VBIASL	35	DVSS	47	DAMCLK
12	DREG33	24	VREF	36	AREG36	48	SDAT

### 2.2 Pin-Out Diagram



### 2.3 Pin Signal Descriptions

Pin #	Symbol	Type	Description
1	DALRCK	DO, 2mA, SR	DAC I2S left/right clock
2	DASCLK	DO, 2mA, SR	DAC I2S serial clock
3	VOLDN	DI, ST, PU	Volume down (edge trigger with de-bouncing)
4	SPDIFO	DO, 4mA, SR	SPDIF Output
5	DR	DI, 8mA, PD, 5VT	EEPROM interface data read from EEPROM
6	DW	DO, 4mA, SR	EEPROM interface data write to EEPROM
7	SK	DO, 4mA, SR	EEPROM Interface Clock (100KHz)
8	CS	DO, 4mA, SR	EEPROM Interface Chip Select
9	MUTER	DI, ST, PU	Mute Recording (Edge Trigger with de-Bouncing)
10	PWRSEL	DI, ST, PU	H: Pull Up to 3.3V; L: Pull Down to Ground Speaker Mode H : Self Power with 100mA ; L : Bus Power with 500mA Headset Mode H : Bus Power with 100mA ; L : Bus Power with 500mA
11	DREG18	P	1.8V Regulator Output for Digital Core
12	DREG33	P	3.3V Regulator Output for Digital I/O
13	MODE	DI, ST, PD	H: Pull Up to 3.3V; L: Pull Down to Ground When MICONLY:H MODE L : Headset Mode: Playback & Recording H : Speaker Mode: Playback Only When MICONLY:L MODE L : Stereo MIC Mode: Stereo Recording H : Mono MIC Mode: Mono Recording
14	LEDO	DO, SR, 4mA	LED for Operation; Output H for Power On; Toggling for Data Transmit
15	DVSS	P	Digital Ground
16	GPIO4	DIO, 8mA, PD, 5VT	GPIO Pin
17	GPIO5	DIO, 8mA, PD, 5VT	GPIO Pin
18	GPIO6	DIO, 8mA, PD, 5VT	GPIO Pin
19	MUTEPL	DI, ST, PU	Mute Playback (Edge Trigger with de-Bouncing)
20	LEDR	DO, SR, 4mA	LED for Mute Recording Indicator; Output H when Recording is Muted
21	TEST	DI, ST, PD	Test Mode Select Pin; Pull Low for Normal Operation
22	AVSS	P	Analog Ground
23	VBIASL	AO	Microphone Bias Voltage Supply for Left Channel (3V)
24	VREF	AO	Connecting to External Decoupling Capacitor for Embedded Bandgap Circuit; 1.75V Output
25	MICINL	AI	Microphone Input for Left Channel
26	VBIASR	AO	Microphone Bias Voltage Supply for Right Channel (3V)
27	MICINR	AI	Microphone Input for Right Channel
28	AVDD	P	5V Analog Power for Analog Circuit
29	LOL	AO	Line Out Left Channel
30	LOBS	AO	DC 1.75V Output for Line Out Bias
31	LOR	AO	Line Out Right Channel
32	AVSS	P	Analog Ground
33	AVDD	P	5V Analog Power for Analog Circuit
34	DVDD	P	5V Power Supply to Internal Regulator
35	DVSS	P	Digital Grounding
36	AREG36	P	3.6V analog power for analog circuit

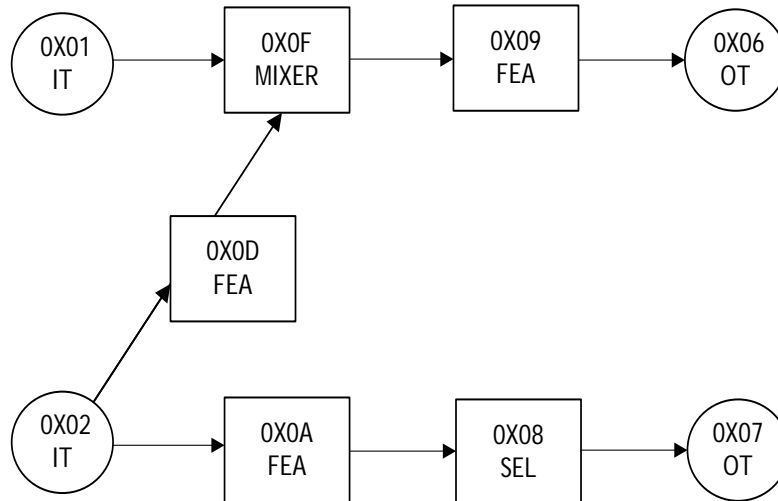
37	DREG18	P	1.8V Regulator Output for Digital Core
38	MICONLY	DI, ST, PU	Microphone only and Headset Topology Selection H: Pull Up to 3.3V; L: Pull Down to Ground MICONLY H: Headset or Speaker Topology L: Microphone Only Topology
39	MSEL	DI, ST, PU	Mixer Enable/Disable or Selector On/Off Pin H: Pull Up to 3.3V, L: Pull Down to Ground When MICONLY: H MSEL L: Without AA Mixer H: With AA Mixer (Default Mute) When MICONLY: L MSEL L: Selector is off H: Selector is on Descriptors are changed accordingly
40	VOLUP	DI, ST, PU	Volume Up (Edge Trigger with de-Bouncing)
41	PDSW	DO, 4mA, OD	Power Down Switch Control (for PMOS Polarity) 0: Normal Mode, 1: Power Down Mode
42	DREG33	P	3.3V Regulator Output for Digital I/O
43	USBDP	AIO	USB Data D+
44	USBDM	AIO	USB Data D-
45	SCLK	DI, ST, PD, 5VT	External MCU Serial Bus Clock Pin for I2C
46	SDOUT	DO, 2mA, SR	DAC I2S data output
47	DAMCLK	DO, 2mA, SR	DAC MCLK 11.2896 MHz output for 44.1KHz sampled data and 12.288 MHz output for 48KHz sampled data
48	SDAT	DIO, 8mA, PD, 5VT	External MCU Serial Bus Data Pin for I2C

Note: DI / DO / DIO - Digital Input / Output / Bi-Directional Pin, AI / AO / AIO - Analog Input / Output / Bi-Directional Pin, SR - Slew Rate Control, ST - Schmitt Trigger, PD / PU - Pull Down / Pull Up, 5VT - 5 Volt Tolerant (3.3V Pin), OD - Open Drain, P - Power Supply Pin

### 3. USB Topology

The CM118B supports USB Headset / USB Speaker / USB Microphone topology that can be selected by pins. Detail setting please refer to chapter 6.4 - Jumper Pins and Mode Setting

#### 3.1 Headset Topology with Mixer



#### Device Descriptor

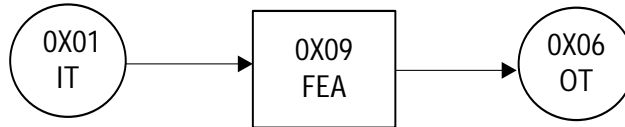
Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Total 18 Bytes
1	bDescriptorType	1	01	Device descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	8	Endpoint zero Size = 8 bytes
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	0016	Product ID
12	bcdDevice	2	0100	Device compliant to the Audio Device Class specification version 1.00
14	iManufacturer	1	01	Index of string descriptor that characterizes the manufacturer
15	iProduct	1	02	Index of string descriptor that characterizes the product
16	iSerialNumber	1	00	Index of string descriptor that characterizes the device's serial number
17	bNumConfigurations	1	01	Configurations number = 1

#### Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Total 9 Bytes
1	bDescriptorType	1	02	Configuration descriptor
2	wTotalLength	2	XXXX	Total length of data returned for this configuration: Programmable by MSEL and MODE pin
4	bNumInterfaces	1	04	Number of interfaces supported by this configuration: 0: control interface      1: ISO-OUT interface

				2: ISO-IN interface      3: INT-IN(HID) interface
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor that characterizes this configuration
7	bmAttributes	1	80	Bus Power and support Remote Wakeup
8	bMaxPower	2	32	Maximum power consumption of the USB Device: 100mA

### 3.2 Speaker Topology



#### Device Descriptor

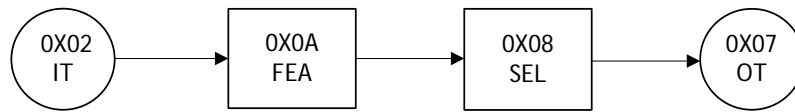
Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	08	Endpoint zero packet size
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	0016	Product ID
12	bcdDevice	2	0100	Device release number
14	iManufacturer	1	01	Index of string descriptor that characterizes the manufacturer
15	iProduct	1	02	Index of string descriptor that characterizes the product
16	iSerialNumber	1	00	Index of string descriptor that characterizes the serial number
17	bNumConfigurations	1	01	Number of configuration

#### Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration descriptor
2	wTotalLength	2	008A	Total length of data returned for this configuration
4	bNumInterfaces	1	03	Number of interfaces supported by this Configuration: 00: Control 01: ISO-Out 02: INT-IN (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor that characterizes this configuration
7	bmAttributes	1	80	Attributes(PWRSEL=0:Bus Powered, 1:SELF Powered)
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA



### 3.3 Microphone Topology



#### Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	08	Endpoint zero packet size
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	0016	Product ID
12	bcdDevice	2	0100	Device release number
14	iManufacturer	1	01	Index of string descriptor that characterizes the manufacturer
15	iProduct	1	02	Index of string descriptor that characterizes the product
16	iSerialNumber	1	00	Index of string descriptor that characterizes the serial number
17	bNumConfigurations	1	01	Number of configuration

#### Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration descriptor
2	wTotalLength	2	xxxx	Total length of data returned for this configuration
4	bNumInterfaces	1	03	Number of interfaces supported by this Configuration: 00: Control 01: ISO-IN 02: INT-IN (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor that characterizes this configuration
7	bmAttributes	1	80	Attributes(PWRSEL=0:Bus Powered, 1:SELF Powered)
8	bMaxPower	1	32	Maximum power consumption from bus = 100mA

## 4. Function Description

### 4.1 Content Format for EEPROM (93C46)

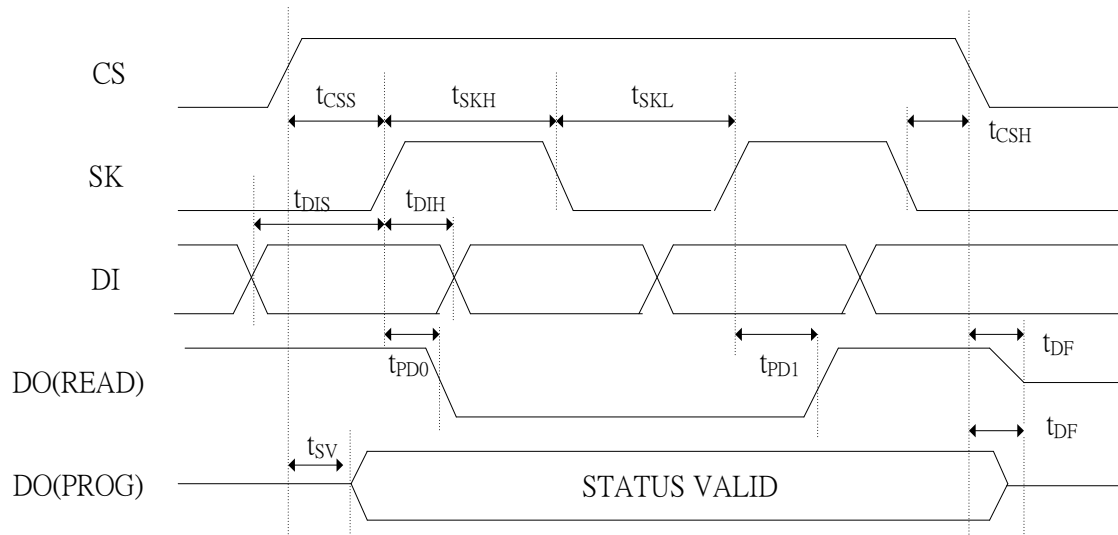
The CM118B integrates USB transceiver, internal oscillator and regulator so that only several passive components are necessary for the USB interface connection. Default USB descriptors are embedded in the CM118B; therefore there is no additional design effort needed for a generic USB operation. For customized product, customer can attach a SPI interface 93C46 EEPROM to override the embedded VID, PID and initial/max/min volume settings. The CM118B automatically detects 93C46 existence and performs the overwrite function during power up.

Each address has 2-byte data, prefix `0x` means hex number

Address (Hex)	Description	
0x00	bit[15:4] Magic Word -- 0x670X where X = bit 4, 3, 2, 1 bit[3] The value within address 0x2A, 0x2B, 0x32 is valid 1: valid 0: invalid bit[2] reserved, should be 1 bit[1] serial number enable control 1: enable, 0: disable(default) bit[0] reserved, should be 1	
0x01	VID 2-byte	
0x02	PID 2-byte	
0x03	Serial number 1st byte (bit15-bit8, first character)	Serial number length (bit7-bit0)
0x04 ~ 0x09	Serial number 12-byte	
0x0A	Product string 1st byte (bit15-bit8, first character)	Product string length (bit7-bit0) [0x3E->30,0x40->31Char]
0x0B ~ 0x19	Product string 30-byte (default: USB Audio Device)	
0x1A	Manufacturer string 1st byte (bit15-bit8, first character)	Manufacturer string length (bit7-bit0) [0x3E->30,0x40->31Char]
0x1B ~ 0x29	Manufacturer string 30-byte (default: C-Media Electronics Inc.)	
0x2A	bit[15: 9] DAC initial volume (7-bit, default = -10dB) bit[8: 3] ADC initial volume (6-bit, default = 8dB) bit[2] DAC EEPROM MAX/MIN volume valid bit[1] ADC EEPROM MAX/MIN volume valid bit[0] AA EEPROM MAX/MIN volume valid	
0x2B	bit[15:11] AA initial volume (5-bit, default = -7dB) bit[10] Reserved, should be 0 bit[9] Boost mode 0: 22dB 1:12dB (default) bit[8] Reserved, should be 0 bit[7] Total Power Control 1:enable, 0:disable(default) bit[6] Reserved, should be 0 bit[5] MIC High Pass Filter 1:enable(default), 0:disable bit[4] MIC PLL Adjust 1:enable, 0:disable(default) bit[3] MIC BOOST 1:enable (default), 0:disable bit[2] DAC Output Terminal property 1: Headset, 0: Speaker(default) bit[1] HID, 1: enable (default), 0: disable bit[0] Remote wakeup, 1:enable, 0:disable(default)	
0x2C	bit[15:0] DAC Minimum Volume (0xD300, DAC-Min.=-45dB, default=-37dB)	
0x2D	bit[15:0] DAC Maximum Volume (0x0000, DAC-Max.=0dB, default=0dB)	
0x2E	bit[15:0] ADC Minimum Volume(0xEA00, ADC-Min.=-22dB, default=-12dB)	
0x2F	bit[15:0] ADC Maximum Volume(0x1700, ADC-Max.=+23dB, default=+23dB)	
0x30	bit[15:0] AA Minimum Volume (0xE900, AA-Min.=-23dB, default=-23dB)	
0x31	bit[15:0] AA Maximum Volume (0x0800,AA-Max.+8dB, default=+8dB)	
0x32	EE_OPTION2 Register bit[3] Reserved, should be 0 bit[2] Reserved, should be 0 bit[1] Reserved, should be 1 bit[0] EE_Stereo, 1: stereo ADC for headset topology, 0: mono ADC for headset	

	topology
~ END	

#### 4.2 EEPROM SPI Interface Timing Information



Symbol	Parameter	Test Condition*	Min	Typ	Max	Units
$f_{SK}$	SK Clock Frequency	$2.7V \leq V_{CC} \leq 5.5V$	0		200	KHz
$t_{SKH}$	SK High Time	$2.7V \leq V_{CC} \leq 5.5V$	250			ns
$t_{SKL}$	SK Low Time	$2.7V \leq V_{CC} \leq 5.5V$	250			ns
$t_{CS}$	Minimum CS Low Time	$2.7V \leq V_{CC} \leq 5.5V$	250			ns
$t_{CSS}$	CS Setup Time	$2.7V \leq V_{CC} \leq 5.5V$	50			ns
$t_{DIS}$	DI Setup Time	$2.7V \leq V_{CC} \leq 5.5V$	100			ns
$t_{CSH}$	CS Hold Time	$2.7V \leq V_{CC} \leq 5.5V$	0			ns
$t_{DIH}$	DI Hold Time	$2.7V \leq V_{CC} \leq 5.5V$	100			ns
$t_{PD1}$	Output Delay to "1"	$2.7V \leq V_{CC} \leq 5.5V$			250	ns
$t_{PD0}$	Output Delay to "0"	$2.7V \leq V_{CC} \leq 5.5V$			250	ns
$t_{SV}$	CS to Status Valid	$2.7V \leq V_{CC} \leq 5.5V$			250	ns
$t_{DF}$	CS to DO in High Impedance	$2.7V \leq V_{CC} \leq 5.5V$			100	ns
$t_{WP}$	Write Cycle Time	$4.5V \leq V_{CC} \leq 5.5V$	0.1	3	10	ms

\* based on ATMEL 93C46 EEPROM data

### 4.3 Jumper Pins and Mode Settings

Jumper pins can be used to set the configuration of CM118B. These jumper pin settings affect both USB descriptors and USB audio topology.

#### 4.3.1 MICONLY Pin / Mode Pin and MSEL Pin

If MICONLY pin is switched to 0 (Microphone mode), the recording only function of CM118B is activated and there's no playback function declared to the host. At this setting, MODE pin selects MONO/STEREO inputs, and MSEL pin selects whether the descriptor will have SELECTOR Unit or not. In other cases, when the MICONLY pin is switched to 1, the device preserved its playback function.

Speaker mode is when MICONLY pin is switched to 1, and MODE pin is also switched to 1, the playback only function of CM118B is activated and there is no recording function declared to the host. At this setting, MSEL pin is ignored while only one input terminal, one output terminal and one feature unit is declared in the USB audio topology. Headset mode is when MICONLY is switched to 1, and MODE pin is switched to 0, the full duplex playback and recording function is declared to the host. The MSEL pin setting decides to activate MIXER Unit or turn it off. EEPROM register EE\_Stereo, 0x32[0] can be used to determined headset mode with stereo ADC (value set to 1) or mono ADC (value set to 0) channels.

Topology	MICONLY	MODE	MSEL	EE_Stereo <sup>1</sup>
<i>Headset</i>				
Headset(Stereo MIC, with Mixer)	1	0	1	1
Headset (Mono Mic, with Mixer)	1	0	1	0
Headset (Stereo Mic, without Mixer)	1	0	0	1
Headset (Mono Mic, without Mixer)	1	0	0	0
<i>Speaker Only</i>				
Speaker	1	1	X	X
<i>Microphone Only</i>				
Mono-Mic (with Selector)	0	1	1	X
Mono-Mic (without Selector)	0	1	0	X
Stereo-Mic (with Selector)	0	0	1	X
Stereo-Mic (without Selector)	0	0	0	X

<sup>1</sup> EE\_Stereo is only configurable with EEPROM, and for IC default value EE\_Stereo is set to 0.

### 4.3.2 Mode Pin and PWRSEL Pin

PWRSEL pin affects the power configuration of CM118B; together with MODE pin there are four combinations that are programmable. As show in the table, only speaker mode can switch to self-power status.

For Speaker and Headset Modes		MODE	
		3.3V (Speaker)	GND (Headset)
PWRSEL	3.3V	Self-Powered with 100mA	Bus Power with 100mA
	GND	Bus Power with 500mA	Bus Power with 500mA

For Microphone Mode		MICONLY	
		3.3V (Microphone)	
PWRSEL	3.3V	Bus Power with 100mA	
	GND	Bus Power with 500mA	

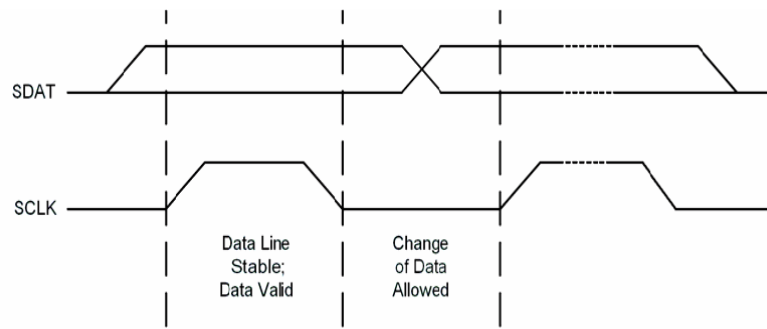
### 4.4 MCU Interface

On MCU serial interface, the CM118B functions as a slave device with bit rate up to 400Kbps (fast mode). MCU can read/write 3 bytes to the CM118B device with a 2-bit register address. Since host side and MCU can both access all of the internal registers, access contention should be avoided on application when both try to access the same register. The 7-bit slave address of the CM118B is assigned as 7'b0111000.

When a one-byte data is written by MCU, the CM118B will transfer totally 4 bytes to the USB host via an additional interrupt pipe. The sequence of the upward HID report is given by: the button status first (address00); then register with address01; followed by register with address02; lastly, register with address03. The USB host will keep polling the upward HID report every 2mS. When there is any button pressed or released, or MCU data coming, the CM118B will transfer the 4 bytes of HID report to the USB host again.

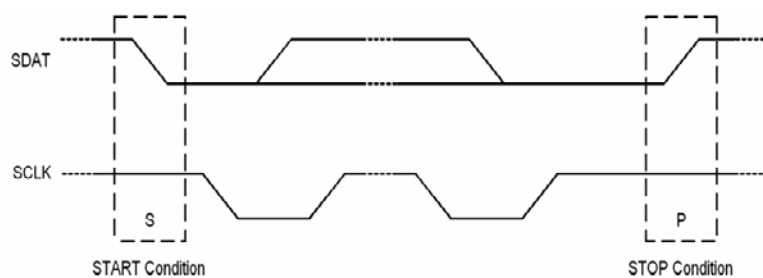
The CM118B can also transfer one byte MCU data from the USB host to its register. This is accomplished by a 'Set Output Report' HID class request via default control pipe. MCU can get this downward byte by polling.

The CM118B has one input pin 'SCLK' where it gets serial clock from MCU, and one open-drain output pin 'SDAT' where it sends or receives serial signal to or from MCU. As shown below, 'SDAT' should best able when 'SCLK' is high, and can only have transition when 'SCLK' is low.



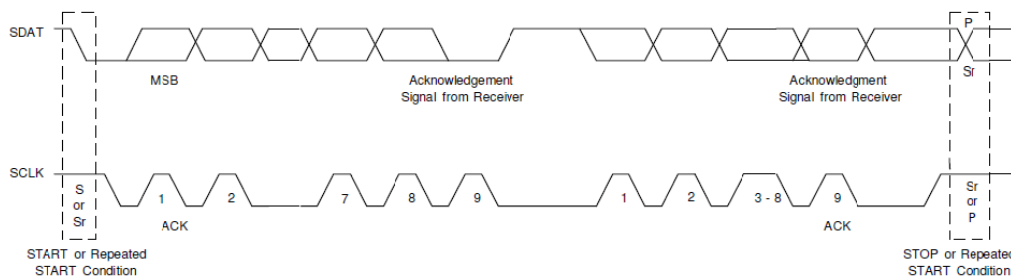
Bit Transfer on the MCU Interface

START and STOP conditions shown below are the exception. Every transaction begins from a START and ends with a STOP or another START (repeated START).



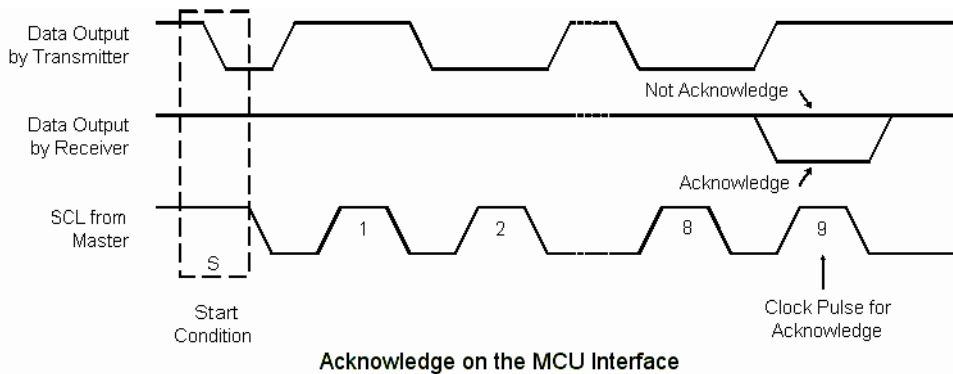
START and STOP Conditions

The figure below demonstrates a typical transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more detailed display about acknowledgement bit. Note that 'SCLK' is always driven by the master.

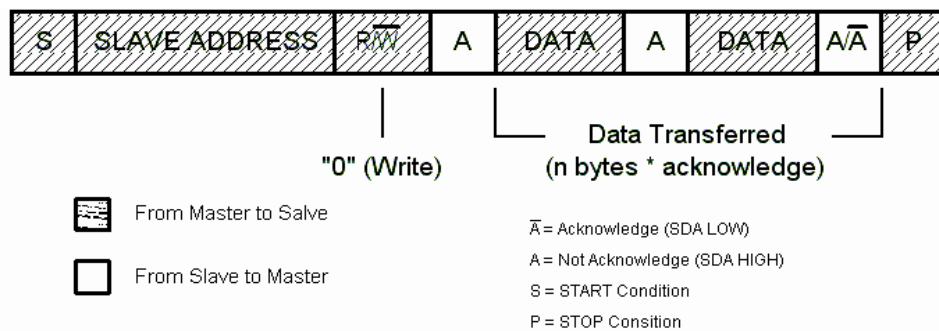


Data Transfer on the MCU Interface

The figure below shows a complete data transfer. After a START, MCU should send 7-bit slave address (7'b0111000) first and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low. The first acknowledgement is always from the CM118B.



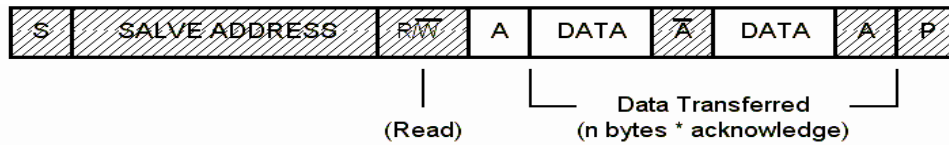
In the write transfer, MCU keeps acting as the master and the transfer direction is not changed. The following figure gives an example of one byte write transfer.



**A Master-Transmitter Addressing a Slave Receiver with a 7-bit Address.  
The Transfer Direction is not Changed.**

The CM118B regards the first DATA byte as the register address. The second DATA byte is the content that MCU writes at the register address. If there is the third DATA byte, the CM118B will auto-increment this byte to the next register address.

The figure below shows an example of two bytes read transfer. Because the CM118B has auto-increment function, the second DATA byte will be the register data on the next address.



A Master reads a Salve immediately after the first Byte

Note: The USB host tries to get new HID data every 2mS. It's quite slow. If the continuous write transfers are too close in terms of time, the former transfer may have no effect.

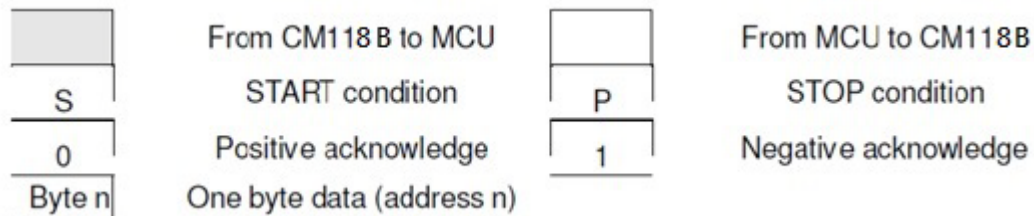
The figure below shows typical transactions between MCU and t h e CM118B. After a START, MCU should send 7-bit slave address (0111000) first and then the 8<sup>th</sup> bit denotes a read transfer when it's high; or a write transfer when it's low.

MCU write:

S	0x70	0	0x00	0	Byte 0	0	Byte 1	0	Byte 2	0	Byte 3	0	P
---	------	---	------	---	--------	---	--------	---	--------	---	--------	---	---

MCU read:

S	0x70	0	0x04	0								
S	0x71	0	Byte 0	0	Byte 1	0	Byte 2	0	Byte 3	1	P	



In a write transfer, MCU keeps acting as the transmitter. The CM118B regards the first DATA byte as the start register address (it's better to be 0x00). The next four DATA bytes are the contents that MCU writes to the register addresses. In a read transfer, two transactions are necessary. MCU resets start register address by the first transaction. Then MCU changes in order to be the receiver during the second transaction to get four bytes of data.

Note: Bits 0-3 of the first HID byte always reflect the button activity, so they cannot be written by MCU.



#### 4.5 HID Feature and Descriptor

HID feature is provided by CM118B, so user settings (volume up / volume down / playback mute button) were all reported to the host to synchronize host side setting. In addition, CM118B internal registers can be accessed via HID function call.

USB protocols can configure devices at start up or when they are plugged in at run time. These devices are broken down into various device classes. Each device class defines the common behavior and protocols for devices that has similar functions. The HID (Human Interface Device) class is one of the device classes.

The HID class consists primarily of devices that are used by humans to control the operation of computer systems. Typical examples of HID class devices include keyboards and pointing devices (i.e. mouse, trackballs, and joysticks)

##### HID Interface Descriptor

Offset	Field	Size	Value(Hex)	Description
0	bLength	1	09	Sizeofthisdescriptor:9byte
1	bDescriptorType	1	04	INTERFACE descriptor type
2	bInterfaceNumber	1	03	Number of interface: 3
3	bAlternateSetting	1	00	Alternate 0
4	bNumEndpoints	1	01	Number of endpoints used by this interface:1
5	bInterfaceClass	1	03	HID Interface Class
6	bInterfaceSubClass	1	00	No Subclass
7	bInterfaceProtocol	1	00	Must be set to 0
8	iInterface	1	00	Index of a string descriptor that describes this interface

##### HID Descriptor

Offset	Field	Size	Value(Hex)	Description
0	bLength	1	09	Total 9 bytes
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version 1.00
4	bCountryCode	1	00	-
5	bNumDescriptors	1	01	-
6	bDescriptorType	1	22	Report descriptor
7	wDescriptorLength	2	003C	Numeric expression equal to the total size of the optional descriptor: 60 Bytes

**Interrupt in Endpoint Descriptor**

Offset	Field	Size	Value(Hex)	Description
0	bLength	1	07	Total 7 bytes
1	bDescriptorType	1	05	ENDPOINT descriptor type
2	bEndpointAddress	1	87	IN Endpoint Endpoint number=3
3	bmAttributes	1	03	Interrupt endpoint type
4	wMaxPacketSize	2	0004	Maximum packet size: 4 bytes
6	bInterval	1	2	2ms

## 4.6 Internal Registers

All internal registers of the CM118B can be accessed via generic HID functional calls without the need to develop kernel mode driver. Total of 4bytes of data can be read or write from HID. Input report is for read while output report is for write. Internal registers of the CM118B are used to control GPIO, S/PDIF output, EEPROM and MCU data access. Host side HID or external MCU can access the CM118B internal registers. With both sides accessed to the same set of registers, two-way communication can be achieved.

### 4.6.1 Access via HID Class Command

HID interrupt will occur when HID\_IR0-3 are updated by button status, or updated by MCU (and GPI in case HID\_IR0[7:6] == 2'b00).

#### HID Get\_Input\_Report Format

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h A1	8'h 01 (Get_Report)	16'h 01 00 (Rpt Type + Rpt ID)	16'h 00 02 16'h 00 03 (Interface)	16'h 00 04 (4 bytes)	Report

Input Data Format:

byte 0	HID IR0[7:0]
byte1	HID IR1[7:0]
byte2	HID IR2[7:0]
byte3	HID IR3[7:0]

## HID Set\_Output\_Report Format

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 21	8'h 09 (Set_Report)	16'h 02 00 (Rpt Type + Rpt ID)	16'h 00 02 16'h 00 03 (Interface)	16'h 00 04 (4 bytes)	Report

Output Data Format:

byte 0	HID OR0[7:0]
byte1	HID OR1[7:0]
byte2	HID OR2[7:0]
byte3	HID OR3[7:0]

### 4.6.2 Register Definitions

Offset 0x00--HID\_IR0 (HID input report byte 0)

Bits	Read/Write	Description	Default
7-6	R	When HID_OR0[7] == 1'b0: HID_IR0-3 are programmed by MCU (and GPI) 0: HID_IR1 is used as GPI 1: HID_IR0-3 are used as generic HID registers 2: Values written to HID_IR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1, EEPROM_CTRL 3: Reserved When HID_OR0[7] == 1'b1: Always 2'b11	0x0
5	R	When HID_OR0[7] == 1'b0: Generic registers programmed by MCU When HID_OR0[7] == 1'b1: Mapped from MCU_CTRL[5]	0x0
4	R	Reserved	0x0
3	R	0: No activity on Record-Mute button 1: Record-Mute button pressed then released	0x0
2	R	0: No activity on Playback-Mute button 1: Playback-Mute button pressed then released	0x0
1	R	0: Volume-Down button released 1: Volume-Down button pressed	0x0
0	R	0: Volume-Up button released 1: Volume-Up button pressed	0x0

Offset 0x01--HID\_IR1 (HID input report byte 1)

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7] == 1'b0: GPI (when HID_IR0[7:6] == 2'b00); or Generic registers programmed by MCU (otherwise) When HID_OR0[7] == 1'b1: Mapped from EEPROM_DATA0	0x00

## Offset 0x02--HID\_IR2 (HID input report byte 2)

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7] == 1'b0: Generic registers programmed by MCU When HID_OR0[7] == 1'b10: Mapped from EEPROM_DATA1 When HID_OR0[7:6] == 2'b11: Mapped to ANA_REG1( {2'b11, ANA_REG1[5:0]} )	0x00

## Offset 0x03--HID\_IR3 (HID input report byte 3)

Bits	Read/Write	Description	Default
7-0	R	When HID_OR0[7] == 1'b0: Generic registers programmed by MCU When HID_OR0[7] == 1'b10: Mapped from EEPROM_CTRL When HID_OR0[7:6] == 2'b11: Mapped to ANA_REG2( {1'b0, ANA_REG2[6:0]} )	0x00

## Offset 0x04--HID\_OR0 (HID output report byte 0) (When HID\_OR0[7:6] != 2'b11)

Bits	Read/Write	Description	Default
7-6	R/W	0x00: HID_OR1-2 are used for GPO; HID_OR0, 3 are used for SPDIF 0x01: HID_OR0-3 are used as generic HID registers 0x10: Values written to HID_OR0-3 are also mapped to MCU_CTRL, EEPROM_DATA0-1, EEPROM_CTRL (see Note) 0x11: HID_OR0 Mapped to Analog Option Reg1 (ANA_REG1[5:0])	0x0
5	R/W	Reserved	0x0
4	R/W	When HID_OR0[7] == 1'b0: Valid bit in SPDIF frame When HID_OR0[7] == 1'b1: Mapped to MCU_CTRL[4] When HID_OR0[7:6] == 2'b11 Mapped to T_IAD_[0]	0x0
3-0	R/W	When HID_OR0[7] == 1'b0: First nibble of SPDIF status channel When HID_OR0[7:6] == 2'b11: [3:1] Mapped to [TIADBUF_, T_IREF_, T_MOD_]	0x0

Note 1: When EEPROM access is done, HID interrupt will occur. USB host will get the result from interrupt pipe

Note 2: HID\_OR0 is used for SPDIF when SPDIF\_CONFIG[5] == 1'b0

## Offset 0x05--HID\_OR1 (HID output report byte 1)

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7:6] == 2'b00: 0: GPO drives L 1: GPO drives H When HID_OR0[7:6] == 2'b01: Generic HID registers When HID_OR0[7:6] == 2'b10: Mapped to EEPROM_DATA0 When HID_OR0[7:6] == 2'b11: Mapped to Power Down Control Register	0x00

## Offset 0x06--HID\_OR2 (HID output report byte 2)

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7:6] == 2'b00: 0: Set GPIO to input mode 1: Set GPIO to output mode When HID_OR0[7:6] == 2'b01: Generic HID registers When HID_OR0[7:6] == 2'b10: Mapped to EEPROM_DATA1 When HID_OR0[7:6] == 2'b11: Mapped to ADC_CTRL2 Control Register	0x00

## Offset 0x07--HID\_OR3 (HID output report byte 3)

Bits	Read/Write	Description	Default
7-0	R/W	When HID_OR0[7:6] == 2'b00: Category byte of SPDIF status channel When HID_OR0[7:6] == 2'b10: Mapped to EEPROM_CTRL When HID_OR0[7:6] == 2'b11 Mapped to Analog Option Reg2(ANA_REG2[6:0] ( [6:4] Mapped to TP_INAD_[2:0]; [3:0] Mapped to B_PLL[3:0] )	0x00

Note: HID\_OR3 is used for SPDIF when SPDIF\_CONFIG[5] == 1'b0

## 5. Electrical Characteristics

### 5.1 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Dvmin	Min Digital Supply Voltage	- 0.3	V
Dvmax	Max Digital Supply Voltage	+ 6	V
Avmin	Min Analog Supply Voltage	- 0.3	V
Avmax	Max Analog Supply Voltage	+ 6	V
Dvinout	Voltage on any Digital Input or Output Pin	-0.3 to +5.5	V
Avinout	Voltage on any Analog Input or Output Pin	-0.3 to +3.96	V
TBstgB	Storage Temperature Range	-40 to +125	° C
ESD (HBM)	ESD Human Body Mode	+-4000	V
ESD (MM)	ESD Machine Mode	+-200	V
Latch Up	JEDEC Standard No.78, Mar 1997	200	mA

### 5.2 DC Specifications

Symbol	Parameter	Condition	Min*	Max*	Units
V <sub>IL</sub>	Input Low Voltage		-0.3	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	5.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = -2, -4, -8 mA	0.0	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>IH</sub> = 2, 4, 8 mA	2.4	3.6	V

\*For digital IO pins only

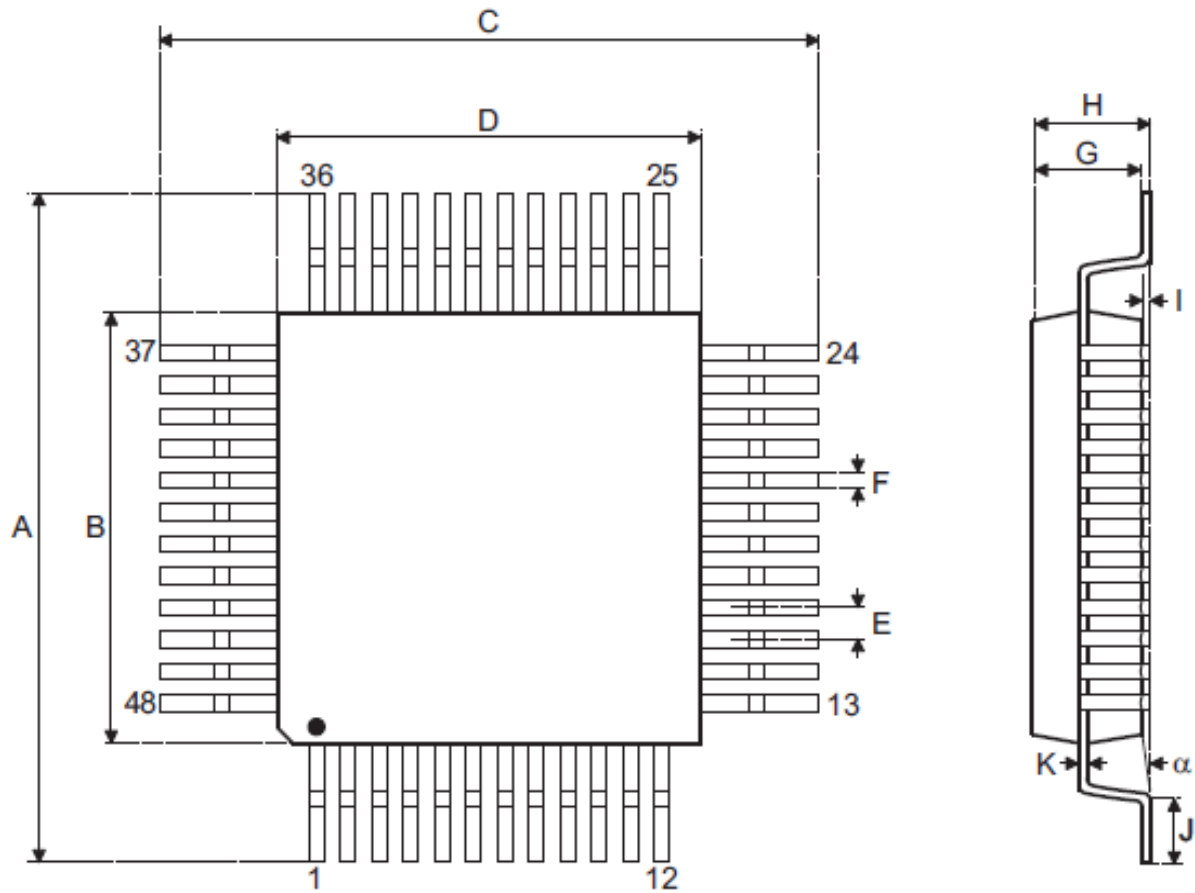
### 5.3 Operation Conditions

Operation conditions				
	Min	Typ	Max	Unit
Analog Supply Voltage	4.5	5.0	5.5	V
Digital Supply Voltage	4.5	5.0	5.5	V
Total Power Consumption*	-	37.25		mA
Suspend Mode Power Consumption	-	1.58		mA
Operating ambient temperature	-15	-	70	° C

\*Test Conditions: AVDD = 5V, DVDD = 5V, Playback Signal = 1kHz Sine Wave @ full scale, Output Loading = 10kOhm, LEDs are removed, ADC are operating but Inputs are opened.

**5.4 Electrical Parameters**

	Min	Typ	Max	Unit
<b>DAC (10K Ohm Loading)</b>				
Resolution	-	16	-	Bits
THD + N (-3dBr)	-	-72	-	dB
SNR	-	93	-	dB
Silent SNR	-	98	-	dB
Dynamic range	-	92	-	dB
Frequency response 48KHz	20	-	20K	Hz
Frequency Response 44.1KHz	20	-	20K	Hz
Output Voltage (rms)	-	0.995	-	Vrms
<b>DAC (32 Ohm Loading)</b>				
Resolution	-	16	-	Bits
THD + N (-3dBr)	-	-70	-	dB
SNR	-	93	-	dB
Silent SNR	-	98	-	dB
Dynamic range	-	92	-	dB
Frequency response 48KHz	100	-	20K	Hz
Frequency Response 44.1KHz	100	-	20K	Hz
Output Voltage (rms)	-	0.442	-	Vrms
<b>ADC</b>				
Resolution	-	16	-	bit
THD + N (-3dBr)	-	-84	-	dB
SNR	-	90	-	dB
Dynamic Range	-	88.5	-	dB
Frequency Response 48KHz	100	-	20K	Hz
Frequency Response 44.1KHz	100	-	20K	Hz
Input Range	0	-	1.000	Vrms
<b>Amplification</b>				
Volume Control Initial Value		-10		dB
Volume Control Level	-37	-	0	dB
Volume Control Step	-	38	-	Steps
<b>Microphone Input</b>				
Boost Gain	-	12 / 22 (EEPROM)	-	dB
Gain Adjustment Initial Value		8		dB
Gain Adjustment Range	-12	-	23	dB
Gain Adjustment Steps	-	36	-	Steps
Mixer Gain Initial Value		-7		dB
Mixer Gain Adjustment	-23.0	-	8.0	dB
Mixer Gain Adjustment Steps	-	32	-	Steps

**6. Package dimensions**


Symbol	Dimensions in mm		
	Minimum	Normal	Maximum
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
$\alpha$	0°	—	7°



## Reference

- Universal Serial Bus Specification, Version 2.0
- Universal Serial Bus Device Class Definition for Audio Devices, Version 1.0.
- Universal Serial Bus Device Class Definition for Human Interface Devices, Version 1.11

— End of Datasheet —

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