CML Microcircuits
COMMUNICATION SEMICONDUCTORS

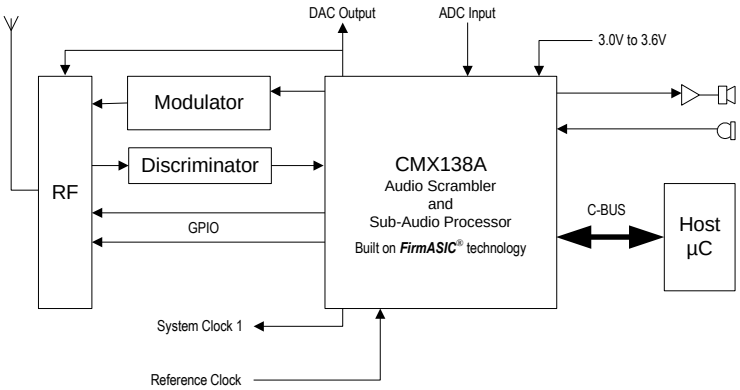
CMX138A
Audio Scrambler and Sub-Audio Signalling Processor

D/138A/4 October 2014

CMX138A: Audio Scrambler and Sub-Audio Signalling Processor with Auxiliary System Clock, ADC and DAC for use in Analogue Radio Systems

Features

- **Programmable Audio Scrambler**
- **Concurrent Audio/Signalling Operations**
- **Full Audio-band Processing: Pre and De-emphasis, Compandor, Scrambler and Selectable 2.55/3 kHz Filters**
- **Auxiliary ADC and Auxiliary DAC**
- **C-BUS Serial Interface to Host µController**
- **Two Analogue Inputs (Mic or Discriminator)**
- **Selectable Audio Processing Order**
- **Sub-audio Signalling: CTCSS, DCS**
- **Auxiliary System Clock Output**
- **Tx Output for Single-point Modulation**
- **Low-power (3.0V to 3.6V) Operation**
- **Flexible Powersave Modes**
- **Available in 28-pin TSSOP Package**



1 Brief Description

The CMX138A is a half-duplex, audio scrambler and sub-audio signalling processor IC for Analogue Two-way Radio applications. This makes it a suitable device for the leisure radio markets (FRS, MURS, PMR446 and GMRS).

This device provides a user programmable frequency inversion audio scrambler, companding and pre/de-emphasis – performing simultaneous processing of Sub-audio and In-band signalling.

Other features include an auxiliary ADC channel and an auxiliary DAC interface (with optional RAMDAC, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in a 28-pin (E1) TSSOP package.

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It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

2 History

Version	Changes	Date
4	• Updated CTCSS detector response times, following product characterisation. Added note 74 about statistical processes.	Oct 2014
3	• Added description of fine attenuation settings to $CD and P4.2, P4.3 • Note that it is possible to alter standard CTCSS settings when in Tx mode, but not custom settings or DCS settings • Update MOD and AUDIO output drive parameters, after characterisation • Correct minor typos and change document status to full issue.	Dec 2012
2	• Enhanced description of C-BUS latency time, just before Fig 4. • Correction to Audio Tone ($CD) register, code 1100_b, section 9.1.19. • Correction to Program Block 4, registers P4.10 and P4.11, section 9.2.5.	Nov 2010
1	• First Issue of CMX138A	Jun 2010

3 Block Diagram

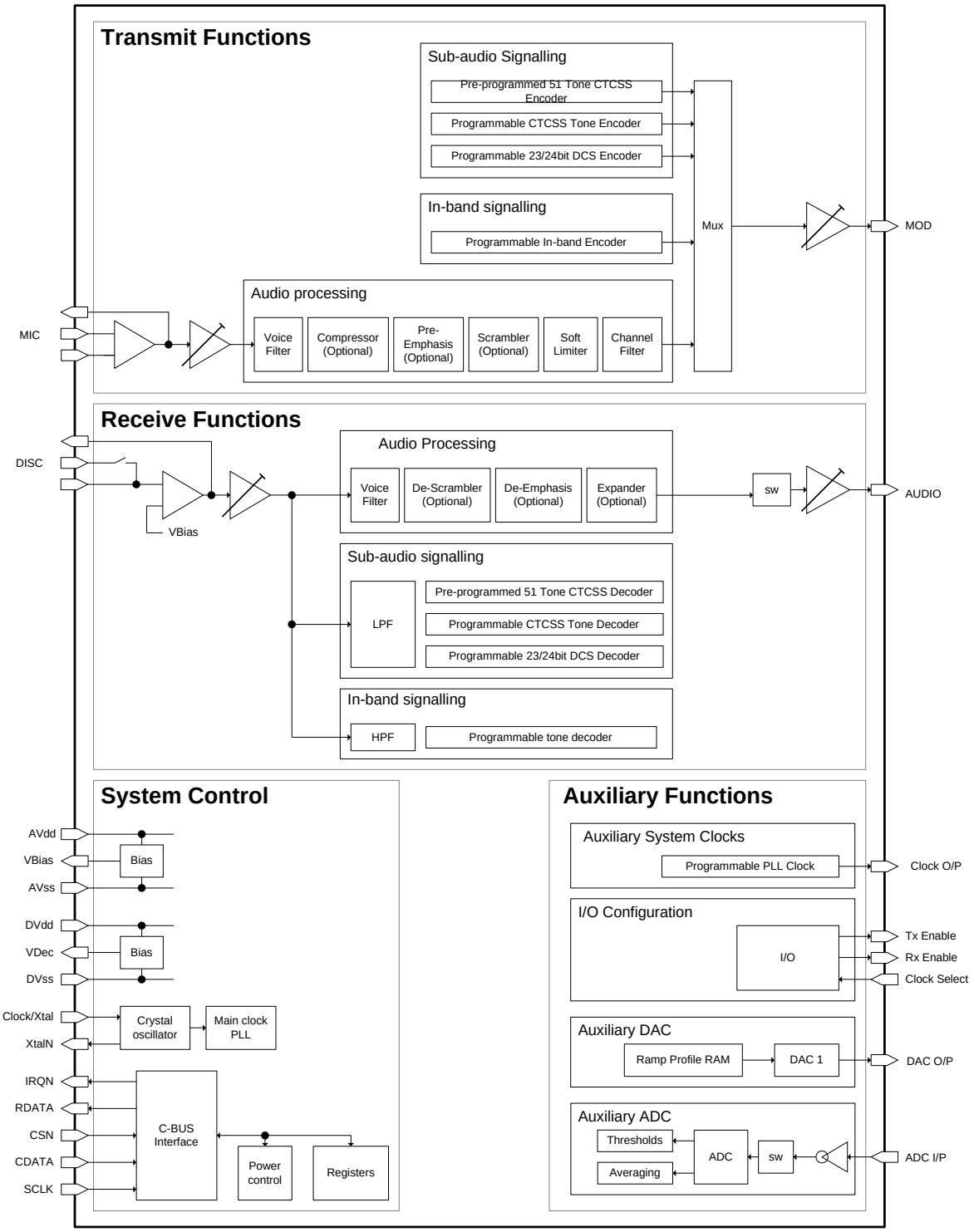


Figure 1 Block Diagram

4 Signal List

CMX138A	Signal Name	Type	Description
1	TXENA	OP	Digital output pin – TxENA (active low).
2	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DVSS by capacitors mounted close to the device pins. No other connections allowed.
3	SYSCLK	OP	Synthesised digital system clock output.
4	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DVSS when active and is high impedance when inactive. An external pull-up resistor is required.
5	RDATA	TS OP	C-BUS: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
6	SCLK	IP	C-BUS: The C-BUS serial clock input from the µC.
7	CDATA	IP	C-BUS: Serial data input from the µC.
8	CSN	IP	C-BUS: The C-BUS chip select input from the µC - there is no internal pull-up on this input.
9	DVDD	PWR	The 3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the device pins.
10	XTAL/CLOCK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source.
11	XTALN	OP	The output of the on-chip Xtal oscillator inverter.
12	DVSS	PWR	Digital ground.
13	MOD	OP	Modulator output.
14	MICFB	OP	MIC input amplifier feedback.
15	MICN	IP	MIC inverting input.
16	MICP	IP	MIC non-inverting input.
17	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
18	AUXADC	IP	Auxiliary ADC input (inverted).
19	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when VBIAS pin will discharge to AV_{SS}. Must be decoupled to AVSS by a capacitor mounted close to the device pins. No other connections allowed.
20	DISCN2	IP	DISC inverting input 2.
21	DISCN1	IP	DISC inverting input 1.
22	DISCFB	OP	DISC input amplifier feedback.
23	AUDIO	OP	Audio output.
24	AVSS	PWR	Analogue ground.
25	AUXDAC	OP	Auxiliary DAC output/RAMDAC.
26	DVSS	PWR	Digital ground.

CMX138A	Signal Name	Type	Description
27	CLKSEL	IP+PU	Clock speed select (hi = 6.144MHz, lo = 3.6864MHz).
28	RXENA	OP	Digital output pin – RxENA (active lo).

Notes: IP = Input (+ PU/PD = internal pullup/pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

4.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

5 External Components

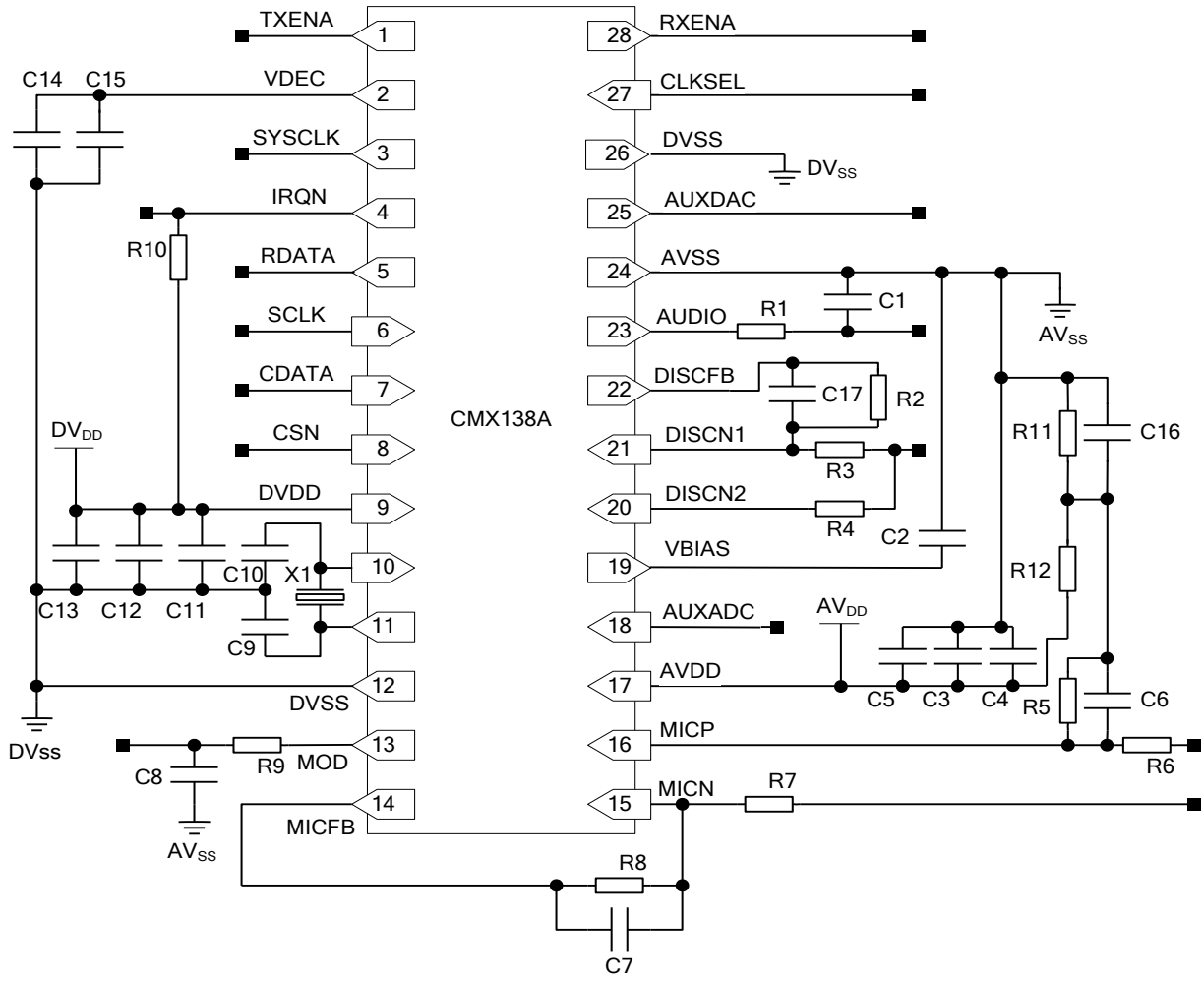


Figure 2 CMX138A Recommended External Components

R1	See note 3	R8	100kΩ	C1	See note 3	C9	39pF
R2	100kΩ	R9	See note 3	C2	100nF	C10	39pF
R3	100kΩ	R10	10kΩ	C3	10µF	C11	10µF
R4	100kΩ	R11	10kΩ	C4	10nF	C12	10nF
R5	100kΩ	R12	10kΩ	C5	10nF	C13	10nF
R6	100kΩ			C6	100pF	C14	10µF
R7	100kΩ			C7	100pF	C15	10nF
				C8	See note 3	C16	100nF
X1	6.144MHz See note 1					C17	100pF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1 X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance.

2 R2 and R3 should be selected to provide the desired dc gain of the discriminator input, as follows:

$$|GAIN_{DISC}| = R2 / R3$$

The gain should be such that the resultant output at the DISCFB pin is within the discriminator input signal range specified in 7.11.2. If the DISCN2 pin is selected the gain becomes:

$$|GAIN_{DISC}| = R2 / (R3//R4)$$

(assuming that R3 and R4 are both connected to the same input signal).

3 R5, R6, R7 and R8 should be selected to provide the desired dc gain of the microphone input.

The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 7.11.1. For optimum performance with low signal microphones, an additional external gain stage may be required. C6 and C7 should be chosen to maintain a flat low pass response up to 3kHz.

If a single-ended microphone is used, then R6 should be connected to V_{BIAS} and R5 deleted.

R1 and C1 should be chosen to maintain a flat low pass response up to 3kHz.

R9 and C8 should be chosen to maintain a flat low pass response up to 3kHz.

4 If the DISC input is ac coupled, the selection of the coupling capacitor should allow for frequencies from below 50Hz and up to 3kHz to be passed without significant distortion to allow both Audio and sub-audio decoders to function within their specification.

5 If the MIC input is dc coupled, the selection of the coupling capacitor should allow for frequencies from 300Hz and up to 3kHz to be passed without significant distortion to allow the audio filtering and processing to function within their specification.

5.1 PCB Layout Guidelines and Power Supply Decoupling

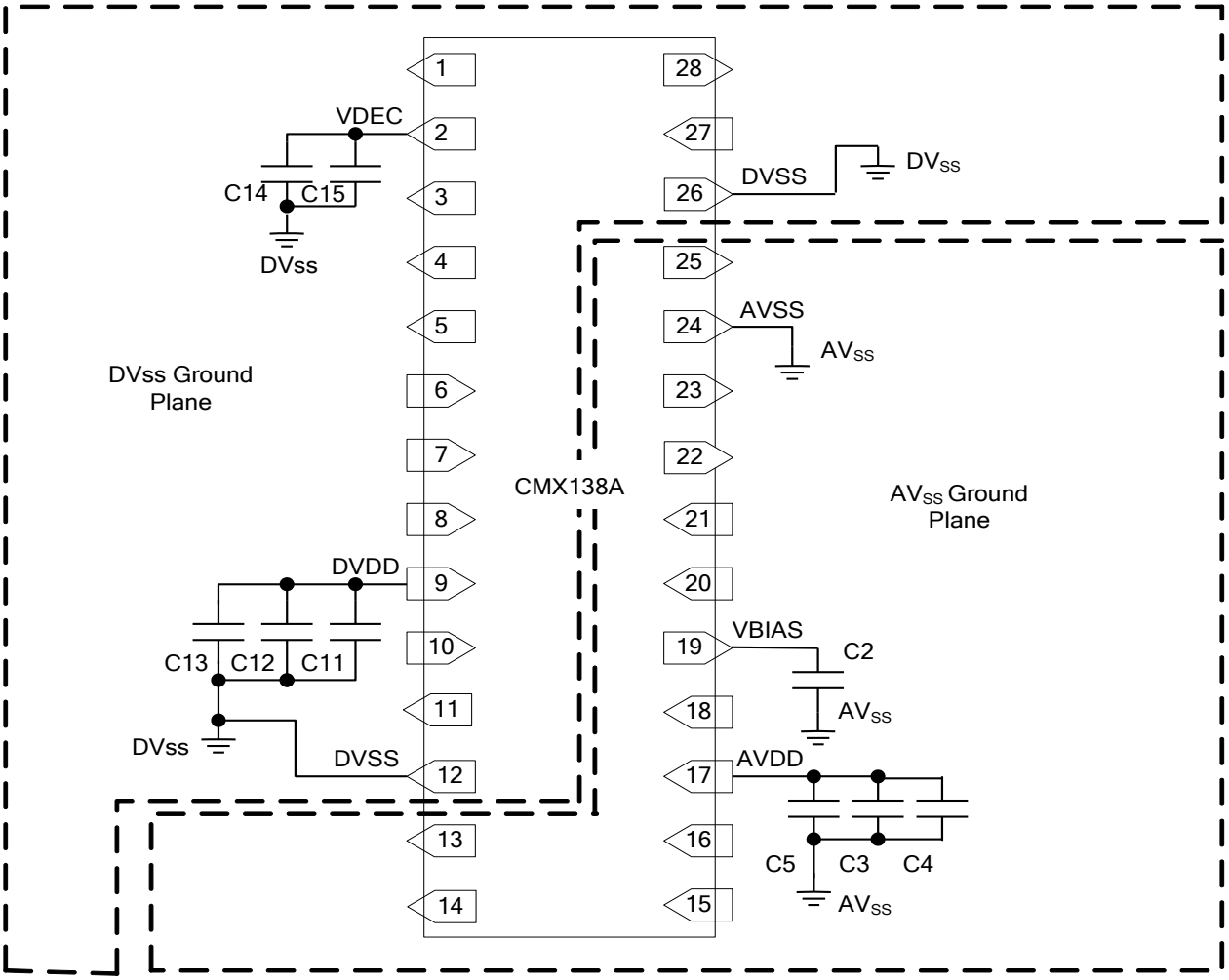


Figure 3 CMX138A Power Supply Connections and De-coupling

Notes:

1. It is important to protect the analogue pins from extraneous in-band noise and to minimise the impedance between the device and the supply and bias de-coupling capacitors. The de-coupling capacitors should be as close as possible to the device. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS}, and DV_{SS} supplies in the area of the CMX138A, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

2. V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input-impedance buffer.

6 General Description

The CMX138A is intended for use in half duplex analogue two way mobile radio or family radio equipment and is particularly suited to enhanced MURS/GMRS/FRS designs. The CMX138A provides a user programmable frequency inversion audio scrambler integrated with signal processing functions, CTCSS, DCS and in-band tones, permitting sophisticated levels of tone control and voice processing. A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The CMX138A includes a crystal clock generator, with buffered output, to provide a common system clock if required. A block diagram of the CMX138A is shown in Figure 1.

The signal processing blocks are assigned to particular inputs/outputs. A facility to completely bypass the device is provided (with programmable gain).

Tx functions:

- Single microphone input with input amplifier, programmable gain adjust and AGC
- Filtering selectable for 12.5kHz and 25kHz channels
- Selectable pre-emphasis
- Selectable compression
- Selectable frequency inversion voice scrambling
- Programmable scrambler inversion frequency
- Selectable audio processing order
- Single-point modulation outputs with programmable level adjustment
- Pre-programmed 51-tone CTCSS encoder
- 180 degree CTCSS phase shift generation
- Programmable 23/24-bit DCS encoder
- Programmable In-band Tone generator
- Programmable audio tone generator (for custom audio tones)

Rx functions:

- Demodulator input with input amplifier and programmable gain adjustment
- Audio-band and sub-audio rejection filtering
- Selectable de-emphasis
- Selectable expansion
- Selectable frequency inversion voice de-scrambling
- Programmable scrambler inversion frequency
- Selectable audio processing order
- Software volume control
- 1 from 51 CTCSS decoder + Tone Clone™ mode
- 23/24-bit DCS decoder
- In-band Tone decoder

Auxiliary functions:

- Programmable system clock output
- Auxiliary ADC
- Auxiliary DAC, with built-in programmable RAMDAC
- Selectable default Xtal options, 6.144MHz or 3.6864MHz

Interface:

- C-BUS: 4-wire high speed synchronous serial command/data bus
- Open drain IRQ to host
- Two Output Enable pins

7 Detailed Descriptions

7.1 Xtal Frequency

The CMX138A is designed to work with a Xtal or external frequency source of 6.144MHz or 3.6864MHz (as selected by the state of the CLKSEL pin). If either of these default configurations is not suitable, then Program Register Block 3 should to be loaded with the correct values to ensure that the device will work to specification with the user specified clock frequency. A table of common values can be found in Table 2. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24.576MHz can be used.

The register values in Table 2 are shown in hex (however only the lower 10 bits are relevant), the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode). Check that the PRG flag is set in the Status register ($C6 bit 0 is set to '1') before writing each new P3.2 – P3.7 value via the Programming register ($C8). If a default frequency is not used, the register values in Table 2 should be programmed into the CMX138A immediately after power-up.

Table 2 Xtal/clock Frequency Settings for Program Block 3

Program Register			External frequency source (MHz)								
			3.579	**3.6864**	**6.144**	9.0592	12.0	12.8	16.368	16.8	19.2
P3.2	Idle	GP Timer	*$017*	***$017***	**$018**	*$018*	$019	$019	*$018*	$019	$018
P3.3		VCO output and AUX clk divide	*$085*	***$085***	**$088**	*$10F*	*$10F*	*$110*	*$095*	*$115*	$099
P3.4	Rx or Tx	Ref clk divide	*$043*	**$024**	**$040**	$0C6	$07D	$0C8	$155	$15E	$0C8
P3.5		PLL clk divide	*$398*	**$1E0**	**$200**	$370	$200	$300	$400	$400	$200
P3.6		VCO output and AUX clk divide	*$140*	**$140**	**$140**	$140	$140	$140	$140	$140	$140
P3.7		Internal ADC / DAC clk divide	*$008*	**$008**	**$008**	$008	$008	$008	$008	$008	$008
Connect CLKSEL pin to:			DV_{SS}	**DV_{SS}**	**DV_{DD}**	DV_{DD}	DV_{DD}	DV_{DD}	DV_{DD}	DV_{DD}	DV_{DD}

7.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX138A and the host µC; this interface is compatible with microwire, SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 8.1.1.

The device will monitor the state of the C-BUS registers that the host has written to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be utilised (using the IRQ mask register, $CE). It is permissible for the host to poll the IRQ pin if the host uC does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($C6) for status changes.

7.2.1 C-BUS Operation

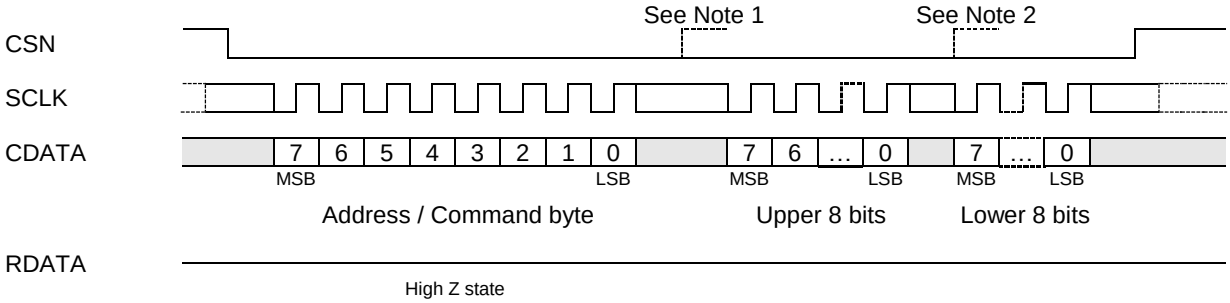
This block provides for the transfer of data and control or status information between the CMX138A's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single

Address byte sent from the µC which may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX138A's Write Only registers, or one or more data byte(s) read out from one of the CMX138A's Read Only registers, as illustrated in Figure 4.

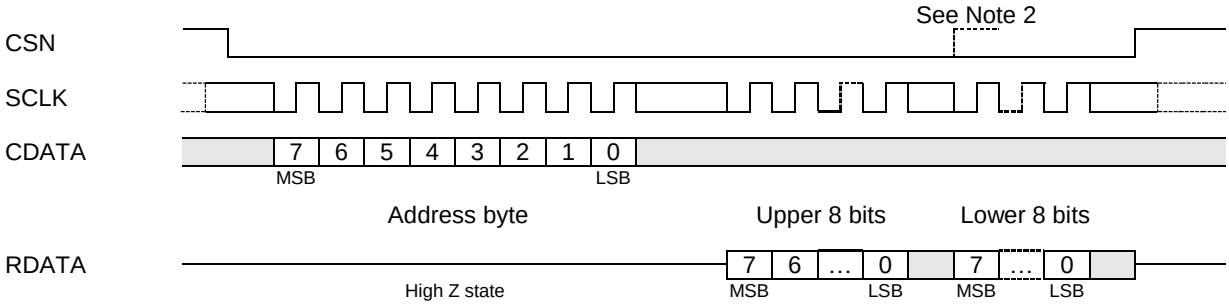
Data sent from the µC on the CDATA line is clocked into the CMX138A on the rising edge of the SCLK input. RData sent from the CMX138A to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 11.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the CMX138A responding to the C-BUS command. Ensure that this C-BUS latency time (up to 250µs) is observed when writing multiple commands to the same C-BUS register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 4 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Device Control

CMX138A can be set into many modes to suit the environment in which it is to be used. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

1. Enable the relevant hardware sections via the Power Down Control register
2. Set the appropriate mode registers to the desired state (Audio, In-band, Sub-Audio etc.)
3. Select the required Signal Routing and Gain
4. Use the Mode Control register to place the device into Rx or Tx mode

To conserve power when the device is not actively processing an analogue signal, place the device into Idle mode. Additional powersaving can be achieved by disabling the unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled.

See:
- Power Down Control - $C0 write
- Mode Control – $C1 write

7.3.1 Signal Routing

The CMX138A offers a flexible routing architecture, with two signal inputs, a single signal processing path with an optional bypass and both Tx Modulation and Audio outputs. Each of the signalling processing blocks is routed directly to the appropriate input and output blocks.

See:
- Analogue Output Gain - $B1 write
- AuxADC and TX MOD Mode - $A7 write
- Mode Control – $C1 write.

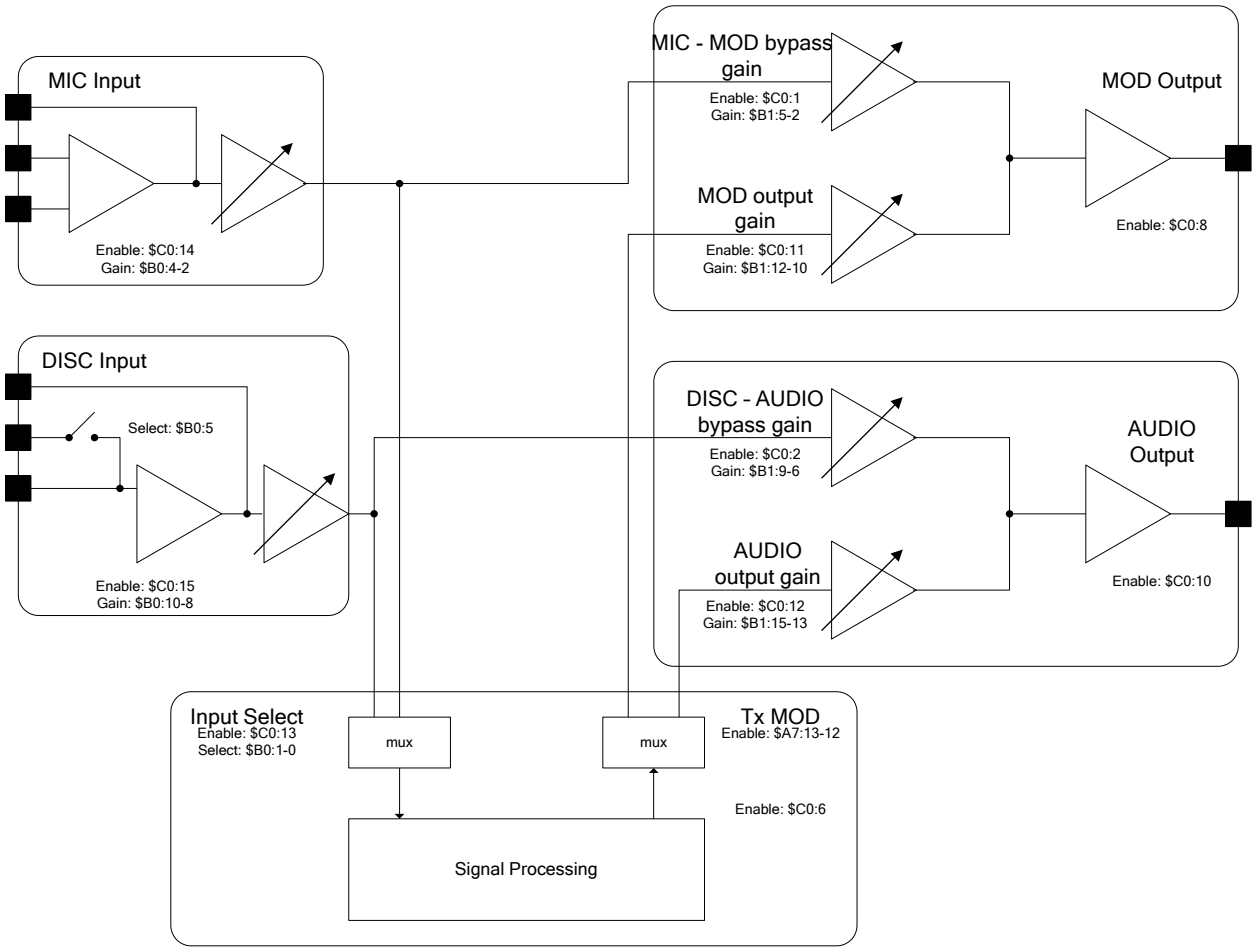


Figure 5 Signal Routing

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Gain control available via the Programming registers.

See:

- Analogue Input Gain - $B0 write
- Analogue Output Gain - $B1 write
- Audio Tone - $CD: 16-bit write.

7.3.2 Mode Control

The CMX138A operates in one of three modes:

- Idle
- Rx
- Tx

At power-on or following a Reset, the device will automatically enter Idle mode, which allows for the maximum powersaving whilst still retaining the capability of monitoring the AuxADC input (if enabled). It is only possible to write to the Programming register whilst in Idle mode.

See:

- Mode Control – $C1 write.

7.4 Audio Functions

The audio signal can be processed in several ways, depending on the implementation required, by selecting the relevant bits in the Audio Control – $C2 write register. In both Rx and Tx, a selectable channel filter to suit either the 12.5kHz or 25kHz TIA/ETSI channel mask can be selected. This filter also incorporates a selectable hard or soft limiter to reduce the effects of over-modulation. Other features include 300Hz HPF, pre- and de-emphasis, companding and frequency inversion scrambling, all of which may be individually enabled. The order in which these features are executed is selectable to ensure compatibility with existing implementations and provide optimal performance (see section 9.2.5).

7.4.1 Audio Receive Mode

The CMX138A operates in half duplex, so whilst in receive mode the transmit path (microphone input and modulator output amplifiers) can be disabled and powered down. The audio output signal level is equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to minimise unwanted audible transients. In the powersave state, the audio output pin enters a hi-Z state, however, if left enabled and the preceding stages powersaved, it will be driven to the V_{BIAS} level.

See:

- Audio Control – $C2 write.

Receiving Audio Band Signals

When a voice-based signal is being received, it is up to the host µC, in response to signal status information provided by the CMX138A, to control muting/enabling of the audio signal to the AUDIO output.

The discriminator path through the device has a programmable gain stage. Whilst in receive mode this should normally be set to 0dB (the default) gain.

Receive Filtering

The incoming signal is filtered, as shown in Figure 6 (with the 300Hz HPF also active), to remove sub-audio components and to minimise high frequency noise. When appropriate, the audio signal can then be routed to the AUDIO output. Separate selectable filters are available for:

- 300Hz High Pass (to reject sub-audible signalling)
- 2.55kHz Low Pass (for 12.5kHz channel operation)
- 3.0kHz Low Pass (for 25kHz channel operation)

Note that with no filters selected, the low frequency response extends to below 5Hz at the low end but still rolls off above 3.3kHz at the top end.

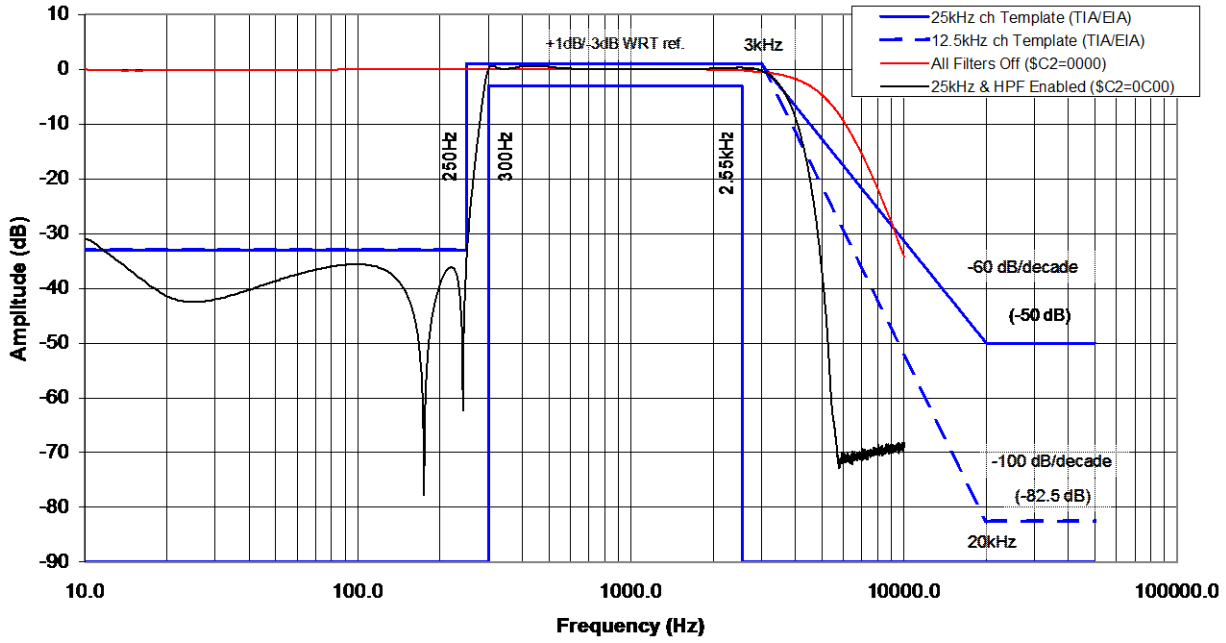


Figure 6 Rx 25kHz Channel Audio Filter Frequency Response

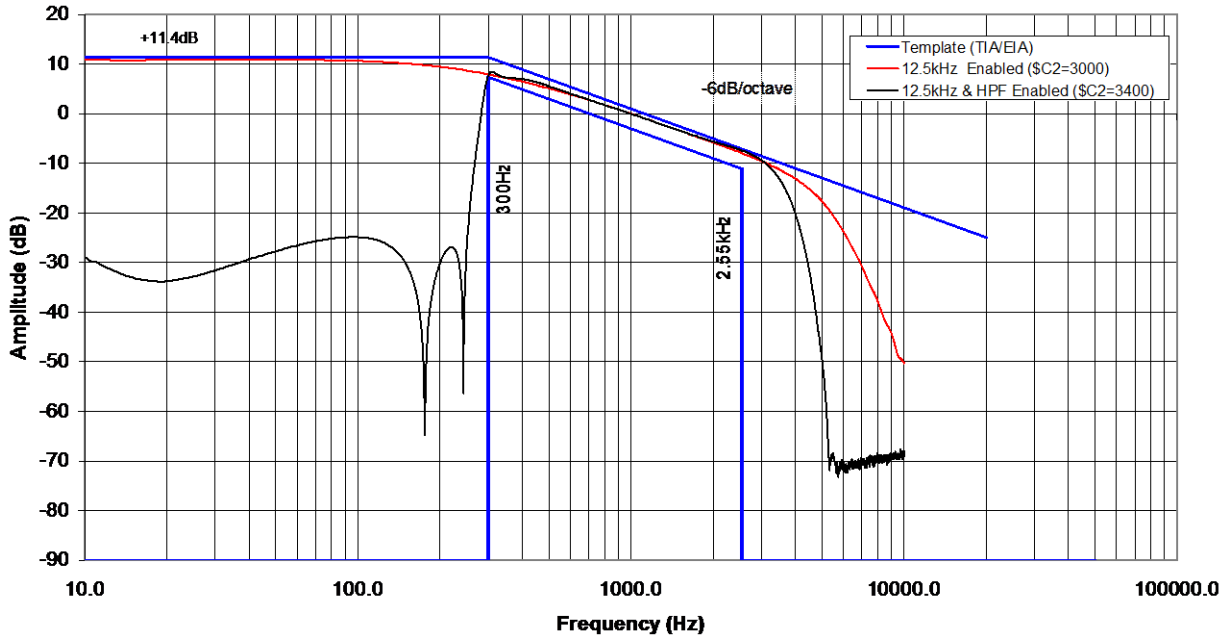


Figure 7 De-emphasis Curve for TIA/EIA-603 Compliance

De-emphasis
Optional de-emphasis at -6dB per octave from 300Hz to 3000Hz (shown in Figure 7) can be selected, to facilitate compliance with TIA/EIA-603, EN 300 086, EN 301 025 etc. The template shows the +1, -3dB limits.

Rx Companding (Expanding)

The CMX138A incorporates an optional syllabic compandor in both transmit and receive modes. This expands received audio band signals that have been similarly compressed in the transmitter to enhance dynamic range. See section 7.4.3 and:

- Audio Control – $C2 write.

Audio De-scrambling
The CMX138A incorporates an optional frequency inversion de-scrambler in receive mode. This de-scrambles received audio band signals that have been scrambled in the transmitter. The inversion frequency can be programmed using the Scramble Frequency register, $CB. The default value is 3300Hz.

See:
- Audio Control – $C2 write
- Scrambler Inversion Frequency – $CB write.

7.4.2 Audio Transmit Mode
The device operates in half duplex, so when the device is in transmit mode the receive path (discriminator and audio output amplifiers) should be disabled, and can be powered down, by the host µC.

A single modulator output with programmable gain is provided which combines both the audio and sub-audio signals to facilitate single or two-point modulation.

To avoid spurious transmissions when changing from Rx to Tx the MOD output is ramped to the quiescent modulator output level, V_{BIAS} before switching. Similarly, when starting a transmission, the transmitted signal is ramped up from the quiescent V_{BIAS} level and when ending a transmission the transmitted signal is ramped down to the quiescent V_{BIAS} level. The ramp rates are set in the Programming register P4.6 and enabled by bits 0,1 of the Analogue Input Gain register. When the modulator output is disabled, their outputs will be set to V_{BIAS}. When the modulator output driver is powered down, its output will enter a hi-Z state (high impedance), so the external RF modulator should be disabled to avoid unwanted transmissions.

For all transmissions, the host µC must only enable signals after the appropriate data and settings for those signals are loaded into the C-BUS registers. As soon as any signalling is enabled the CMX138A will use the settings to control the way information is transmitted.

A programmable gain stage in the microphone input path facilitates a host controlled VOGAD capability.

See:
- Audio Control – $C2 write
- Analogue Input Gain - $B0 write.

Processing Audio Signals for Transmission over Analogue Channels
The microphone input, with programmable gain, can be selected as the audio input source. Pre-emphasis is selectable with either of the two analogue Tx audio filters (for 12.5kHz and 25kHz channel spacing). These are designed for use in EN 300 086, TIA/EIA-603 or EN 301 025 compliant applications. When the 300Hz HPF is enabled, it will attenuate sub-audio frequencies below 250Hz by more than 33dB with respect to the signal level at 1kHz.

These filters, together with a built in limiter, help ensure compliance with EN 300 086 and EN 301 025 (25kHz and 12.5kHz channel spacing) when levels and gain settings are set up correctly in the target system. The channel filters incorporate a soft-limiter function by default, however, should a hard-limiter be required, this can be enabled by setting bit 13 of Program Register P4.9 (see section 9.2.5). The level at which the limiter starts to operate can also be adjusted using Program Register P4.7 (see section 9.2.5).

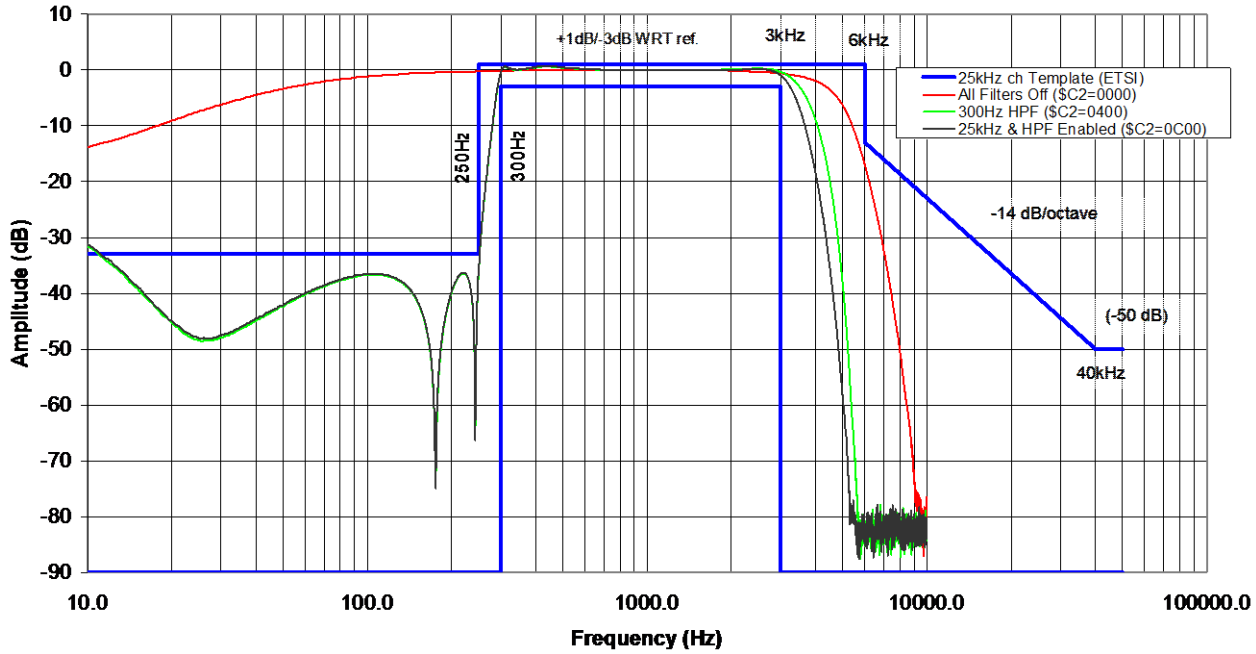


Figure 8 Tx Channel Audio Filter Response and Template (ETSI)

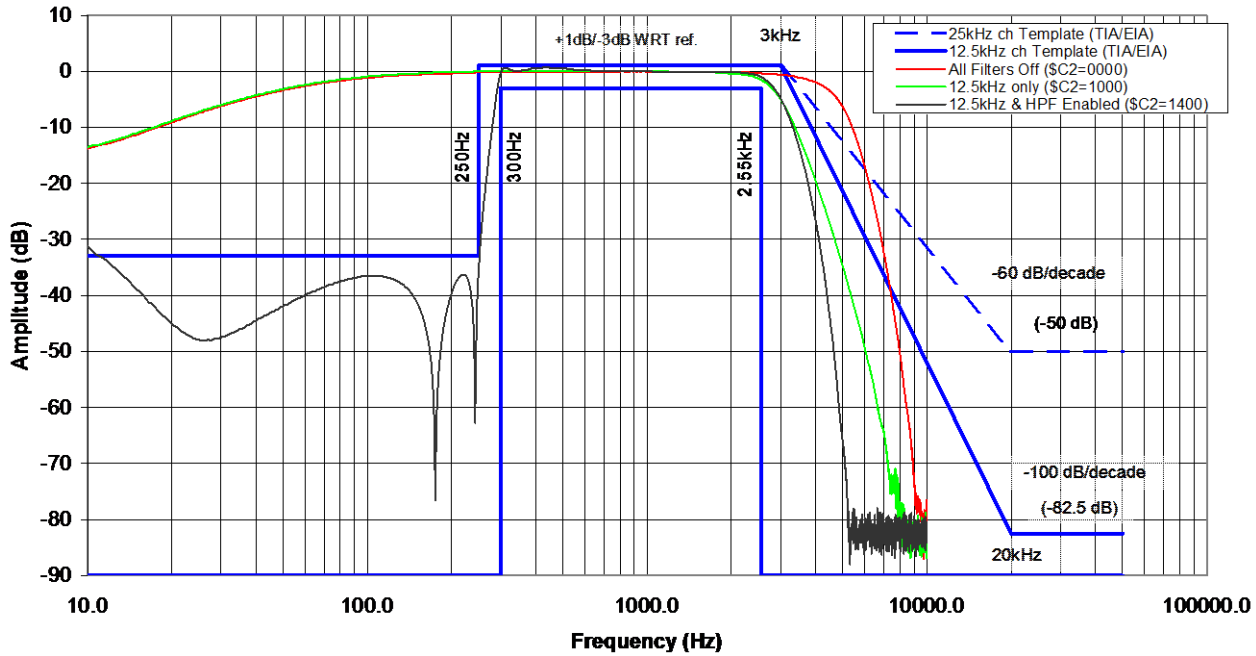


Figure 9 Tx Channel Audio Filter Response and Template (TIA)

The characteristics of the 12.5kHz channel filter fit the template shown in Figure 8 and Figure 9. This filter also facilitates implementation of systems compliant with TIA/EIA-603 'A' , 'B' and 'C' bands .

The CMX138A provides selectable pre-emphasis filtering of +6dB per octave from 300Hz to 3000Hz, matching the template shown in Figure 10.

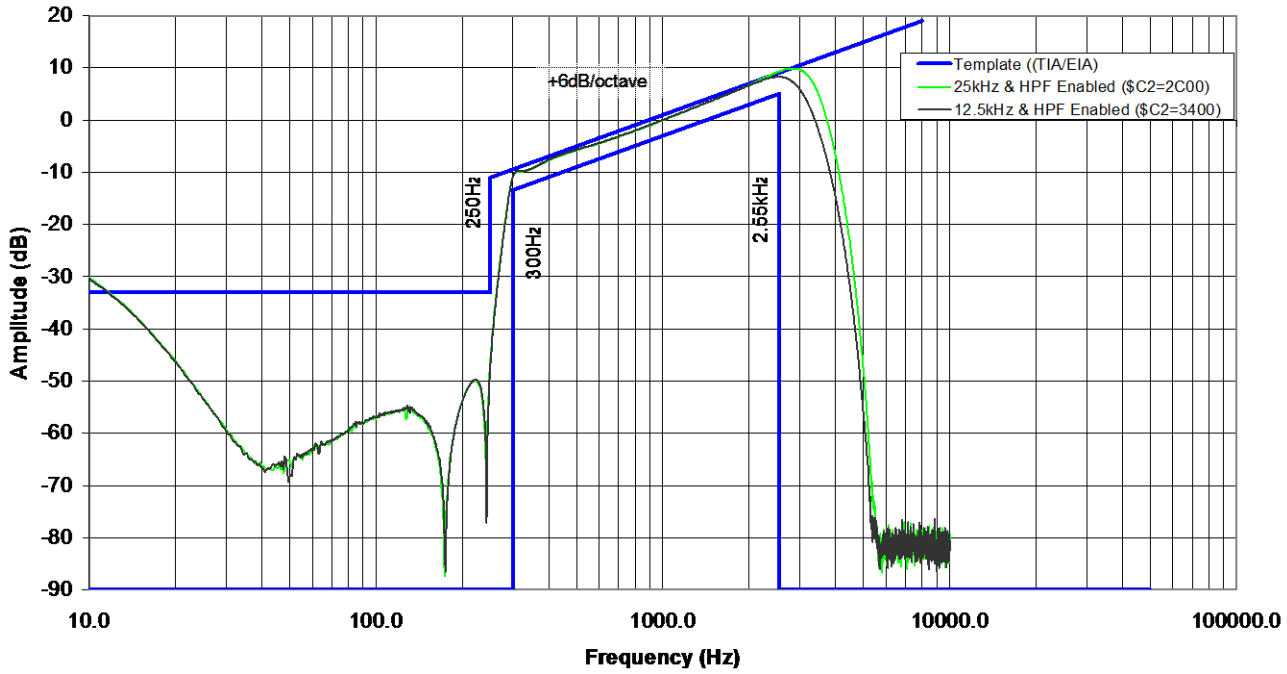


Figure 10 Audio Frequency Pre-emphasis

Modulator Output Routing

The sub-audio component is combined with the audio band signal and this composite signal routed to the MOD output in accordance with the settings of:

- AuxADC and TX MOD Mode - $A7 write
- Analogue Output Gain - $B1 write

Input AGC

An Automatic Gain Control system can be enabled by setting the relevant bits of the Program register P4.9. The setting of the Input 1 Gain stage is recorded when the device enters Tx mode and if the signal exceeds the pre-set threshold, the Input 1 Gain is automatically reduced in 3.2dB steps until it falls within the operational levels or the range of the gain stage is exhausted. When the signal level drops, the gain will be automatically increased in 3.2dB steps at the rate set in P4.9 until the initial value has been reached. For maximum effect the system should be designed such that the +22.4dB setting of the Input 1 Gain stage achieves the nominal levels. To ensure consistent operation, it is recommended that the Input 1 Gain stage value be re-initialised before entering Tx mode. The signal that is used as an input to this process can be selected to be either:

- Output of Input1 gain stage
- Output of the Pre-emphasis filter.

by selecting the relevant bit in P4.9. The Pre-emphasis option should only be chosen if this block is actually in use.

- Analogue Output Gain - $B1 writeProgram Block 4 – Gain and Offset Setup:

Tx Companding (Compressing)
The CMX138A incorporates an optional syllabic compandor in both transmit and receive mode. This compresses audio band signals before transmission to enhance dynamic range. See section 7.4.3 and:

- Audio Control – $C2 write.

Audio Scrambling
The CMX138A incorporates an optional frequency inversion scrambler in transmit and receive modes. This scrambles transmitted audio band signals, which can then be de-scrambled in the receiver. The inversion frequency can be programmed using the Scramble Frequency register, $CB. The default value is 3300Hz. The scrambler frequency may be changed while the device is in an active Rx or Tx mode.

See:
- Audio Control – $C2 write
- Scrambler Inversion Frequency – $CB write

7.4.3 Audio Compandor

The compandor is comprised of a compressor and an expandor. The compressor's function is to reduce the dynamic range of a given signal by attenuating larger amplitudes while amplifying smaller amplitudes. The expandor's function is to expand the dynamic range of a given signal by attenuating small amplitude signals (e.g. noise) while amplifying large amplitude signals. The compressor is used prior to transmission and the expandor is used in the receiver. Hence, using a compandor will enhance performance in a communication system by transmitting a compressed signal, which is less likely to be corrupted by noise, and then at the receiver expanding the compressed signal, which will push the noise picked up during transmission down further.

The CMX138A uses a "syllabic compandor." This type of compandor, as opposed to the instantaneous compandor (e.g. μ/A-law PCM), responds to changes in the average envelope of the signal amplitude according to a syllabic time constant τ. Typically, the steady state output for the compressor is proportional to the square root of the input signal, i.e: for a 2 dB change in input signal, the output change will be 1 dB. Generally for voice communication systems a compressor is expected to have an input dynamic range of 60 dB, providing an output dynamic range of 30 dB. The expandor does the inverse.

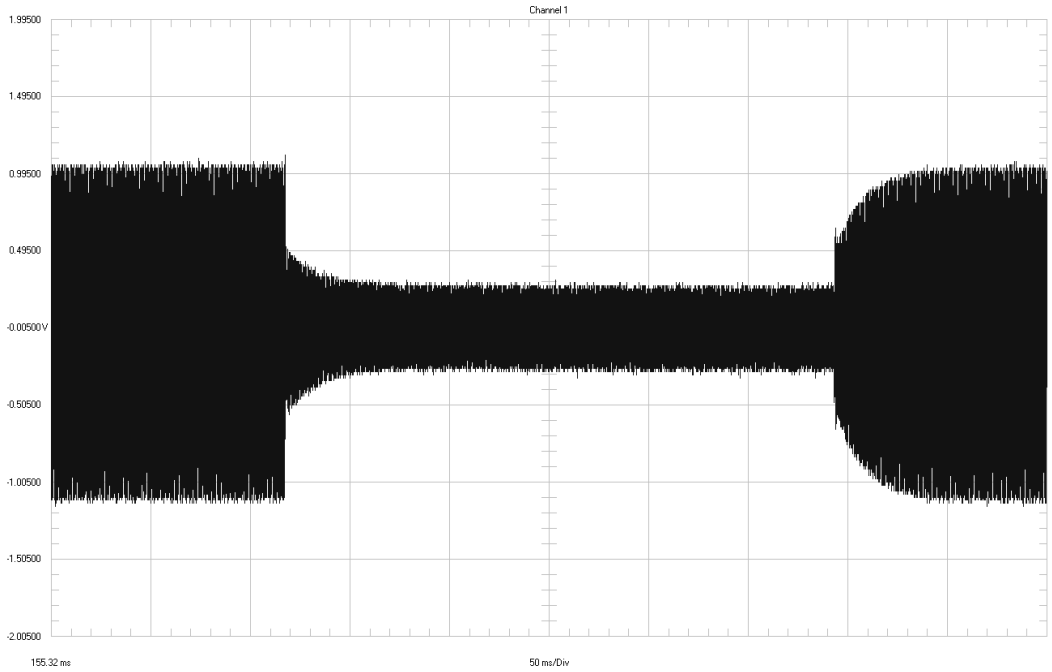


Figure 11 Expandor Transient Response

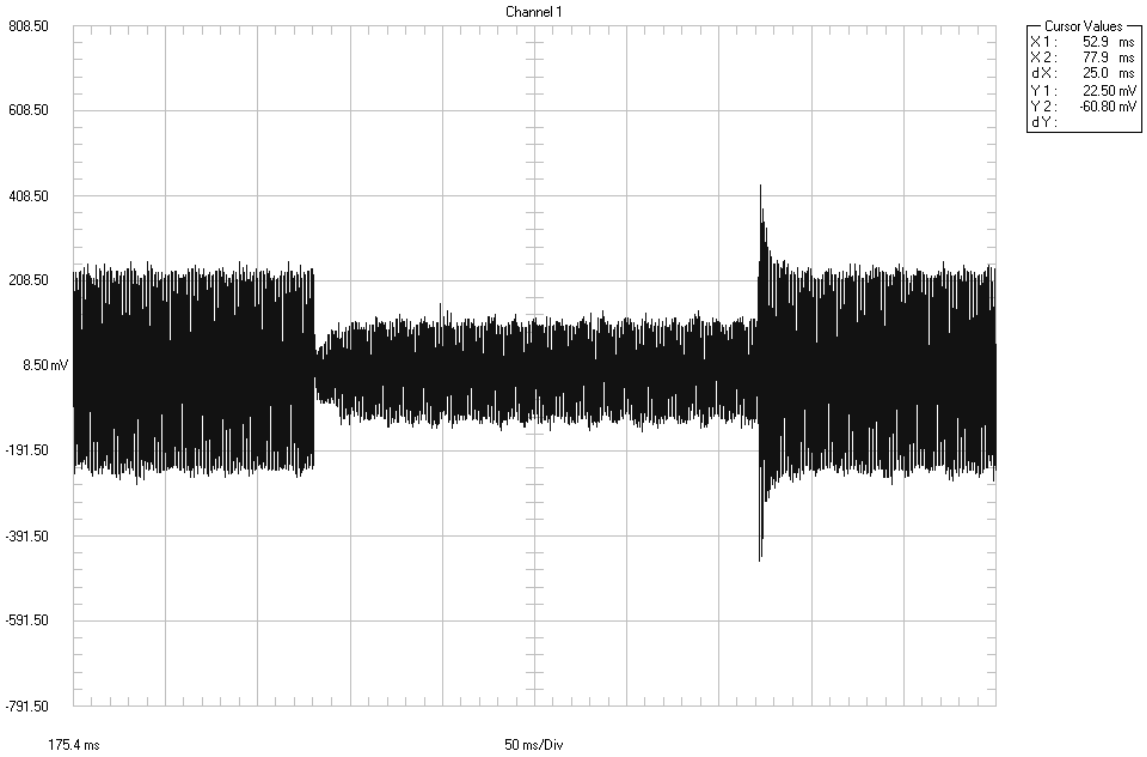


Figure 12 Compressor Transient Response

7.5 Sub-audio Signalling

Sub-audio signalling is available in the audio band below 260Hz. When sub-audio signalling is enabled, the 300Hz HPF in the audio section should also be enabled to remove the sub-audio signalling from the audio signal (in both Tx and Rx). Both CTCSS tones and DCS codes are supported, as well as a special Tone Clone™ mode which will report back any received CTCSS tone rather than look for a specific tone. There are 51 CTCSS tones defined in the CMX138A and there is provision for a user-specified tone. In Tx only, tone phase adjustment (180 or 120 degrees) to implement “Reverse Tone Burst” for squelch tail elimination can be accomplished by setting b9, b8 of the Audio Control register, $C2.

The DCS coder/decoder supports both 23- and 24-bit modes with both true and inverse modulation formats and the 134Hz end of transmission burst.

The CTCSS tone and DCS code values for both Rx and Tx operation are specified in the Audio Control register ($C2), in the lowest 8 bits (shown in decimal):

- 0 No tone
- 1 to 83 DCS code 1 to 83
- 84 User-defined DCS code
- 101 to 183 Inverted DCS code 1 to 83
- 184 Inverted user-defined DCS code
- 200 CTCSS Tone Clone™ mode
- 201 to 254 CTCSS tones 1 to 51, User, XTCSS and DCS off tones
- 255 Invalid tone.

These are detailed in Table 3. The inverted DCS codes are shown in the grey section of the table.

The CTCSS and DCS functions are enabled by the relevant bits in the Mode Control register, $C1, so that the host can turn the functionality on or off without having to re-program the values in the Audio Control register, $C2.

See:

- Analogue Input Gain - $B0 write
- Mode Control – $C1 write
- Audio Control – $C2 write.

DCS and Inverted DCS Codes									CTCSS Tones		
Decimal	HEX	data	Decimal	HEX	data	Decimal	HEX	data	Decimal	HEX	data
0	**000**	**No Tone**	64	040	532	128	080	*172*	192	0C0	x
1	001	023	65	041	546	129	081	*174*	193	0C1	x
2	002	025	66	042	565	130	082	*205*	194	0C2	x
3	003	026	67	043	606	131	083	*223*	195	0C3	x
4	004	031	68	044	612	132	084	*226*	196	0C4	x
5	005	032	69	045	624	133	085	*243*	197	0C5	x
6	006	043	70	046	627	134	086	*244*	198	0C6	x
7	007	047	71	047	631	135	087	*245*	199	0C7	x
8	008	051	72	048	632	136	088	*251*	**200**	**0C8**	**Tone Clone**
9	009	054	73	049	654	137	089	*261*	201	0C9	67
10	00A	065	74	04A	662	138	08A	*263*	202	0CA	71.9
11	00B	071	75	04B	664	139	08B	*265*	203	0CB	74.4
12	00C	072	76	04C	703	140	08C	*271*	204	0CC	77
13	00D	073	77	04D	712	141	08D	*306*	205	0CD	79.7
14	00E	074	78	04E	723	142	08E	*311*	206	0CE	82.5
15	00F	114	79	04F	731	143	08F	*315*	207	0CF	85.4
16	010	115	80	050	732	144	090	*331*	208	0D0	88.5
17	011	116	81	051	734	145	091	*343*	209	0D1	91.5
18	012	125	82	052	743	146	092	*346*	210	0D2	94.8
19	013	131	83	053	754	147	093	*351*	211	0D3	97.4
20	014	132	**84**	**054**	**User Code**	148	094	*364*	212	0D4	100
21	015	134	85	055	x	149	095	*365*	213	0D5	103.5
22	016	143	86	056	x	150	096	*371*	214	0D6	107.2
23	017	152	87	057	x	151	097	*411*	215	0D7	110.9
24	018	155	88	058	x	152	098	*412*	216	0D8	114.8
25	019	156	89	059	x	153	099	*413*	217	0D9	118.8
26	01A	162	90	05A	x	154	09A	*423*	218	0DA	123
27	01B	165	91	05B	x	155	09B	*431*	219	0DB	127.3
28	01C	172	92	05C	x	156	09C	*432*	220	0DC	131.8
29	01D	174	93	05D	x	157	09D	*445*	221	0DD	136.5
30	01E	205	94	05E	x	158	09E	*464*	222	0DE	141.3
31	01F	223	95	05F	x	159	09F	*465*	223	0DF	146.2
32	020	226	96	060	x	160	0A0	*466*	224	0E0	151.4
33	021	243	97	061	x	161	0A1	*503*	225	0E1	156.7
34	022	244	98	062	x	162	0A2	*506*	226	0E2	162.2
35	023	245	99	063	x	163	0A3	*516*	227	0E3	167.9
36	024	251	100	064	x	164	0A4	*532*	228	0E4	173.8
37	025	261	101	065	*023*	165	0A5	*546*	229	0E5	179.9
38	026	263	102	066	*025*	166	0A6	*565*	230	0E6	186.2
39	027	265	103	067	*026*	167	0A7	*606*	231	0E7	192.8
40	028	271	104	068	*031*	168	0A8	*612*	232	0E8	203.5
41	029	306	105	069	*032*	169	0A9	*624*	233	0E9	210.7
42	02A	311	106	06A	*043*	170	0AA	*627*	234	0EA	218.1
43	02B	315	107	06B	*047*	171	0AB	*631*	235	0EB	225.7
44	02C	331	108	06C	*051*	172	0AC	*632*	236	0EC	233.6
45	02D	343	109	06D	*054*	173	0AD	*654*	237	0ED	241.8
46	02E	346	110	06E	*065*	174	0AE	*662*	238	0EE	250.3
47	02F	351	111	06F	*071*	175	0AF	*664*	239	0EF	69.3
48	030	364	112	070	*072*	176	0B0	*703*	240	0F0	62.5
49	031	365	113	071	*073*	177	0B1	*712*	241	0F1	159.8
50	032	371	114	072	*074*	178	0B2	*723*	242	0F2	165.5
51	033	411	115	073	*114*	179	0B3	*731*	243	0F3	171.3
52	034	412	116	074	*115*	180	0B4	*732*	244	0F4	177.3
53	035	413	117	075	*116*	181	0B5	*734*	245	0F5	183.5
54	036	423	118	076	*125*	182	0B6	*743*	246	0F6	189.9
55	037	431	119	077	*131*	183	0B7	*754*	247	0F7	196.6
56	038	432	120	078	*132*	**184**	**0B8**	**User Code**	248	0F8	199.5
57	039	445	121	079	*134*	185	0B9	x	249	0F9	206.5
58	03A	464	122	07A	*143*	186	0BA	x	250	0FA	229.1
59	03B	465	123	07B	*152*	187	0BB	x	251	0FB	254.1
60	03C	466	124	07C	*155*	188	0BC	x	**252**	**0FC**	**User Tone**
61	03D	503	125	07D	*156*	189	0BD	x	**253**	**0FD**	**XTCSS**
62	03E	506	126	07E	*162*	190	0BE	x	**254**	**0FE**	**DCS off**
63	03F	516	127	07F	*165*	191	0BF	x	**255**	**0FF**	**Invalid Tone**

Table 3 DCS Codes and CTCSS Tones

7.5.1 Receiving and Decoding CTCSS Tones

The CMX138A is able to accurately detect valid CTCSS tones quickly, to avoid losing the beginning of audio or data transmissions, and is able to continuously monitor the detected tone with minimal probability of falsely dropping out. The received signal is filtered in accordance with the template shown in Figure 13, to prevent signals outside the sub-audio range from interfering with the sub-audio tone detection.

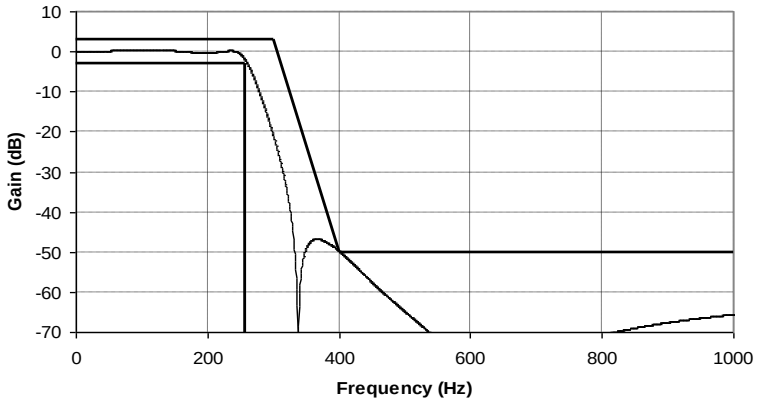


Figure 13 Low Pass Sub-audio Band Filter for CTCSS and DCS

Once a valid CTCSS tone has been detected, Status register ($C6) b11 will be set and the host µC can then route the audio band signal to the audio output. The audio band signal is extracted from the received signal by bandpass filtering as shown in Figure 6.

To optimise the CTCSS tone decoder, adjustable decoder bandwidths and threshold levels allow the user to trade-off decode certainty against signal-to-noise performance when congestion or range restrict the system performance. The tone decoder bandwidth and threshold level are set in P2.1 of the Programming register ($C8) and the desired tone is programmed in the Audio Control register ($C2). In systems which make use of tones 41 to 51 or other “split” tones (tones in between the frequencies of tones 1 to 40), the CTCSS decoder bandwidth should be reduced to avoid false detection of adjacent tones.

When enabled, an interrupt will be issued when an input signal matching a CTCSS tone in Table 3 changes state (ie: on, off or to or from a different tone). If a sub-audio tone is present, but it is not one of the valid CTCSS tones (as shown in Table 3), then it will be reported as an unrecognised tone. If a tone other than the programmed tone is detected, it will be reported as an Invalid tone, unless Tone Cloning is enabled, in which case it will report the detected tone number. Note that CTCSS phase changes are not detected. If enabled, an IRQ will be generated under the following conditions:

State change from:	To:	IRQ	Tone Status value b7-0
No Tone	Own Tone	yes	Own Tone
Own Tone	No Tone	yes	$00
No Tone	Unrecognised Tone	yes	$FF
Unrecognised Tone	No Tone	yes	$00
No Tone	Invalid Tone	yes	$FF or detected Tone
Invalid Tone	No Tone	yes	$00

Tone Cloning™

Tone Cloning™ facilitates the detection of CTCSS tones 1 to 39 in receive mode which allows the device to non-predictively detect any tone in this range. This mode is activated by programming CTCSS Tone Number 00 (b0-7 of Audio Control register = 200 decimal). The received tone number will be reported in the Tone Status register ($CC) and can then be programmed into the Audio Control register by the host µC. The cloned tone will only be active when CTCSS is enabled in the Mode Control register ($C1). This setting has no effect in Tx mode and the CTCSS generator will output no signal.

T Tone Cloning™ is a trademark of CML Microsystems Plc.

Tone Cloning™ should not be used in systems where tones 41 to 51 or other “split” tones (tones between the frequencies of tones 1 to 40) may be received. The all-call tone 40 can still be used after Tone Cloning™ has been performed. The CTCSS decoder detection bandwidth should be set to its lowest value (in P2.1 of the Programming Register) to ensure accurate detection.

CTCSS Tones

Table 3 lists the CTCSS tones available, the tone numbers and the equivalent (decimal) values that need to be programmed into b7-0 of the Audio Control register ($C2) and which will be reported back in the Tone Status register ($CC).

Notes

1. Register value 00 in b0-7 of the Tone Status register ($CC) indicates that none of the above sub-audio tones is being detected. If register value 00 is programmed into the Audio Control register ($C2) and CTCSS enabled in the Mode Control register ($C1), only CTCSS tone 40 (240 decimal) will be scanned for. If CTCSS transmit is selected, this tone setting will cause the CTCSS generator to output no signal.
2. Tone number 40 (240 decimal) provides an all-user CTCSS tone option; regardless of the sub-audio tones set, the CMX138A will report the presence of this tone whenever the CTCSS detector is enabled. This feature is useful for implementing emergency type calls e.g. All-Call.
3. Tone number 55 (255 decimal) is reported in the Tone Status register ($CC), when CTCSS receive is enabled and a sub-audio tone is detected that does not correspond to the selected tone or the all-call tone (tone number 40). This could be a tone in the sub-audio band which is not in the table or a tone in the table which is not the selected tone or All-Call tone.
4. Tones 40 to 51 (240 to 251 decimal) are not in the TIA-603 standard.
5. Tone number 52 (252 decimal) will select the User Programmable Tone value in Program Block 2 – CTCSS and DCS Setup.
6. Tone number 53 (253 decimal) will select the XTCSS call maintenance tone, 64.7Hz.
7. Tone number 54 (254 decimal) will select the DCS turn-off tone, 134.4Hz.
8. Tone Clone, register value 200, is a write-only value to the Audio Control register ($C2). It will not be reported back in the Tone Status register ($CC). Instead, the received tone number is reported back in this register.

7.5.2 Receiving and Decoding DCS Codes

DCS code is in NRZ format and transmitted at 134.4±0.4bps. The CMX138A is able to decode any 23- or 24-bit pattern in either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 4. The CMX138A can detect a valid DCS code quickly enough to avoid losing the beginning of audio transmissions.

Table 4 DCS Modulation Modes

Modulation Type:	Data Bit:	FM Frequency Change:
A	0	Negative frequency shift
	1	Positive frequency shift
B	0	Positive frequency shift
	1	Negative frequency shift

The CMX138A detects the DCS code that matches the programmed code defined in the Audio Control register ($C2) in either its true or inverted form. Register values 1 to 83 correspond to modulation type A (“true”) and register values 101 to 183 correspond to modulation type B (“inverted”). A facility for a user-defined code is available via Program Block 2 – CTCSS and DCS Setup. The signal inversion caused by the input amplifier is automatically compensated for in the device, so that a true DCS signal applied at its input will be decoded as a true code in the Tone Status register ($CC). Note that monitoring this signal at the DISCFB pin will show an inverted waveform.

To detect the pre-programmed DCS code, the signal is low-pass filtered to suppress all but the sub-audio band, using the filter shown in Figure 13. Further equalisation filtering, signal slicing and level detection are performed to extract the code being received. The extracted code is then matched with the

programmed 23- or 24-bit DCS code to be recognised, in the order least significant first through to most significant DCS code bit last. Table 5 shows a selection of valid 23-bit DCS codes: this does not preclude other codes being programmed. Recognition of a valid DCS code will be flagged if the decode is successful (3 or less errors) by setting b10 of the Status register ($C6) to 1. A failure to decode is indicated by clearing this bit to 0. This bit is updated after the decoding of every 4th bit of the incoming signal. The actual code received is reported back in the Tone Status register ($CC) according to Table 3, so that the host µC can determine if it was the true or inverted form of the code.

Once a valid DCS code has been detected, the host µC can route the audio band signal to the audio output. The audio signal is extracted from the received input signal by band pass filtering, see Figure 6.

The end of DCS transmissions is indicated by a 134.4 ±0.5Hz tone for 150-200ms. When a valid DCS code has been detected, the CMX138A will automatically scan for the turn-off tone. When the DCS turn-off tone is detected it will cause a DCS interrupt and report tone 54 (Tone Status b0-7 value 254 decimal); the receiver audio output can then be muted by the host. Note that, due to the asynchronous nature of the turn-off tone, it is possible for both a “no-tone” and a “turn-off” tone to be indicated at the end of a DCS transmission. Note that DCS detection and CTCSS detection can not be performed concurrently.

Table 5 DCS 23 Bit Codes

Reg Value True	Reg Value Invert	**DCS Code**	DCS bits 22-12	DCS bits 11-0	Reg Value True	Reg Value Invert	**DCS Code**	DCS bits 22-12	DCS bits 11-0	Reg Value True	Reg Value Invert	**DCS Code**	DCS bits 22-12	DCS bits 11-0
1	*101*	**023**	763	813	*29*	*129*	**174**	18B	87C	*57*	*157*	**445**	7B8	925
2	*102*	**025**	6B7	815	*30*	*130*	**205**	6E9	885	*58*	*158*	**464**	27E	934
3	*103*	**026**	65D	816	*31*	*131*	**223**	68E	893	*59*	*159*	**465**	60B	935
4	*104*	**031**	51F	819	*32*	*132*	**226**	7B0	896	*60*	*160*	**466**	6E1	936
5	*105*	**032**	5F5	81A	*33*	*133*	**243**	45B	8A3	*61*	*161*	**503**	3C6	943
6	*106*	**043**	5B6	823	*34*	*134*	**244**	1FA	8A4	*62*	*162*	**506**	2F8	946
7	*107*	**047**	0FD	827	*35*	*135*	**245**	58F	8A5	*63*	*163*	**516**	41B	94E
8	*108*	**051**	7CA	829	*36*	*136*	**251**	627	8A9	*64*	*164*	**532**	0E3	95A
9	*109*	**054**	6F4	82C	*37*	*137*	**261**	177	8B1	*65*	*165*	**546**	19E	966
10	*110*	**065**	5D1	835	*38*	*138*	**263**	5E8	8B3	*66*	*166*	**565**	0C7	975
11	*111*	**071**	679	839	*39*	*139*	**265**	43C	8B5	*67*	*167*	**606**	5D9	986
12	*112*	**072**	693	83A	*40*	*140*	**271**	794	8B9	*68*	*168*	**612**	671	98A
13	*113*	**073**	2E6	83B	*41*	*141*	**306**	0CF	8C6	*69*	*169*	**624**	0F5	994
14	*114*	**074**	747	83C	*42*	*142*	**311**	38D	8C9	*70*	*170*	**627**	01F	997
15	*115*	**114**	35E	84C	*43*	*143*	**315**	6C6	8CD	*71*	*171*	**631**	728	999
16	*116*	**115**	72B	84D	*44*	*144*	**331**	23E	8D9	*72*	*172*	**632**	7C2	99A
17	*117*	**116**	7C1	84E	*45*	*145*	**343**	297	8E3	*73*	*173*	**654**	4C3	9AC
18	*118*	**125**	07B	855	*46*	*146*	**346**	3A9	8E6	*74*	*174*	**662**	247	9B2
19	*119*	**131**	3D3	859	*47*	*147*	**351**	0EB	8E9	*75*	*175*	**664**	393	9B4
20	*120*	**132**	339	85A	*48*	*148*	**364**	685	8F4	*76*	*176*	**703**	22B	9C3
21	*121*	**134**	2ED	85C	*49*	*149*	**365**	2F0	8F5	*77*	*177*	**712**	0BD	9CA
22	*122*	**143**	37A	863	*50*	*150*	**371**	158	8F9	*78*	*178*	**723**	398	9D3
23	*123*	**152**	1EC	86A	*51*	*151*	**411**	776	909	*79*	*179*	**731**	1E4	9D9
24	*124*	**155**	44D	86D	*52*	*152*	**412**	79C	90A	*80*	*180*	**732**	10E	9DA
25	*125*	**156**	4A7	86E	*53*	*153*	**413**	3E9	90B	*81*	*181*	**734**	0DA	9DC
26	*126*	**162**	6BC	872	*54*	*154*	**423**	4B9	913	*82*	*182*	**743**	14D	9E3
27	*127*	**165**	31D	875	*55*	*155*	**431**	6C5	919	*83*	*183*	**754**	20F	9EC
28	*128*	**172**	05F	87A	*56*	*156*	**432**	62F	91A	*84*	*184*	User Defined		

Notes:

1. Register value 84 will select the User Programmable DCS code value in Program Block 2 – CTCSS and DCS Setup Register value 184 will select the inverted form of the User Programmable DCS code.
2. Note that the Audio Control register values are shown in decimal.

7.5.3 Transmit CTCSS Tone

The sub-audio CTCSS tone generated is defined in the Audio Control register ($C2). Table 3 lists the CTCSS tones and the corresponding decimal values for programming b0-7 of the register. To facilitate Squelch Tail elimination and Reverse Tone Burst, the phase of the transmitted tone can be altered by either 120, 180 or 240 degrees by setting b9, b8 in the Audio Control register ($C2). The phase change is not instantaneous, but implemented by retarding the phase of the tone to its new value over a number of cycles to avoid the generation of spurious signals. A 180 degree change will be completed within 20ms.

7.5.4 Transmit DCS Code

A 23- or 24-bit sub-audio DCS code can be generated, as defined by the Audio Control register ($C2). The same DCS code pattern is used for detection and transmission. The DCS code is NRZ encoded at 134.4±0.4 bps, low-pass filtered and added to the audio band signal, before being passed to the modulator output stages. Valid 23-bit DCS codes and the corresponding settings for the Audio Control Register are shown in Table 5, and include a user-defined facility. The least significant bit of the DCS code is transmitted first and the most significant bit is transmitted last. The CMX138A is able to encode and transmit either of the two DCS modulation modes defined by TIA/EIA-603 (true and inverted) described in Table 4. If 24-bit mode is required, bit 11 of Programming register P2.1 should be set. The MOD output inverts the signal from the device, so, depending on the detailed design of the following modulator sections, it may be necessary to select an inverted DCS code in the Audio Control register ($C2) in order to produce a true DCS code "on-air".

To signal the end of the DCS transmission, the host should set the Audio Control register ($C2) to the DCS turn off tone (register value b0-7 = 254 decimal) for 150ms to 200ms. After this time period has elapsed the host should then disable DCS in the Mode Control register ($C1). Note that if a CTCSS tone is to be transmitted following the DCS turn-off tone (in a subsequent transmission) the new CTCSS value will need to be written to the Audio Control register ($C2) immediately after the selection of Tx mode.

7.6 In-band Signalling – User Tones

The CMX138A supports a user-programmable in-band tone between 288Hz and 3000Hz. Note that if a tone below 400Hz is used, sub-audio signalling should be disabled and the 300Hz HPF disabled.

By default, the CMX138A will use a 1750Hz tone, however this may be changed by the host to any valid tone within its operational range by use of the Programming register. This ensures that the device can remain compatible with all available tone systems in use. The CMX138A does not implement automatic repeat tone insertion or deletion: it is up to the host to correctly implement the appropriate protocol.

Selection of the In-band signalling mode is performed by bits 10-9 of the Mode register ($C1). Detection of the selected In-band signalling mode can be performed in parallel with audio or data reception.

See:

- Mode Control – $C1 write
- Tx In-band Tone - $C3 write
- Tone Status - $CC read.

7.6.1 Receiving and Decoding In-band Tone

In-band tones can be used to flag the start of a call or to confirm the end of a call. If they occur during a call the tone may be audible at the receiver. When a valid input signal is detected, it will be reported in the Tone Status register, $CC. If the input signal matches the In-band tone value then b15 will be set (tone detected), otherwise b14-11 will be set (unrecognised tone) – see Table 6. If enabled, an IRQ will be generated as shown below:

State Change From:	To:	IRQ	Tone Status Value b15-11
No Tone	Own Tone	yes	10000
Own Tone	No Tone	yes	00000
No Tone	Unrecognised Tone	no	00000
Own Tone	Unrecognised Tone	yes	01111
Unrecognised Tone	No Tone	no	00000

The frequency of the tone is defined in Programming register P1.2.

Adjustable decoder bandwidths and threshold levels are programmable via the Programming register. These allow certainty of detection to be traded against signal to noise performance when congestion or range limits the system performance. The in-band signal is derived from the received input signal after the bandpass filtering shown in Figure 6.

Table 6 In-band Tone

b15	b14	b13	b12	b11	Rx Mode $CC	Tx Mode $C3
0	0	0	0	0	No Tone	No Tone
1	0	0	0	0	Tone Detected	Transmit In-band Tone
x	1	1	1	1	Unrecognised Tone	*reserved*

7.6.2 Transmitting In-band Tone

The In-band tone to be generated is defined in the TX TONE register ($C3). The tone level is set in the Programming register (P1.0). The In-band tone must be transmitted without other signals in the audio band, so the host µC must disable the audio path prior to initiating transmission of an In-band tone and restore it after the In-band tone transmission is complete.

7.7 Auxiliary ADC Operation

The input to the Auxiliary ADC is routed through an inverting op-amp from the AuxADC input pin under control of the AuxADC and Tx MOD mode register, $A7. Conversions will be performed as long as the input source is selected; to stop the ADC, the input source should be set to “none”. Register $C0, b6 (BIAS) must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the Signal Routing register, $A7, the length of the averaging is determined by the value in the Programming register (P3.0), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value. The proportion is determined by the value of the average counter in P3.0, as follows:

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value,

1 = 25% of the current value will be added to 75% of the last average value

2 = 12.5% etc.

The maximum useful value of this field is 8. For a step input signal, this provides an exponential-style response in the output data.

High and low thresholds may be independently applied to the ADC channel (the comparison is applied after averaging, if this is enabled) and b8 of the IRQ Status register ($C6) will be set (and an IRQ generated, if enabled) whenever the signal crosses above the High threshold or below the Low threshold (except in the case where the high threshold has been set below the low threshold). The threshold status can be determined from b15 and b14 of the AuxADC data register ($A9). The thresholds are programmed via the AuxADC Threshold register ($B5). Auxiliary ADC data is read back in the AuxADC Data register ($A9) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled). Note that the thresholds are inverted due to the op-amp on the AuxADC input pin.

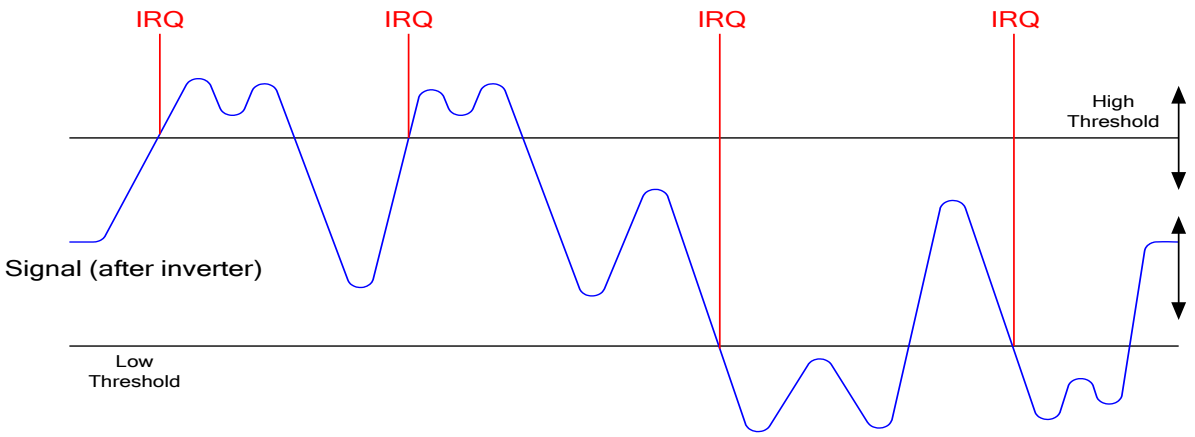


Figure 14 AuxADC IRQ Operation

To avoid multiple threshold IRQs when a noisy signal is present, the thresholds can be re-programmed following the initial event to provide hysteresis.

See:

- AuxADC and TX MOD Mode - $A7 write
- AuxADC Data - $A9 read
- AuxADC Threshold Data - $B5 write.

7.8 Auxiliary DAC/RAMDAC Operation

The Auxiliary DAC channel is programmed via the AuxDAC Control register, $A8. AuxDAC may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 11), but this may be over-written with a user defined profile by writing to Programming register P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. The AuxDAC output holds the user-programmed level during a powersave operation if left enabled, otherwise it will return to zero.

See:

- AuxDAC Control/Data - $A8 write.

7.9 Digital System Clock Generator

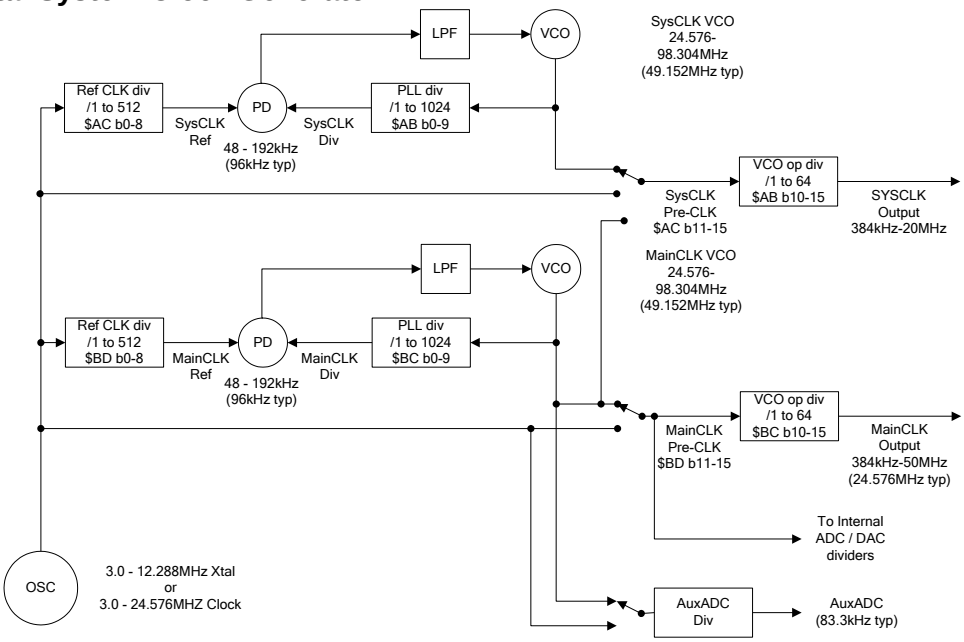


Figure 15 Digital Clock Generation Schemes

The CMX138A includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in Figure 2, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 6.144MHz or 3.6864MHz Xtal is assumed for the default functionality provided in the CMX138A (see section 7.1).

7.9.1 Main Clock Operation

A PLL is used to create the Main Clock (nominally 24.576MHz) for the internal sections of the CMX138A. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose Timer and the signal processing block. It should be noted that in Idle mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX138A defaults to the settings appropriate for a 6.144MHz or 3.6864MHz Xtal, however if other frequencies are to be used (to facilitate commonality of Xtals between the external RF synthesizers and the CMX138A for instance) then the Program Block registers P3.2 to P3.7 will need to be programmed appropriately at power-on. A table of common values is provided in Table 2. The C-BUS registers $BC and $BD are controlled automatically and must not be accessed directly by the user.

See:

- Program Block 3 – AuxDAC, RAMDAC and Clock Control:

7.9.2 System Clock Operation

A System Clock output, SysClock1 Out, is available to drive additional circuits, as required. This is a phase locked loop (PLL) clock that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure register ($AB) controls the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure register ($AC) controls the values of the Reference Divider and signal routing configurations. The PLL is designed for a reference frequency of 96kHz. If not required, this clock can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 15. Note that at power-on the System Clock output is turned off and the output is held at '0'.

See:

- System Clk PLL Data - $AB write
- System Clk REF - $AC write.

7.10 GPIO

Two pins on the CMX138A are provided for Rx and Tx Enables. These pins become active low when the device enters the appropriate mode. These can be used for driving external circuitry and have the advantage of having minimal delay from the activation of the selected mode and so are not dependant upon any delays due to the transfer of commands / data over the C-BUS.

$C1 Mode	b1	b0	Tx_ENA	Rx_ENA
Idle	0	0	1	1
Rx	0	1	1	0
Tx	1	0	0	1
reserved	1	1	1	1

7.11 Signal Level Optimisation

The internal signal processing of the CMX138A will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) – (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. Compared to the reference level of 308mV rms, this is a signal of +8.69dB. This should not be exceeded at any stage.

7.11.1 Transmit Path Levels

For the maximum undistorted signal out of the MOD attenuator, the signal level at the output of the Analogue block should not exceed +8.69dB, assuming both fine and coarse output attenuators are set to a gain of 0dB. The sub-audio level is normally set to 31mV rms ±1.0dB, which means that the output from the soft limiter must not exceed 803mV rms. If pre-emphasis is used, an output signal at 3000Hz will have three times the amplitude of a signal at 1000Hz, so the signal level before pre-emphasis should not exceed 268mV rms. If the compressor is also used, its 'knee' is at 100mV rms, which would allow a signal into the compressor of 718mV rms, which is less than the maximum signal level. The Fine Input Gain adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the MICFB pin would be 54mV rms. With the lowest gain setting (0dB), the maximum allowable input signal level at the MICFB pin would be 718mV rms.

In some applications where there is a requirement for the system to operate with a significant overload on the MIC input (+20dB) an external limiter may be required to ensure that the signal input does not exceed the recommended CMX138A input levels. This can result in significant harmonic content (above 6kHz) that should be removed by suitable input filtering.

7.11.2 Receive Path Levels

For the maximum undistorted signal out of the audio attenuator, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output attenuators are set to a gain of 0dB. In this case, there is no sub-audio signal to be added, so the maximum signal level remains at 838mV rms. If de-emphasis is used, an output signal at 300Hz will have three and a third times the amplitude of a signal at 1000Hz, so the signal level before de-emphasis should not exceed 251mV rms. If the expander is also used, its 'knee' is at 100mV rms, which would allow a signal into the expander of 158mV rms. The Fine Input Gain adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input Gain adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the DISCFB pin would be 12.0mV rms. With the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 158mV rms. The signal level of +8.69dB (838mV rms) is an absolute maximum, which should not be exceeded anywhere in the signal processing chain if severe distortion is to be avoided.

8 C-BUS Register Summary

Table 7 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC and TX MOD Mode	16
$A8	W	AuxDAC Control/Data	16
$A9	R	AuxADC Data	16
$AA	R	Checksum 2 lo	16
$AB	W	System Clk PLL Data	16
$AC	W	System Clk REF	16
$AD		*reserved*	
$AE		*reserved*	
$AF		*reserved*	
$B0	W	Analogue Input Gain	16
$B1	W	Analogue Output Gain	16
$B2		*reserved*	
$B3		*reserved*	
$B4		*reserved*	
$B5	W	AuxADC Threshold Data	16
$B6		*reserved*	
$B8	R	Checksum 1 hi	16
$B9	R	Checksum 1 lo	16
$BB		*reserved*	
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power-Down Control	16
$C1	W	Mode Control	16
$C2	W	Audio Control	16
$C3	W	Tx In-band Tone	16
$C5	R	Device ID	16
$C6	R	Status	16
$C7		*reserved*	
$C8	W	Programming	16
$C9		*reserved*	
$CA		*reserved*	
$CB	W	Scrambler Inversion Frequency	16
$CC	R	Tone Status	16
$CD	W	Audio Tone	16
$CE	W	Interrupt Mask	16
$CF		*reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8.1.1 Interrupt Operation

The CMX138A will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the Status register, except the Programming Flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The Programming Flag bit is set to 1 only when it is permissible to write a new word to the Programming register. See:

- Status – $C6 read
- Interrupt Mask - $CE write

8.1.2 General Notes

In normal operation, the most significant registers are:

- Mode Control – $C1 write
- Status – $C6 read
- Analogue Input Gain - $B0 write
- Analogue Output Gain - $B1 write
- Audio Control – $C2 write.

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed, whilst setting the Mode register to Idle will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

The CMX138A manages the internal clocks automatically to minimise power consumption, using the default values loaded in Program Block 3.

9 Configuration Guide

9.1 C-BUS Register Details

		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
01	w	C-BUS Reset															
A7	w	AuxADC, TX mode	0	0	Tx MOD		0	0	0	0	Aux ADC Av mode	Aux ADC ip select				RampUP	RampDN
A8	w	AuxDAC Ctrl Data	ENA	0	0	RamDAC	0	0	Aux DAC data								
A9	r	AuxADC 1 Data	Threshold Status		x	x	x	Aux ADC data									
A9	r																
AA	r																
AA	r	pon checksum 2 lo	power-on checksum 2 lo														
AB	w	Sys Clk PLL Data	System CLK1 VCO divider				System CLK1 Feedback divider										
AC	w	System Clk REF	op select	ENA CLK	ENA DIV	bypass	IP sel	OP slew rate	Ref CLK divider								
AD	w																
AE	w																
B0	w	Analog Input Gain	0	0	0	0	0	DISC Input gain		0	0	DISCsel	MIC Input gain			Rx / Tx select	
B1	w	Analog Output Gain	AUDIO ouput gain			MOD output gain			DISC-AUDIO bypass gain		MIC-MOD bypass gain					0	0
B2	w																
B3	w																
B4	r																
B5	w	AuxADC Threshold	ADC sel	Hi / Lo	0	0	0	Aux ADC Threshold data									
B6	w																
B7	w																
B8	r	pon checksum 1 hi	power-on checksum 1 lo														
B9	r	pon checksum 1 lo	power-on checksum 1 hi														
BA	r																
BB	r																
C0	w	Power Down Ctrl	DISC amp	MIC amp	Input ena	AUD gain	MOD gain	AUD ena	0	MOD ena	0	BIAS ena	reset	Protect	XTAL dis	DISC by	MIC by	0
C1	w	Mode Control	0	Audio	0	0	0	In-Band modes		0	0	Sub Audio mode		0	0	0	Idle / Rx / Tx	
C2	w	Audio Control	scramble	compand	emphasis	12k5	25k	hpf	CTCSS Invert		Sub Audio tone number - CTCSS / DCS / none							
C3	w	Tx In-band Tone	Tx In-band tone					0	0	0	0	0	0	0	0	0	0	0
C5	r	Device ID																
C6	r	Status	IRQ	x	Rx In	x	CTCSS	DCS	x	AuxADC	x	x	x	x	x	x	x	Program
C7	w																	
C8	w	Programming	Prgram Block Address					Program Block Data										
C9	r																	
CA	w																	
CB	w	Scrambler Freq	0	0	Scrambler Inversion Frequency													
CC	r	Tone Status	In-Band Tone Detected				x	x	x	Detected DCS or CTCSS code								
CD	w	Audio Tone	0	0	0	0	Audio Tone Frequency											
CE	w	Interrupt Mask	IRQ	0	Rx In	0	CTCSS	DCS	0	AuxADC	0	0	0	0	res	0	Program	
CF	w	Test Control																

The detailed descriptions of the C-BUS registers are presented in numerical order and should be read in conjunction with the relevant functional descriptions.

9.1.1 Reset Operations

A reset is automatically performed when power is applied to the CMX138A. A reset can be issued as a C-BUS command, either as a General Reset command ($01), or by setting the appropriate bit (b5) in the Powerdown Control register ($C0). In the latter case, an option exists to protect the values held in the Program Block (which is accessed via the Programming register, $C8). The action of each reset type is shown in the table below:

Table 8 Reset Operations

	Reset type	Protect bit ($C0 b4) state	Program Block state
1	Power On	cleared by h/w	default
2	General Reset (C-BUS $01)	cleared by h/w	default
3	Reset (C-BUS $C0 b5)	0	default
4	Reset (C-BUS $C0 b5)	1	protected

Following a Reset operation, the internal checksum values are made available in the $AA, $B8 and $B9 registers. The device ID is available in $C5.

The status of the Power-Down register, $C0, can be read back in $C4 to ensure that C-BUS communications are operational.

9.1.2 General Reset - $01 write

The General Reset command has no data attached to it. It puts the device registers into the states listed below. A power-on reset performs the same action.

ADDR.	REGISTER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$A7	AuxADC/TX MOD Mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A8	AuxDAC Control/Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$A9	AuxADC data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AA	*power-on checksum 2 lo*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$AB	System Clk PLL Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AC	System Clk Ref	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AD	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AE	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$AF	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B0	Analogue Input Gain	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B1	Analogue Output Gain	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B2	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B3	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B4	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B5	AuxADC Threshold Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B6	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B8	*power-on checksum 1 hi*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$B9	*power-on checksum 1 lo*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$BB	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$BC	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$BD	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$BE	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$BF	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C0	PowerDown Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C1	Mode Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C2	Audio Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C3	Tx In-band Tone	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C5	*product identification*	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c
$C6	Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C7	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C8	Programming	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C9	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CA	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CB	Scrambler Inv. Frequency	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CC	Tone Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CD	Audio Tone	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CE	Interrupt Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CF	*reserved*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes: 'c' is the power-on checksum or product identification, returned in registers $AA, $B8, $B9 and $C5. Any registers not mentioned above are undefined.

9.1.3 AuxADC and TX MOD Mode - $A7 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Tx MOD Mode		0	0	0	0	0	AuxADC AV Mode		AuxADC I/P Select			RU	RD

b15-14 reserved, clear to 0

b13	b12	Tx MOD mode output
1	**1**	**In-band + Sub-Audio**
1	0	*reserved*
0	1	*reserved*
0	0	bias

For normal operation, these bits should both be set to 1 in both Rx and Tx modes.

b11-7 reserved, clear to 0

b6	b5	AuxADC Averaging Mode
1	1	*reserved*
1	0	*reserved*
0	1	rolling average, uses Program Block 3.0 value
0	0	No averaging

b4	b3	b2	AuxADC Input Select
1	1	1	*reserved*
1	1	0	*reserved*
1	0	1	*reserved*
1	0	0	*reserved*
0	1	1	*reserved*
0	1	0	*reserved*
0	0	1	AuxADC
0	0	0	off

b1 MOD Ramping Up 0 = off 1 = enable
b0 MOD Ramping Down 0 = off 1 = enable

9.1.4 AuxDAC Control/Data - $A8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	0	0	RAM DAC	0	0	AUX DAC data / RAMDAC control									

b15 enable Aux DAC 0 = disable 1 = enable
b14 *reserved*
b13 *reserved*
b12 RAMDAC enable 0 = AuxDAC operates normally
1 = AuxDAC operates as a RAMDAC[1]. Data in b0-6 controls the RAMDAC functions.
b11 *reserved*
b10 *reserved*
b9 – b0 AuxDAC data (unsigned)

[1] Do NOT write to directly to AuxDAC whilst the RAMDAC is in operation. RAMDAC is only available when in Tx mode.

Note: when $A8 b12 is set to 1, writing data to this register controls the RAMDAC settings. Writing to AuxDAC whilst the RAMDAC is still ramping may cause un-intended operation. In this mode b9 to b0 perform the following functions:

b9 reserved, clear to 0
b8 reserved, clear to 0
b7 reserved, clear to 0
b6 RAMDAC RAM access, 0 resets the internal RAMDAC address pointer.

			RAMDAC Scan Time	
b5	b4	b3	Divider	Time (ms)
0	0	0	1024	10.50
0	0	1	512	5.25
0	1	0	256	2.63
0	1	1	128	1.31
1	0	0	64	0.66
1	0	1	32	0.33
1	1	0	16	0.16
1	1	1	8	0.08

b2 Scan direction: 0 = ramp down 1 = ramp up
b1 Autocycle 0 = disable 1 = continuous ramp up/down
b0 RAMDAC start 0 = stop 1 = start RAMDAC ramping

Before using the RAMDAC, the AuxDAC must be powered up by writing $8000, then after the C-BUS latency period of 250µs:

To initiate a RAMDAC ramp up write: $9005.
To initiate a RAMDAC ramp down, write: $9001.

To place AuxDAC back into powersave, it must be written to explicitly. Do NOT change IDLE/Rx/Tx mode whilst the RAMDAC is still ramping.

9.1.5 AuxADC Data - $A9 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Threshold status		x	x	x	x	AUX ADC Data									

b15, b14 Threshold Status

b15 = 1 signal is above the high threshold
= 0 signal is below the high threshold
b14 = 1 signal is below the low threshold
= 0 signal is above the low threshold

b13 *reserved*
b12 *reserved*
b11 *reserved*
b10 *reserved*
b9 –b0 AuxADC data or last reading (unsigned) - $000 = DV_{DD}, $3FF = DV_{SS}

9.1.6 System Clk PLL Data - $AB write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCO OP Divide Ratio <5-0>						PLL Feedback Divide Ratio <9-0>									

b15-b10 divide the selected output clock source by the value in these bits, to generate the System Clk output. Divide by 64 is selected by setting these bits to '0'.

b9-b0 divide System Clk PLL VCO clock by the value set in these bits as feedback to the PLL phase detector (PD); when the PLL is stable, this will be the same frequency as the internal reference as set by b8-b0 of the System Clk Reference and Source Configuration register ($AC). Divide by 1024 is selected by setting these bits to '0'.

9.1.7 System Clk REF - $AC write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Select & PS Clock Sources					OP Slew		Ref Clock Divide Ratio <8-0>								

b15,12,11 Clk output divider source

SYSCLK Source	b15	b12	b11
Xtal	0	x	x
Sys Clk PLL	1	0	0
Main PLL	1	0	1
Reserved: <do not use>	1	1	x

b14 Powersave PLL 0 = powersave 1 = enabled

b13 Powersave Output Divider 0 = powersave / bypass 1 = enabled

b10-9 Output Slew Rate

b10	b9	Output Slew Rate
0	0	normal
0	1	slow
1	X	fast

b8-b0 Reference Clk divide value. Divide by 512 is selected by setting these bits to '0'.

Note that on power-up, or after a General Reset, the default settings will not provide a SYSCLK output. To set SYSCLK to the XTAL frequency it is first necessary to write a '1' to bit 10 of the System CLK PLL data register ($AB) and also write a '1' to bit 13 of the System CLK REF register ($AC). This will set SYSCLK to the XTAL frequency and also make the signal available on the SYSCLK pin.

9.1.8 Analogue Input Gain - $B0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	DISC Input Gain			0	0	DISC select	MIC Input Gain			Rx/Tx	

b15 to 11 reserved – clear to 0

b10	b9	b8	DISC Input Gain
b4	b3	b2	MIC Input Gain
0	0	0	0dB
0	0	1	3.2dB
0	1	0	6.4dB
0	1	1	9.6dB
1	0	0	12.8dB
1	0	1	16.0dB
1	1	0	19.2dB
1	1	1	22.4dB

b7 to 6 are reserved - clear to 0

b5 DISCselect: 0 – select DISCN1 input only

1 – select DISCN2 input (does NOT disconnect DISCN1 input)

b1	b0	Rx/Tx
0	0	Idle
0	1	Idle
1	0	Rx
1	1	Tx

Note that b1, b0 of this register control the routing of the signal to the processing blocks, whereas b1, b0 of the Mode register ($C1) control the processing functions of the device. BOTH registers MUST be set appropriately for the device to operate correctly in Rx or Tx modes.

9.1.9 Analogue Output Gain - $B1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUDIO Output Gain			MOD Output Gain			DISC-AUDIO Bypass				MIC-MOD Bypass				0	0

b15	b14	b13	AUDIO Output Gain
b12	**b11**	**b10**	**MOD Output Gain**
0	0	0	mute
0	0	1	-19.2dB
0	1	0	-16.0dB
0	1	1	-12.8B
1	0	0	-9.6dB
1	0	1	-6.4dB
1	1	0	-3.2dB
1	1	1	0dB

b9	b8	b7	b6	DISC-AUDIO Bypass Gain
b5	**b4**	**b3**	**b2**	**MIC-MOD Bypass Gain**
0	0	0	0	mute
0	0	0	1	-22.4dB
0	0	1	0	-19.2dB
0	0	1	1	-16.0dB
0	1	0	0	-12.8dB
0	1	0	1	-9.6dB
0	1	1	0	-6.4dB
0	1	1	1	-3.2dB
1	0	0	0	0dB
1	0	0	1	3.2dB
1	0	1	0	6.4dB
1	0	1	1	9.6B
1	1	0	0	12.8dB
1	1	0	1	16.0dB
1	1	1	0	19.2dB
1	1	1	1	22.4dB

Bits 1, 0 are reserved – clear to 0

9.1.10 AuxADC Threshold Data - $B5 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC sel	Hi /Lo	0	0	0	0	Aux ADC Threshold Data									

b15 AuxADC select 0 = AuxADC 1 = reserved – do not use
b14 high/low select 0 = low threshold 1 = high threshold
b13 *reserved* 0
b12 *reserved* 0
b11 *reserved* 0
b10 *reserved* 0
b9 –b0 threshold data

9.1.11 Power Down Control - $C0 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISC Input	MIC Input	Input ENA	AUD Gain	MOD Gain	AUD ENA	0	MOD ENA	0	BIAS	Reset	Prot	XTAL DIS	DISC bypass	MIC bypass	0

b15 DISC Input/Gain block enable 0 = off 1 = enabled
b14 MIC Input/Gain block enable 0 = off 1 = enabled
b13 Input amp enable 0 = off 1 = enabled
b12 AUD Gain block enable 0 = off 1 = enabled
b11 MOD Gain block enable 0 = off 1 = enabled
b10 AUD Output enable 0 = off 1 = enabled
b9 reserved must be cleared to 0
b8 MOD Output enable 0 = off 1 = enabled
b7 reserved must be cleared to 0
b6 BIAS block enable 0 = off 1 = enabled
b5 Reset 0 = normal 1 = reset/powersave
b4 Program Block Protect 0 = normal 1 = protected
If cleared, the Program Blocks will be initialised on Power on or Reset. If set, then the Program Blocks will retain their previous contents.
b3 XTAL disable 0 = enabled 1 = disabled/powersave
Setting this bit effectively stops all signal processing within the device.
b2 DISC bypass gain 0 = disabled / powersave 1 =enabled
b1 MIC bypass gain 0 = disabled / powersave 1 =enabled
b0 reserved must be cleared to 0

Note: Care should be taken when writing to b5 and b3. These are automatically programmed to an operational state following a power-on (ie: all 0's). Writing a 1 to either b5 or b3 will effectively cause the device to cease all processing activity, including responding to other C-BUS commands (except General Reset, $01).

When b5 is set, the device will be held in reset and all signal processing will cease (including AuxADC operation.

When b3 is set the Xtal is disabled. When b3 is subsequently cleared, it may take some time for the clock signal to become stable, hence care should be taken in using this feature.

9.1.12 Mode Control – $C1 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Audio	0	0	0	In-band modes		0	0	Sub Audio Mode		0	0	0	Idle/Rx/Tx	

b15	*reserved*	0	
b14	Audio processing enable	0 = off	1 = enabled
b13-11	*reserved*	0	
b10	Audio Tone enable	0 = off	1 = enabled
b9	In-band Tone enable	0 = off	1 = enabled
b8,7	*reserved*	0	
b6	CTCSS enable	0 = off	1 = enabled
b5	DCS enable	0 = off	1 = enabled
b4-2	*reserved*	0	
b1, b0	Operational Mode	00 IDLE	
		01 Rx	
		10 Tx	
		11 *reserved*	

Changes to the settings of the bits in this register are implemented as soon as they are received over the C-BUS (note that the C-BUS has a potential latency of up to 250µs).

In Tx mode, it is only permissible to select ONE of the following at any time:
Audio Tone
In-band Tone

It is essential that changes to the Program Register and the Audio Control register are completed before entering Rx or Tx mode. It is possible, however, to change the CTCSS tone whilst in Tx mode if the CTCSS enable bit is set in the Mode Control Register. DCS codes and custom CTCSS tones cannot be updated in Tx mode.
The following other registers or bits can be changed as appropriate (Note: not all possible changes are appropriate), whilst the device is in Tx or Rx mode:

- Analogue Input Gain - $B0 write
- AuxADC and TX MOD Mode - $A7 write
- Analogue Output Gain - $B1 write
- Power Down Control - $C0 write
- Tx In-band Tone - $C3 write
- Audio Tone - $CD: 16-bit write
- Scrambler Inversion Frequency – $CB write
- Interrupt Mask - $CE write

9.1.13 Audio Control – $C2 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
scra-mble	comp	emph	12k5	25k	hpf	CTCSS Phase		Sub Audio Tone Number: CTCSS/DCS/none							

b15	Audio Scrambling enable	0 = off	1 = enabled
b14	Audio Compandor enable	0 = off	1 = enabled
b13	Audio Pre/De-emphasis	0 = off	1 = enabled
b12	Audio 12.5kHz Filter enable	0 = off	1 = enabled
b11	Audio 25kHz Filter enable	0 = off	1 = enabled
b10	Audio 300Hz HPF enable	0 = off	1 = enabled
b9, b8	CTCSS Phase	00 0 degrees (normal)	
		01 120 degrees	
		10 180 degrees	

		11	240 degrees
b7 – b0	Sub-Audio Tone number (dec)	0	no tone
		1 to 83	select DCS code 1 to 83
		84	select User Defined DCS code
		101 to 183	select DCS tone 1 to 83 inverted
		184	select User Defined DCS code inverted
		200	select Tone Clone™ mode
		201 to 251	select CTCSS tone 1 to 51
		252	select User Defined CTCSS tone
		253	select XTCSS maintenance tone
		254	select DCS turn-off tone
		255	Invalid tone

See Table 3. Selecting the 'DCS turn-off tone (254)' during DCS transmit will cause the DCS turn off tone to be transmitted. CTCSS does not need to be enabled in the Mode Control register to receive the 'DCS turn off tone'.

If the Tone Clone™ mode is selected this allows the device in Rx to non-predictively detect any CTCSS frequency in the range of valid tones, the received tone number will be reported in the Tone Status register ($CC) and the CTCSS decoder detection bandwidth should be set to its lowest value (P2.1).

9.1.14 Tx In-band Tone - $C3 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx In-band tone					0	0	0	0	0	0	0	0	0	0	0

b15-11 In-band Tone, see Table 6 In-band Tone in the Datasheet.
b10-6 reserved, clear to '0'.
b5-0 0.

9.1.15 Status – $C6 read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	0	Rx in	0	CTCSS	DCS	0	Aux ADC	0	0	0	0	0	0	0	PRG

b15 IRQ
Changes in the Status register will cause this bit to be set to 1 if the corresponding interrupt mask bit is enabled. An interrupt request is issued on the IRQN pin when this bit is 1 and the IRQ MASK bit (b15 of Interrupt Mask register, $CE) is set to 1.
b14 reserved
b13 In-band Tone event
The Tone Status register $CC should be read to determine the exact cause. Cleared to 0 in Tx.
b12 reserved
b11 CTCSS event
A CTCSS code has been detected or ceased. The Tone Status register $CC should be read to determine the exact cause. Cleared to 0 in Tx.
b10 DCS event
A DCS code has been detected or ceased. The Tone Status register $CC should be read to determine the exact cause. Cleared to 0 in Tx.
b9 reserved
b8 AuxADC Threshold change
AUX ADC signal has just gone above the high threshold or has just gone below the low threshold The AuxADC data register $A9 should be read to determine the exact cause.
b7 *reserved*
b6 *reserved*
b5 *reserved*
b4 *reserved*

b3 *reserved*
b2 *reserved*
b1 *reserved*
b0 Program Register Ready
When set to 1, this bit indicates that the Program Register, $C8 is available for the host to write to it. Cleared by writing to the Programming Register, $C8.

Bits 2 to 15 of the Status register are cleared to '0' after the Status register is read. Detection of the DCS turn off tone and removal of the DCS code are both flagged as DCS events in the Status register, not as CTCSS events.

The data in this register is not valid if bit 5 of the Power-Down Control register, $C0 is set to 1.

9.1.16 Programming – $C8 write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Program Block Address				Program Block Data											

See section 9.2 for a definition of programming block operation.

9.1.17 Scrambler Inversion Frequency – $CB write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Scrambler Inversion Frequency													

Bits 13-0 set the inversion frequency of the audio scrambler. By default this is set to 3300Hz with the value $2333. The value of this field can be calculated by: V= (f_{inv} / 0.7324) *2.

Other common values are:

f_{inv}	$CB register (hex)	
3000	2000	
3100	2111	
3200	2222	
3300	**2333**	**default**
3400	2444	

Note that this register can be changed whilst in Rx or Tx mode.

9.1.18 Tone Status - $CC read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tone Detected					x	x	x	Detected DCS or CTCSS code							

This word holds the current status of the CMX138A sub-audio and In-band tone sections. This word should be read by the host after an interrupt caused by a DCS, CTCSS or In-band tone event. In Tx mode this register will be cleared to '0'.

b15-11 Detected In-band frequency; identifies the frequency by its position in Table 6 In-band Tone. A change in the state of bits 15 to 11 will cause bit 13 of the Status register ($C6), 'In-band State Change', to be set to '1'.

b10-8 *reserved*

b7–0 Detected DCS or CTCSS code, identifies the detected sub-audio tone by its position in Table 3 DCS Codes and CTCSS Tones.

9.1.19 Audio Tone - $CD: 16-bit write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Audio Tone											
0	0	1	0	Audio Tone Level											
0	1	0	0	Voice Level											
0	1	1	0	Output1 Fine Gain (also see P4.2)											
1	0	0	0	Output2 Fine Gain (also see P4.3)											
1	0	1	0	Tx Voice level multiplier											
1	0	1	1	*reserved*											
1	1	0	0	*reserved*											
1	1	0	1	Tx Sub-audio level											
1	1	1	0	*reserved*											
1	1	1	1	*reserved*											
				All other values reserved											

Bits 15-12 determine how the remaining bit fields will be interpreted:

0000_b:

When the appropriate bits of the Mode Control register ($C1, b10) are set an audio tone will be generated with the frequency set by bits (11-0) of this register in accordance with the formula below. If bits 11-0 are programmed with '0' no tone (i.e. Vbias) will be generated when the Audio Tone is enabled.

Frequency = Audio Tone (i.e. 1Hz per LSB)

The Audio Tone frequency should only be set to generate frequencies from 300Hz to 3000Hz.

The host should disable other Audio band signalling and set the correct audio routing before generating an audio tone and re-enable signalling and audio routing on completion of the audio tone. The timing of intervals between these actions is controlled by the host µC.

This register may be written to whilst the audio tone is being generated, any change in frequency will take place after the end of the C-BUS write to this register. This allows complex sequences (e.g. ring or alert tunes) to be generated for the local speaker (Tx or Rx via the AUDIO pin) or transmitted signal (Tx via the MOD pins).

0010_b:

The Audio Tone Level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. Note that this adjustment will also affect the In-Band tone generator. This register operates in parallel with P1.0, but allows the level to be adjusted “on-the-fly” without needing to drop back into Idle mode.

0100_b:

In Rx mode, the Voice Level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. Note that this adjustment will only affect signals in the Voice processing path as enabled by Mode Control register ($C1, b14) in Rx. This allows the Voice level to be adjusted “on-the-fly” and in conjunction with the Audio Output attenuator ($B0, b3-0), offers a “fine gain” volume control. Approximate values for 0.2dB steps are shown in Table 9.

b11-0 Value (hex)	Attenuation (dB)	b11-0 Value (hex)	Attenuation (dB)
FFF	0	D50	1.6
F90	0.2	CF0	1.8
F40	0.4	CB0	2.0
EE0	0.6	C60	2.2
EA0	0.8	C20	2.4
E50	1.0	BF0	2.6
DE0	1.2	BA0	2.8
DA0	1.4	B60	3.0

Table 9 Voice Level Attenuation

0110_b:

The Output1 (AUDIO) level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. This register operates in parallel with P4.2, but allows the level to be adjusted “on-the-fly” without needing to drop back into Idle mode.

b11-0 Value (hex)	Attenuation (dB)	b11-0 Value (hex)	Attenuation (dB)
FFF	0	CB5	2.0
FA2	0.2	C6B	2.2
F47	0.4	C22	2.4
EEE	0.6	BDC	2.6
E97	0.8	B97	2.8
E42	1.0	B53	3.0
DEF	1.2	B11	3.2
D9D	1.4	AD1	3.4
D4E	1.6	AB1	3.5
D01	1.8		

Table 10 Voice Level Attenuation

Gain = 20 x log(OG / 4095)dB. OG is the unsigned integer value in the ‘Output Fine Gain’ field.

(Please note that differences between the calculated values and measured levels are due to truncation of the programmed values).

1000_b:

The Output2 (MOD) level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. This register operates in parallel with P4.3, but allows the level to be adjusted “on-the-fly” without needing to drop back into Idle mode. Also, see Table 10.

1010_b:

This sets the value of the Tx Voice level multiplier at the output of the Tx limiter stage. This can be useful in situations where it has been necessary to use a small limiting threshold and still maintain an acceptable level at the MOD outputs. The default state is x1.

b2	b1	b0	Tx Voice Level Multiplier
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	0	0	x16
1	0	1	x32

1101_b:

The Sub- Audio Tone Level may be attenuated by the value written to b11-0. The default value of $FFF is equivalent to x1. This register operates in parallel with P2.0, but allows the level to be adjusted “on-the-fly” without needing to drop back into Idle mode.

9.1.20 Interrupt Mask - $CE write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	0	Rx in	0	CTCSS	DCS	0	Aux ADC	0	0	0	0	0	0	0	PRG

Bit	Value	Function
15	1	Enable selected interrupts
	0	Disable all interrupts (IRQN pin not activated)
14	0	*reserved*
13	1	Enable interrupt when a change to a In-band tone is detected
	0	Disabled
12	0	*reserved*
11	1	Enable interrupt when a change to CTCSS tone is detected
	0	Disabled
10	1	Enable interrupt on a change in the detect status of the DCS decoder
	0	Disabled
8	1	Enable interrupt when the AuxADC status changes
	0	Disabled
7	0	*reserved*
6	0	*reserved*
5	0	*reserved*
4	0	*reserved*
3	0	*reserved*
2	0	*reserved*
1	0	*reserved*
0	1	Enable interrupt when Prog Flag bit of the Status register changes from '0' to '1' (see Programming register $C8)
	0	Disabled

To minimise the processing load on the host µC, it is advisable to only enable the interrupts that are relevant for any given operational mode.

9.1.21 Reserved - $CF write

This C-BUS address is allocated for production testing and must not be accessed in normal operation.

9.2 Programming Register Operation

In order to support radio systems that may not comply with the default settings of the CMX138A, a set of program register blocks is available to customise the features of the device. It is envisaged that these blocks will only be written to following a power-on of the device and hence can only be accessed while the device is in Idle mode. Access to these blocks is via the Programming register ($C8).

All other interrupt sources should be disabled while loading the program register blocks.

The Programming register should only be written to when the Programming Flag bit (bit 0) of the Status register is set to 1 and the Rx and Tx modes are disabled (bits 0 and 1 of the Mode Control register both '0'). The Programming Flag is cleared when the Programming register is written to by the host. When the corresponding programming action has been completed (normally within 250µs) the CMX138A will set the flag back to 1 to indicate that it is now safe to write the next programming value. The Programming register must not be written to while the Programming Flag bit is 0. Programming is performed by writing a sequence of 16-bit words to the Programming register in the order shown in the following tables. Writing data to the Programming register MUST be performed in the order shown for each of the blocks, however the order in which the blocks are written is not critical. If later words in a block do not require updating the user may stop programming that block when the last change has been performed. e.g: If only 'Fine Output Gain 1' needs to be changed the host will need to write to P4.0, P4.1 and P4.2 only.

The user must not exceed the defined word counts for each block. P4.8 is allocated for production testing and must not be accessed in normal operation.

The high order bits of each word define which block the word belongs to, and if it is the first word of that block:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11 – Bit 0
1	x	x	x	1st data for each block
0	x	x	x	2nd and following data
x	1	0	0	Write to block 0 (12 bit words)
x	1	0	1	Write to block 1 (12 bit words)
x	1	1	0	Write to block 2 (12 bit words)
x	1	1	1	Write to block 3 (12 bit words)
x	0	Write to block 4 (14 bit words)		

9.2.1 Program Block 0 – reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

9.2.2 Program Block 1 – In-band Tone Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio Band Tones Tx Level											Emph
P1.1	0	1	0	1	0	0	Audio Band Detect Threshold						In-band Tone Detect Bandwidth			
P1.2	0	1	0	1	User Programmable In-band Tone											

Default values: P1.0: $800
P1.1: $009
P1.2 $942 (1750Hz)

$C8 (P1.0) Audio Band Tones Tx Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.0	1	1	0	1	Audio Band Tones/data Tx Level											Emph

Bits 11 (MSB) to 1 (LSB) set the transmitted In-band tone, Audio Tone (pk-pk) with a resolution of AV_{DD}/2048 per LSB (1.611mV per LSB at AV_{DD} =3.3V). Valid range for this value is 0 to 1536 – use with care as higher values may result in signal "clipping".

Bit 0 controls In-band tone de-emphasis. When In-band tones are enabled in the Mode Control register ($C1), de/pre-emphasis is enabled in the Audio Control register ($C2) and this bit (b0) is set to '1'; signals going to the In-band tone detector are de-emphasised in accordance with Figure 7 of the datasheet. This combination of settings should only be used in Rx mode. If this bit is set, then in Tx mode, the user is advised to clear the de/pre-emphasis bit in the Audio Control register ($C2).

$C8 (P1.1) In-band tone Detect Bandwidth and Audio Band Detect Threshold

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.1	0	1	0	1	0	0	Audio Band Detect Threshold						In-band Tone Detect Bandwidth			

The 'detect threshold' bits (bits 9 to 4) set the minimum In-band tone signal level that will be detected. The levels are set according to the formula:

$$\text{Minimum Level} = \text{Detect Threshold} \times 3.993\text{mV rms at } AV_{DD} = 3.3\text{V}$$

The In-band tone detected bandwidth is set in accordance with the following table:

					BANDWIDTH	
	Bit 3	Bit 2	Bit 1	Bit 0	Will Decode	Will Not Decode
	1	0	0	0	±1.1%	±2.4%
Recommended for EEA ⇒	**1**	**0**	**0**	**1**	**±1.3%**	**±2.7%**
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%

$C8 (P1.2) User-Programmable In-band Tone

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1.2	0	1	0	1	Programmable In-band Tone											
					N (see below)							R (see below)				

This word set the programmable In-band tone used in transmit and receive. The frequency is set in bits 11-0 according to the formula:

N = Integer part of (0.042666 x frequency)

R = (0.042666 x frequency - N) x 6000 / frequency (round to nearest integer).

Example: For 1010Hz, N = 43, R = 1. The programmed tones must only be set to frequencies from 288Hz to 3000Hz (R MUST NOT exceed 31 decimal).

9.2.3 Program Block 2 – CTCSS and DCS Setup

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Tx Level											
P2.1	0	1	1	0	DCS 24	0	CTCSS and DCS Detect Threshold						CTCSS Detect Bandwidth			
P2.2	0	1	1	0	User Defined DCS Code bits 11 – 0											
P2.3	0	1	1	0	User Defined DCS Code bits 23/22 – 12											
P2.4	0	1	1	0	User Defined CTCSS code N						User Defined CTCSS Code R					
P2.5	0	1	1	0	Sub-audio Drop-out Time				0							
P2.6	0	1	1	0	*reserved*											

Default values:

P2.0	$800	P2.3	$000
P2.1	$008	P2.4	$000
P2.2	$000	P2.5	$000
		P2.6	$000

$C8 (P2.0) CTCSS and DCS TX LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.0	1	1	1	0	CTCSS and DCS Level											

Bits 11 (MSB) to 0 (LSB) set the transmitted CTCSS or DCS sub-audio signal level (pk-pk) with a resolution of AV_{DD}/16384 per LSB (0.201mV per LSB at AV_{DD} =3.3V, giving a range 0 to 824.8mV pk-pk).

$C8 (P2.1) CTCSS TONE BW AND LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.1	0	1	1	0	DCS 24	0	CTCSS and DCS Detect Threshold						CTCSS Detect Bandwidth			

Bit 11, DCS 24: When this bit is set to '1' 24 bit DCS codes are transmitted and decoded. When this bit is cleared to '0' 23 bit codes are used.

The 'detect threshold' bits (bits 9 to 4) set the minimum CTCSS or DCS signal level that will be detected. The levels are set according to the formula:

CTCSS Minimum Level = Detect Threshold × 2.2mV rms at AV_{DD} = 3.3V or

DCS Minimum Level = Detect Threshold × 6.22mV pk-pk at AV_{DD} = 3.3V

The CTCSS detected tone bandwidth is set in accordance with the following table:

	Bit 3	Bit 2	Bit 1	Bit 0	BANDWIDTH Will Decode	BANDWIDTH Will Not Decode
Recommended for use with split tones and Tone Clone™	0	1	1	0	±0.5%	±1.8%
	0	1	1	1	±0.8%	±2.1%
Recommended for CTCSS ⇒	**1**	**0**	**0**	**0**	**±1.1%**	**±2.4%**
	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%

$C8 (P2.2-3) DCS CODE (LOWER) and DCS CODE (UPPER)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.2	0	1	1	0	DCS Data (bits 11-0)											
P2.3	0	1	1	0	DCS Data (bits 23/22-12)											

These words set the User Defined DCS code to be transmitted or searched for. The least significant bit (bit 0) of the DCS code is transmitted or compared first and the most significant bit is transmitted or compared last. Note that DCS Data bit 23 is only used when bit 11 (DCS 24) of P2.1 is set to '1'.

$C8 (P2.4) User Defined CTCSS Tone

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.4	0	1	1	0	User Defined CTCSS code N						User Defined CTCSS Code R					

Calculate the values of N and R for the desired CTCSS frequency by:

N = integer (0.24 * User Frequency)

R = round (((0.24 * User Frequency) – N) * 3000 / User Frequency) + 0.5

Eg: for 150.1Hz, N=36, R=1 so P2.4 = $6901

$C8 (P2.5) Sub-audio Drop Out Time

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.5	0	1	1	0	Sub-audio Drop Out Time				0							

The Sub-audio Drop Out Time defines the time that the sub-audio signal detection can drop out before loss of sub-audio is asserted. The period is set according to the formula:

Time = Sub-audio Drop Out Time × 8.0ms [range 0 to 120ms]

The setting of this register defines the maximum drop out time that the device can tolerate. The setting of this register also determines the de-response time, which is typically 90ms longer than the programmed drop out time.

$C8 (P2.6) Reserved – do not access

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P2.6	0	1	1	0	*reserved* – set to $000											

9.2.4 Program Block 3 – AuxDAC, RAMDAC and Clock Control:

This block is divided into two sub-blocks to facilitate loading the RAMDAC buffer. Set bit 15 to restart a loading sequence. If bit 10 is set then loading the first ten locations will be skipped. If bit 10 is clear, the first ten locations must be loaded before continuing to the RAMDAC load.

The Internal clk dividers only require modification if a non-standard XTAL frequency is used (see Table 2).

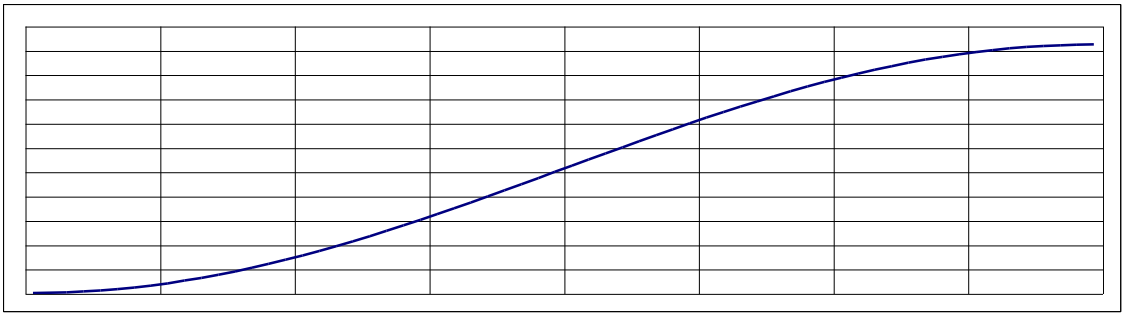
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P3.0	1	1	1	1	0	0	AuxADC Average Counter									
P3.1	0	1	1	1	0	0	Reserved – set to 000									
P3.2	0	1	1	1	0	0	GP Timer value in Idle mode									
P3.3	0	1	1	1	0	0	VCO output and AUX clk divide in Idle mode									
P3.4	0	1	1	1	0	0	Ref clk divide in Rx or Tx mode									
P3.5	0	1	1	1	0	0	PLL clk divide in Rx or Tx mode									
P3.6	0	1	1	1	0	0	VCO output and AUX clk divide in Rx or Tx mode									
P3.7	0	1	1	1	0	0	Internal ADC / DAC clk divide in Rx or Tx mode									
P3.8	0	1	1	1	0	0	AuxADC Internal Control 1									
P3.9	0	1	1	1	0	0	AuxADC Internal Control 2									
P3.10	0	1	1	1	0	0	AuxADC Internal Control 3									
P3.11	1	1	1	1	0	1	User Defined RAMDAC data 0									
P3.12	0	1	1	1	0	1	User Defined RAMDAC data xx									
P3.74	0	1	1	1	0	1	User Defined RAMDAC data 63									

Default Values:

P3.0	$000
P3.1	$000
P3.2 - P3.7:	see Table 2
P3.8	$000 - do not change this value
P3.9	$101 - do not change this value
P3.10	$002 - do not change this value
P3.11 - P3.74:	see Table 11

Table 11 RAMDAC Values

Default DAC RAM Contents After Reset (hexadecimal)															
0 000	1 001	2 003	3 006	4 00A	5 010	6 017	7 01F	8 028	9 033	10 03E	11 04B	12 059	13 068	14 078	15 089
16 09A	17 0AD	18 0C1	19 0D5	20 0EA	21 100	22 116	23 12D	24 145	25 15D	26 175	27 18E	28 1A7	29 1C0	30 1D9	31 1F3
32 20C	33 226	34 23F	35 258	36 271	37 28A	38 2A2	39 2BA	40 2D2	41 2E9	42 2FF	43 315	44 32A	45 33E	46 352	47 365
48 376	49 387	50 397	51 3A6	52 3B4	53 3C1	54 3CC	55 3D7	56 3E0	57 3E8	58 3EF	59 3F5	60 3F9	61 3FC	62 3FE	63 3FF



9.2.5 Program Block 4 – Gain and Offset Setup:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain													
P4.1	0	0	*reserved* - clear to '0'													
P4.2	0	0	Fine Output Gain 1 - AUDIO													
P4.3	0	0	Fine Output Gain 2 - MOD													
P4.4	0	0	Output 1 Offset Control - AUDIO													
P4.5	0	0	Output 2 Offset Control - MOD													
P4.6	0	0	Ramp Rate Control													
P4.7	0	0	Limiter Setting (all '1' s = V_{BIAS} +/- AV_{DD} / 2)													
P4.8	0	0	*reserved*													
P4.9	0	0	Audio Filter Sequence													
P4.10	0	0	*reserved*													
P4.11	0	0	Input AGC threshold level													

Default values:

P4.0	$8000	P4.6	$0000
P4.1	$0000	P4.7	$3FFF
P4.2	$0000	P4.8	$119A
P4.3	$0000	P4.9	$004B
P4.4	$0000	P4.10	$0608
P4.5	$0000	P4.11	$0FFF

$C8 (P4.0) Fine Input Gain

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.0	1	0	Fine Input Gain (unsigned integer)													

Gain = 20 × log([32768-IG]/32768)dB. IG is the unsigned integer value in the 'Fine Input Gain' field.

Fine input gain adjustment should be kept within the range 0 to -3.5dB. This adjustment occurs after the coarse input gain adjustment (register $B0). This setting affects both MIC and DISC inputs.

$C8 (P4.1) Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.1	0	0	*reserved* - clear to '0'													

This register is reserved and should be cleared to '0'.

$C8 (P4.2-3) Fine Output Gain 1 and Fine Output Gain 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.2	0	0	Fine Output Gain 1 – AUDIO (unsigned integer)													
P4.3	0	0	Fine Output Gain 2 – MOD (unsigned integer)													

Gain = 20 × log([32768-OG]/32768)dB. OG is the unsigned integer value in the 'Fine Output Gain' field.

Fine output gain adjustment should be kept within the range 0dB to -3.5dB ($000 to $2A73). This adjustment occurs before the coarse output gain adjustment (register $B1). Alteration of Fine Output Gain 1 will affect the gain of the AUDIO output, and Fine Output Gain 2 will affect the MOD output.

b13-0 Value (hex)	Attenuation (dB)	b13-0 Value (hex)	Attenuation (dB)
0	0	1A53	2.0
2EA	0.2	1CA4	2.2
5C3	0.4	1EE7	2.4
88B	0.6	211D	2.6
B43	0.8	2346	2.8
DEB	1.0	2562	3.0
1084	1.2	2772	3.2
130E	1.4	2976	3.4
1589	1.6	2A74	3.5
17F5	1.8		

Table 12 Voice Level Attenuation

(Please note that differences between the calculated values and measured levels are due to truncation of the programmed values).

$C8 (P4.4-5) Output 1 Offset and Output 2 Offset

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.4	0	0	2's Complement Offset for Output 1 (AUDIO), Resolution = AV_{DD} / 65536 per LSB													
P4.5	0	0	2's Complement Offset for Output 2 (MOD), Resolution = AV_{DD} / 65536 per LSB													

The Programmed value is subtracted from the output signal. Can be used to compensate for inherent offsets in the output path via AUDIO (Output 1 Offset) and MOD (Output 2 Offset). It is recommended that the offset correction is kept within the range +/-50mV. This adjustment occurs before the coarse output gain adjustment (register $B1), therefore an alteration to the latter register will require a compensation to be made to the output offsets.

$C8 (P4.6) Ramp Rate Control

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.6	0	0	Ramp Rate Up Control (RRU)							Ramp Rate Down Control (RRD)						

The MOD ramp-up and ramp-down rates can be independently programmed and enabled (via bits 0,1 of register $A7). The ramp rates should be programmed before ramping any outputs.

Time to ramp-up to full gain = (1 + RRU) × 1.333ms
Time to ramp down to zero gain = (1 + RRD) × 1.333ms

Ramp up starts from when the transmit mode starts (Mode Control Register bit 1 set = '1'). Ramp down starts from when transmit mode is turned off (Mode Control Register bit 1 cleared = '0').

$C8 (P4.7) Transmit Limiter Control

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.7	0	0	Limiter Setting, Resolution = AV_{DD} / 16384 per LSB													

This unsigned number sets the clipping point (maximum deviation from the centre value) for the MOD output. The maximum setting ($3FFF) is $V_{BIAS} \pm (AV_{DD}/2)$ i.e. output limited from 0 to AV_{DD}.

The limiter is set to maximum following a C-BUS Reset or a Power-Up Reset. The levels of internally generated signals may need to be adjusted by setting appropriate transmit levels to avoid un-intentional limiting. The limiter is active whenever either of the 12.5 or 25kHz Channel filters are selected (both in Rx or Tx).

$C8 (P4.8) Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.8	0	0	*reserved* – set to $119A													

Reserved – set to $119A

$C8 (P4.9) Audio Filter sequence

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.9	0	0	lim	src	Input AGC				Pre-emp		Comp		Scramble		300Hz	

b13 selects the hard limiter in the audio processing path when set to 1, instead of the default soft Limiter.

b12 sets the source of the reference signal when InputAGC function is active.

0 = Audio Input
1 = Pre-emphasis output

b11-8 control the hardware InputAGC function and its release timer for Voice/Audio signals on Input 1 in 64ms steps:

0000	InputAGC off
0001	InputAGC on, release time = 64ms
0010	InputAGC on, release time = 128ms
0011	InputAGC on, release time = 196ms
0100	InputAGC on, release time = 256ms
0101	InputAGC on, release time = 320ms
- - - -	- -
1111	InputAGC on, release time = 960ms

b7-0 set the order of the Audio Filter processing. This feature can be used to optimise the signal to noise performance of particular radio hardware designs. Each filter/process block can be specified in any order. Each two-bit field specifies the order in which the process will be executed in Tx mode, therefore it is imperative that each set of bit fields be different. The reverse sequence is used in Rx mode. The voice filter and soft limiter will always be implemented as the final block in the Tx sequence.

The default settings are:

- Pre-emphasis: 01 (pre-emphasis in position 1)
- Compandor: 00 (Compandor in position 0)
- Scramble: 10 (Scrambler in position 2)
- 300Hz HPF: 11 (HPF in position 3)

which will implement the line-up as shown in Figure 16 and Figure 17.

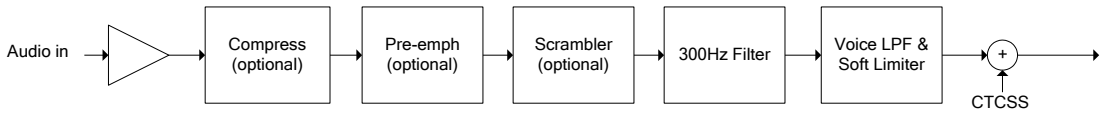


Figure 16 Default Tx Audio Filter Line-up

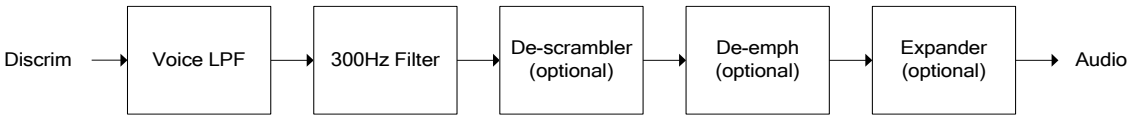


Figure 17 Default Rx Audio Filter Line-up

$C8 (P4.10) Reserved

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.10	0	0	*reserved* – set to $0608													

Reserved – set to $0608

$C8 (P4.11) Input AGC Threshold Level

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4.11	0	0	Threshold Level													

This unsigned hex number sets the threshold level for the Input AGC function.
Default is $0FFF = $V_{BIAS} \pm AV_{DD}/4$.

9.2.6 Initialisation of the Programming Register Blocks:

Removal of the Signal Processing block from reset (Power-Down register $C0 b5 1→ 0), with the Protect Bit (Power-Down register $C0 b4 = 0) kept low, will cause all of the Programming register words (P0 – P4) to be reset to their default values.

10 Application Notes

11 Performance Specification

11.1 Electrical Performance

11.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD} - DV_{SS}	–0.3	4.5	V
AV_{DD} - AV_{SS}	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS}	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

E1 Package (28-pin TSSOP)	Min.	Max.	Unit
Total Allowable Power Dissipation at Tamb = 25°C	–	1100	mW
… Derating	–	11.1	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

11.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
V_{DEC} – DV_{SS}	12	2.25	2.75	V
Operating Temperature		–40	+85	°C
XTAL/CLK Frequency (using a Xtal)	11	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	11	3.0	24.576	MHz

Notes: 11 Nominal XTAL/CLK frequency is 6.144MHz.
12 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.

11.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.01% (100ppm); Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Input stage gain = 0dB. Output stage attenuation = 0dB.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
AI_{DD} + DI_{DD} (AV_{DD} = 3.3V, DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	35	120	µA
AI_{DD} only (AV_{DD} = 3.3V)		–	4	–	µA
IDLE Mode	22				
AI_{DD} + DI_{DD} (AV_{DD} = 3.3V, DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	1.0	–	mA
AI_{DD} only (AV_{DD} = 3.3V)		–	35	–	µA
Rx Mode	22				
AI_{DD} + DI_{DD} (AV_{DD} = 3.3V, DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	7.0	–	mA
AI_{DD} only (AV_{DD} = 3.3V)		–	3.2	–	mA
Tx Mode	22				
AI_{DD} + DI_{DD} (AV_{DD} = 3.3V, DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	8.5	–	mA
AI_{DD} only (AV_{DD} = 3.3V)		–	3.3	–	mA
Additional Current for Auxiliary System Clock (output running at 6.144MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	538	–	µA
Additional Current for Auxiliary ADC					
AI_{DD} (AV_{DD} = 3.3V)		–	290	–	µA
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	20	–	µA
Additional Current for Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	215	–	µA
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	4	–	µA

Notes: 21 Tamb = 25°C, not including any current drawn from the device pins by external circuitry.
22 System clocks, auxiliary circuits, audio scrambler, compander and pre/de-emphasis disabled, but all other digital circuits (including the Main Clock PLL) enabled. A single analogue path is enabled through the device.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	25				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')		–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 120µA)		90%	–	–	DV_{DD}
(I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = 360µA)		–	–	10%	DV_{DD}
(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output impedance		–	22	–	kΩ

Notes: 25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' pulse width		31	15	–	–	ns
'Low' pulse width		31	15	–	–	ns
Input impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal start up (from powersave)			–	20	–	ms
Auxiliary System Clk Output						
XTAL/CLK input to CLOCK_OUT timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' pulse width		33	76	81.38	87	ns
'Low' pulse width		33	76	81.38	87	ns
V_{BIAS}						
Start up time (from powersave)			–	30	–	ms
Microphone, Discriminator Inputs (MIC, DISC)						
Input Impedance		34	–	> 10	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage gain (I/P = 1mV rms at 100Hz)			–	80	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz XTAL fitted and 6.144MHz output selected.

34 With no external components connected, measured at dc.

35 Centered about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, or MICFB

37 Design value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Output and Audio Output (MOD, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance Enabled	42	–	6	–	Ω
Output Impedance Disabled	42	–	200	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±3.5	mA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		300	–	–	Ω
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance Enabled	42	–	6	–	Ω
Output Impedance Disabled	42	–	200	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±3.5	mA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		300	–	–	Ω

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at 1kHz, AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADC					
Resolution	55	–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	62.4	–	µs
Input Impedance					
Resistance		–	100	–	kΩ
Capacitance		–	5	–	pF
Zero Error	56	0	–	±20	mV
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±2	LSBs
Auxiliary 10 Bit DAC					
Resolution	55	–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error	57	0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±2	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

55 Designed for 10-bit accuracy, but only 8-bit accuracy is guaranteed

56 Input offset from a nominal V_{BIAS} input, which produces a $0200 ADC output.

57 Output offset from a $0200 DAC input, measured wrt a nominal V_{BIAS} output.

11.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.01% (100ppm); Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Input stage gain = 0dB, Output stage attenuation = 0dB.

AC Parameters (cont.)		Notes	Min.	Typ.	Max.	Unit
CTCSS Detector		74				
Sensitivity	(Pure Tone)	71	–	−26	–	dB
Response Time	(Composite Signal)	72	190	220	250	ms
De-response Time	(Composite Signal)	72, 75	–	240	–	ms
Dropout Immunity		75	–	160	–	ms
Frequency Range			60	–	260	Hz
In-band Tone Detector		74				
Sensitivity	(Pure Tone)	73	–	−26	–	dB
Response Time	(Good Signal)		–	29	–	ms
De-response Time	(Good Signal)		–	–	50	ms
Drop-out Immunity			–	–	20	ms
Frequency Range	(In-band tone)		288	–	3000	Hz
DCS Decoder		74				
Sensitivity		71	44	–	–	mVpk-pk
Bit-Rate Sync Time			–	2	–	edges

Notes:

71 Sub-Audio Detection Level threshold set to 15.4mV rms (CTCSS) or 44mV pk-pk (DCS).

72 Composite signal = 308mVrms at 1kHz + 75mVrms Noise + 31mV rms Sub-Audio signal. Noise bandwidth = 5kHz Band Limited Gaussian. For Sub-Audio signals above 100Hz. Signals below 100Hz will take longer to detect.

73 In-band Tone Detection Level threshold set to 16mV rms.

74 Detection and decoding involve statistical processes which can, on occasion, result in figures outside the limits quoted.

75 With sub-audio dropout time (P2.5) set to = 120ms. The typical dropout immunity is approximately 40ms more than the programmed dropout immunity. The typical de-response time is approximately 90ms longer than the programmed dropout immunity. See section 9.2.3 P2.5.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Audio Compandor					
Attack Time		–	4.0	–	ms
Decay Time		–	13	–	ms
0dB Point	84	–	100	–	mVrms
Compression/Expansion ratio		–	2:1	–	
CTCSS Encoder					
Frequency Range		60.0	–	260	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	81	−1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%
In-band Tone Encoder					
Frequency Range		288	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	83	−1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%
DCS Encoder					
Bit Rate		–	134.4	–	bps
Amplitude Tolerance	81	−1.0	0	+1.0	dB

Notes:
81 AV_{DD} = 3.3V and Tx Sub-Audio Level set to 88mV p-p (31mV rms).
82 Measured at MOD output.
83 AV_{DD} = 3.3V and Tx Audio Level set to 871mV p-p (308mV rms).
84 AV_{DD} = 3.3V.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Received Audio	91	300	–	3300	Hz
12.5kHz Channel Transmitted Audio	92	300	–	2550	Hz
25kHz Channel Transmitted Audio	93	300	–	3000	Hz
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		−2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise (Tx path)	96	–	−53.7	–	dBm
Residual Hum and Noise (Rx path)	96	–	−74.8	–	dBm
Pre-emphasis	94	–	+6	–	dB/oct
De-emphasis	95	–	−6	–	dB/oct
Audio Scrambler					
Inversion Frequency	98	2632	3300	3496	Hz
Pass-band (assuming 3300Hz inversion frequency)	99	300	–	3000	Hz
Audio Expandor					
Input Signal Range	97	–	–	0.55	Vrms

Notes:

91 The receiver audio filter complies with the characteristic shown in Figure 6. The high pass filtering removes sub-audio components from the audio signal.

92 The 12.5kHz channel filter complies with the characteristic shown in Figure 9.

93 The 25kHz channel filter complies with the characteristic shown in Figure 8.

94 The pre-emphasis filter complies with the characteristic shown in Figure 10.

95 The de-emphasis filter complies with the characteristic shown in Figure 7.

96 Psophometric weighting; pre/de-emphasis, compandor and 25kHz channel filter selected.

97 AV_{DD} = 3.3V.

98 Use of a scrambler inversion frequency other than 3300Hz will shift the scrambled voice signal outside the audio band, so that some of the signal will be lost in the channel filter. The result is that the descrambled voice signal will have a restricted bandwidth. The limits quoted are subjective and relate to the onset of a loss of speech intelligibility.

99 -6dB points.

11.2 C-BUS Timing

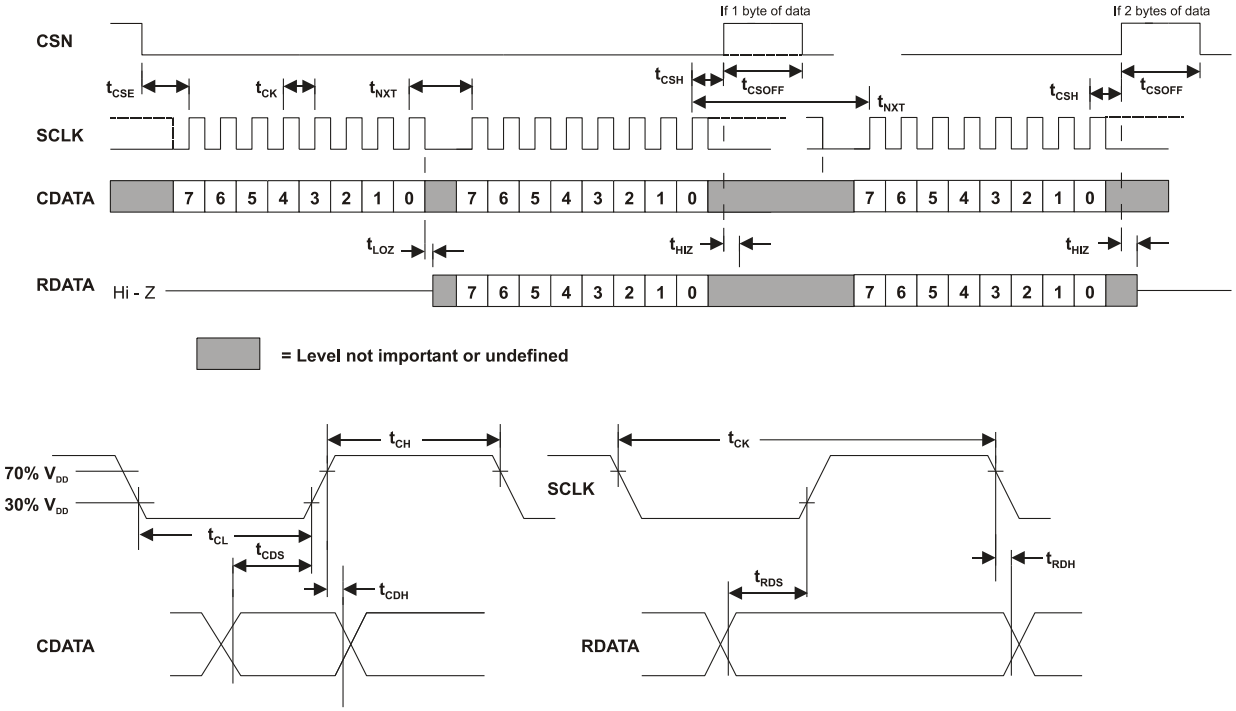


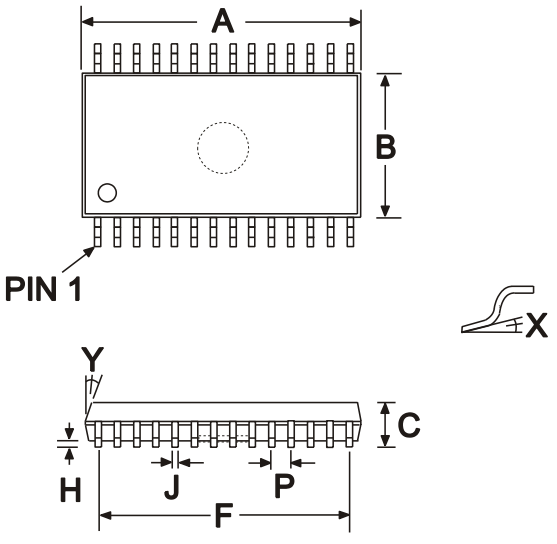
Figure 18 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX138A can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

11.3 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A	9.60		9.80
*	B	4.30		4.50
	C	--------		1.20
	E	6.20		6.60
	F		8.45	
	H	0.05		0.15
	J	0.17		0.30
	L	0.45		0.75
	P		0.65	
	T	0.08		0.20
	X	0°		8°
	Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Figure 19 Mechanical Outline of 28-pin TSSOP (E1)

Order as part no. CMX138AE1

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

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