Consumer Microcircuits Limited

M-I-X-E-D S-I-G-N-A-L S-O-L-U-T-I-O-N-S

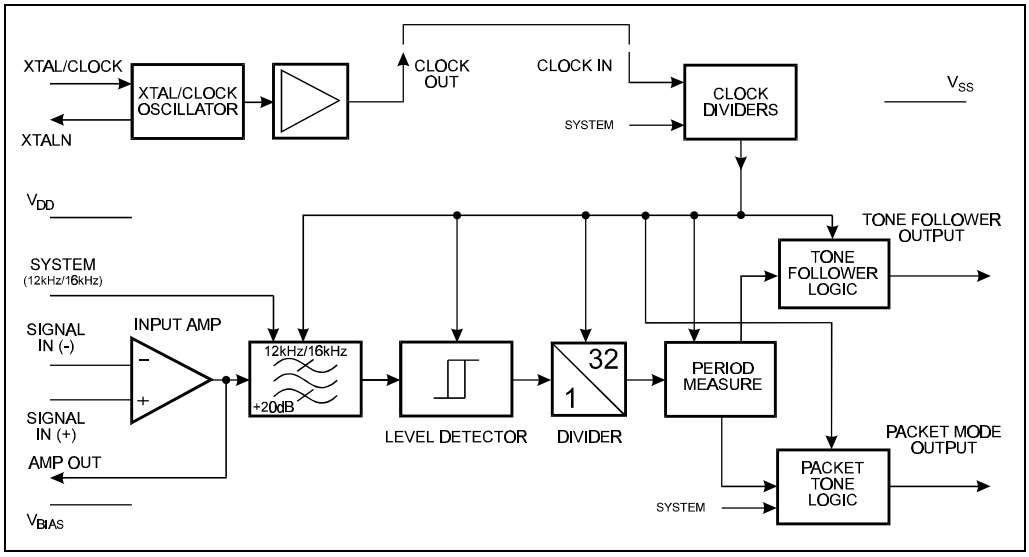
CMX631A
Low Voltage SPM Detector

D/631A/1 May 1998

Provisional Information

Features and Applications

- **Detects 12kHz or 16kHz SPM Frequencies**
- **Tone Follower and Packet Mode Outputs**
- **High Speech-Band Rejection Properties**
- **Low Power Operation (2.7V <0.8mA)**
- **Call Charge Applications on PABX Line Cards**
- **Complex and/or Simple Telephone Systems**
- **Remote Telephone/Payphones**



Brief Description

The CMX631A is a low-power, system-selectable Subscriber Pulse Metering (SPM) detector that indicates the presence of either 12kHz or 16kHz telephone call-charge frequencies on a telephone line.

Deriving its input directly from the telephone line, input amplitude/sensitivities are component adjustable to the user's national 'Must/Must-Not Decode' specifications via an on-chip input amplifier. The 12kHz and 16kHz frequency limits are accurately defined by the use of an external 3.579545MHz telephone-system Xtal or clock-pulse input.

The CMX631A demonstrates exceptional 12kHz and 16kHz performance in the presence of both voice and noise. This device may operate from a single or differential analogue signal input, from which two individual logic outputs will be produced; a Tone Follower Output and a Packet Mode Output.

This system (12kHz/16kHz) selectable integrated circuit, requires a 2.7V to 5.5V power supply which may be line-powered, is available in the following packages: 24-pin SSOP (CMX631AD5), 16-pin SOIC (CMX631AD4), and 16-pin PDIP (CMX631AP3). Additional package styles may be available to meet specific design requirements.

CONTENTS

1 Block Diagram

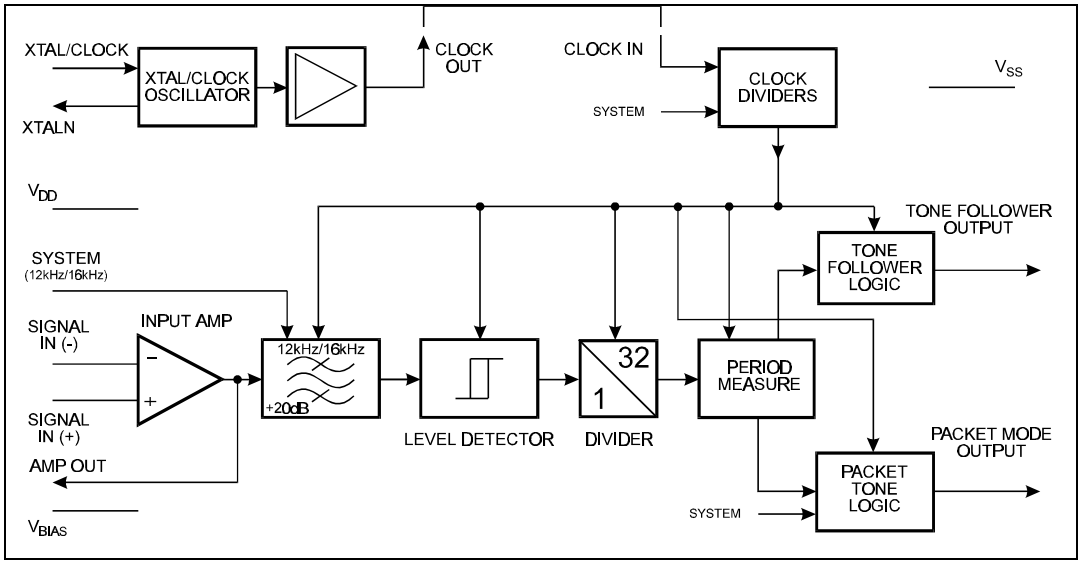


Figure 1: Block Diagram

2 Signal List

Packages		Signal		Description
D5	D4/P3	Name	Type	
1	1	Xtal/Clock	I/P	The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the Xtal output; circuit components are on-chip. When using a Xtal input, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is used at the Clock In pin, this (Xtal/Clock) pin must be connected directly to VDD . See Figure 2 and Section 3 - External Components.
4	2	XtalN	O/P	The output of the on-chip clock oscillator inverter.
5	3	Clock Out	O/P	A clock signal derived from the on-chip Xtal oscillator. If the on-chip oscillator is used, this pin should be connected directly to the Clock In pin. This output should not be used to clock other devices
6	4	Clock In	I/P	The 3.579545MHz clock pulse input to the internal clock dividers. If an externally generated clock pulse is used, the Xtal/Clock input pin should be connected to V_{DD}. See Section 3 External Components.
8	7	V_{BIAS}	Power	The output of the on-chip bias circuitry. Held internally at $V_{DD}/2$, this pin should be de-coupled to V_{SS}. See Figure 2.
12	8	V_{SS}	Power	Negative supply (GND).
13	9	Signal In +	I/P	The positive input to the input gain adjusting signal amplifier. See Section 4.3, Sensitivity Setting and 4.4, 'Will'/'Will Not' Detect Frequencies.
17	10	Signal In -	I/P	The negative input to the input gain adjusting signal amplifier. See Section 4.3, Sensitivity Setting and 4.4, 'Will'/'Will Not' Detect Frequencies.
18	11	Amp Out	O/P	The output of the input gain adjusting signal amplifier. See Section 4.3, Sensitivity Setting and 4.4, 'Will'/'Will Not' Detect Frequencies.
19	13	Tone Follower Output	O/P	This output provides a logic '0' for the period of a detected tone and a logic '1' for a NOTONE detection. See 4.1, Tone Follower Mode and Figure 3.
20	14	Packet Mode Output	O/P	This output provides a logic '0' for a detected tone and a logic 1 for NOTONE detection and will ignore a small fluctuation or fade during the tone signal. See Section 4.2, Packet Mode and Figure 3.
21	15	System	I/P	This logic input selects the device operation to either 12kHz (logic 1) or 16kHz (logic '0') SPM systems. This input has an internal 1MΩ pull-up resistor (12kHz).
24	16	V_{DD}	Power	Positive supply. A single, stable power supply is required. Critical levels and voltages within the CMX631A are dependent upon this supply. This pin should be de-coupled to V_{SS} by a capacitor mounted close to the pin. Note: If this device is line powered, the resulting power supply must be stable. See Section 5.1.1 - Protection against High Voltages.
2, 3, 7, 9, 10, 11, 14, 15, 16, 22, 23	5,6,12	N/C		No internal connection; leave open circuit.

3 External Components

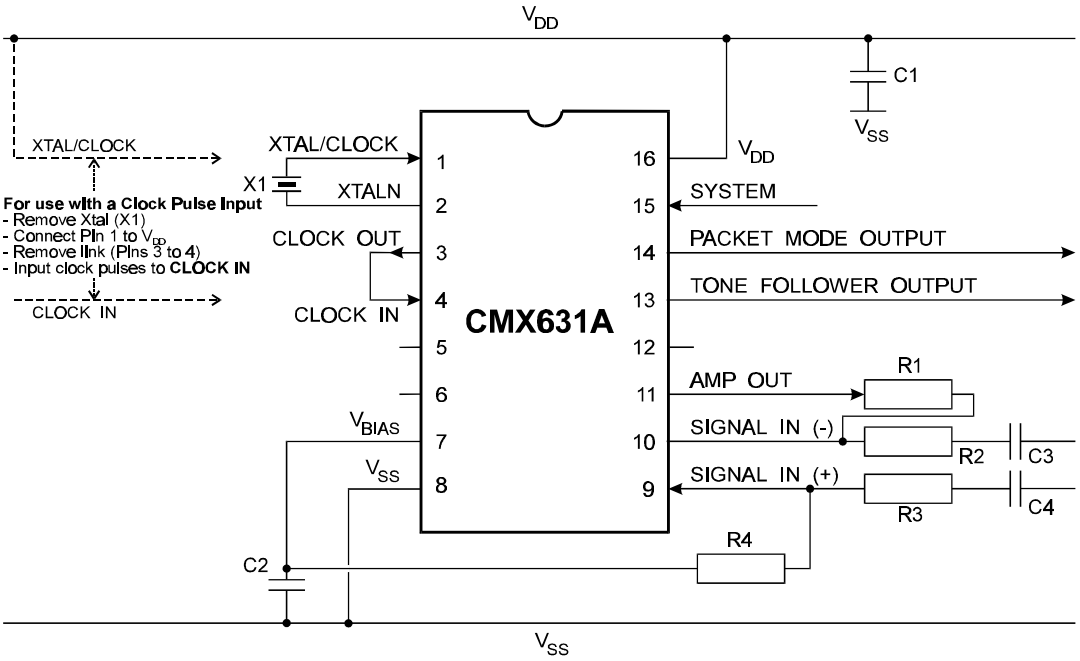


Figure 2: Recommended External Components

R1	Note 1	$R_{FEEDBACK}$	C1	1.0µF	±20%
R2	Note 1	$R_{IN(-)}$	C2	1.0µF	±20%
R3	Note 1	$R_{IN(+)}$	C3	$C_{IN(-)}$	
R4	Note 1	R_{BIAS}	C4	$C_{IN(+)}$	
			X1	Note 2, 3, 4 3.579545MHz	

Table 2: Recommended External Components

Recommended External Component Notes:

1. When calculating input gain components, for correct operation R1 and R4 should always be ≥ 33kΩ.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. The on-chip crystal circuitry includes a feedback resistor (nominally 2MΩ) between pins 1 and 2 and load capacitors on pins 1 and 2 (nominally 10pF each, excluding package and board parasitics).
4. When using an external clock input, X1 should be removed, Pin 1 (Xtal/Clock) should be tied to V_{DD}, the Clock In and Clock Out jumper should be removed, and the external clock signal applied to Clock In.

4 General Description

4.1 Tone Follower Mode

The Tone Follower Output produces a logic ‘0’ when a valid signal is detected. A logic ‘1’ signifies a NOTONE or bad decode. See Figure 3.

4.2 Packet Mode

The Packet (Cumulative Tone) Mode Output will respond and/or de-respond after a cumulative 40ms of good tone (or NOTONE) in any 48ms period by providing a Logic level output. See Figure 3.

This process will ignore small fluctuations or fades of a valid frequency input and is available for µProcessor ‘wake-up’, Minimum tone detection, NOTONE indication or transient avoidance.

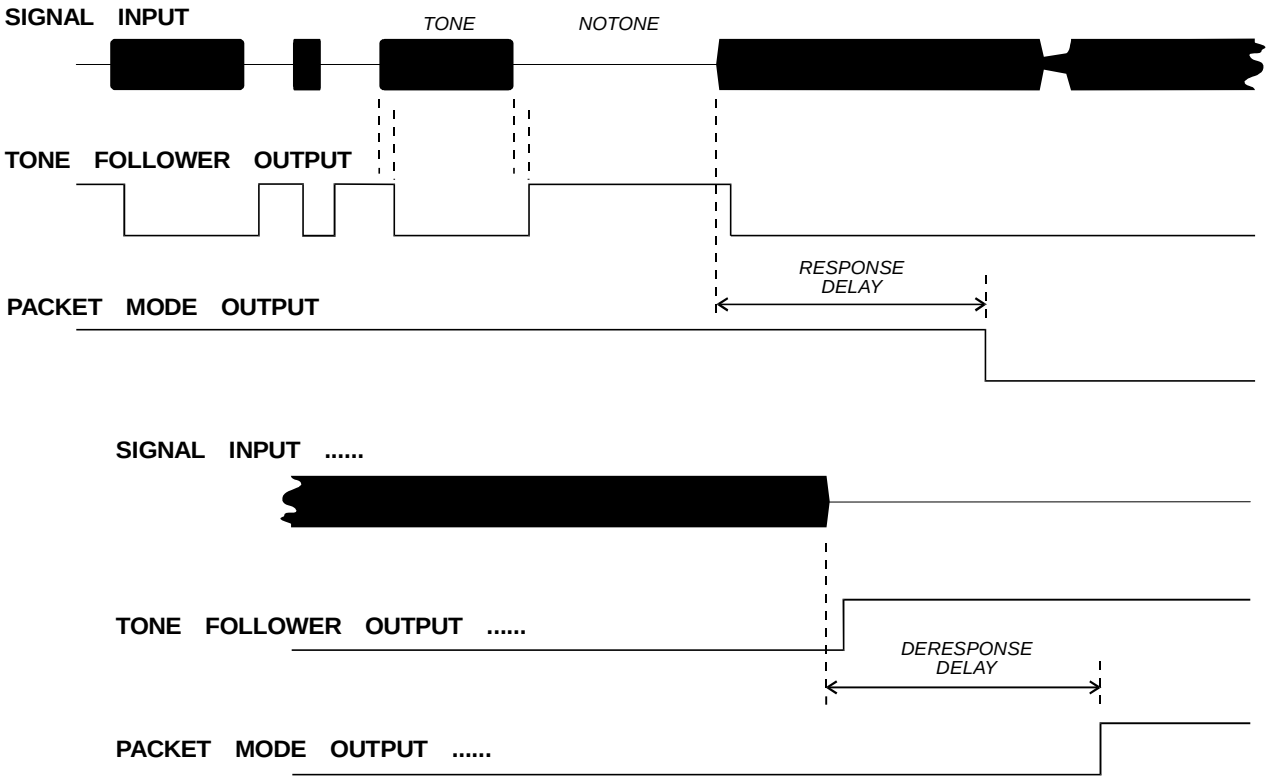


Figure 3: Tone Follower and Packet Mode Outputs

4.3 Sensitivity Setting

The CMX631A input sensitivity can be accurately adjusted and set to support many national 12kHz and 16kHz SPM specifications.

4.3.1 Input Gain Calculation

The input amplifier, with external circuitry, is used to set the sensitivity of the CMX631A to conform to the user's national level specification with regard to ‘Must’ and ‘Must-Not’ decode signal levels.

With reference to the graphs in Figure 4 and Figure 5, the following steps will assist in the determination of the required gain/attenuation.

1. Draw two horizontal lines from the Y-axis [Signal Level (dB)] in Figure 4 and Figure 5. The upper line represents the required ‘Must’ decode level. The lower line represents the required ‘Must-Not’ decode level
2. Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis [Amplifier Gain (dB)]. The point where the vertical line meets the X-axis indicates the minimum Input Amp gain required for reliable decoding of valid signals.
3. Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis. The point where the vertical line meets the X-axis will indicate the maximum allowable Input Amp gain. Input signals at or below the ‘Must-Not’ decode level will not be detected as long as the amplifier gain is no higher than this level.

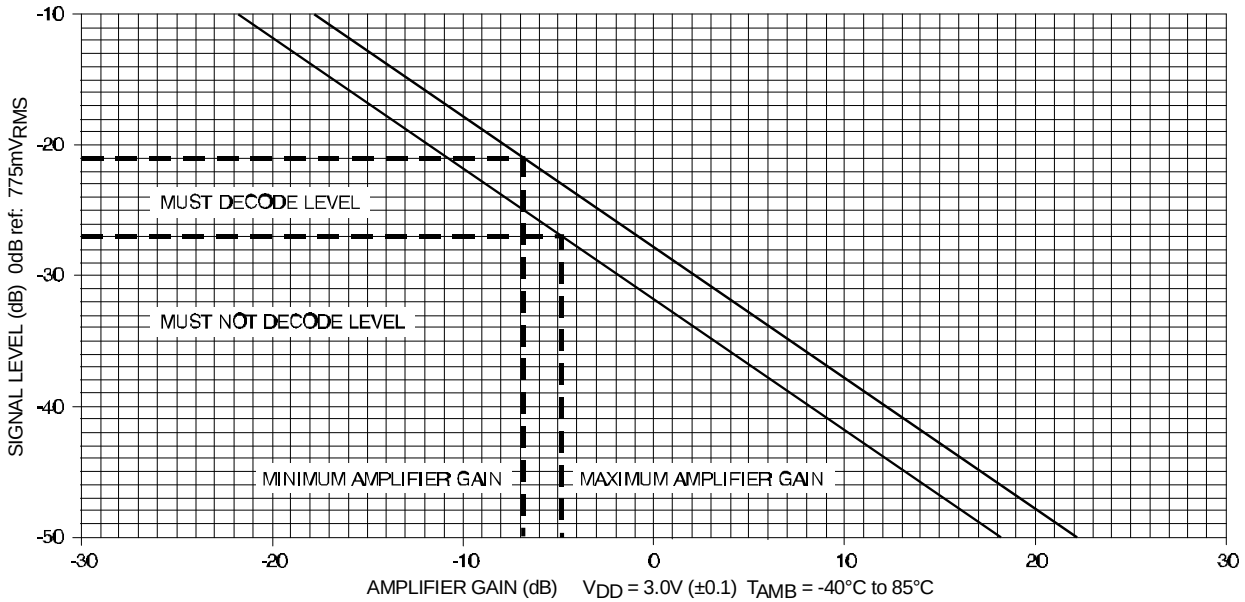


Figure 4: Input Gain Calculation Graph for V_{DD} = 3.0V

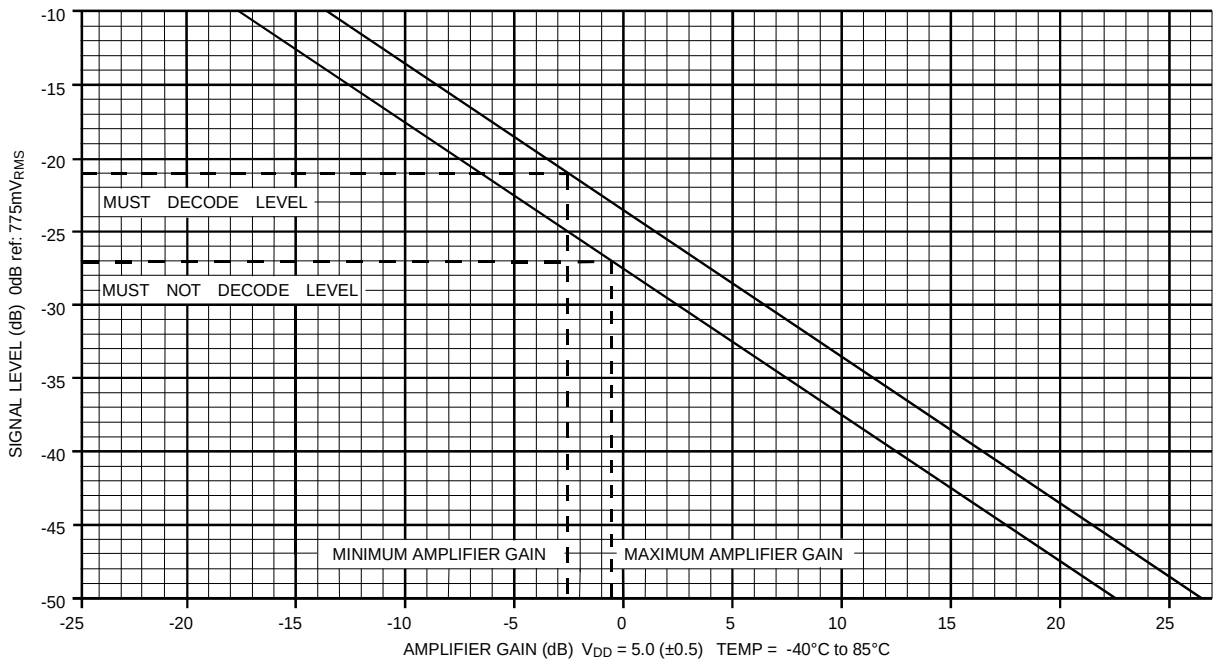


Figure 5: Input Gain Calculation Graph for V_{DD} = 5.0V

4.3.2 Input Gain Components

Refer to the gain components found in Table 2 and Figure 2. The user should calculate and select external components (R1/R2/C3 and R3/R4/C4) to provide amplifier gain within the limits obtained in 4.3.1 Input Gain Calculation.

Component tolerances should not move the gain-figure outside these limits. The graphs Figure 4 and Figure 5 are for the calculation of input gain components for a CMX631A using a V_{DD} of 3.0 (±0.1) or V_{DD} of 5.0 (±0.5).

4.4 'WILL'/'WILL-NOT' Detect Frequencies

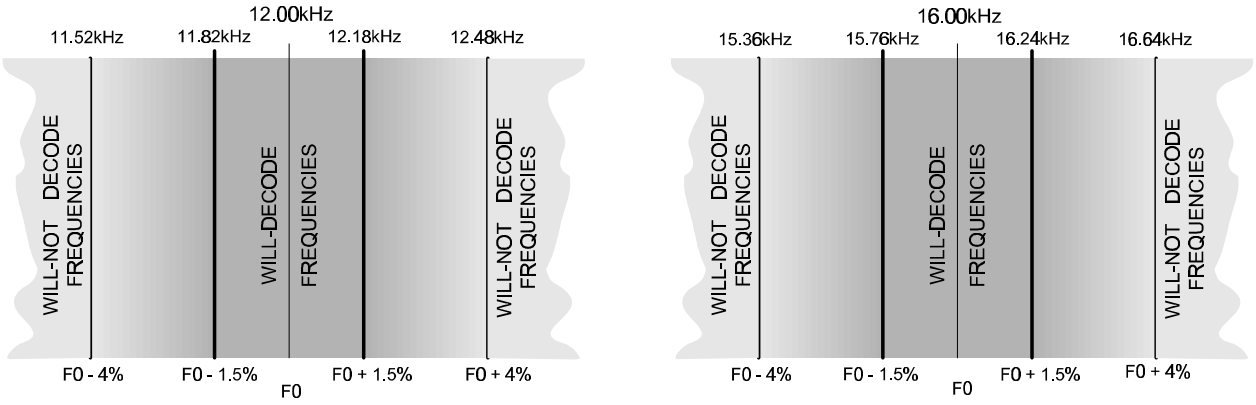


Figure 6: 'WILL'/'WILL-NOT' Detect Frequencies

5 Applications

5.1 Input Configurations

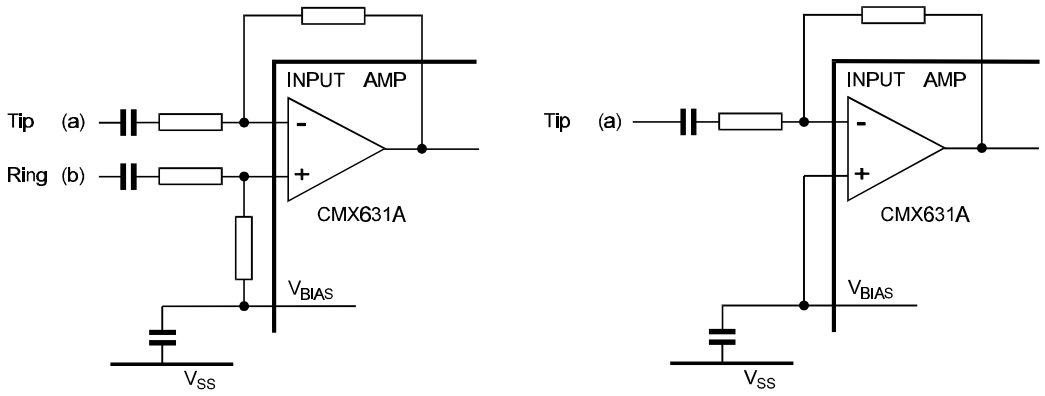


Figure 7: Input Configurations

5.1.1 Protection Against High Voltages

Telephone systems may have high DC and AC voltages present on the line. If the CMX631A is a part of host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} +0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the CMX631A will require protection diodes at its signal inputs (+ and -). The breakdown voltage of the capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the DC voltages plus all expected signal peaks.

5.1.2 Aliasing

Due to the sampling nature of switched-capacitor filters used in the CMX631A, high frequency noise or unwanted signals can alias into the passband, disrupting detection. External components must be chosen carefully to avoid alias effects.

Possible Alias Frequencies:

12kHz Mode = 52kHz

16kHz Mode = 69kHz

If other filtering in the system has not attenuated these alias frequencies, capacitors should be employed across resistors R1 and R4 to provide anti-alias filtering.

The low-pass cutoff frequency should be chosen to be approximately 20kHz to 25kHz for a 12kHz system, or 25kHz to 30kHz for a 16kHz system.

i.e.

$$C = \frac{1}{2 \times \pi \times f_0 \times (R1 \text{ or } R4)}$$

When anti-alias capacitors are used, an allowance must be made for reduced gain at the SPM frequency (12kHz or 16kHz).

The 'Clock-Out' Pin

The Clock-Out pin is intended to drive the CMX631A Clock-In pin only. It is not recommended that it be used to clock other devices within the host equipment.

6 Performance Specification

6.1 Electrical Specifications

6.1.1 Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD}-V_{SS})	-0.3		7.0	V
Voltage on any pin to V_{SS}	-0.3		(V_{DD} + 0.3)	V
Current into ……				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pin	-20		20	mA

D4 / P3 Packages	Min.	Typ.	Max.	Unit
Total allowable device dissipation at T_{AMB} 25°C			800	mW
Derating above T_{AMB} 25°C			13	mW/°C
Operating Temperature	-40		85	°C
Storage Temperature	-40		85	°C

D5 Package	Min.	Typ.	Max.	Unit
Total allowable device dissipation at T_{AMB} 25°C			550	mW
Derating above T_{AMB} 25°C			9	mW/°C
Operating Temperature	-40		85	°C
Storage Temperature	-40		85	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})	2.7	3.0/5.0	5.5	V
Operating Temperature	-40		85	°C
Xtal/Clock Frequency	3.558918		3.589368	MHz

6.1.3 Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.0V to 5.0V @ T_{AMB} = -40°C to 85°C
Audio Level 0dB (ref.) = 775mV_{RMS}, Noise Bandwidth = 50kHz
Xtal/Clock Frequency = 3.579545MHz, System Setting = 12kHz or 16kHz

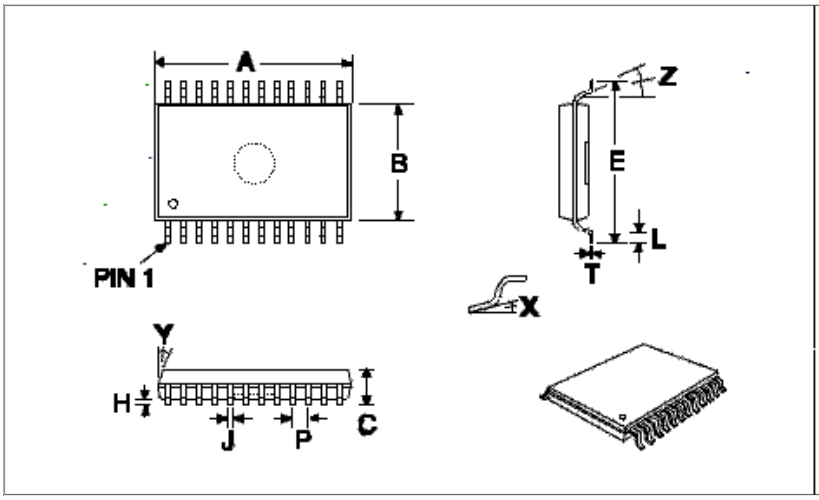
		Notes	Min.	Typ.	Max.	Units
Supply Current						
V_{DD} = 3.0V			-	-	0.8	mA
V_{DD} = 5.0V			-	-	2.2	mA
Logic Inputs/Outputs						
Input Logic '1'			70.0	-	-	%V_{DD}
Input Logic '0'			-	-	30.0	%V_{DD}
Output Logic '1'			90.0	-	-	%V_{DD}
Output Logic '0'			-	-	10.0	%V_{DD}
Xtal/Clock or Clock In Frequency			3.558918	-	3.589368	MHz
External Clock Pulse Width						
High			100	-	-	ns
Low			100	-	-	ns
Input Amplifier						
D. C. Gain			60.0	-	-	dB
Bandwidth (-3dB)			-	100	-	Hz
Input Impedance			-	1.0		MΩ
Logic Impedances						
Input						
System			0.7	-	3.8	MΩ
Clock In			10.0	-	-	MΩ
Output			-	14.0	30.0	kΩ
Overall Performance						
12kHz Detect Bandwidth		1	11.820	-	12.180	kHz
12kHz Not-detect Frequencies	(below 12kHz)	1	-	-	11.520	kHz
12kHz Not-detect Frequencies	(above 12kHz)	1	12.480	-	-	kHz
16kHz Detect Bandwidth		1	15.760	-	16.240	kHz
16kHz Not-detect Frequencies	(below 16kHz)	1	-	-	15.360	kHz
16kHz Not-detect Frequencies	(above 16kHz)	1	16.640	-	-	kHz
Sensitivity						
V_{DD} = 3.0V±0.1V		2	-27.8	-	-31.8	dBm
V_{DD} = 5.0V±0.5V		2	-23.5	-	-27.5	dBm
Tone Operating Characteristics						
Signal-to-Noise Requirements	(Amp Input)	3, 4, 5, 6	22.0	20.0	-	dB
Signal-to-Voice Requirements	(Amp Input)	3, 4, 5, 7	-36.0	-40.0	-	dB
Signal-to-Voice Requirements	(Amp Output)	5, 6	-25.0	-	-29.0	dB
Tone Follower Mode		1, 8				
Response and De-Response Time					10.0	ms
Packet Mode		1, 8				
Response and De-Response Time			40.0	-	48.0	ms

Operating Characteristics Notes:

1. With adherence to Signal-to-Voice and Signal-to-Noise specifications.
2. With Input Amplifier gain set to unity gain. See Section 4.3 for description of sensitivity setting.
3. Common Mode SPM and balanced voice signal.
4. Immune to false responses.
5. Immune to false de-responses.
6. With SPM and voice signal amplitudes balanced. To avoid false de-responses due to saturation, the peak to peak voice+noise level at the output of the Input Amp (12/16kHz Filter Input) should be no greater than the dynamic range of the device.
7. Maximum voice frequencies = 3.4kHz.
8. Response, De-Response and Power-up Response timing.

6.2 Packages

The CMX631A is available in the following packages. Additional package styles may be available to meet specific design requirements.

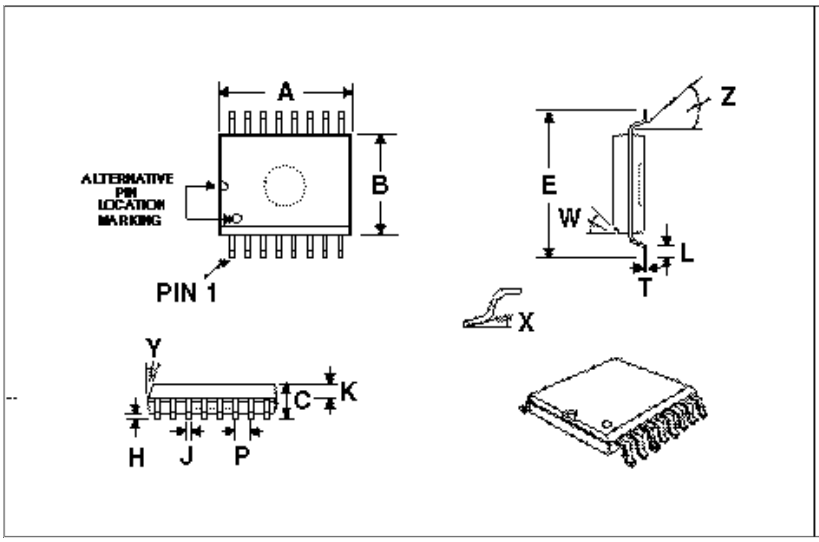


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin SSOP Mechanical Outline: *order as part no. CMX631AD5*

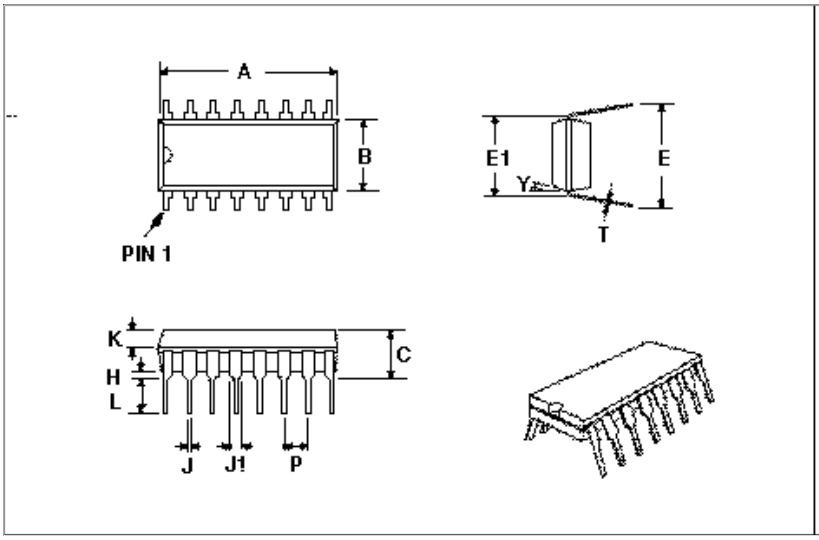


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 16-pin SOIC Mechanical Outline: *order as part no. CMX631AD4*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91)
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 16-pin PDIP Mechanical Outline: *order as part no. CMX631AP3*

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

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This notification is relevant product information to which it is attached.

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