CML Microcircuits
COMMUNICATION SEMICONDUCTORS

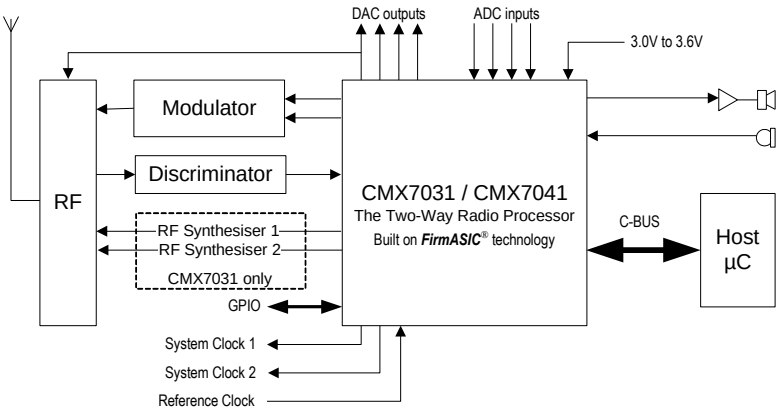
CMX7031/CMX7041
The Two-Way Radio Processor

D/7031/41_FI1.x/13 July 2013 **DATASHEET** Provisional Issue

7031/7041 FI-1.5: Baseband Audio and Data Processor with Auxiliary System Clocks, ADCs and DACs for use in Analogue Radio Systems

Features

- **Concurrent Audio/Signalling/Data Operations**
- **Full Audio-band Processing: Pre and De-emphasis, Compandor, Scrambler and Selectable 2.55/3.0 kHz Filters**
- **2 x RF Synthesisers (CMX7031 only)**
- **Inband Signalling: Selcall, DTMF, NOAA NWR**
- **3 x Analogue Inputs (Mic or Discriminator)**
- **2 x Auxiliary ADCs and 4 x Auxiliary DACs**
- **C-BUS Serial Interface to Host µController**
- **Low-power (3.0V to 3.6V) Operation**
- **Available in 64-pin, 48-pin LQFP and VQFN Packages**
- **Selectable Audio Processing Order**
- **MSK/FFSK Data Modem with Packet or Free-format Modes with FEC, CRC, Interleaving and Scrambling**
- **Enhanced DSC Modem for Marine Applications, offering support for DSC expansion sequences and transmission of continuous distress signals**
- **Sub-Audio Signalling: CTCSS, DCS, XTCSS**
- **Tx Outputs for Single, Two-Point or I/Q Mod.**
- **559bps PSK Modulator**
- **2 x Auxiliary System Clock Outputs**
- **Flexible Powersave Modes**



This document contains:

1. Brief Description

The CMX7031/CMX7041 FI 1.5 is a full-function, half-duplex, audio, signalling and data processor IC. This makes it a suitable device for both the leisure radio markets (FRS, MURS, PMR446 and GMRS) and for professional radio products (PMR/LMR, Marine and Trunking) with or without signalling and data facilities.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external EEPROM or from a host µController over the built-in C-BUS serial interface. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 1.5.

Continued…

The CMX7031 features two on-chip RF synthesisers, with easy Rx/Tx frequency changeover, and programmable system clocks to minimise chip count in the final application.

The CMX7041 is identical in functionality to the CMX7031 with the exception that the two on-chip RF Synthesisers have been deleted, which enables it to be supplied in a smaller package and with two extra GPIO pins. This document refers to both parts generically as the CMX7031, unless otherwise stated.

When loaded with Function Image™ 1.5, both devices perform simultaneous processing of sub-audio and inband signalling and audio band processing (including frequency inversion scrambling, companding and pre- or de-emphasis).

Other features include a complete MSK/FFSK modem for packetised or free-format data, a DSC modem, two auxiliary ADC channels with four selectable inputs and up to four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained by registering your interest in these products with your local CML representative.

CONTENTS

Table Page

Figure Page

1.1. History

Version	Changes	Date
13	• Added support for DSC expansion sequences (section 7.11), minor modification to the Status ($C6) register b7 (section 9.1.21) and new bit definition in the Programming Register (section 9.2.1) • Updated RAMDAC description in section 9.1.4 • Function Image Updates (section 9.3) updated	17.7.13
12	• Added SPI port descriptive text in section 7.4.1 and other minor corrections.	27.10.11

<table>
<tr><th>Version</th><th>Changes</th><th>Date</th></tr>
<tr><td>11</td><td>• C11, DISC input capacitor changed to 470nF to optimise CTCSS/DCS decode timing.
• Updated CTCSS detection parametrics</td><td>17.10.11</td></tr>
<tr><td>10</td><td>• Correct RF Synthesiser specification, following further evaluation</td><td>16.06.11</td></tr>
<tr><td>9</td><td>• Correct an error in the EEPROM FI-loading flowchart and clarify the reset options available in sections 7.3 and 10.1.</td><td>27.04.11</td></tr>
<tr><td>8</td><td><table>
<tr><th>section</th><th>change</th></tr>
<tr><td>2, 3 and 4, etc</td><td>Revised usage of pin names, to coincide with other FIs</td></tr>
<tr><td>3.1</td><td>Addition of Signal Definitions section</td></tr>
<tr><td>4</td><td>Clarification of Vdec decoupling - Note 8</td></tr>
<tr><td>5, 7.19 and 10.1.27</td><td>Clarification of usage of gain, attenuation and level terms</td></tr>
<tr><td>7.3</td><td>Revised FI loading flowcharts, Figs 7 and 8</td></tr>
<tr><td>7.10.4</td><td>Identified the position of the Rx Frame Sync pattern in the Rx Data 1 register.</td></tr>
<tr><td>7.20 and 10.1</td><td>Revised and corrected the C-BUS Register table.
Table in section 10.1 is now hyperlinked.</td></tr>
<tr><td>8.1.3</td><td>Corrected the range of the N divider (RF PLL)</td></tr>
<tr><td>10.1.2</td><td>Operation of General Reset command clarified</td></tr>
<tr><td>10.1.9</td><td>Definitions of fine and coarse adjustments clarified</td></tr>
<tr><td>10.1.11</td><td>Corrected the range of the R divider (RF PLL)</td></tr>
<tr><td>10.1.27</td><td>Definition of Audio Tone register ($CD) clarified</td></tr>
<tr><td>10.2</td><td>Programming register limit of P4.8 increased to P4.12</td></tr>
<tr><td>10.2.3</td><td>Footnote added to definition of P2.0</td></tr>
<tr><td></td><td>Various typographical corrections and clarifications</td></tr>
<tr><td></td><td></td></tr>
</table></td><td>27.01.10</td></tr>
<tr><td>7</td><td><table>
<tr><th>section</th><th>change</th></tr>
<tr><td>3</td><td>GPIO1&2 defined as Rx and Tx Enable</td></tr>
<tr><td></td><td>C-BUS signal names standardised</td></tr>
<tr><td></td><td>ADC signal names standardised</td></tr>
<tr><td>7.12</td><td>559bps encoder added</td></tr>
<tr><td>7.13</td><td>Note that WAT detector will re-arm after 500ms of tone</td></tr>
<tr><td>Fig 24</td><td>Updated to latest version</td></tr>
<tr><td></td><td>Contact details updated</td></tr>
<tr><td></td><td></td></tr>
</table></td><td>03.04.09</td></tr>
<tr><td>6</td><td><table>
<tr><th>section</th><th>change</th></tr>
<tr><td>7.9.1</td><td>Added text on re-starting frame sync detection.</td></tr>
<tr><td>7.17</td><td>FI-1.3.8.2 qualification for GPIO A & B.</td></tr>
<tr><td>Fig 25</td><td>FI-1.3.8.2 qualification.</td></tr>
<tr><td>8.1.3</td><td>Power supply parametric updated.</td></tr>
<tr><td>8.1.4</td><td>Note 75 corrected.</td></tr>
<tr><td></td><td>Note 76 added.</td></tr>
<tr><td></td><td>DTMF levels corrected.</td></tr>
<tr><td></td><td>Residual hum & noise levels corrected.</td></tr>
<tr><td></td><td></td></tr>
</table></td><td>26.01.09</td></tr>
</table>

<table>
<tr><th>Version</th><th>Changes</th><th>Date</th></tr>
<tr><td>5</td><td>
<table>
<tr><th>section</th><th>change</th></tr>
<tr><td>Fig 1</td><td>Text corrected on RF Synth block</td></tr>
<tr><td>3</td><td>RxENA and TxENA added to pin list table</td></tr>
<tr><td>7.5.1</td><td>Text on inversion frequency added</td></tr>
<tr><td>7.5.2</td><td>Extraneous “the” removed
More C-BUS references added</td></tr>
<tr><td>7.6.1</td><td>Note 8 clarified</td></tr>
<tr><td>7.17</td><td>RxENA, TxENA description and reference to GPIO A & B added</td></tr>
<tr><td>Figure 25</td><td>Revised to show Tx Voice Level multiplier</td></tr>
<tr><td>Table 3</td><td>CTCSS IRQ states added</td></tr>
<tr><td></td><td></td></tr>
</table>
</td><td>05.09.08</td></tr>
<tr><td>4</td><td>
<table>
<tr><th>section</th><th>change</th></tr>
<tr><td>3</td><td>Note on metal pad added</td></tr>
<tr><td>7.1</td><td>Settings for 9.0592 xtal replaced with 9.216MHz</td></tr>
<tr><td>7.2</td><td>Note on C-BUS latency added</td></tr>
<tr><td>7.2</td><td>Additional text for IRQ operation added</td></tr>
<tr><td>7.3</td><td>Pull-up Resistors on BOOTEN pins changed to 220k</td></tr>
<tr><td>7.5.2</td><td>Input AGC section added</td></tr>
<tr><td>7.6.1</td><td>CTCSS phase change detection corrected</td></tr>
<tr><td>7.13</td><td>AuxADC threshold operation clarified and Fig 21 added</td></tr>
<tr><td>7.14</td><td>AuxDAC output in Powersave clarified</td></tr>
<tr><td>7.16.2</td><td>Default states of SYSCLK1 & 2 defined for both CMX7031 and CMX7041</td></tr>
<tr><td>8.1.3</td><td>Aux ADC conversion time corrected</td></tr>
<tr><td>8.1.4</td><td>Reference to P2.4 corrected to P2.5 in Note 7</td></tr>
<tr><td>8.1.4</td><td>Scrambler pass-band corrected</td></tr>
<tr><td>Fig 1</td><td>Typos in Block Diagram corrected</td></tr>
<tr><td>Fig 2,3,4,5</td><td>Components re-numbered, C4 removed</td></tr>
<tr><td>Fig 24</td><td>Minimum CLK input changed from 4MHz to 3MHz</td></tr>
<tr><td>Fig 26,27,28,29</td><td>Package drawings updated</td></tr>
</table>
</td><td>21.07.08</td></tr>
<tr><td>2, 3</td><td>Updates to reflect changes to the FI.</td><td>Jul 2007
Sep 2007</td></tr>
<tr><td>1</td><td>Original document.</td><td>Jan 2007</td></tr>
</table>

It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

2. Block Diagram

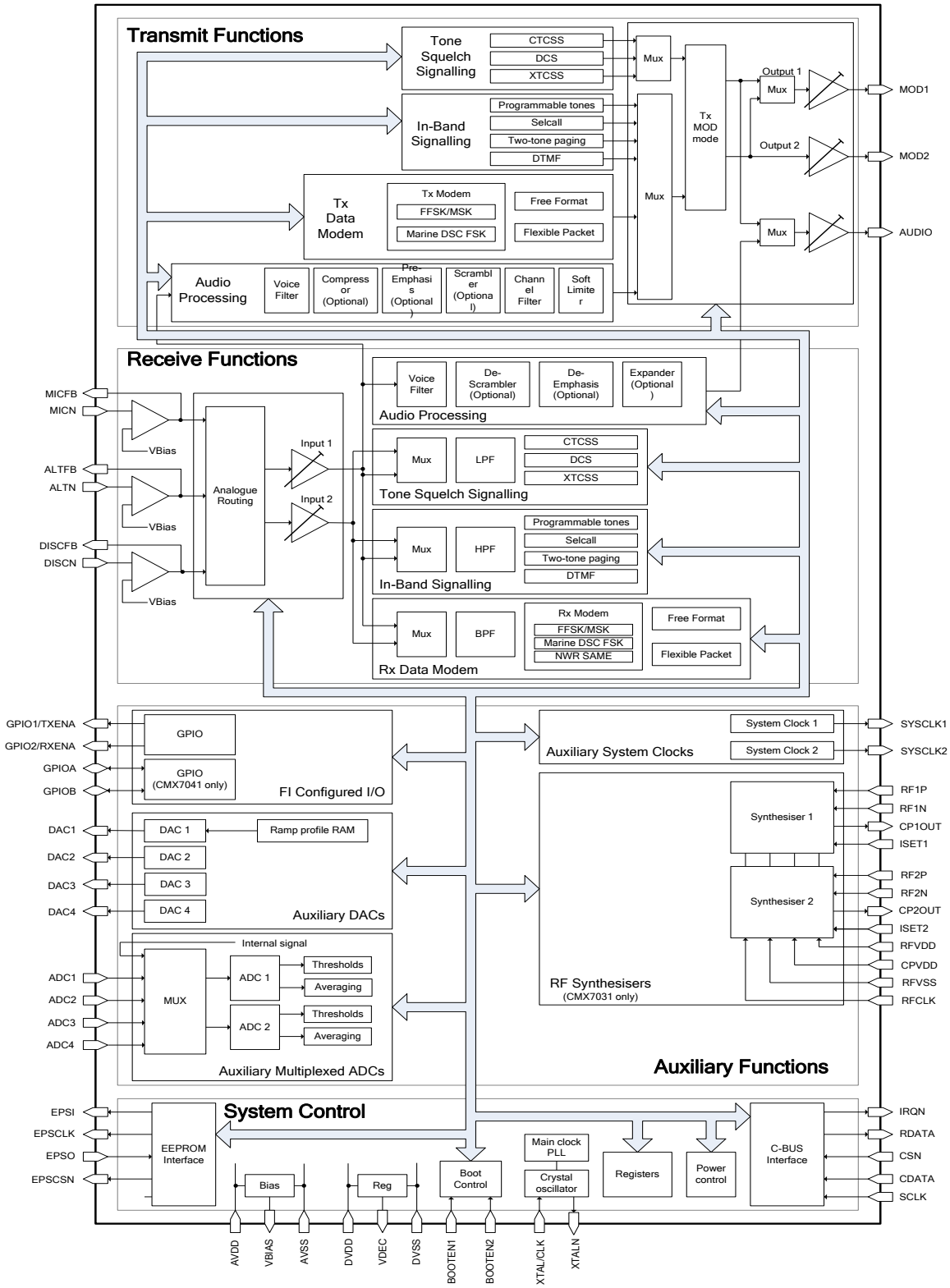


Figure 1 Block Diagram

3. Signal List

CMX7031 64-pin Q1/L9	CMX7041 48-pin Q3/L4	Pin Name	Type	Description
1	**8**	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
2	-	RF1N	IP	RF Synthesiser #1 Negative Input.
3	-	RF1P	IP	RF Synthesiser #1 Positive Input.
4	-	RFVSS	PWR	The negative supply rail (ground) for the 1st RF synthesiser.
5	-	CP1OUT	OP	1st Charge Pump output.
6	-	ISET1	IP	1st Charge Pump Current Set input.
7	-	RFVDD	PWR	The 2.5V positive supply rail for the RF synthesisers. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
8	-	RF2N	IP	RF Synthesiser #2 Negative Input.
9	-	RF2P	IP	RF Synthesiser #2 Positive Input.
10	-	RFVSS	PWR	The negative supply rail (ground) for the 2nd RF synthesiser.
11	-	CP2OUT	OP	2nd Charge Pump output.
12	-	ISET2	IP	2nd Charge Pump Current Set input.
13	-	CPVDD	PWR	The 3.3V positive supply rail for the RF charge pumps. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
14	-	RFCLK	IP	RF Clock Input (common to both synthesisers)[1].
15	-	-	NC	Reserved – do not connect this pin.
16	-	-	NC	Reserved – do not connect this pin.
17	-	-	NC	Reserved – do not connect this pin.
18	**9**	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
19	**10**	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
-	**11**	GPIOA	OP	General Purpose I/O pin (CMX7041 only)
-	**12**	GPIOB	OP	General Purpose I/O pin (CMX7041 only)
20	**13**	SYSCLK1	OP	Synthesised Digital System Clock Output 1.
21	**14**	DVSS	PWR	Digital Ground.
22	-	-	NC	Reserved – do not connect this pin.
23	**15**	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)
24	**16**	DISCN	IP	Channel 1 inverting input.
25	**17**	DISCFB	OP	Channel 1 input amplifier feedback.

[1] To minimise crosstalk, this signal should be connected to the same clock source as XTAL/CLOCK input.

CMX7031 64-pin Q1/L9	CMX7041 48-pin Q3/L4	Pin Name	Type	Description	
26	**18**	ALTN	IP	Channel 2 inverting input.	
27	**19**	ALTFB	OP	Channel 2 input amplifier feedback.	
28	**20**	MICFB	OP	Channel 3 input amplifier feedback.	
29	**21**	MICN	IP	Channel 3 inverting input.	
30	**22**	AVSS	PWR	Analog Ground.	
31	**23**	MOD1	OP	Modulator 1 output.	
32	**24**	MOD2	OP	Modulator 2 output.	
33	**25**	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when VBIAS will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.	
34	**26**	AUDIO	OP	Audio output.	
35	**27**	ADC1	IP	Auxiliary ADC input (1)	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 9.1.3 for details
36	**28**	ADC2	IP	Auxiliary ADC input (2)	
37	**29**	ADC3	IP	Auxiliary ADC input (3)	
38	**30**	ADC4	IP	Auxiliary ADC input (4)	
39	**31**	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
40	**32**	DAC1	OP	Auxiliary DAC output 1/RAMDAC.	
41	**33**	DAC2	OP	Auxiliary DAC output 2.	
42	**34**	AVSS	PWR	Analogue Ground.	
43	**35**	DAC3	OP	Auxiliary DAC output 3.	
44	**36**	DAC4	OP	Auxiliary DAC output 4.	
-	**37**	DVSS	PWR	Digital Ground.	
45	**38**	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.	
46	**39**	XTAL/CLK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source.	
47	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter.	
48	**41**	DVDD	PWR	The 3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVss by capacitors mounted close to the device pins.	
49	**42**	CDATA	IP	C-BUS: Serial data input from the µC.	
50	**43**	RDATA	TS OP	C-BUS: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.	
51	**44**	-	NC	Reserved – do not connect this pin.	

CMX7031 64-pin Q1/L9	CMX7041 48-pin Q3/L4	Pin Name	Type	Description
52	**45**	DVSS	PWR	Digital Ground.
53	-	-	NC	Reserved – do not connect this pin.
54	**46**	SCLK	IP	C-BUS: The C-BUS serial clock input from the µC.
55	**47**	SYSCLK2	OP	Synthesised Digital System Clock Output 2.
56	**48**	CSN	IP	C-BUS: The C-BUS chip select input from the µC - there is no internal pullup on this input.
57	-	-	NC	Reserved – do not connect this pin.
58	**1**	EPSI	OP	EEPROM Serial Interface: SPI bus Output.
59	**2**	EPSCLK	OP	EEPROM Serial Interface: SPI bus Clock.
60	**3**	EPSO	IP+PD	EEPROM Serial Interface: SPI bus Input.
61	**4**	EPSCSN	OP	EEPROM Serial Interface: SPI bus Chip Select.
62	**5**	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
63	**6**	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
64	**7**	DVSS	PWR	Digital Ground.
EXPOSED METAL PAD	EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q1 & Q3 packages only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connection is permitted.**

Notes: IP = Input (+ PU/PD = internal pullup/pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

3.1. Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
RFV_{DD}	RFVDD	Power supply for RF synthesiser circuits
CPV_{DD}	CPVDD	Power supply for RF charge pump
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits
RFV_{SS}	RFVSS	Ground for all RF circuits

4. External Components

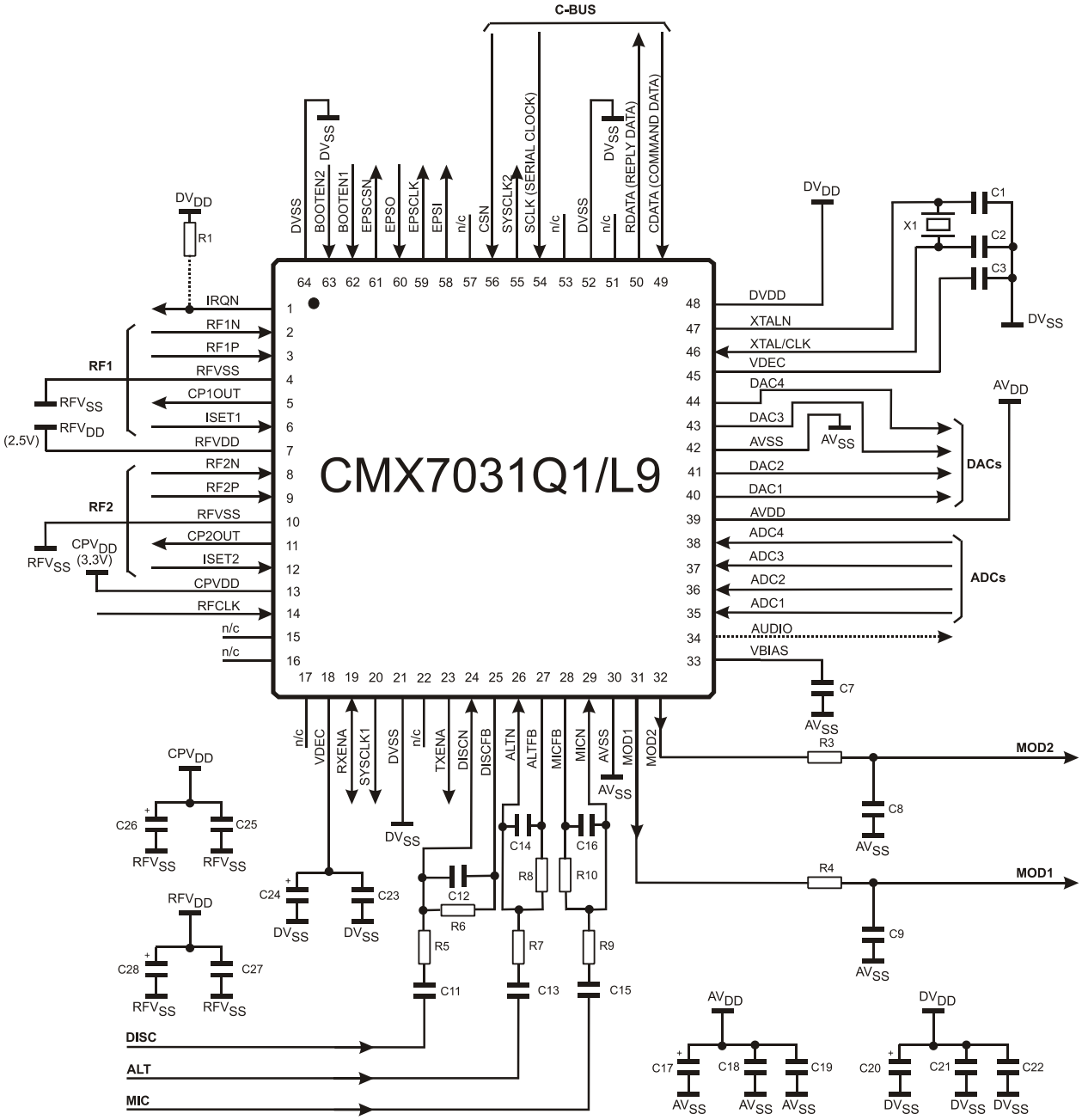


Figure 2 CMX7031 Recommended External Components

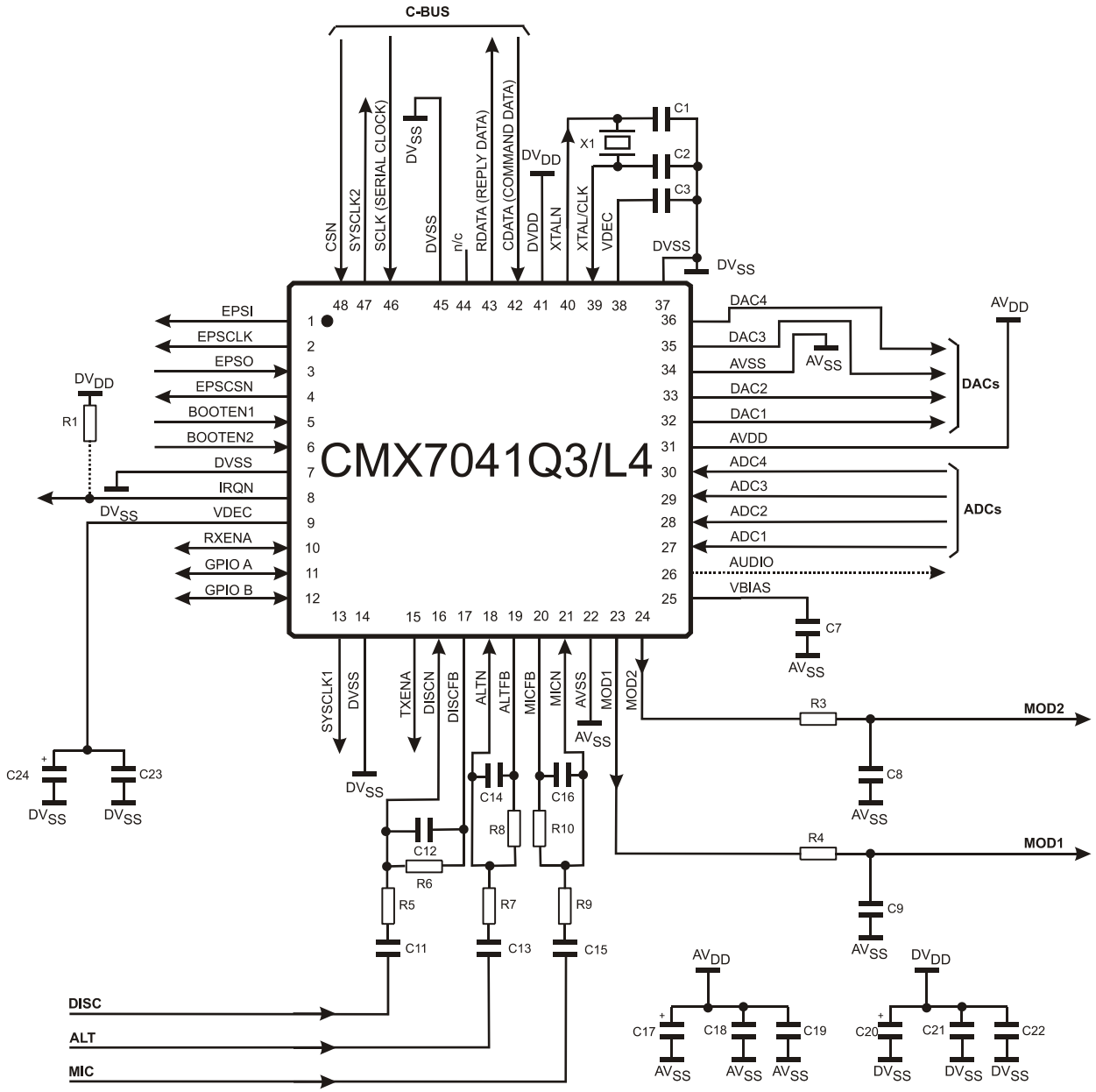


Figure 3 CMX7041 Recommended External Components

R1	100kΩ	C1	18pF	C11	See note 5	C21	10nF
R2	100kΩ	C2	18pF	C12	100pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10nF
R4	100kΩ	C4	*not used*	C14	100pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5	C25	10nF
R6	100kΩ	C6	100pF	C16	180pF	C26	10µF
R7	See note 3	C7	100nF	C17	10µF	C27	10nF
R8	100kΩ	C8	100pF	C18	10nF	C28	10µF
R9	See note 4	C9	100pF	C19	10nF	X1	6.144MHz
R10	100kΩ	C10	*not used*	C20	10µF		See note 1

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 6.144MHz crystal is assumed, other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain (assuming C11 is not present) of the discriminator input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the discriminator input signal range specified in 7.19.2.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the alternative input as follows:

$$|GAIN_{ALT}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 7.19.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 7.19.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C11, C13 and C15 should be selected to maintain the lower frequency roll-off of the microphone, alternative and discriminator inputs as follows:

$$C11 \geq 470nF \times |GAIN_{DISC}|$$
$$C13 \geq 1.0\mu F \times |GAIN_{ALT}|$$
$$C15 \geq 30nF \times |GAIN_{MIC}|$$

   C11 should be chosen to optimise the frequency and response times of the CTCSS/DCS decoders. Some applications may require this capacitor to be increased to 1µF.

6. ALT and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AVss.

7. C5 (AUDIO out) should be increased to 1.0µF if frequencies below 300Hz need to be used on this pin.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

5. PCB Layout Guidelines and Power Supply Decoupling

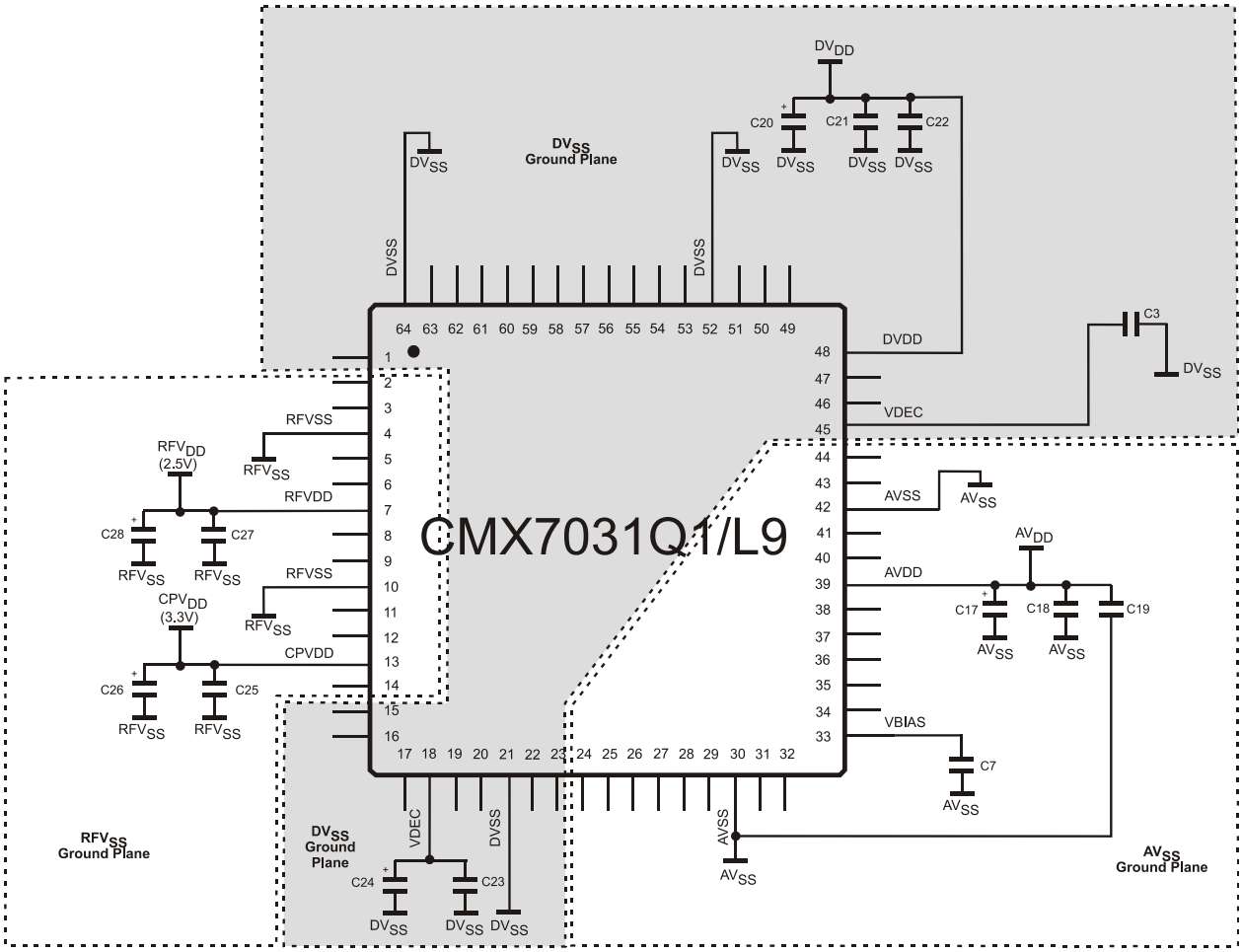


Figure 4 CMX7031 Power Supply Connections and De-coupling

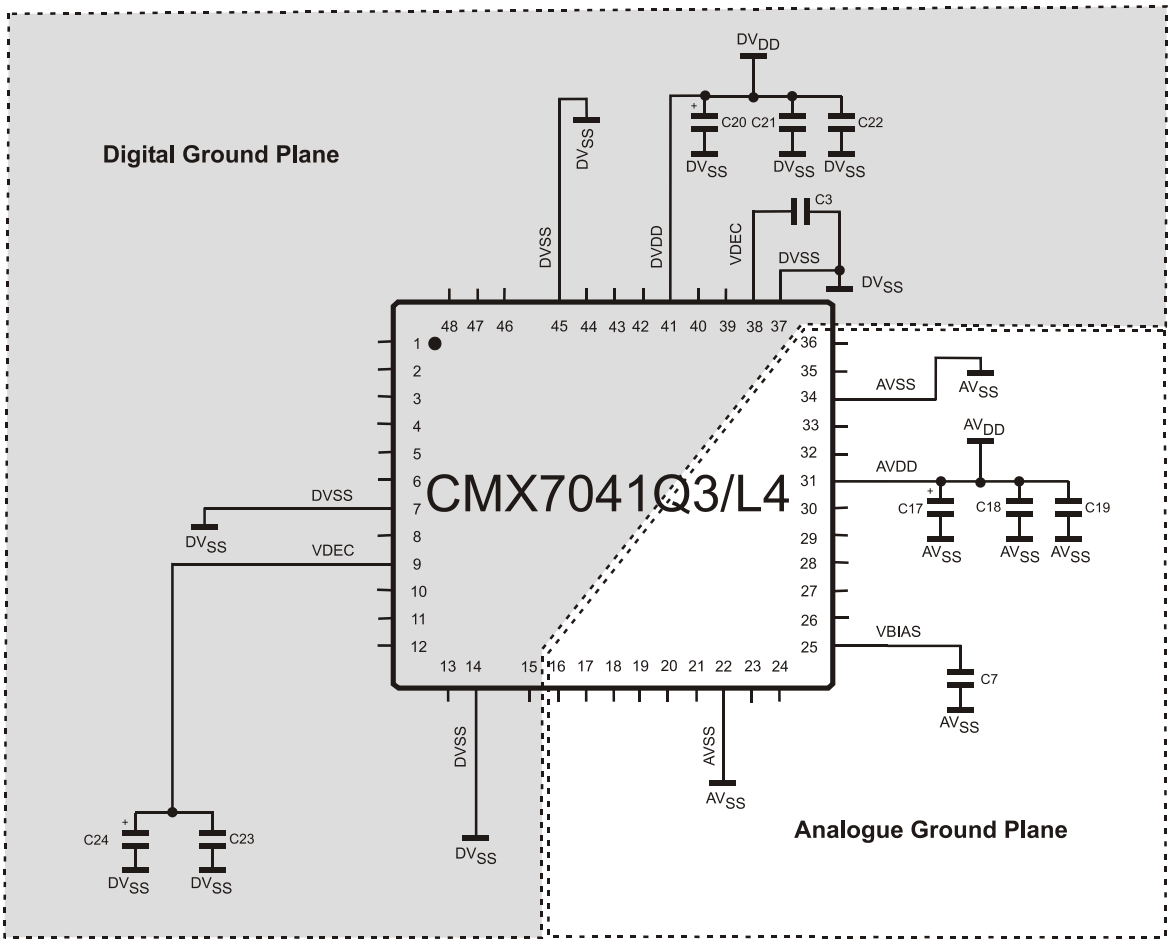


Figure 5 CMX7041 Power Supply Connections and De-coupling

Component Values as per Figure 2.

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the device and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22, C24 and C25 should be as close as possible to the device. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS}, RFV_{SS} and DV_{SS} supplies in the area of the CMX7031, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal X1 may be replaced with an external clock source.

The 2.5V V_{DEC} output can be used to supply the 2.5V RFV_{DD}, to remove the need for an external 2.5V regulated supply. V_{DEC} can be directly connected to RFV_{DD}, in which case C23 should be omitted.

6. General Description

The CMX7031/CMX7041 are intended for use in half duplex analogue two way mobile radio or family radio equipment and is particularly suited to both the PMR/Marine markets and enhanced MURS/GMRS/FRS with GPS terminal designs. The CMX7031/CMX7041 provide radio signal encoder and decoder functions for: Audio, Inband tones, DTMF, XTCSS, CTCSS, DCS and MSK/FFSK/FSK data, permitting simple to sophisticated levels of tone control and data transfer. A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The CMX7031/CMX7041 include a crystal clock generator, with buffered output, to provide a common system clock if required. A block diagram of the CMX7031/CMX7041 is shown in Figure 1.

The signal processing blocks can be individually assigned to either of two signal processing paths, which in turn, can be routed from any of the three audio/discriminator input pins. This allows for a very flexible routing architecture and allows the facility for different processing blocks to act on different analogue inputs. Eg: CTCSS may be processed from the DISC input, while Selcall can be processed from the ALT input in parallel. For Marine use, it would be typical to route Rx Audio from the working channel receiver through from the DISC input, while at the same time routing the DSC FSK modem from the DSC channel 70 receiver from the ALT input.

Tx functions:

- Single/dual microphone inputs with input amplifier and programmable gain adjustment
- Filtering selectable for 12.5kHz and 25kHz channels
- Selectable pre-emphasis
- Selectable compression
- Selectable frequency inversion voice scrambling
- Selectable Audio Processing order
- 2-point modulation outputs with programmable level adjustment
- I/Q modulation outputs with programmable level adjustment
- Pre-programmed 51 tone CTCSS encoder
- 120/180 degree CTCSS phase shift generation
- Programmable 23/24bit DCS encoder
- Programmable Selcall generator
- Programmable audio tone generator (for custom audio tones)
- Programmable DTMF generator
- Pre-programmed XTCSS and Inband tone encoder
- 1200/2400 baud MSK/FFSK modem and data packet encoder (suitable for text messaging/paging, caller identification, caller location, digital poll of remote radio location, GPS information in NMEA 0183 format, data transfer, MPT1327 etc.) incorporating interleaving, FEC, CRC and data scrambler
- 1200bps FSK modem for DSC use (to ITU-R M.493-11). Also offers support for enhanced DSC functions (support for DSC expansion sequences and transmission of continuous distress signals)
- 559bps PSK modem
- Tx Enable output

Rx functions:

- Single/dual demodulator inputs with input amplifier and programmable gain adjustment
- Audio-band and sub-audio rejection filtering
- Selectable de-emphasis
- Selectable expansion
- Selectable frequency inversion voice de-scrambling
- Selectable Audio Processing order
- Software volume control
- 1 from 51 CTCSS decoder + Tone Clone™ mode
- 120/180 degree CTCSS phase shift detection
- 23/24bit DCS decoder
- Selcall decoder
- DTMF decoder

- Pre-programmed Inband tone decode with XTCSS 4-tone addressing
- 1200/2400 baud MSK/FFSK data packet decoder with automatic bit rate recognition, 16 bit frame sync detector, error correction, data de-scrambler and packet disassembly
- 1200bps FSK modem for DSC use (to ITU-R M.493-11). Also offers support for enhanced DSC functions (support for DSC expansion sequences and transmission of continuous distress signals)
- NWR SAME and WAT detector
- Rx Enable output

Auxiliary Functions:

- 2 flexible Integer-N RF synthesisers (CMX7031 only)
- 2 programmable system clock outputs
- 2 auxiliary ADCs with selectable input paths
- 4 auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- C-BUS, 4 wire high speed synchronous serial command/data bus
- Open drain IRQ to host
- 2 GPIO pins (CMX7041 only)
- EEPROM boot mode
- C-BUS boot mode
- SPI-Codec (only available when FI is loaded into CMX7131/CMX 7141 devices)

7. Detailed Descriptions

7.1. Xtal Frequency

The CMX7031/CMX7041 are designed to work with a Xtal or external frequency source of 6.144MHz. If this default configuration is not used, then Program Register Block 3 (see User Manual 9.2.4) needs to be loaded with the correct values to ensure that the device will work to specification with the user specified clock frequency. A table of common values can be found in Table 2. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24.576MHz can be used.

The register values in Table 2 are shown in hex (however only the lower 10 bits are relevant), the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode).

Table 2 Xtal/clock Frequency Settings for Program Block 3

Program Register			External frequency source (MHz)							
			3.579	**6.144**	9.216	12.0	12.8	16.368	16.8	19.2
P3.2	Idle	GP Timer	*$017*	**$018**	$018	$019	$019	*$018*	$019	$018
P3.3		VCO output and AUX clk divide	*$085*	**$088**	$08C	*$10F*	*$110*	*$095*	*$115*	$099
P3.4	Rx or Tx	Ref clk divide	*$043*	**$040**	$060	$07D	$0C8	$155	$15E	$0C8
P3.5		PLL clk divide	*$398*	**$200**	$200	$200	$300	$400	$400	$200
P3.6		VCO output and AUX clk divide[§]	*$140*	**$140**	$140	$140	$140	$140	$140	$140
P3.7		Internal ADC/DAC clk divide	*$008*	**$008**	$008	$008	$008	$008	$008	$008

[§] *Note that if the SPI-Codec routing is used in Rx mode on a CMX7131/CMX7141 then this value will need to be changed from $140 to $0C0.*

7.2. Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7031/CMX7041 and the host µC; this interface is compatible with microwire, SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 7.20.1.

The CMX7031/CMX7041 will monitor the state of the C-BUS registers that the host has written to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

To minimise activity on the C-BUS interface, optimise response times and ensure reliable data transfers, it is advised that the IRQ facility be utilised (using the IRQ mask register, $CE). It is permissible for the host to poll the IRQ pin if the host uC does not support a fully interrupt-driven architecture. This removes the need to continually poll the C-BUS status register ($C6) for status changes.

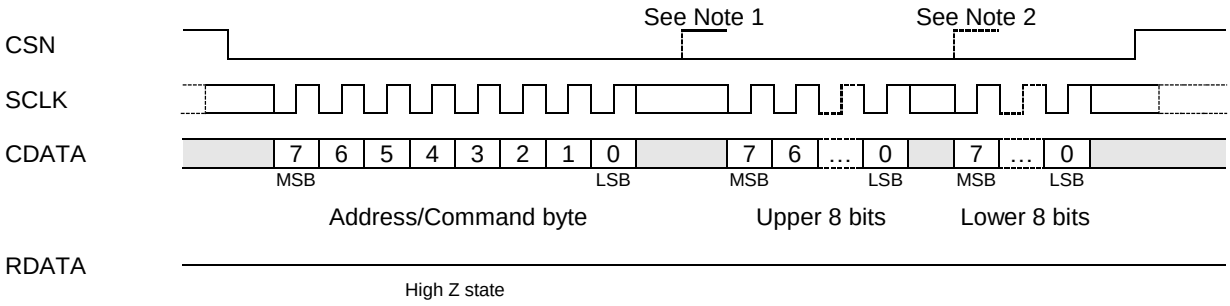
7.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7031/CMX7041's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single Address byte sent from the µC which may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX7031/CMX7041's Write Only Registers, or one or more data byte(s) read out from one of the CMX7031/CMX7041's Read Only Registers, illustrated in Figure 6.

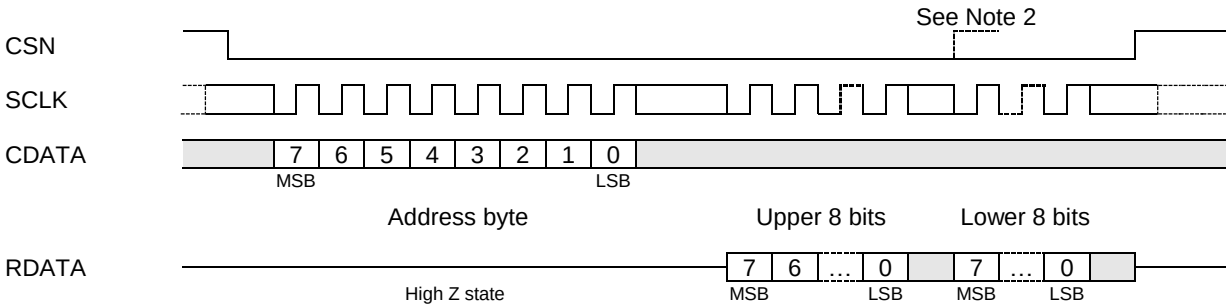
Data sent from the µC on the CDATA line is clocked into the CMX7031/CMX7041 on the rising edge of the SCLK Clock input. RDATA sent from the CMX7031/CMX7041 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 8.2. Note that, due to internal timing constraints, there maybe a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 6 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and REDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3. Function Image™ Load and Activation

The Function Image™(FI) file, which defines the operational capabilities of the device, may be obtained from the CMLTechnical Portal, following product registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external EEPROM. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7031/CMX7041 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low-current pulldown devices.

For C-BUS load operation, both pins should be pulled high by connecting them to V_{DD} either directly or via a 220kΩ resistor (see Table 3).

For EEPROM load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the EEPROM in-situ from the host, either a jumper to V_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Table 3).

Once the FI has been loaded, the CMX7031/CMX7041 performs these actions:

(1) the product identification code $7031 is reported in C-BUS register $C5
(2) the FI version code is reported in C-BUS register $C9
(3) the two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) the device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) once activated, the device initialises fully, enters idle mode and becomes ready for use, and the Programming Flag (bit 0 of the Status register, $C6) will be set.

The checksums should be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and become unresponsive to all further host commands (including General Reset). A power-on reset is required to recover from this state.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 3 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
EEPROM load	0	1
No FI load	0	0

Note: In the rare event that a General Reset needs to be issued without the requirement to re-load the FI, the BOOTEN pins must both be cleared to '0' before issuing the Reset command. The Checksum values will be reported and the Device Activation code will need to be sent in a similar manner as that shown in Figure 8. There will not be any FI loading delay. This assumes that a valid FI has been previously loaded and that V_{DD} has been maintained throughout the reset to preserve the data.

7.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7031/CMX7041 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7031/CMX7041 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX7031/CMX7041.

Each time the device is powered up its Function Image™ must first be loaded and then activated. These two steps assign internal device resources and determine all device features. The device does not operate until the Function Image™ is loaded and activated.

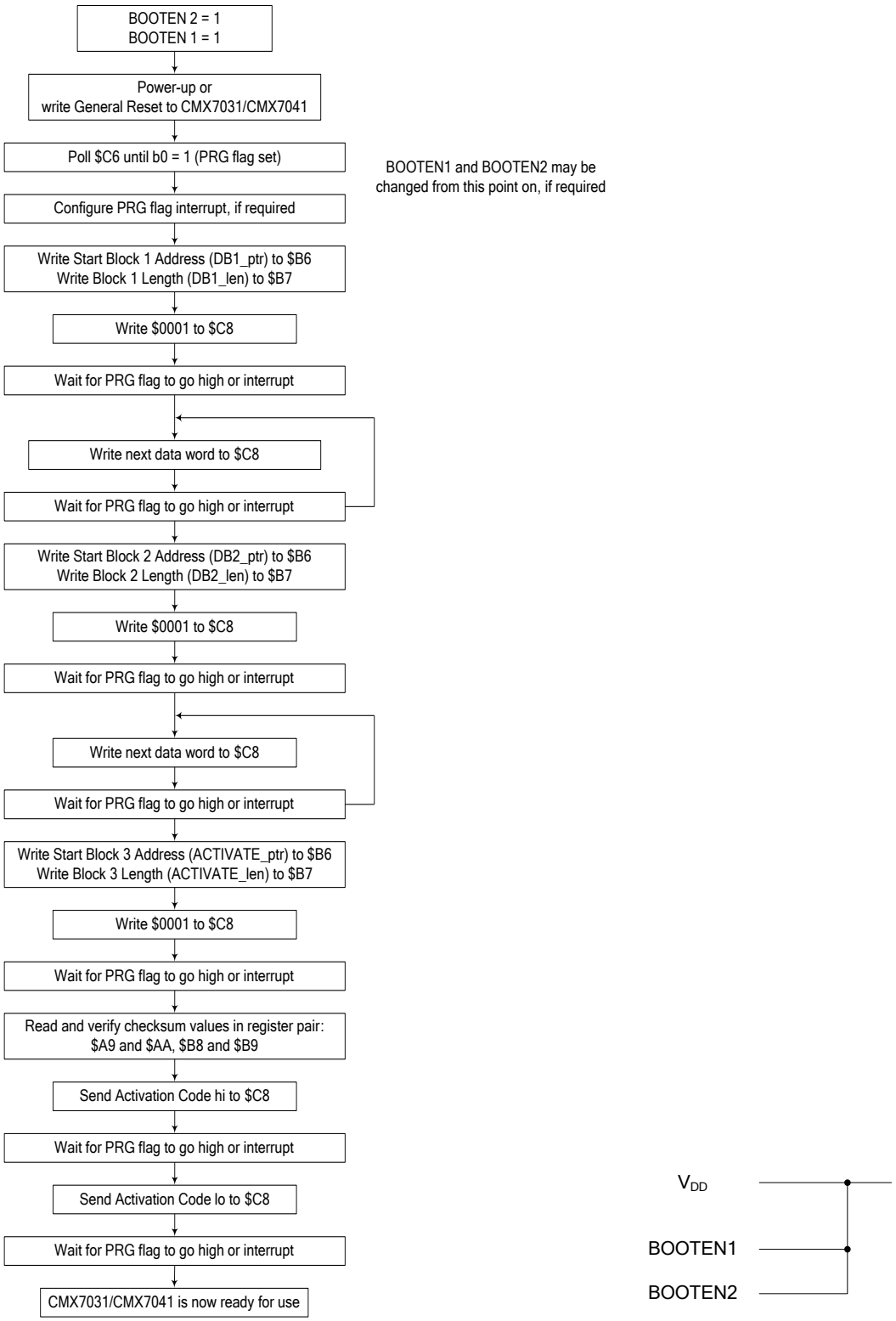


Figure 7 FI Loading from Host

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

7.3.2 FI Loading from EEPROM

The FI must be converted into a format for the EEPROM programmer (normally Intel Hex) and loaded into the EEPROM either by the host or an external programmer. The CMX7031/CMX7041 needs to have the BOOTEN pins set to EEPROM load, and then on power-on, or following a C-BUS General Reset, the CMX7031/CMX7041 will automatically load the data from the EEPROM without intervention from the host controller.

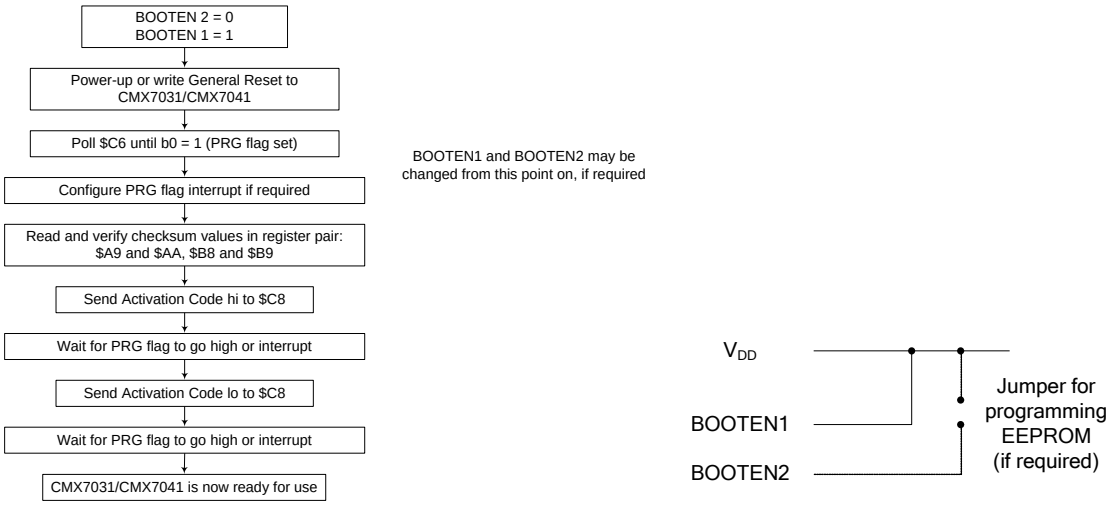


Figure 8 FI Loading from EEPROM

The CMX7031/CMX7041 has been designed to function with Atmel AT25HP512 serial EEPROM and the AT25F512 flash EEPROM devices[2], however other manufacturers parts may also be suitable. The time taken to load the FI is dependant on the Xtal frequency, with a 6.144MHz Xtal, it should load in less than 1 second.

[2] Note that these two devices have slightly different addressing schemes. FI 1.5 is compatible with both schemes, whereas previous FI 's were only compatible with the AT25HP512 addressing scheme.

7.4. Device Control

The CMX7031/CMX7041 can be set into many modes to suit the environment in which it is to be used. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

1. enable the relevant hardware sections via the Power Down Control register
2. set the appropriate mode registers to the desired state (Audio, Inband, Sub-Audio, Data etc.),
3. select the required Signal Routing and Gain
4. use the Mode Control register to place the device into Rx or Tx mode.

Note that when the device changes from Idle mode to either Tx or Rx, the MOD or AUDIO outputs may exhibit a momentary “spike” as the output stages become active. This can be negated by selecting the appropriate output routing path a short time (approx. 1ms) after changing mode.

To conserve power when the device is not actively processing an analogue signal, place the device into Idle mode. Additional Powersaving can be achieved by disabling the unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled.

See:

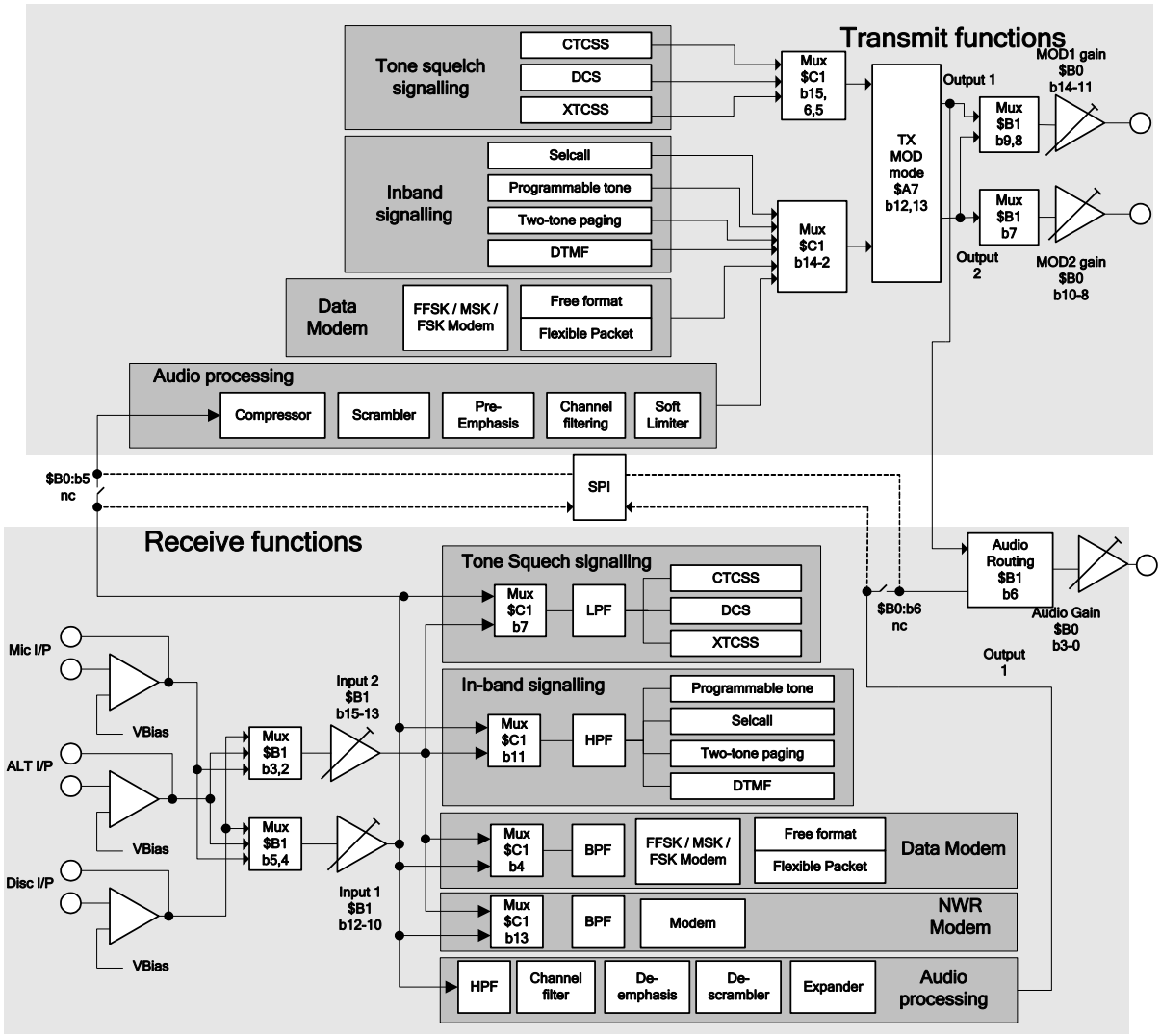
- Power Down Control – $C0 write
- Mode Control – $C1 write

7.4.1 Signal Routing

The CMX7031/CMX7041 offers a very flexible routing architecture, with three signal inputs, two separate signal processing paths and a selection of two modulator outputs (to suit 2-point as well as I/Q modulation schemes) and a single Audio output. Each of the signalling processing blocks can be independently routed to either of the Input blocks, which can be routed to any of the three input signal pins. The Audio/Voice processing blocks are always routed to Input 1. The outputs from signal processing blocks are determined by the settings of the AuxADC and TX MOD mode register in Tx mode.

See:

- Input Gain and Output Signal Routing – $B1 write
- AuxADC and TX MOD Mode – $A7 write
- Mode Control – $C1 write



Note: SPI-Codec routing is only available when this Function Image™ is loaded into the CMX7131/CMX7141.

Figure 9 Signal Routing

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Gain control available via the Programming registers and the Audio Tone register.

See:
- Analogue Output Gain – $B0 write
- Input Gain and Output Signal Routing – $B1 write
- Audio Tone – $CD: 16-bit write-only

Additionally, on the CMX7131 and CMX7141 only, the Input1 or Output1 signals may be “intercepted” and routed to the full-duplex SPI port, where they are presented and received as 16-bit signed PCM values sampled at 8ksps, to allow for external processing of these signals. This port is shared with the Serial Memory, but uses the SSOUT pin as the chip select signal. By default, this function is disabled.

There is no independent SPI port on the CMX7031 or CMX7041, so this “intercept” routing is not available.

See:
- Analogue Output Gain – $B0 write

7.4.2 Mode Control

The CMX7031/CMX7041 operates in one of three modes:

- IDLE
- Rx
- Tx

At power-on or following a Reset, the device will automatically enter IDLE mode, which allows for the maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled). It is only possible to write to the Programming register whilst in IDLE mode.

See:
- Mode Control – $C1 write

7.5. Audio Functions

The audio signal can be processed in several ways, depending on the implementation required, by selecting the relevant bits in the Audio Control – $C2 write register. In both Rx and Tx, a selectable channel filter to suit either the 12.5kHz or 25kHz TIA/ETSI channel mask can be selected. This filter also incorporates a soft limiter to reduce the effects of over-modulation. Other features include 300Hz HPF, pre- and de-emphasis, companding and frequency inversion scrambling, all of which may be individually enabled[3]. The order in which these features are executed is selectable to ensure compatibility with existing implementations and provide optimal performance (see User Manual section 9.2.5). The default configuration is backwards compatible with the CMX7031/7041 FI-1.2 implementation, however the alternate settings shown in the User Manual section 9.2.5 may provide better performance.

7.5.1 Audio Receive Mode

The CMX7031/CMX7041 operates in half duplex, so whilst in receive mode the transmit path (microphone input and modulator output amplifiers) can be disabled and powered down if required. The AUDIO output signal level is equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to minimise unwanted audible transients. The Off/Powersave level of the modulator outputs is the same as the V_{BIAS} pin, so the audio output level must also be at this level before switching.

See:

- Audio Control – $C2 write

Receiving Audio Band Signals

When a voice-based signal is being received, it is up to the host µC, in response to signal status information provided by the CMX7031/CMX7041, to control muting/enabling of the audio signal to the AUDIO output.

The discriminator path through the device has a programmable gain stage. Whilst in receive mode this should normally be set to 0dB (the default) gain.

Receive Filtering

The incoming signal is filtered, as shown in Figure 10 (with the 300Hz HPF also active), to remove sub-audio components and to minimise high frequency noise. When appropriate, the audio signal can then be routed to the AUDIO output. Separate selectable filters are available for:

- 300Hz High Pass (to reject sub-audible signalling)
- 2.55kHz Low Pass (for 12.5kHz channel operation)
- 3.0kHz Low Pass (for 25kHz channel operation)

Note that with no filters selected, the low frequency response extends to below 5Hz at the low end but still rolls off above 3.3kHz at the top end.

[3] The typical responses shown in Figure 10, Figure 12, Figure 13 and Figure 14 were recorded using the PE0201 Evkit, DISC in to AUDIO and MOD1 out.

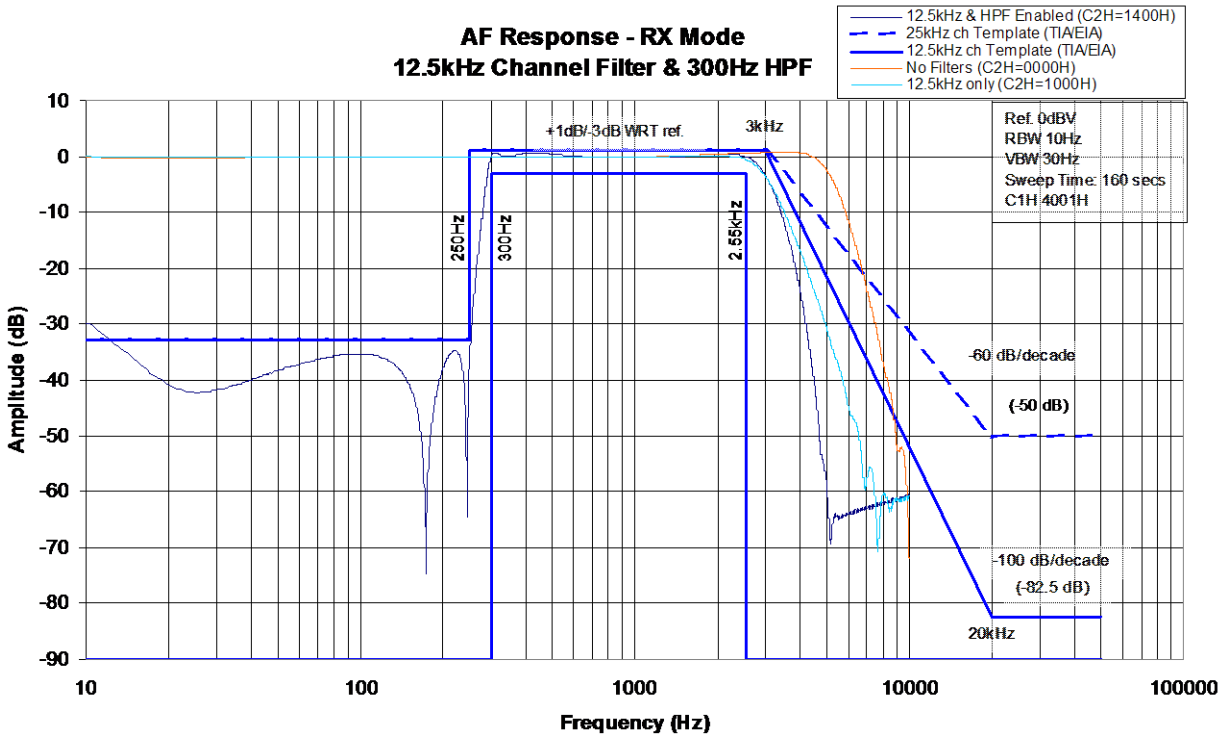


Figure 10 Rx 12.5kHz Channel Audio Filter Frequency Response

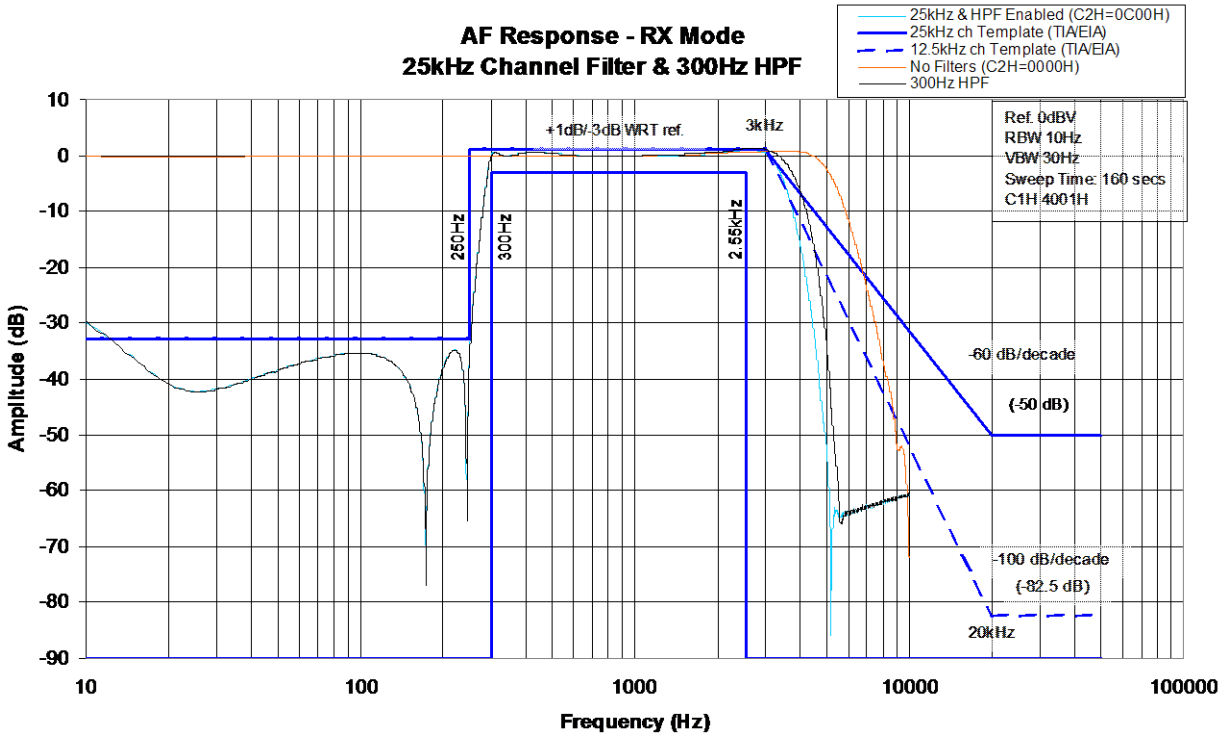


Figure 11 Rx 25kHz Channel Audio Filter Frequency Response

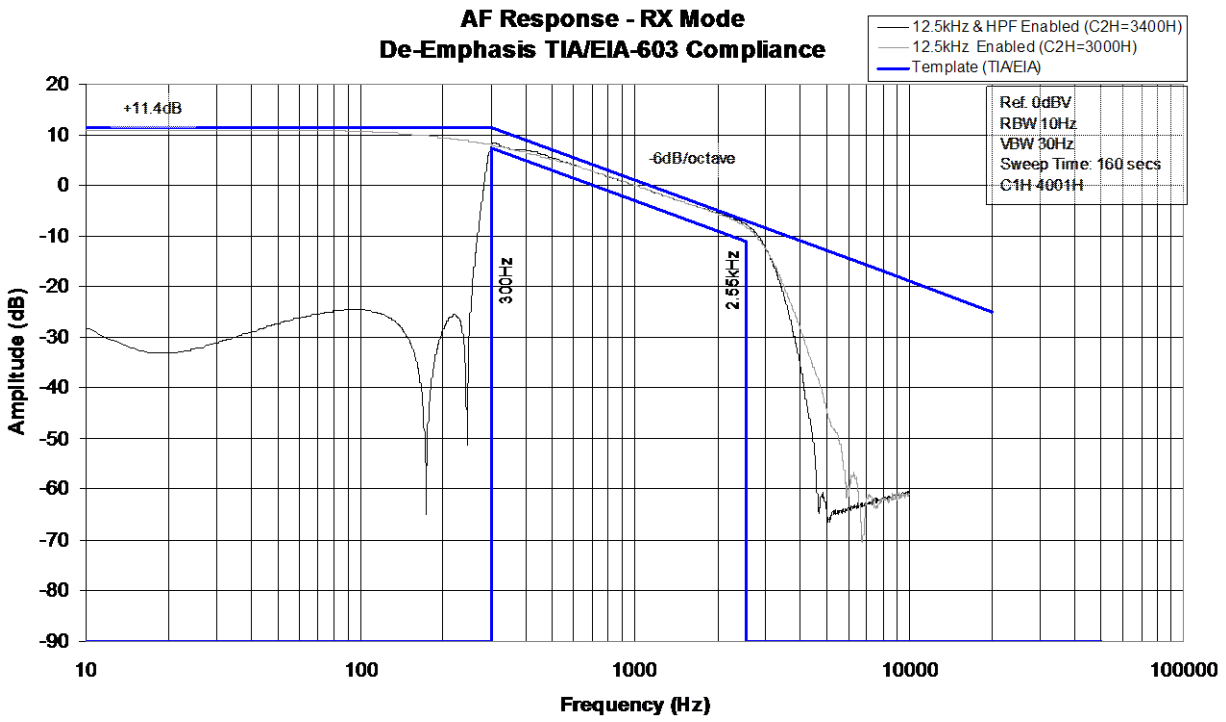


Figure 12 De-emphasis Curve for TIA/EIA-603 Compliance

De-emphasis
Optional de-emphasis at -6dB per octave from 300Hz to 3000Hz (shown in Figure 12) can be selected, to facilitate compliance with TIA/EIA-603, EN 300 086, EN 301 025 etc. The template shows the +1, -3dB limits.

Rx Companding (Expanding)
The CMX7031/CMX7041 incorporates an optional syllabic compandor in both transmit and receive modes. This expands received audio band signals that have been similarly compressed in the transmitter to enhance dynamic range. See section 7.5.3 and:

- Audio Control – $C2 write

Audio De-scrambling
The CMX7031/CMX7041 incorporates an optional frequency inversion de-scrambler in receive mode. This de-scrambles received audio band signals that have been scrambled in the transmitter. The inversion frequency defaults to 3300Hz, but may be modified by writing to P4.8.

See:
- Audio Control – $C2 write

7.5.2 Audio Transmit Mode

The device operates in half duplex, so when the device is in transmit mode the receive path (discriminator and audio output amplifiers) should be disabled, and can be powered down, by the host µC.

Two modulator outputs with independently programmable gains are provided to facilitate single or two-point modulation, separate sub-audio and audio band outputs. If one of the modulator outputs is not used it can be disabled to conserve power.

To avoid spurious transmissions when changing from Rx to Tx the MOD 1 and MOD 2 outputs are ramped to the quiescent modulator output level, V_{BIAS} before switching (if enabled by b7 of the Analogue Gain register, $B0). Similarly, when starting a transmission, the transmitted signal is ramped up from the

quiescent V_{BIAS} level and when ending a transmission the transmitted signal is ramped down to the quiescent V_{BIAS} level. The ramp rates are set in the Programming register P4.6. When the modulator outputs are disabled, their outputs will be set to V_{BIAS}. When the modulator output drivers are powered down, their outputs will be floating (high impedance), so the RF modulator will need to be turned off.

For all transmissions, the host µC must only enable signals after the appropriate data and settings for those signals are loaded into the C-BUS registers. As soon as any signalling is enabled the CMX7031/CMX7041 will use the settings to control the way information is transmitted.

A programmable gain stage in the microphone input path facilitates a host controlled VOGAD capability, or an internal AGC function may be used.

See:

- Audio Control – $C2 write
- AuxADC and TX MOD Mode – $A7 write
- Input Gain and Output Signal Routing – $B1 write

Processing Audio Signals for Transmission over Analogue Channels

The microphone input(s), with programmable gain, can be selected as the audio input source. Pre-emphasis is selectable with either of the two analogue Tx audio filters (for 12.5kHz and 25kHz channel spacing). These are designed for use in EN 300 086, TIA/EIA-603 or EN 301 025 compliant applications. When the 300Hz HPF is enabled, it will attenuate sub-audio frequencies below 250Hz by more than 33dB with respect to the signal level at 1kHz.

These filters, together with a built in limiter, help ensure compliance with EN 300 086 and EN 301 025 (25kHz and 12.5kHz channel spacing) when levels and gain settings are set up correctly in the target system.

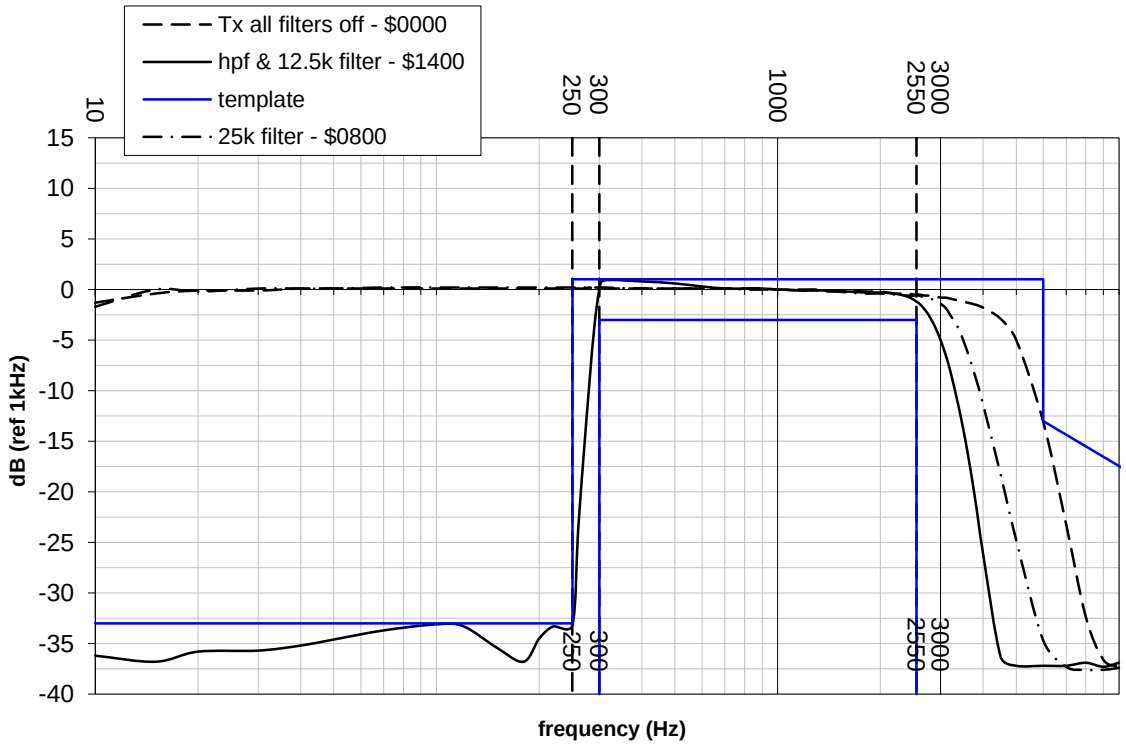


Figure 13 Tx Channel Audio Filter Response and Template (ETSI)

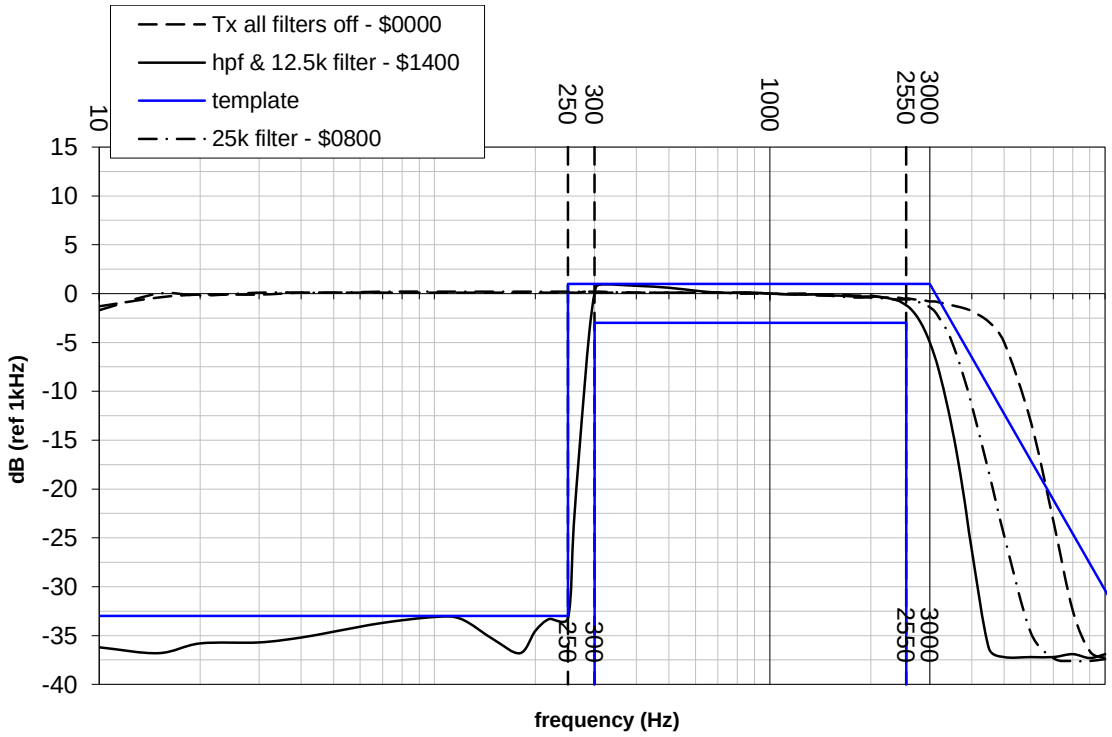


Figure 14 Tx Channel Audio Filter Response and Template (TIA)

The characteristics of the 12.5kHz channel filter fit the template shown in Figure 13 and Figure 14. This filter also facilitates implementation of systems compliant with TIA/EIA-603 'A' , 'B' and 'C' bands.

The CMX7031/CMX7041 provides selectable pre-emphasis filtering of +6dB per octave from 300Hz to 3000Hz, matching the template shown in Figure 15.

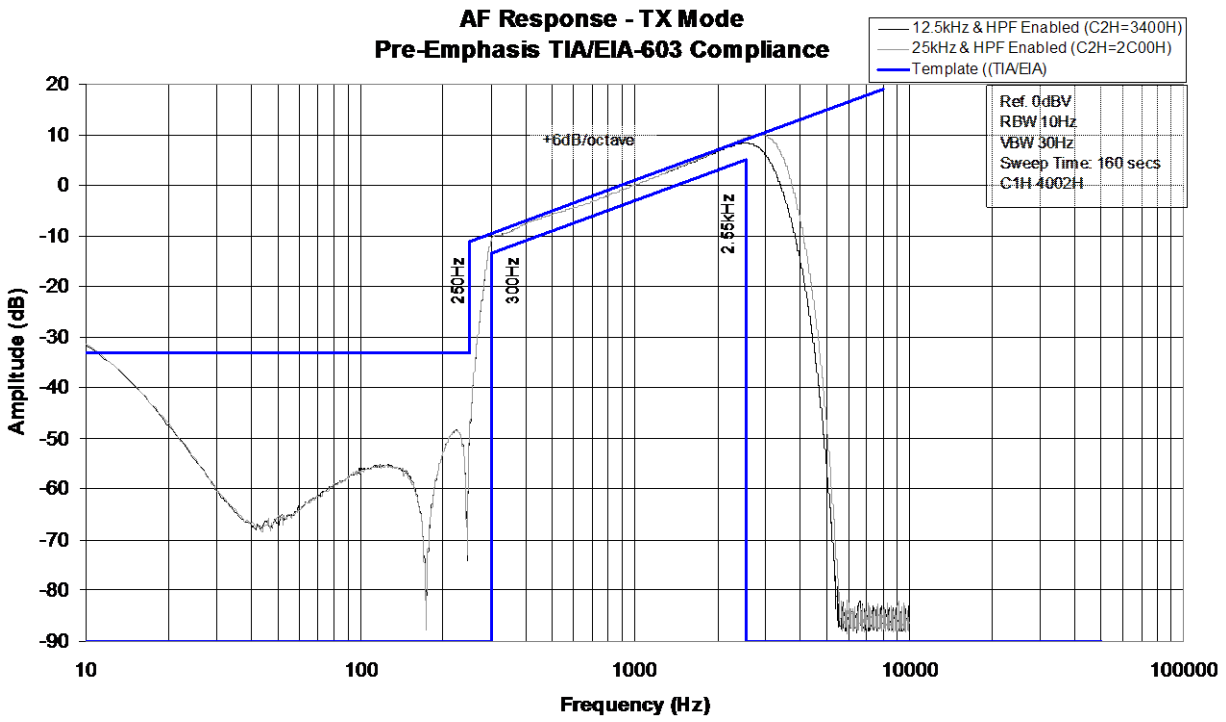


Figure 15 Audio Frequency Pre-emphasis

Modulator Output Routing

The sub-audio component can be combined with the audio band signal and this composite signal routed to both MOD1 and MOD2 outputs, or the sub-audio and audio band signal can be output separately (sub-audio to MOD2 and audio band to MOD1), in accordance with the settings of:

- AuxADC and TX MOD Mode – $A7 write
- Input Gain and Output Signal Routing – $B1 write

Alternatively, the combined sub-audio and audio band composite signal can be output on MOD1 and 2 in a phase/quadrature (I/Q) format suitable for direct upconversion to the final RF signal. Due to the nature of the I/Q modulation, this mode is only feasible in RF channels/systems which have a maximum frequency deviation of 3kHz or less. Additional test modes are provided for calibrating external circuits. Tx I/Q mode is particularly suitable for data transmission.

Input AGC

An Automatic Gain Control system can be enabled by setting the relevant bits of the Program register P4.9. The setting of the Input 1 Gain stage is recorded when the device enters Tx mode and if the signal exceeds the pre-set threshold, the Input 1 Gain is automatically reduced in 3.2dB steps until it falls within the operational levels or the range of the gain stage is exhausted. When the signal level drops, the gain will be automatically increased in 3.2dB steps at the rate set in P4.9 until the initial value has been reached. For maximum effect the system should be designed such that the +22.4dB setting of the Input 1 Gain stage achieves the nominal levels. To ensure consistent operation, it is recommended that the Input 1 Gain stage value be re-initialised before entering Tx mode. The signal that is used as an input to this process can be selected to be either:

- Output of Input 1 gain stage
- Output of the Pre-emphasis filter

by selecting the relevant bit in P4.9. The Pre-emphasis option should only be chosen if this block is actually in use.

- Input Gain and Output Signal Routing – $B1 write
- Program Block 4 – Gain and Offset Setup:

Tx Companding (Compressing)
The CMX7031/CMX7041 incorporates an optional syllabic compandor in both transmit and receive mode. This compresses audio band signals before transmission to enhance dynamic range. See section 7.5.3 and:

- Audio Control – $C2 write

Audio Scrambling
The CMX7031/CMX7041 incorporates an optional frequency inversion scrambler in transmit mode. This scrambles audio band signals, to be de-scrambled in the receiver. The inversion frequency defaults to 3300Hz, but maybe modified by writing to P4.8.

See:
- Audio Control – $C2 write

7.5.3 Audio Compandor

The compandor is comprised of a compressor and an expandor. The compressor's function is to reduce the dynamic range of a given signal by attenuating larger amplitudes while amplifying smaller amplitudes. The expandor's function is to expand the dynamic range of a given signal by attenuating small amplitude signals (e.g. noise) while amplifying large amplitude signals. The compressor is used prior to transmission and the expandor is used in the receiver. Hence, using a compandor will enhance performance in a communication system by transmitting a compressed signal, which is less likely to be corrupted by noise, and then at the receiver expanding the compressed signal, which will push the noise picked up during transmission down further.

The CMX7031/CMX7041 uses a "syllabic compandor." This type of compandor, as opposed to the instantaneous compandor (e.g. μ/A-law PCM), responds to changes in the average envelope of the signal amplitude according to a syllabic time constant τ. Typically the steady state output for the compressor is proportional to the square root of the input signal. Ie:, for a 2 dB change in input signal, the output change will be 1 dB. Generally for voice communication systems a compressor is expected to have an input dynamic range of 60 dB, providing an output dynamic range of 30 dB. The expandor does the inverse.

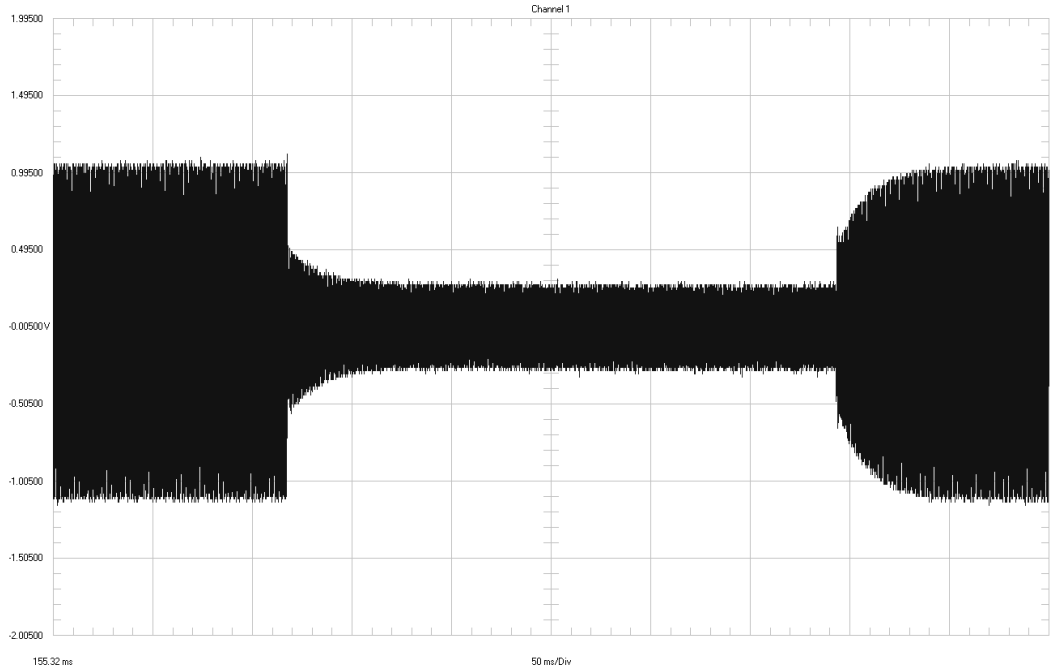


Figure 16 Expandor Transient Response

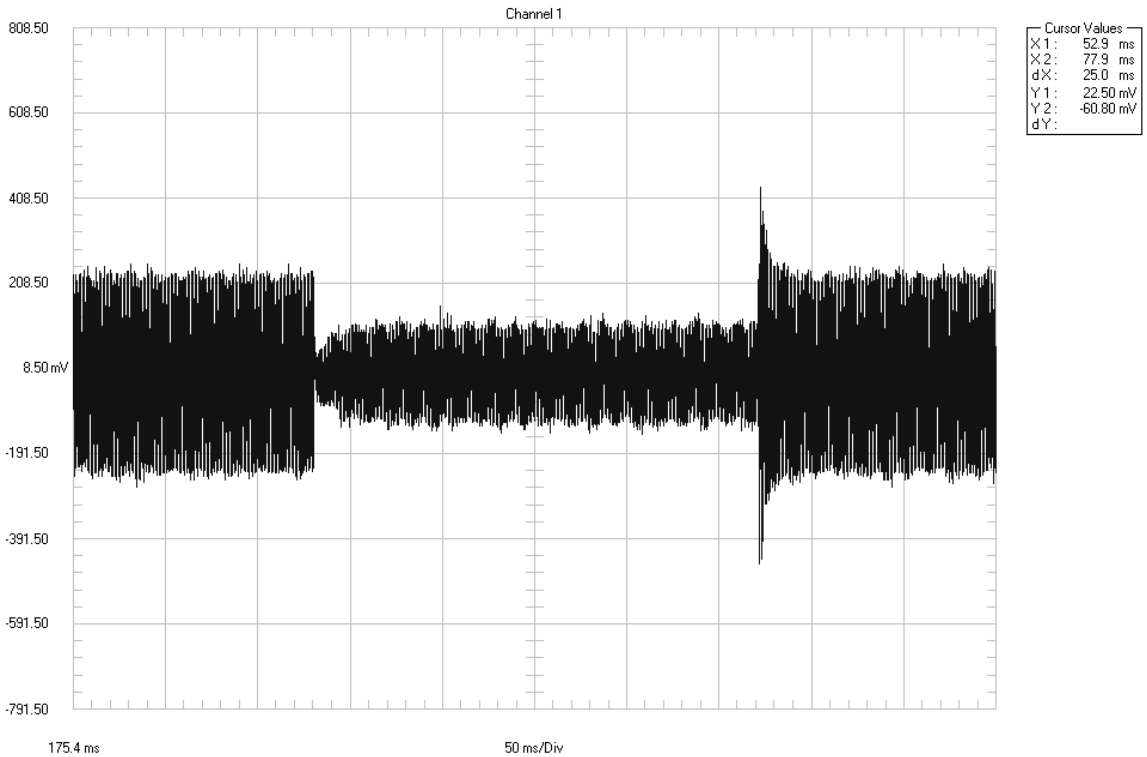


Figure 17 Compressor Transient Response

7.6. Sub-audio Signalling

Sub-audio signalling is available in the audio band below 260Hz. When sub-audio signalling is enabled, the 300Hz HPF in the audio section should also be enabled to remove the sub-audio signalling from the audio signal (in both Tx and Rx). Both CTCSS tones and DCS codes are supported, as well as a special "tone-cloning" mode which will report back any received CTCSS tone rather than look for a specific tone. There are 51 CTCSS tones defined in the CMX7031/CMX7041 and there is provision for a user-specified tone. Tone inversion to implement "Reverse Tone Burst" for squelch tail elimination can be accomplished by inverting the output of the MOD1 and MOD2 outputs ($B0) or by using the phase change facility in the Audio Control register ($C2).

The DCS coder/decoder supports both 23- and 24-bit modes with both true and inverse modulation formats and the 134Hz end of transmission burst.

The CTCSS tone and DCS code values for both Rx and Tx operation are specified in the Audio Control register ($C2), in the lowest 8 bits (shown in decimal):

- 0 no tone
- 1 to 83 DCS code 1 to 83
- 84 User-defined DCS code
- 101 to 183 Inverted DCS code 1 to 83
- 184 Inverted user-defined DCS code
- 200 CTCSS Tone Clone™ mode
- 201 to 254 CTCSS tones 1 to 51, User, XTCSS and DCSoff tones
- 255 Invalid tone

The CTCSS and DCS functions are enabled by the relevant bits in the Mode Control register, $C1, so that the host can turn the functionality on or off without having to re-program the values in the Audio Control register, $C2.

See:

- Analogue Output Gain – $B0 write
- Mode Control – $C1 write
- Audio Control – $C2 write

7.6.1 Receiving and Decoding CTCSS Tones

The CMX7031/CMX7041 is able to accurately detect valid CTCSS tones quickly to avoid losing the beginning of audio or data transmissions, and is able to continuously monitor the detected tone with minimal probability of falsely dropping out. The received signal is filtered in accordance with the template shown in Figure 18, to prevent signals outside the sub-audio range from interfering with the sub-audio tone detection.

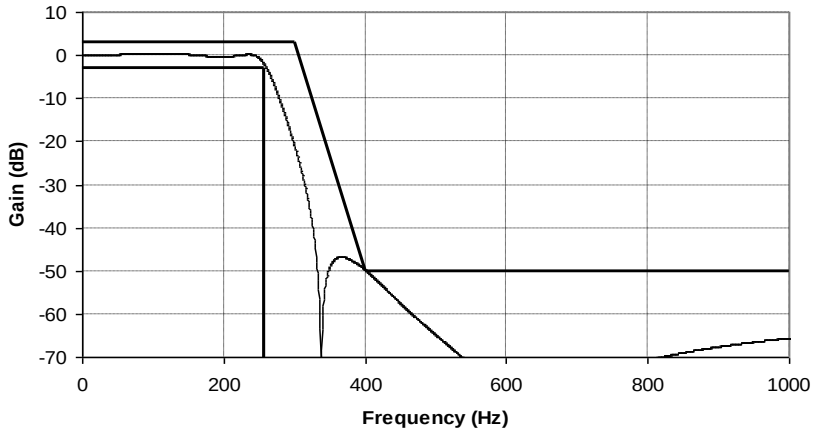


Figure 18 Low Pass Sub-Audio Band Filter for CTCSS and DCS

Once a valid CTCSS tone has been detected, Status register ($C6) b11 will be set and the host µC can then route the audio band signal to the audio output. The audio band signal is extracted from the received signal by band pass filtering as shown in Figure 10.

To optimise the CTCSS tone decoder, adjustable decoder bandwidths and threshold levels allow the user to trade-off decode certainty against signal to noise performance when congestion or range restrict the system performance. The tone decoder bandwidth and threshold level are set in P2.1 of the Programming register ($C8) and the desired tone is programmed in the Audio Control register ($C2). In systems which make use of tones 41 to 50 or other “split” tones (tones in between the frequencies of tones 1 to 40), the CTCSS decoder bandwidth should be reduced to avoid false detection of adjacent tones.

The CMX7031/CMX7041 includes a CTCSS tone phase detector which reacts to a phase change in the received tone of +/- 90 degrees by setting bit 9 of the Tone Status register ($CC) and asserting b11 of the Status register ($C6). This feature can be used to detect both 180 and 120 degree phase changes and so allow the host to mute the audio appropriately (Squelch Tail Elimination).

Tone Cloning™

Tone Cloning™ facilitates the detection of CTCSS tones 1 to 39 in receive mode which allows the device to non-predictively detect any tone in this range. This mode is activated by programming CTCSS Tone Number 00 (b0-7 of Audio Control = 200 decimal). The received tone number will be reported in the Tone Status register and can then be programmed into the Audio Control register by the host µC. The cloned tone will only be active when CTCSS is enabled in the Mode Control register. This setting has no effect in Tx mode and the CTCSS generator will output no signal.

Tone cloning™ should not be used in systems where tones 41 to 51 or other “split” tones (tones between the frequencies of tones 1 to 40) may be received. The all-call tone 40 can still be used after tone cloning has been performed. The CTCSS decoder detection bandwidth should be set to its lowest value (in P2.1 of the Programming Register) to ensure accurate detection.

CTCSS Tones

Table 5 lists the CTCSS tones available, the tone numbers and the equivalent (decimal) values that need to be programmed into the Audio Control register ($C2) and which will be reported back in the Tone Status register ($CC). If enabled, an IRQ will be generated under the following conditions:

Table 4 CTCSS IRQ Conditions

State change from:	To:	IRQ	Tone Status value b7-0
No Tone	Own Tone	yes	Own Tone
Own Tone	No Tone	yes	$00
No Tone	Unrecognised Tone	yes	$FF
Unrecognised Tone	No Tone	yes	$00
No Tone	Invalid Tone	yes	$FF or detected Tone
Invalid Tone	No Tone	yes	$00

T Tone Cloning™ is a trademark of CML Microsystems Plc.

Table 5 CTCSS Tones

Register Value		Tone		Register Value		Tone		Register Value		Tone	
dec	**hex**	**No.**	**Freq (Hz)**	**dec**	**hex**	**No.**	**Freq(Hz)**	**dec**	**hex**	**No.**	**Freq (Hz)**
000	00	n/a	No Tone	218	DA	18	123.0	237	ED	37	241.8
200	C8	0	ToneClone	219	DB	19	127.3	238	EE	38	250.3
201	C9	1	67.0	220	DC	20	131.8	239	EF	39	69.3
202	CA	2	71.9	221	DD	21	136.5	240	F0	40	*62.5*
203	CB	3	74.4	222	DE	22	141.3	241	F1	41	*159.8*
204	CC	4	77.0	223	DF	23	146.2	242	F2	42	*165.5*
205	CD	5	79.7	224	E0	24	151.4	243	F3	43	*171.3*
206	CE	6	82.5	225	E1	25	156.7	244	F4	44	*177.3*
207	CF	7	85.4	226	E2	26	162.2	245	F5	45	*183.5*
208	D0	8	88.5	227	E3	27	167.9	246	F6	46	*189.9*
209	D1	9	91.5	228	E4	28	173.8	247	F7	47	*196.6*
210	D2	10	94.8	229	E5	29	179.9	248	F8	48	*199.5*
211	D3	11	97.4	230	E6	30	186.2	249	F9	49	*206.5*
212	D4	12	100.0	231	E7	31	192.8	250	FA	50	*229.1*
213	D5	13	103.5	232	E8	32	203.5	251	FB	51	*254.1*
214	D6	14	107.2	233	E9	33	210.7	252	FC	52	User
215	D7	15	110.9	234	EA	34	218.1	253	FD	53	XTCSS
216	D8	16	114.8	235	EB	35	225.7	254	FE	54	DCSoff
217	D9	17	118.8	236	EC	36	233.6	255	FF	55	Invalid

Notes:

1. Register value 000 in b0-7 of the Tone Status register ($CC) indicates that none of the above sub-audio tones is being detected. If register value 000 is programmed into the Audio Control register ($C2) and CTCSS enabled in the Mode Control register ($C1), only CTCSS tone 40 (240 decimal) will be scanned for. If CTCSS transmit is selected, this tone setting will cause the CTCSS generator to output no signal.
2. Tone number 40 (240 decimal) provides an all-user CTCSS tone option; regardless of the sub-audio tones set, the CMX7031/CMX7041 will report the presence of this tone whenever the CTCSS detector is enabled. This feature is useful for implementing emergency type calls e.g. All-Call.
3. Tone number 55 (255 decimal) is reported in the Tone Status register ($CC), when CTCSS receive is enabled and a sub-audio tone is detected that does not correspond to the selected tone or the all-call tone (tone number 40). This could be a tone in the sub-audio band which is not in the table or a tone in the table which is not the selected tone or All-Call tone.
4. Tones 40 to 51 (241 to 251 decimal) are not in the TIA-603 standard.
5. Tone number 52 (252 decimal) will select the User Programmable Tone value in Program Block 2 – CTCSS and DCS Setup:
6. Tone number 53 (253 decimal) will select the XTCSS call maintenance tone, 64.7Hz
7. Tone number 54 (254 decimal) will select the DCS turn-off tone, 134.4Hz.
8. Tone Clone, register value 200, is a write-only value to $C2. The received tone number will be reported back in $CC.

7.6.2 Receiving and Decoding DCS Codes

DCS code is in NRZ format and transmitted at 134.4 ±0.4bps. The CMX7031/CMX7041 is able to decode any 23- or 24-bit pattern in either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 6. The CMX7031/CMX7041 can detect a valid DCS code quickly enough to avoid losing the beginning of audio transmissions.

Table 6 DCS Modulation Modes

Modulation Type:	Data Bit:	FM Frequency Change:
A	0	Negative frequency shift
	1	Positive frequency shift
B	0	Positive frequency shift
	1	Negative frequency shift

The CMX7031/CMX7041 detects the DCS code that matches the programmed code defined in the Audio Control register ($C2) in either its true or inverted form. Register values 1 to 83 correspond to modulation type A (“true”) and register values 101 to 183 correspond to modulation type B (“inverted”). A facility for a user-defined code is available via Program Block 2 – CTCSS and DCS Setup:

To detect the pre-programmed DCS code, the signal is low-pass filtered to suppress all but the sub-audio band, using the filter shown in Figure 18. Further equalisation filtering, signal slicing and level detection are performed to extract the code being received. The extracted code is then matched with the programmed 23- or 24-bit DCS code to be recognised, in the order least significant first through to most significant DCS code bit last. Table 7 shows a selection of valid 23-bit DCS codes: this does not preclude other codes being programmed. Recognition of a valid DCS code will be flagged if the decode is successful (3 or less errors) by setting b10 of the Status register ($C6) to 1. A failure to decode is indicated by clearing this bit to 0. This bit is updated after the decoding of every 4th bit of the incoming signal. The actual code received is reported back in the Tone Status register ($CC) according to Table 7, so that the host µC can determine if it was the true or inverted form of the code.

Once a valid DCS code has been detected, the host µC can route the audio band signal to the AUDIO output. The audio signal is extracted from the received input signal by band pass filtering, see Figure 10.

The end of DCS transmissions is indicated by a 134.4 ±0.5Hz tone for 150-200ms. When a valid DCS code has been detected, the CMX7031/CMX7041 will automatically scan for the turn-off tone. When a DCS turn off tone is detected it will cause a DCS interrupt and report tone 54 (Tone Status b0-7 value 254 decimal); the receiver audio output can then be muted by the host.

Note that DCS detection and CTCSS detection cannot be performed concurrently.

Table 7 DCS 23-bit Codes

Reg value True	Reg value Invert	DCS Code	DCS bits 22-12	DCS bits 11-0	Reg value True	Reg value Invert	DCS Code	DCS bits 22-12	DCS bits 11-0	Reg value True	Reg value Invert	DCS Code	DCS bits 22-12	DCS bits 11-0
1	*101*	**023**	763	813	*29*	*129*	**174**	18B	87C	*57*	*157*	**445**	7B8	925
2	*102*	**025**	6B7	815	*30*	*130*	**205**	6E9	885	*58*	*158*	**464**	27E	934
3	*103*	**026**	65D	816	*31*	*131*	**223**	68E	893	*59*	*159*	**465**	60B	935
4	*104*	**031**	51F	819	*32*	*132*	**226**	7B0	896	*60*	*160*	**466**	6E1	936
5	*105*	**032**	5F5	81A	*33*	*133*	**243**	45B	8A3	*61*	*161*	**503**	3C6	943
6	*106*	**043**	5B6	823	*34*	*134*	**244**	1FA	8A4	*62*	*162*	**506**	2F8	946
7	*107*	**047**	0FD	827	*35*	*135*	**245**	58F	8A5	*63*	*163*	**516**	41B	94E
8	*108*	**051**	7CA	829	*36*	*136*	**251**	627	8A9	*64*	*164*	**532**	0E3	95A
9	*109*	**054**	6F4	82C	*37*	*137*	**261**	177	8B1	*65*	*165*	**546**	19E	966
10	*110*	**065**	5D1	835	*38*	*138*	**263**	5E8	8B3	*66*	*166*	**565**	0C7	975
11	*111*	**071**	679	839	*39*	*139*	**265**	43C	8B5	*67*	*167*	**606**	5D9	986
12	*112*	**072**	693	83A	*40*	*140*	**271**	794	8B9	*68*	*168*	**612**	671	98A
13	*113*	**073**	2E6	83B	*41*	*141*	**306**	0CF	8C6	*69*	*169*	**624**	0F5	994
14	*114*	**074**	747	83C	*42*	*142*	**311**	38D	8C9	*70*	*170*	**627**	01F	997
15	*115*	**114**	35E	84C	*43*	*143*	**315**	6C6	8CD	*71*	*171*	**631**	728	999
16	*116*	**115**	72B	84D	*44*	*144*	**331**	23E	8D9	*72*	*172*	**632**	7C2	99A
17	*117*	**116**	7C1	84E	*45*	*145*	**343**	297	8E3	*73*	*173*	**654**	4C3	9AC
18	*118*	**125**	07B	855	*46*	*146*	**346**	3A9	8E6	*74*	*174*	**662**	247	9B2
19	*119*	**131**	3D3	859	*47*	*147*	**351**	0EB	8E9	*75*	*175*	**664**	393	9B4
20	*120*	**132**	339	85A	*48*	*148*	**364**	685	8F4	*76*	*176*	**703**	22B	9C3
21	*121*	**134**	2ED	85C	*49*	*149*	**365**	2F0	8F5	*77*	*177*	**712**	0BD	9CA
22	*122*	**143**	37A	863	*50*	*150*	**371**	158	8F9	*78*	*178*	**723**	398	9D3
23	*123*	**152**	1EC	86A	*51*	*151*	**411**	776	909	*79*	*179*	**731**	1E4	9D9
24	*124*	**155**	44D	86D	*52*	*152*	**412**	79C	90A	*80*	*180*	**732**	10E	9DA
25	*125*	**156**	4A7	86E	*53*	*153*	**413**	3E9	90B	*81*	*181*	**734**	0DA	9DC
26	*126*	**162**	6BC	872	*54*	*154*	**423**	4B9	913	*82*	*182*	**743**	14D	9E3
27	*127*	**165**	31D	875	*55*	*155*	**431**	6C5	919	*83*	*183*	**754**	20F	9EC
28	*128*	**172**	05F	87A	*56*	*156*	**432**	62F	91A	*84*	*184*	User Defined		

Notes:

1. Register value 84 will select the User Programmable DCS code value in Program Block 2 – CTCSS and DCS Setup: Register value 184 will select the Inverted form of the User Programmable DCS code.
2. Note that the Audio Control register values are shown in decimal.

7.6.3 Transmit CTCSS Tone

The sub-audio CTCSS tone generated is defined in the Audio Control register ($C2). Table 5 lists the CTCSS tones and the corresponding decimal values for programming b0-7 of the register. To facilitate Squelch Tail elimination and Reverse Tone Burst, the phase of the transmitted tone can be altered by either 120, 180 or 240 degrees by setting b9, b8 in the Audio Control register ($C2). The phase change is not instantaneous, but implemented by retarding the phase of the tone to its new value over a number of cycles to avoid the generation of spurious signals. A 180 degree change will be completed within 20ms.

7.6.4 Transmit DCS Code

A 23- or 24-bit sub-audio DCS code can be generated, as defined by the Audio Control register ($C2). The same DCS code pattern is used for detection and transmission. The DCS code is NRZ encoded at 134.4±0.4 bps, low-pass filtered and added to the audio band signal, before being passed to the modulator output stages. Valid 23-bit DCS codes and the corresponding settings for the Audio Control Register are shown in Table 7, and include a user-defined facility. The least significant bit of the DCS code is transmitted first and the most significant bit is transmitted last. The CMX7031/CMX7041 is able to encode

and transmit either of the two DCS modulation modes defined by TIA/EIA-603 (true and inverted) described in Table 6. If 24-bit mode is required, bit 11 of Programming register P2.1 should be set.

To signal the end of the DCS transmission, the host should set the Audio Control register ($C2) to the DCS turn off tone (register value b0-7 = 254 decimal) for 150ms to 200ms. After this time period has elapsed the host should then disable DCS in the Mode Control register ($C1).

7.7. Inband Signalling – Selcall/DTMF/User Tones

The CM7031 supports both Selcall, DTMF and user-programmable Inband tones between 288Hz and 3000Hz. Note that if tones below 400Hz are used, sub-audio signalling should be disabled and the 300Hz HPF disabled.

By default, the CMX7031/CMX7041 will load the EEA Selcall tone set, however this may be over-written by the host with any valid set of tones within its operational range by use of the Programming register. This ensures that the device can remain compatible with all available tone systems in use. The CMX7031/CMX7041 does not implement automatic repeat tone insertion or deletion: it is up to the host to correctly implement the appropriate Selcall protocol.

Selection of the Inband signalling mode is performed by bits 11-9 of the Mode register ($C1). Detection of the selected Inband signalling mode can be performed in parallel with audio or data reception.

See:

- Mode Control – $C1 write
- Tx Inband Tones – $C3 write
- Tone Status – $CC read

7.7.1 Receiving and Decoding Inband Tones

Inband tones can be used to flag the start of a call or to confirm the end of a call. If they occur during a call the tone may be audible at the receiver. When enabled, an interrupt will be issued when a signal matching a valid Inband tone changes state (ie: on, off or a change to different tone).

The CMX7031/CMX7041 implements QTC coding using the EEA tone set. Other addressing and data formats can be implemented by loading the Programming registers with the appropriate values. The custom tones (1-4) permit other audio tones to be encoded or decoded. The frequency of each tone is defined in the Programming registers P1.18 to P1.21.

In receive mode the CMX7031/CMX7041 scans through the tone table sequentially. The code reported will be the first one that matches the incoming frequency and b13 of the IRQ Status register, $C6, will be asserted.

Adjustable decoder bandwidths and threshold levels are programmable via the Programming register. These allow certainty of detection to be traded against signal to noise performance when congestion or range limits the system performance. The Inband signal is derived from the received input signal after the band pass filtering shown in Figure 10.

Table 8 Inband Tones

Custom Tones: (b15 = 0)		
b14 - 11		Freq.
Dec	Hex	(Hz)
0	0	No Tone
1	1	Custom Tone 1 P1.18[1]
2	2	Custom Tone 2 P1.19[1]
3	3	Custom Tone 3 P1.20[1]
4	4	Custom Tone 4 P1.21[1]
5	5	Reserved
6	6	
7	7	
8	8	
9	9	
10	A	
11	B	
12	C	
13	D	
14	E	
15	F	Unrecognised Tone

Selcall Tones: (b15 = 1)		
b14 - 11		Freq.
Dec	Hex	(Hz)
0	0	1981 (P1.2)
1	1	1124 (P1.3)
2	2	1197 (P1.4)
3	3	1275 (P1.5)
4	4	1358 (P1.6)
5	5	1446 (P1.7)
6	6	1540 (P1.8)
7	7	1640 (P1.9)
8	8	1747 (P1.10)
9	9	1860 (P1.11)
10	A	1055 (P1.12)
11	B	930 (P1.13)
12	C	2247 (P1.14)
13	D	991 (P1.15)
14	E	2110[2] (P1.16)
15	F	2400 (P1.17)

Notes:

1 Custom tones 1-4 provide user programmable tone options for both transmit and receive modes as set in the indicated Program register, for programming information see section 9.2.2 in the CMX7031/CMX7041 User Manual.

2 Normally, tone 14 is the repeat tone. This code must be used in transmit mode when the new code to be sent is the same as the previous one. e.g. to send '333' the sequence '3R3' should be sent, where 'R' is the repeat tone. When receiving Selcall tones, the CMX7031/CMX7041 will indicate the repeat tone when it is received. It is up to the host to interpret and decode the tones accordingly.

7.7.2 Receiving DTMF Tones

DTMF Tone detection may be enabled in the Mode Register ($C1) in parallel with other Inband Tone modes (however, this is not recommended due to the increased likelihood of false detects). When a DTMF tone has been detected, b10 of the Tone Status Register ($CC) and b12 of the IRQ Status register, $C6, will be set. This value will over-write any existing Inband tone value that may be present. The DTMF detector returns the values shown below in Table 9.

7.7.3 Transmitting Inband Tones

The Inband tone to be generated is defined in the TX TONE register ($C3). The tone level is set in the Programming register (P1.0). The Inband tone must be transmitted without other signals in the audio band, so the host µC must disable the audio or data paths prior to initiating transmission of an Inband tone and restore them after the Inband tone transmission is complete. Table 8 shows valid Inband tones, together with the values for programming the Inband bits of the TX Inband Tones register.

Custom Inband tone frequencies are set in P1.18-21 of the Programming register ($C8). See section 9.2.2 in the CMX7031/CMX7041 User Manual for programming details.

7.7.4 Transmitting DTMF Tones

The DTMF signals to be generated are defined in the TX TONE register ($C3). Single tones and twist (lower frequency tone reduced by 2dB) can be enabled by setting the appropriate bit in the $C3 register to '1'. The DTMF level is set in programming register P1.0. The DTMF tones must be transmitted on their own, the host µC must disable audio band signals prior to initiating transmission of the DTMF tones and (if required) restore the audio band signals after the DTMF transmission is complete. Table 9 shows the DTMF tone pairs, together with the values for programming the 'Tone Pair' field of the TX TONE register.

Table 9 DTMF Tone Pairs

Tone Code (Hex)	Key Pad Position	Low Tone (Hz)	High Tone (Hz)
1	1	697	1209
2	2	697	1336
3	3	697	1477
4	4	770	1209
5	5	770	1336
6	6	770	1477
7	7	852	1209
8	8	852	1336
9	9	852	1477
A	0	941	1336
B	*	941	1209
C	#	941	1477
D	A	697	1633
E	B	770	1633
F	C	852	1633
0	D	941	1633

Note: Only the underlined tone is generated when the 'Single Tone' bit is enabled.

7.7.5 Alternative Selcall Tone Sets

These may be loaded via the Programming register to locations P1.2 to P1.17. See section 9.2.2 in the CMX7031/CMX7041 User Manual.

Table 10 Alternative Selcall Tone Sets

	Frequency (Hz)				
Tone Number	EIA	EEA	CCIR	ZVEI 1	ZVEI 2
(P1.2) 0	600	1981	1981	2400	2400
(P1.3) 1	741	1124	1124	1060	1060
(P1.4) 2	882	1197	1197	1160	1160
(P1.5) 3	1023	1275	1275	1270	1270
(P1.6) 4	1164	1358	1358	1400	1400
(P1.7) 5	1305	1446	1446	1530	1530
(P1.8) 6	1446	1540	1540	1670	1670
(P1.9) 7	1587	1640	1640	1830	1830
(P1.10) 8	1728	1747	1747	2000	2000
(P1.11) 9	1869	1860	1860	2200	2200
(P1.12) A (10)	2151	1055	2400	2800	885
(P1.13) B (11)	2435	930	930	810	810
(P1.14) C (12)	2010	2247	2247	970	740
(P1.15) D (13)	2295	991	991	885	680
(P1.16) E (14)	459	2110	2110	2600	970
(P1.17) F (15)	NoTone	2400	1055	680	2600

7.8. XTCSS Signalling

XTCSS signalling combines the capabilities of the CTCSS and Selcall signalling systems described earlier to provide a simple address/format protocol. XTCSS is used to identify the start and, optionally, the end of voice/data/other call. It provides additional information and control over the basic CTCSS method of channel coding.

XTCSS coding starts with a 4-tone sequence indicating the address and content of the following message. Immediately after the 4-tone sequence an optional sub-audio maintenance tone may be sent for the

duration of the call. At the end of the call the maintenance tone is removed and an optional 4-tone sequence is sent, indicating the end of message (EOM).

See:

- Modem Rx Address – $B6 write
- Mode Control – $C1 write
- Audio Control – $C2 write
- Status – $C6 read
- Rx Data 1 and 2/XTCSS – $C5 and $C9 read
- Tx Data 1 and 2/XTCSS – $CA and CB write

7.8.1 XTCSS Tx

The first two tones of the 4-tone sequence represent the address of the radio to be called and are loaded into the Modem Address register ($B6). The following two tones are “steering” digits which indicate the type of communication (voice, scrambled voice, data etc.) that follows. These are loaded into the Tx Data 2 register ($CB).

The device will transmit the 4 tones in sequence, raise an interrupt when this is complete and then automatically generate the XTCSS maintenance tone (if enabled). At the end of the message the maintenance tone is disabled by clearing the XTCSS maintenance tone setting in the Audio Control register ($C2).

7.8.2 XTCSS Rx

By enabling XTCSS reception the host instructs the CMX7031/CMX7041 to search for a valid 4-tone sequence. An interrupt (if enabled) will be generated when this occurs. The 4-tone sequence will be indicated in the C-BUS register ($C9) for the host to read out using the tone numbers in Table 8. To be valid, the 4 tones must be preceded and followed by silence in the audio band (signals below the audio detect level - see Program register P1.1) for the programmed no-tone time

If enabled, by setting the XTCSS maintenance tone setting in the Audio Control Register ($C2), the sub-audio tone will be searched for after a valid 4-tone Inband sequence. The state of the sub-audio maintenance tone will only be indicated to the host if CTCSS detection is also enabled. After the 4-tone sequence is detected the maintenance tone can be used by the host to detect fades and the end of the message and hence can disable the audio path as required. The CMX7031/CMX7041 will automatically search for the 4-tone set whenever the XTCSS enable bit is set and maintenance tone is not decoded.

It is possible (although unlikely) that a fade will exactly coincide and obliterate 2 lots of 4-tone sequences indicating an EOM and the start of a new message. In this case, the host could misinterpret the received signal as a long fade and enable the voice when the maintenance tone reappears. It is therefore recommended that the host operates a timer that is started on loss of maintenance tone. If this times out, the host can then assume that the fade is long enough that the original call is lost or has become so corrupted that it is not worth continuing with. The host can then choose to restore the audio path on the next occurrence of a valid XTCSS tone set. Note that the XTCSS detector operates independently and the host may enable or disable the audio path at any time.

7.9. MSK/FFSK Data Modem

The CMX7031/CMX7041 supports both 1200 and 2400 bps MSK/FFSK data modes (see section 7.11 for details of the 1200 bps FSK mode suitable for use in the Marine VHF band for Digital Selective Calling (DSC) to ITU-R M.493-11 and section 7.12 for a 559bps PSK encoder). In Rx mode, the device can be set to look for either of the MSK or FFSK modes, however, once a valid mode has been found, it will stay in that mode until the host resets it.

See:

- Mode Control – $C1 write
- Modem Control – $C7 write
- Rx Data 1 and 2/XTCSS – $C5 and $C9 read
- Tx Data 1 and 2/XTCSS – $CA and CB write

7.9.1 Receiving MSK/FFSK Signals

The CMX7031/CMX7041 can decode incoming MSK/FFSK signals at either 1200 or 2400 baud data rates, automatically detecting the rate from the received signal. Alternatively, a control word may set the baud rate, in which case the device only responds to signals operating at that rate. The form of MSK/FFSK signals for these baud rates is shown in Figure 19.

The received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The recovered data is stored in a 2- or 4-byte buffer (grouped into 16-bit words) and an interrupt issued to indicate received data is ready. Data is transferred over the C-BUS under host µC control. If this data is not read before the next data is decoded it will be overwritten and it is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged, see Table 13. The MSK/FFSK bit clock is not output externally.

The extracted data is compared with the 16-bit programmed Frame Sync pattern (preset to $CB23 following a RESET command). An interrupt will be flagged when the programmed Frame Sync pattern is detected or when the following Frame Head is decoded, see section 7.10.3. The host µC may stop the frame sync search by disabling the MSK/FFSK demodulator. Once a valid Frame Sync pattern has been detected, the frame sync search algorithm is disabled; it may be re-started by the host disabling the Modem Control bits of the Mode register ($C1:b2,3) and then re-enabling them (taking note of the C-BUS latency time).

If the CMX7031/CMX7041 has been set to decode a Frame Head before interrupting, it will check the CRC portion of the Frame Head Control Field. If this indicates a corrupt Frame Head then a search for a new frame sync pattern will be automatically restarted.

FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component. The device will handle the sub-audio signals as previously described. If a sub-audio signal turns off during reception of FFSK, it is up to the host µC to turn off the decoding as the device will continue receiving and processing the incoming signal until commanded otherwise by the host µC.

The host µC must keep track of the message length or otherwise determine the end of reception (e.g. by using sub-audio information to check for signal presence) and disable the demodulator at the appropriate time. Note that when using packets with embedded size information, the CMX7031/CMX7041 will indicate when the last data block has been received.

7.9.2 Transmitting MSK/FFSK Signals

The MSK/FFSK encoding operates in accordance with the bit settings in the Modem Control register ($C7). When enabled the modulator will begin transmitting data using the settings and values in block 0 of the Programming register (bit sync and frame sync patterns), the Modem Control register and the Tx Data registers. Therefore, these registers should be programmed to the required values before transmission is enabled.

The CMX7031/CMX7041 generates its own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 19 and Table 11. The binary data is taken from Tx DATA 1 and 2 registers ($CA and $CB), most significant bit first. The following data words must be provided over the C-BUS within certain time limits to ensure the selected baud rate is maintained. The time limits will be dependent on the data coding being used, see Table 13.

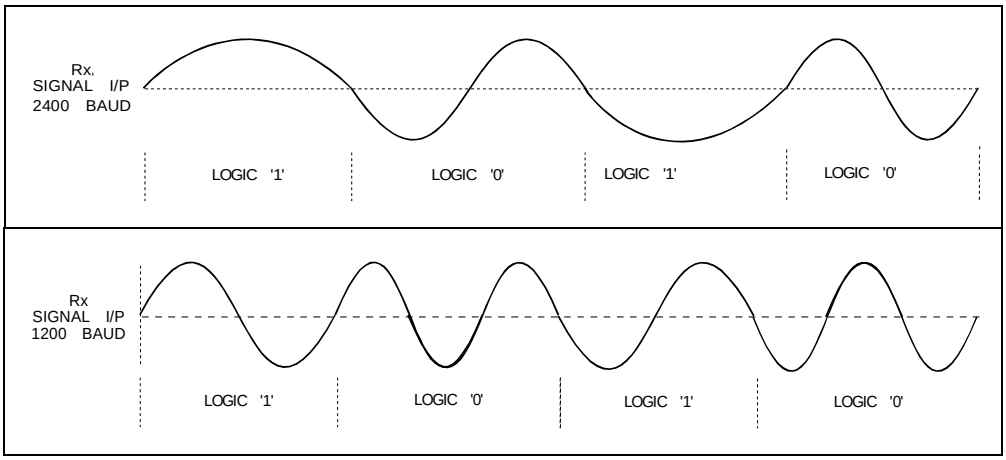


Figure 19 Modulating Waveforms for 1200 and 2400 Baud MSK/FFSK Signals

The table below shows the combinations of frequencies and number of cycles to represent each bit of data, for both baud rates.

Table 11 Data Frequencies for each Baud Rate

Baud Rate	Data	Frequency	Number of Cycles
1200baud	1	1200Hz	one
	0	1800Hz	one and a half
2400baud	1	1200Hz	half
	0	2400Hz	one

Note: FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component.

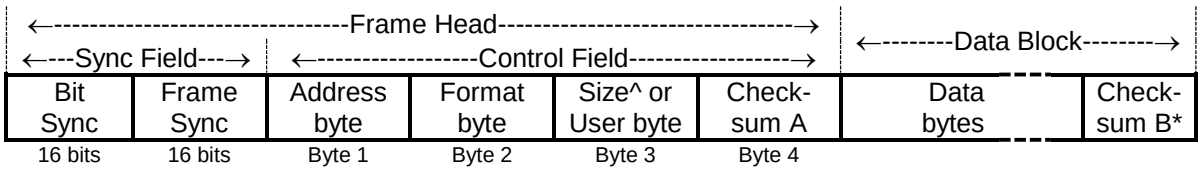
7.10. MSK/FFSK Data Packetising

The CMX7031/CMX7041 has extensive data packetising features that can be controlled by the Modem Control register ($C7). The CMX7031/CMX7041 can packetise data in a variety of formats so the user can have the optimum data throughput for various signal to noise ratios. Data is transferred in packets or frames, each frame is made up of a Frame Head followed by any associated user data. The Frame Head is composed of a 16-bit Bit Sync and 16-bit Frame Sync pattern immediately followed by a 4 bytes Control Field. The 4 bytes start with an 8-bit address followed by 1 byte carrying information about the format of the following Data Block. The next byte indicates the size of the packet or can be used freely, depending on the format selected. The last byte is a checksum to detect if any of the 4 Control Field bytes has been corrupted.

7.10.1 Tx Hang Bit

When transmitting MSK/FFSK data of formats 0, 2 or 3, the user should ensure that the data is terminated with a hang bit. To do this, the host must set the 'Last Data' bit in the Modem Control register ($C7) after the last data word has been loaded into the Tx Data 1 register ($CA), as described in section 9.1.25 in the CMX7031/CMX7041 User Manual. This will append a hang bit onto the end of the current word and will stop modulating after the hang bit has been transmitted. It will also generate an interrupt (if enabled) when the hang bit has left the modulator.

7.10.2 Frame Format



* Checksum B not applied to all Data Block types
^ Byte 3 is only reserved on sized data blocks.

The Data Block is made up from the user data. This consists of a variable number of data bytes optionally encoded to ensure secure delivery over a radio channel to the receiver. Checksum B is only applied at the end of sized Data Blocks, the receiver can then detect if any of the user data has been corrupted. Checksum B is composed of 16 bits for messages ≤16 bytes and 32 bits for longer messages.

7.10.3 Frame Head

The Frame Head allows the receiver to detect and lock on to MSK/FFSK signals, provides basic addressing to screen out unwanted messages and indicates the format, coding and length of any following data.

In Frame Formats 3, 4 and 5, the four Control Field bytes have Forward Error Correction (FEC) applied to them in the transmitter, this adds 4 bits to every byte and the receiver can correct errors in the received bytes. The 4 received bytes are then checked for a correct CRC, so that corrupted Frame Heads can be rejected. If checksum A indicates that the Control Field bytes are correct, the Address (byte 1) is compared with that stored in the MSK Header Address bits of Modem Address register, $B6 (b15:8). If a match occurs, or if the received address is '40', then an interrupt is raised indicating a valid Frame Head has been received. The Frame Head is 80 bits long (16 + 16 + {4x12}). The contents of a received Frame Head can be read from Rx Data registers $C5 and $C9.

7.10.4 Data Block Coding

The Data Block follows the Frame Head and can be coded with different levels of error correction and detection. The Data Block format is controlled by Frame Format selected in Frame Head byte 2, see also section 9.1.22 in the CMX7031/CMX7041 User Manual. Messages can take the following formats:

Format: Description:

0 **Un-Formatted Data**. This mode should be used with the En_RAW bit (b10 of the Modem Control Register) set to 1. The Interleave and Scrambler settings are ignored. This mode can be useful when interfacing to a system using a different format to those available.

In transmit, the device will transmit only the data loaded into the TxData 1 register. The host should provide bit sync, frame sync and any required formatting data as well as the Data Block through this register.

In receive, the device will search for the programmed 16-bit Frame Sync pattern, which is reported in the Rx Data 1 register as the first two received bytes, and then output all following data 16 bits at a time. The host will have to perform all other data formatting.

1 **Frame Head only**. No Data Block will be added. This format can be useful for indicating channel or user status by using byte 3 and the User Bit of the Frame Head (see section 9.1.22 in the CMX7031/CMX7041 User Manual).

2 **Frame Head followed by Raw Data**. User data is appended to the Frame Head in 2-byte units with no formatting or CRC added by the CMX7031/CMX7041. No size information is set in the Frame Head and Data Block may contain any even number of bytes per Frame.

3 **Frame Head followed by FEC Coded Data only**. Each byte of the user data has 4 bits of FEC coding added. No size information is set in the Frame Head and Data Block may contain any even number of bytes per Frame. No CRC is added to the data.

4 **Frame Head followed by FEC Coded Data with an automatic CRC** at the end of the Data Block. The number of user data bytes in the Frame must be set in Frame Head byte 3. The CRC is automatically checked in the receiver and the result indicated to the host µC. Up to 255 bytes of user data can be sent in each Frame using this format.

5 **As '4 above', with the addition of all Data Block bytes being interleaved**. This spreads the transmitted information over time and helps reduce the effect of errors caused by fading. Interleaving is performed on blocks of 4 bytes, the CMX7031/CMX7041 automatically adds and strips out pad bytes to ensure multiples of 4 bytes are sent over the radio channel.

Notes:

- Format 0, 1, 2 and 3 have no size information requirement and do not reserve Frame Head byte 3. This byte may be freely used by the host µC to convey information. In Format 4 and 5 this byte must be set to the number of user bytes in the message attached to that Frame Head (≤255) to allow the receiver to correctly decode and calculate the CRC.
- Format 0 data transfers do not provide any frame formatting. In Tx the host µC must transfer the bit and frame sync data before sending the message data. In Rx the host µC must decode all data after the frame sync.

Table 12 Data Block Formatting Types

Data Block Format:	Total over-air bits for an 80-byte message	Air time for MSK/FFSK message (ms) at 1200baud	Air time for MSK/FFSK message (ms) at 2400baud	Over-air efficiency	Burst length protection at 1200baud *[for 2400baud divide both times by 2]*	Probability of detecting errors
2	720	600	300	89%	None	Zero
3	1040	867	433	62%	<0.83ms in any 10ms	Poor
4	1088	907	453	59%	<0.83ms in any 10ms	Excellent
5	1088	907	453	59%	<3.33ms in any 40ms	Excellent

Higher levels of error protection have the penalty of adding extra bits to the over air signal and this reduces the effective bit rate. Less error protection increases the effective bit rate, however in typical radio conditions the penalty is a greater risk of errors leading to repeated messages and a net reduction in effective bit rate compared to using error correction and detection.

7.10.5 CRC and FEC Encoding Information

For messages with FEC coding the following matrix is used to calculate and decode bytes:

Data bits								FEC bits			
7	6	5	4	3	2	1	0	3	2	1	0
1	1	1	0	1	1	0	0	1	0	0	0
1	1	0	1	0	0	1	1	0	1	0	0
1	0	1	1	1	0	1	0	0	0	1	0
0	1	1	1	0	1	0	1	0	0	0	1

8 bit CRC is used in all frame heads with the following generator polynomial (GP):

$x^8 + x^7 + x^4 + x^3 + x^1 + x^0$

16 bit CRC is used at the end of sized data messages of up to 16 bytes with the following GP:

$x^{16} + x^{12} + x^5 + x^0$

32 bit CRC is used at the end of sized data messages of over 16 bytes with the following GP:

$x^{32} + x^{31} + x^{30} + x^{28} + x^{27} + x^{25} + x^{24} + x^{22} + x^{21} + x^{20} + x^{16} + x^{10} + x^9 + x^6 + x^0$

7.10.6 Data Interleaving

The built in MSK/FFSK packetising includes the option of interleaving the data in each block (Type 5). This, together with Forward Error Correction (FEC), reduces the effects of burst errors. Interleaving does not add any bits to the message, the packet is assembled in 'rows' and then transmitting in 'columns'.

Data (8 bits)								FEC (4 bits)			
0	1	2	3	4	5	6	7	8	9	10	11
12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35
36	37	38	39	40	41	42	43	44	45	46	47

In the above example the packet is assembled as 4 rows with 12 bits of information per row. When this packet is interleaved the bits are sent over the communication channel in the following order:

0, 12, 24, 36, 1, 13, 25, 37, 2, 14, ... , 33, 45, 10, 22, 34, 46, 11, 23, 35, 47.

In the receiving modem the packet is re-assembled (de-interleaved) before error correction. The CMX7031/CMX7041 has a built in packet receive modem which is able to recognise (by using the frame head bytes) when the data has been interleaved by the transmitter and will decode the data using the correct method.

7.10.7 Data Scrambling/Privacy Coding

It is preferable for MSK/FFSK over-air data to be reasonably random in nature to ensure the receiver can track timing using the bit changes and to smooth the frequency spectrum. To reduce the possibility of user data causing long strings of 1's or 0's to be transmitted, a 16-bit data scrambler is provided and operates on all bits after the Frame Head.

The default (standard) setting for this scrambler is with a start code (seed) of $FFFF and any receivers with the same seed may decode this data. However, if the transmitter and receiver pre-arrange a different seed then the scrambler will start its sequence in another place and any simple receiver that does not know the transmitted seed will not be able to successfully decode the data. This method gives over 65,000 different starting points and the chance of others decoding data successfully is reduced.

The CMX7031/CMX7041 provides the option of two custom 16-bit words that are programmable by the user in Programming register P0.4 to P0.7. Bits 0 and 1 in the Frame Head Format byte indicate which setting (standard, Seed1, Seed2 or none) the following Data Block has been scrambled with, see section 9.2.1 in the CMX7031/CMX7041 User Manual. Note that a seed of $0000 will effectively turn off the scrambler and provide no protection against long sequences of 1's or 0's. Reception of scrambled data will only be successful when the receiving device has been programmed with the correct (identical) seed to that used by the transmitter.

By using this method the CMX7031/CMX7041 provides a privacy code that will protect against casual monitoring, however the data is not encrypted and a sophisticated receiver can decode the data by using moderately simple decoding techniques. If data encryption is required it must be performed by the host µC. The scrambler function is controlled by bits 0, 1 of the Modem Control register, $C7.

7.10.8 Data Buffer Timing

Data must be transferred at the rate appropriate to the signal type and data format. The CMX7031/CMX7041 buffers data in two 16-bit registers. The CMX7031/CMX7041 will issue interrupts to indicate when data is available or required. The host must respond to these interrupts within the maximum allowable latency for the signal type. Table 13 shows the maximum latencies for transferring signal data to maintain appropriate data throughput.

Table 13 Maximum Data Transfer Latency

Data Format	Max. time to read from or write to data buffer		Data buffer size
	1200 baud	2400 baud	
0	13.3ms	6.6ms	2 bytes
1	N/A*	N/A*	4 bytes
2	13.3ms	6.6ms	2 bytes
3	20ms	10ms	2 bytes
4	40ms	20ms	4 bytes
5	40ms	20ms	4 bytes

* Type 1 message is an isolated Frame Head, there is no subsequent data to load (Tx) or read (Rx).

7.11. FSK 1200bps DSC Modem

In place of the MSK/FFSK modem described in section 7.9, the device can implement a 1200 bps DSC (Digital Selective Call) modem conforming to the requirements of ITU-R M.493-11 for use in Marine VHF band radio equipment. Selecting this function will disable the MSK/FFSK modems. This modem uses tones at 1300 and 2100Hz to represent binary 1's and 0's respectively, with 6dB/octave pre-emphasis in Tx.

Dot Pattern	DX/RX	A	B	C	D	E	F	G	H	I
	Phasing Sequence	Format Specifier	Called Party Address	Category	Self-Identification	Tele-command message	Frequency message	Frequency message	End of sequence	Error-check character
		2 Identical characters	5 characters	1 character	5 characters	2 characters	3 characters	3 characters	3 identical DX characters 1 RX character	1 character

Dot Pattern	DX		DX		DX		DX		DX		DX		A		A		BI		B2		B3		R4		B5		C		DI		D2		D3		D4		D5		EI		E2		FI		F2		F3		GI		G2		G3		H		I		H		H	
		RX7		RX6		RX5		RX4		RX3		RX2		RX1		RX0		A		A		BI		B2		B3		B4		B5		C		D1		D2		D3		D4		D5		EI		E2		FI		F2		F3		GI		G2		G3		H		I

Figure 20 DSC Format

To enable this mode, the En_DSC (bit 11 of the Modem Control register, $C7) must be set. This will disable the MSK/FFSK modem features. The DSC modem itself can then be controlled by setting or clearing En_1200 (bit 2 of the Mode Control register, $C1). Note that, due to the C-BUS latency times, there should be a delay after clearing this bit, before re-enabling it again (see 7.2.1).

With DSC mode selected, bits 8 to 0 of the Modem Control register, $C7, are ignored.

Two modes of operation are provided:

- Raw mode
- Formatted mode (normal or enhanced)

Enhanced operation is available by setting Program Register P0.0 bit 10 and provides:

- Support for DSC expansion sequences (ITU-R M.821-1)
- Support for transmission of continuous distress signals.

Symbol No.	Emitted signal and bit position 1 2 3 4 5 6 7 8 9 10	Symbol No.	Emitted signal and bit position 1 2 3 4 5 6 7 8 9 10	Symbol No.	Emitted signal and bit position 1 2 3 4 5 6 7 8 9 10
00	BBBBBBBYYY	43	YYBYBYBBYY	86	BYYBYBYBYY
01	YBBBBBBYYB	44	BBYYBYBYBB	87	YYYBYBYBYB
02	BYBBBBBYYB	45	YBYYBYBBYY	88	BBBYYBYYBB
03	YYBBBBBYBY	46	BYYYBYBBYY	89	YBBYYBYBYY
04	BBYBBBBYYB	47	YYYYBYBBYB	90	BYBYYBYBYY
05	YBYBBBBYBY	48	BBBBYYBYBY	91	YYBYYBYBYB
06	BYYBBBBYBY	49	YBBBYYBYBB	92	BBYYYBYBYY
07	YYYBBBBYBB	50	BYBBYYBYBB	93	YBYYYBYBYB
08	BBBYBBBYYB	51	YYBBYYBBYY	94	BYYYYBYBYB
09	YBBYBBBYBY	52	BBYBYYBYBB	95	YYYYYBYBBY
10	BYBYBBBYBY	53	YBYBYYBBYY	96	BBBBBYYYBY
11	YYBYBBBYBB	54	BYYBYYBBYY	97	YBBBBYYYBB
12	BBYYBBBYBY	55	YYYBYYBBYB	98	BYBBBYYYBB
13	YBYYBBBYBB	56	BBBYYYBYBB	99	YYBBBYYBYY
14	BYYYBBBYBB	57	YBBYYYBBYY	100	BBYBBYYYBB
15	YYYYBBBBYY	58	BYBYYYBBYY	101	YBYBBYYBYY
16	BBBBYBBYYB	59	YYBYYYBBYB	102	BYYBBYYBYY
17	YBBBYBBYBY	60	BBYYYYBBYY	103	YYYBBYYBYB
18	BYBBYBBYBY	61	YBYYYYBBYB	104	BBBYBYYYBB
19	YYBBYBBYBB	62	BYYYYYBBYB	105	YBBYBYYBYY
20	BBYBYBBYBY	63	YYYYYYBBBY	106	BYBYBYYBYY
21	YBYBYBBYBB	64	BBBBBBYYYB	107	YYBYBYYBYB
22	BYYBYBBYBB	65	YBBBBBYYBY	108	BBYYBYYBYY
23	YYYBYBBBYY	66	BYBBBBYYBY	109	YBYYBYYBYB
24	BBBYYBBYBY	67	YYBBBBYYBB	110	BYYYBYYBYB
25	YBBYYBBYBB	68	BBYBBBYYBY	111	YYYYBYYBBY
26	BYBYYBBYBB	69	YBYBBBYYBB	112	BBBBYYYYBB
27	YYBYYBBBYY	70	BYYBBBYYBB	113	YBBBYYYBYY
28	BBYYYBBYBB	71	YYYBBBYBYY	114	BYBBYYYBYY
29	YBYYYBBBYY	72	BBBYBBYYBY	115	YYBBYYYBYB
30	BYYYYBBBYY	73	YBBYBBYYBB	116	BBYBYYYBYY
31	YYYYYBBBYB	74	BYBYBBYYBB	117	YBYBYYYBYB
32	BBBBBYBYYB	75	YYBYBBYBYY	118	BYYBYYYBYB
33	YBBBBYBYBY	76	BBYYBBYYBB	119	YYYBYYYBBY
34	BYBBBYBYBY	77	YBYYBBYBYY	120	BBBYYYYBYY
35	YYBBBYBYBB	78	BYYYBBYBYY	121	YBBYYYYBYB
36	BBYBBYBYBY	79	YYYYBBYBYB	122	BYBYYYYBYB
37	YBYBBYBYBB	80	BBBBYBYYBY	123	YYBYYYYBBY
38	BYYBBYBYBB	81	YBBBYBYYBB	124	BBYYYYYBYB
39	YYYBBYBBYY	82	BYBBYBYYBB	125	YBYYYYYBBY
40	BBBYBYBYBY	83	YYBBYBYBYY	126	BYYYYYYBBY
41	YBBYBYBYBB	84	BBYBYBYYBB	127	YYYYYYYBBB
42	BYBYBYBYBB	85	YBYBYBYBYY		

B = 0 order of transmitted bits: bit 1 first
Y = 1

Figure 21 DSC Character Format

7.11.1 Receiving 1200 bps FSK (DSC) Signals

In Rx Raw mode (En_RAW=1) the modem will report back all data received as soon as it is enabled. (Note: If a valid DSC signal is not present when the modem is first enabled, it will still attempt to demodulate the input signal and output data. The host must determine if the data is valid or not. It is possible to use the SynC facility to reduce the amount of invalid data presented to the host, but this may also lead to DSC calls with errors in the SynC pattern being missed).

As soon as the En_1200 bit has been asserted, the modem will attempt to demodulate the input signal. Data bits will then be delivered to the Rx Data 1 register, $C5 as they are demodulated, indicated by the Data_RDY bit. It is up to the host to align, decode and validate the data and to subsequently switch the modem off once an EOS (End of Sequence) has been detected (by clearing bit 2 of the Mode Control register, $C1). In this mode, the device does not perform byte alignment or phasing (synchronisation) detection[4].

The host must read the RxData 1 register before the next 16 bits of data have been received, otherwise the data will be lost.

If the SynC facility is used in Raw mode, then the value of SynC must be programmed by the host to a suitable value via the Program registers (P0.0 and P0.1). The values $5555 or $AAAA are suggested for this setting, however, this will not completely remove false detections and the following received data must be analysed before assuming that a valid call is in progress (see ITU-R M.493-11 for details). The SynC enable bit (bit 15 of the Modem Control register, $C7) must be asserted. Setting the En_1200 bit (bit 2 of the Mode Control register, $C1), will activate the DSC modem which will then attempt to decode the signal at it's input. Acquisition of the SynC data pattern will be reported to the host by the setting of the 1k2 bit (bit 3 in the Status register, $C6).

In Rx Formatted mode, (En_Raw=0) the modem will check the incoming bit stream for a valid sequence of phasing characters (3x Rx, 2x Dx+ Rx or Dx + 2 x Rx) and then report any correctly decoded characters in the RxData1 ($C5) register. The characters are packed into the 16-bit register as two 7 bit characters and an additional error indication bit (bits 15 and 7). In the case where an odd number of characters has been received, the unused field will be reported as 0000000_b and the error bit set to 1. This mechanism significantly reduces the amount of data transferred to the host and the host processing requirements.

The decoded 7-bit characters will be delivered to the RxData1 register, $C5, as indicated by the Data_RDY bit. The modem will not report valid data until it has correctly received the initial phasing sequence. Once the Phasing sequence has been detected, the modem's internal DPLL bandwidth will be automatically reduced to improve the error performance. If one of the time-diversity received characters is in error, only the correct one will be reported. If both characters have errors, the last one received will be reported, with bit 7 (MSB) set. The characters reported back will correspond to the data sequence (see Figure 20)[5]:

A A B1 B2 B3 B4 B5 C D1 D2 D3 D4 D5 E1 E2 F1 F2 F3 G1 G2 G3 H I

If enhanced DSC support is enabled the modem will look for further data following the end of the main sequence. If an expansion sequence (as defined by ITU-R M.821-1) is detected, the contents will continue to be delivered to RxData1 until the end of the expansion sequence. If either the main sequence or expansion sequences contained an odd number of bytes the unused field will be reported as 0000000_b and the error bit set to 1. This means that an expansion sequence will always start on a register boundary.

When the end of the received message is detected the Data_END bit will be set in the Status register ($C6).

Main Message		G2		G3		H		I		H		H		AE1		BE1		BE2		BE3		BE4		AE2		CE1		CE2		CE3		CE4		DE		EE		DE		DE	
	F2		F3		G1		G2		G3		H		I		X		X		AE1		BE1		BE2		BE3		BE4		AE2		CE1		CE2		CE3		CE4		DE		EE

Figure 22 Expanded DSC Format

[4] This is similar to the CMX604, CMX910 and CMX7032 operation.

[5] This particular sequence corresponds to the example given in ITU-R M.493-11. Different Telecommands will produce different sequences of varying lengths.

AE1	first expansion data specifier (100 to 106)
AE2	second expansion data specifier (100 to 106)
BEx	characters of first expansion message
CEx	characters of second expansion message
DE	EOS end of sequence
EE	ECC error check character
X	no information (126)

… … F2 F3 G1 G2 G3 H I AE1 BE1 BE2 BE3 BE4 AE2 CE1 CE2 CE3 CE4 DE EE

Note that if a normal DSC sequence is received with enhanced DSC enabled, there will be a delay in setting the Data_END bit whilst the modem processes the remainder of the signal for a possible expansion sequence, indicated by one of the expansion characters (100 to 106) in the correct position.

7.11.2 Transmitting 1200 bps FSK (DSC) Signals

In Tx Raw mode (En_RAW=1) the host must supply all data to be transmitted by the modem via the TxData register ($CA) in the correct order and format to conform to the DSC standards.

Setting the En_1200 bit (bit 2 of the Mode Control register, $C1), will enable the DSC modem which will then transmit the data supplied by the host through the TxData1 register, $CA. Bit 10 of the Modem Control Register, $C7, should also be set to enable/disable Raw data mode as appropriate.

In Tx Formatted mode (En_RAW=0), the modem will automatically transmit the dotting pattern followed by the phasing sequence and then encode the data presented at the TxData1 register ($CA) with the correct checksum bits and then transmit it in the correct position with automatic repetition to conform to the time diversity requirements of the standard. Data in the TxData1 register is presented as two 7-bit characters, in the case where an odd number of characters needs to be sent, then the un-used character should be set to 0000000 and b7 set to 1. The final characters sent by the host should be a valid “End-of-Sequence” character followed by the “Error Check” character.

Valid DSC characters should be supplied by the host through the TxData1 register, $CA. Two characters can be loaded in the same C-BUS write operation. The modem will begin transmitting the dotting sequence followed by the phasing sequence as soon as the En_1200 bit (bit 2 of the Mode Control register, $C1) is set. The format of the data supplied by the host is similar to the Rx format:

A A B1 B2 B3 B4 B5 C D1 D2 D3 D4 D5 E1 E2 F1 F2 F3 G1 G2 G3 H I

There is no facility for automatically generating continuous dotting (preamble), Y data (all 1’s), B data (all 0’s) or phasing (synchronisation) sequences internally, however, the modem will continue to transmit the last data loaded into the TxData1 register, so only a single data load is required.

If a DSC expansion sequence (as defined by ITU-R M.821-1) is required to be transmitted (and the enhanced DSC support is enabled) it should follow on directly from the main sequence end. If the main sequence had an odd number of bytes the padding byte (0000000_b with error bit set) should still be included following the error check character (I). The expansion sequence should be transmitted in the same format as the original message, using the TxData1 register. The last characters should be the EOS and ECC characters of the expansion sequence, (plus a padding byte, $0000000_{b,}$ with error bit set if the expansion sequence contained an odd number of bytes). On writing the last data, the Data_END bit should be set in the modem control register ($C7). The maximum number of over-air characters in an expansion sequence is 38 (corresponds to 17 formatted characters, including EOS and ECC).

The enhanced DSC support feature also allows a special case for distress messages. If a distress message is transmitted following a previous sequence end, the transmission will continue automatically. This will cause the modem to generate another dotting and phasing sequence without a break in transmission. This allows generation of a distress signal with multiple continuous repetitions as described in ITU-R M.493, section 11.1. The modem does not buffer the message bytes after they have been transmitted so the host must send the same sequence multiple times in order to implement the sequence repetition. The special case of a distress signal is detected by the next sequence start (characters A1 and A2) both having the value “112” following the end of the previous sequence. (This is the value which denotes a distress message.)

7.12. PSK Encoder

A 559bps PSK modem is provided to enable transmission of signalling suitable for suitable radio systems. This uses the same Tx data interface as the DSC modem in raw mode and is enabled by setting b4 of the Modem Control register, $C7 along with b10 and b11. This will output 2 ½ cycles of the audio carrier tone (1398Hz) for each data bit. The phase inversion occurs at the zero-crossing point.

Modem Control ($C7)	= $0C10
TxData 1 ($CA)	= user Tx data
Mode Control ($C1)	= $0006

7.13. NOAA/NWR SAME and WAT Decoding

A data decoder and tone detector suitable for use with the NOAA's NWR (NOAA Weather Radio) system is provided in the device. Full details of the system are publicly available from the NOAA web site at http://www.nws.noaa.gov/nwr/ and the CMX7031/CMX7041 provides support for the WAT detection and SAME decoding. It is possible to route the signal input to either Input 1 or Input 2 so that NWR monitoring can be performed in parallel with existing radio operations (subject to suitable RF sections being provided externally).

See:

- NWR Status and Data – $BB read
- Mode Control – $C1 write
- Status – $C6 read
- Modem Control – $C7 write
- Interrupt Mask – $CE write

The NWR SAME data message consists of six possible elements in the following sequence:

1. Preamble
2. Header code
3. Warning Alarm Tone/Attention Signal
4. Voice Message
5. Preamble
6. End Of Message (EOM)

Elements 1, 2, 5, and 6 will always be transmitted in a NWR SAME message and repeated three times. Elements 3 and 4 may or may not be transmitted depending on the specific type of message or its application.

The coded message is transmitted, using Frequency Shift Keying (FSK), in the NWR audio channel. In this application and the implementation currently used by the FCC EAS, it is more accurate to refer to the code format as Audio Frequency Shift Keying (AFSK). It is transmitted at no less than 80% modulation (± 4.0 kHz deviation minimum, ± 5.0 kHz deviation maximum).

The coded message and voice message is transmitted over the NWR transmitter network using standard pre-emphasis for narrow band VHF Frequency Modulation (FM) of 6 dB per octave increasing slope from 300 Hz to 3,000 Hz applied to the modulator.

Preamble. The preamble and header code are transmitted three times with a one second pause (± 5%) between each coded message burst prior to the broadcast of the actual voice message. Then the preamble and End Of Message (EOM) code are transmitted three times with a one second pause (± 5%) between each EOM burst.

Preamble Byte. The first 16 bytes (prior to the header code and EOM) of the data transmission constitute a preamble with each byte having the value $AB (8 bit byte [10101011]). For all bytes, the least significant bit (LSB) is sent first. The bytes following the preamble constitute the actual message data transmission.

NOTE: For NWR system maintenance, NWS will occasionally send a continuous string of preamble code, $AB or a continuous tone through its communications links to the NWR transmitters, for several seconds up to around one minute.

Bit Definition. The following definitions of a bit are based on a bit period equaling 1920 microseconds (± one microsecond).

- The data rate is 520.83 bits per second
- Logic zero is 1562.5 Hz.
- Logic one is 2083.3 Hz
- Mark and space bit periods are equal at 1.92 milliseconds.

Header. Bit and byte synchronization is attained by the preamble code at the beginning of each header code or EOM data transmission. The message data (header) code is transmitted using American Standard Code for Information Interchange (ASCII) characters as defined in ANSI INCITS 4 (rev 86, 2002), with the eighth bit always set to zero. Each separate header code data transmission should not exceed a total of 268 bytes if the maximum allowable geographic locations (31) are included.

Warning Alarm Tone. The Warning Alarm Tone (WAT), if transmitted, is sent within one to three seconds following the third header code burst. The frequency of the WAT is 1050Hz (± 0.3%) for 8 to 10 seconds at no less than 80% modulation (± 4.0 kHz deviation minimum, ± 5.0 kHz deviation maximum).

Voice Message. If transmitted, the actual voiced message begins within three to five seconds following the last NWR SAME code burst or WAT, whichever is last. The voice audio ranges between 20% modulation (± 1 kHz deviation) and 90% modulation (± 4.5 kHz deviation) with occasional lulls near zero and peaks as high as, but not exceeding, 100% modulation (± 5.0 kHz deviation). Total length of the voice message should not exceed two minutes.

Preamble. A repeat of preamble above.

End Of Message. EOM is identified by the use of “NNNN.”

7.13.1 Message Code Format

(Preamble)ZCZC-ORG-EEE-PSSCCC-PSSCCC+TTTT-JJJHHMM-LLLLLLLL- (1 second pause)

(Preamble)ZCZC-ORG-EEE-PSSCCC-PSSCCC+TTTT-JJJHHMM-LLLLLLLL- (1 second pause)

(Preamble)ZCZC-ORG-EEE-PSSCCC-PSSCCC+TTTT-JJJHHMM-LLLLLLLL- (1 to 3 second pause)

1050 Hz Warning Alarm Tone for 8 to 10 seconds – (if transmitted) (3 to 5 second pause)

Voice /spoken oral text of message – (if transmitted) (1 to 3 second pause)

(Preamble) NNNN (1 second pause)

(Preamble) NNNN (1 second pause)

(Preamble) NNNN

7.13.2 WAT Detection

The WAT detector is enabled by setting the NWR bit (b12 of $C1) and indicated by setting b15 of the NWRData register ($BB). If enabled, the NWR IRQ (b14) in the Status register ($C6) will also be set. The detector will be reset after 500ms, so multiple detections may be indicated on long WAT tones.

7.13.3 SAME Decoding

The SAME data is received at 520.83bps and decoded by the CMX7031/CMX7041 whenever the NWR bit (b12 of $C1) is set. Internally, the CMX7031/CMX7041 monitors the selected input until it detects the preamble sequence and then passes the subsequently recovered data to the host uC via the NWRData register ($BB). The decoder will detect the data header and determine if it is “ZCZC” indicating that data follows or “NNNN” indicating the end of a transmission and report these states in bits 13 and 14 of the NWRData register ($BB) respectively). If enabled, the NWR IRQ (b14) in the Status register ($C6) will also be set following the detection of the preamble and on every subsequently received byte.

When the En_NWR_data bit is set, the receiver outputs the received bitstream. The host is allowed to set this bit at any time to get "raw mode" data output with no preamble/header detection and no guarantee of byte alignment.

When the En_NWR_data bit is clear, the receiver searches for a valid SAME transmission but does not output data. If it sees a preamble followed by the data header ("ZCZC"), it raises an IRQ and *automatically* sets the En_NWR_data bit to put itself into data-output mode. It is then up to the host to decide when to clear the En_NWR_data bit to put the receiver back into sync-search mode (thus "re-arming" it).

If the receiver sees a preamble followed by the end-of-message header ("NNNN") while doing sync-search, it informs the host [2] and then continues the search without putting itself into data-output mode.

It is the responsibility of the host to shut the decoder down at the end of a received burst by clearing the En_NWR_data bit (b12 of $C7) to 0.

7.14. Auxiliary ADC Operation

The inputs to the two Auxiliary ADCs can be independently routed to any of the Signal Input pins under control of the AuxADC and TX MOD mode register, $A7. Conversions will be performed as long as a valid input source is selected, to stop the ADCs, the input source should be set to “none”. Register $C0, b6, BIAS, must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC and TX MOD mode register, $A7, the length of the averaging is determined by the value in the Programming register (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in P3.0 and P3.1. For an average value of 0; 50% of the current value will be applied, for a value of 1 = 25%, 2 = 12.5% etc. The maximum useful value of this field is 8.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated if a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 23. The thresholds are programmed via the AuxADC Threshold register, $B5.

Auxiliary ADC data is read back in the AuxADC Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

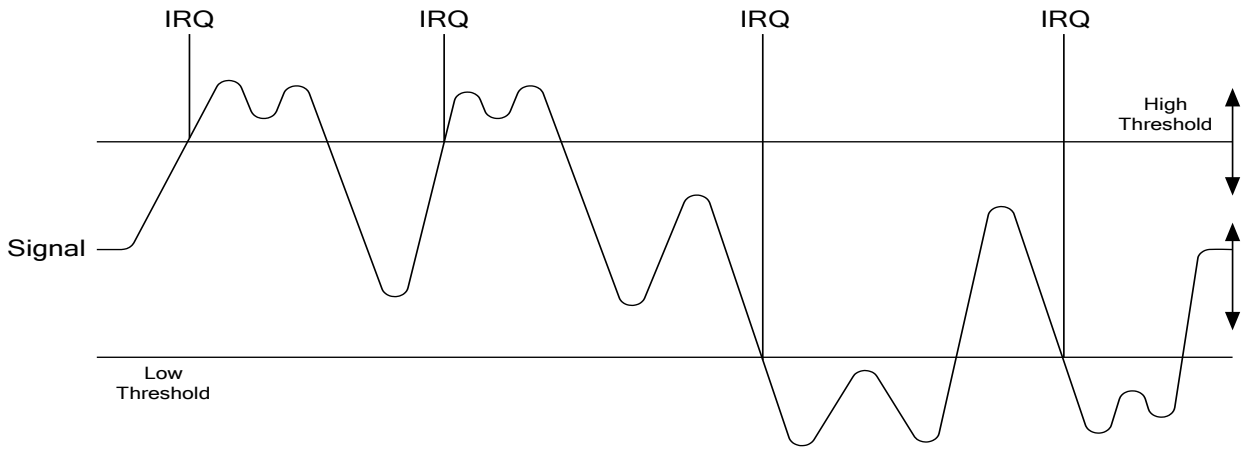


Figure 23 AuxADC IRQ Operation

See:
- AuxADC and TX MOD Mode – $A7 write
- AuxADC1 Data – $A9 read
- AuxADC2 Data – $AA read
- AuxADC Threshold Data – $B5 write

7.15. Auxiliary DAC/RAMDAC Operation

The four Auxiliary DAC channels are programmed via the AuxDAC Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 18), but this may be over-written with a user defined profile by writing to Programming register P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to IDLE or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will become tri-state (high impedance). Note that access to all four AuxDACs is controlled by the AuxDAC Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

See:
- AuxDAC Control/Data – $A8 write

7.16. RF Synthesiser (CMX7031 only)

The CMX7031 includes two Integer-N RF synthesisers, each comprising a divider, phase comparator and charge pump. The divider has two sets of N and R registers: one set can be used for transmit and the other for receive. The division ratios can be set up in advance by means of C-BUS registers. A single C-BUS command will change over from the transmit to the receive division ratios, or vice versa, enabling a fast turnaround.

See:
- RF Channel Data – $B2 write
- RF Channel Control – $B3 write
- RF Channel Status – $B4 8-bit read

External RF components are needed to complete the synthesiser circuit. A typical schematic for one synthesiser, with external components, is shown in Figure 24.

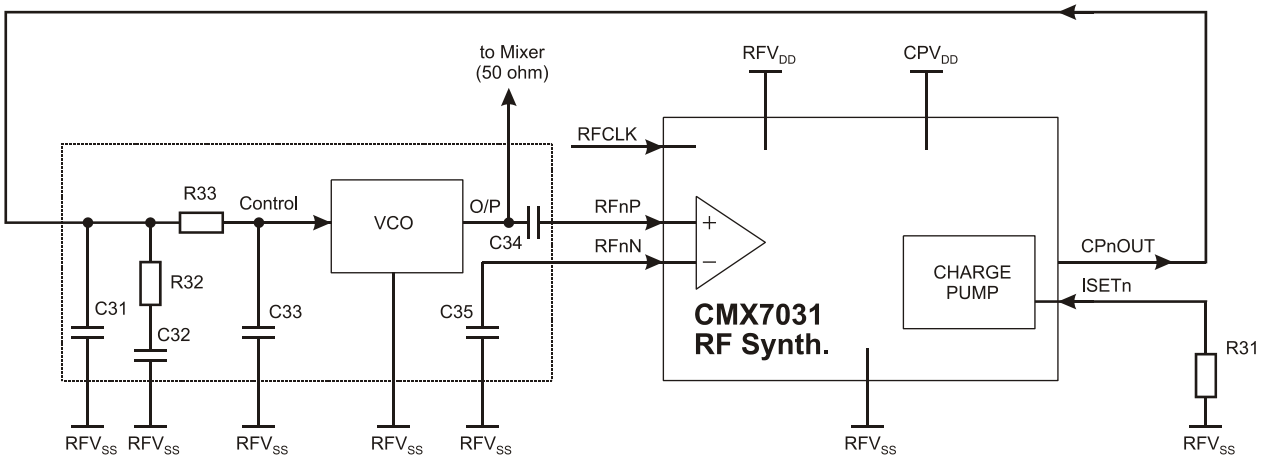


Figure 24 Example RF Synthesiser Components for a 512MHz Receiver

R31	0Ω	C31	820pF
R32	18kΩ	C32	8.2nF
R33	18kΩ	C33	680pF
		C34	1nF
		C35	1nF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Note: R31 is chosen within the range 0Ω to 30kΩ and selects the nominal charge pump current.

It is recommended that C34 and C35 are kept close to the VCO and that the stub from the VCO to the CMX7031/CMX7041 is kept as short as possible. The loop filter components should be placed close to the VCO.

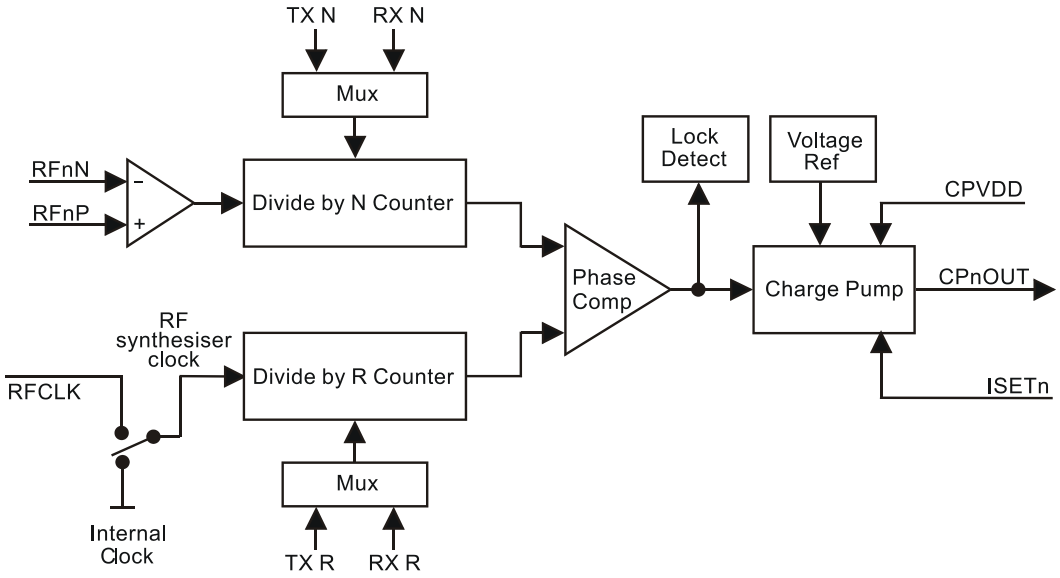


Figure 25 Single RF Channel Block Diagram

The two RF synthesisers are programmable to any frequency in the range 100MHz to 600MHz. Figure 25 is a block diagram of one synthesiser channel. The RF synthesiser clock is selectable between the XTAL or the clock supplied to the RFCLK input pin. The RF synthesiser clock is common to both channels. The charge pump supply (CPVDD) is also common to both channels. The RF input pins, Cpout, Iset and RFV_{SS} pins are channel specific and designated as either RF1P, RF1N, CP1OUT, ISET1, RFV_{SS} or RF2P, RF2N, CP2OUT, ISET2, RFV_{SS} on the Signal List in section 3. The N and R values for Tx and Rx modes are channel specific and can be set from the host µC via the C-BUS. Various channel specific status signals are also accessible via C-BUS. The divide by N counter is 20 bits; the R counter is 13 bits. Typical external components are shown in Figure 24.

Both synthesisers are phase locked loops (PLLs) of the same design, utilising external VCOs and loop filters. The VCOs need to have good phase noise performance although it is likely that the high division ratios used will result in the dominant noise source being the reference oscillator. The phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. Lock detect functions are built in to each synthesiser and the status reported via C-BUS. A transition to out-of-lock can be detected and communicated via a C-BUS interrupt to the host µC. This can be important in ensuring that the transmitter cannot transmit in the event of a fault condition arising.

Two levels of charge pump gain are available to the user, to facilitate the possibility of locking at different rates under program control. A current setting resistor (R31) is connected between the ISET pin (one for each PLL system) and the respective RFV_{SS}. This resistor will have an internally generated band gap voltage expressed across it and may have a value of 0Ω to 30kΩ, which (in conjunction with the on-chip series resistor of 9.6kΩ) will give charge pump current settings over a range of 2.5mA down to 230µA

(including the control bit variation of 4 to 1). The value of the current setting resistor (R31) is determined in accordance with the following formulae:

gain bit set to 1: R31 (in Ω) = (24/Icp) – 9600
gain bit cleared to 0: R31 (in Ω) = (6/Icp) – 9600
where Icp is the charge pump current (in mA).

Note that the charge pump current should always be set to at least 230µA. The 'gain bit' refers to either bit 3 or bit 11 in the RF Channel Control register, $B3.

The step size (comparison frequency) is programmable; to minimise the effects of phase noise this should be kept as high as possible. This can be set as low as 2.5kHz (for a reference input of 20MHz or less), or up to 200kHz – limited only by the performance of the phase comparator.

The frequency for each synthesiser is set by using two registers: an 'R' register that sets the division value of the input reference frequency to the comparison frequency (step size), and an 'N' register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency. This yields the required synthesised frequency (Fs), such that:

$$Fs = (N / R) \times F_{REF}$$ where F_{REF} is the selected reference frequency

Other parameters for the synthesisers are the charge pump setting (high or low)

Since the set-up for the PLLs takes 4 x "RF Channel Data register" writes it follows that, while updating the PLL settings, the registers may contain unwanted or intermediate values of bits. These will persist until the last register is written. It is intended that users should change the content of the "RF Channel Data register" on a PLL that is disabled, powersaved or selected to work from the alternate register set ("Tx" and "Rx" are alternate register sets). There are no interlocks to enforce this intention. The names "Tx" and "Rx" are arbitrary and may be assigned to other functions as required. They are independent sets of registers, one of which is selected to command each PLL by changing the settings in the RF Channel Control – $B3 write register.

For optimum performance, a common master clock should be used for the RF synthesisers (RF Clock) and the baseband sections (Main and Auxiliary System Clocks). Using unsynchronised clocks can result in spurious products being generated in the synthesiser output and in some cases difficulty may be experienced with obtaining lock in the RF synthesisers.

Lock Status

The lock status can be observed by reading the RF Channel Status register, $B4, and the individual lock status bits can (subject to masking) provide a C-BUS interrupt.

The lock detector can use a tolerance of one cycle or four cycles of the reference clock (not the divided version that is used as a comparison frequency) in order to judge phase lock. An internal shift register holds the last three lock status measurements and the lock status bits are flagged according to a majority vote of these previous three states. Hence, one occasional lock error will not flag a lock fail. At least two successive phase lock events are required for the lock status to be true. Note that the lock status bits confirm phase lock to the measured tolerance and not frequency lock. The synthesiser may take more time to confirm phase lock with the lock status bits than the time to switch from channel to channel. The purpose of a 4-cycle tolerance is for the case where a high frequency reference oscillator would not forgive a small phase error.

RF Inputs

The RF inputs are differential and self biased (when not powersaved). They are intended to be capacitatively coupled to the RF signal. The signal should be in the range 0dBm to –20dBm (not necessarily balanced). To ensure an accurate input signal the RF should be terminated with 50Ω as close to the chip as possible and with the "P" and "N" inputs capacitatively coupled to the input and ground, keeping these connections as short as possible. The RF input impedance is almost purely capacitative and is dominated by package and printed circuit board parasitics.

Guidelines for using the RF Synthesisers

- RF input slew rate (dv/dt) should be 14 V/µs minimum.
- The RF Synthesiser 2.5V digital supply can be powered from the VDEC output pin.
- RF clock sources and other, different clock sources must not share common IC components, as this may introduce coupling into the RF. Unused ac-coupled clock buffer circuits should be tied off to a dc supply, to prevent them oscillating.
- It is recommended that the RF Synthesisers are operated with maximum gain Iset (ie. Iset tied to RFVss).
- The loop filter components should be optimised for each VCO.

7.17. Digital System Clock Generators

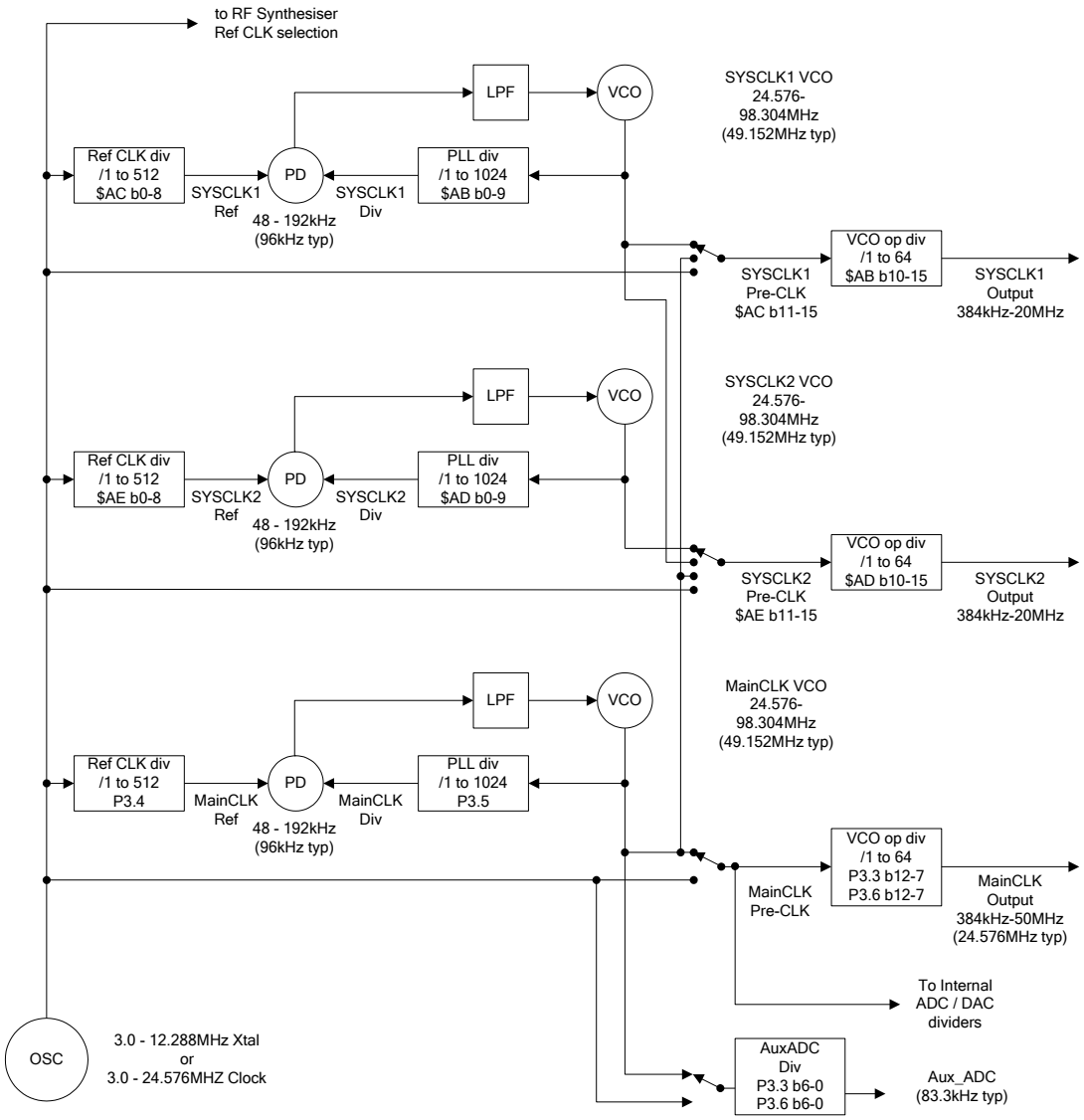


Figure 26 Digital Clock Generation Schemes

The CMX7031/CMX7041 includes a 2-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 5, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 6.144MHz Xtal is assumed for the functionality provided in the CMX7031/CMX7041.

7.17.1 Main Clock Operation

A PLL is used to create the Main Clock (nominally 24.576MHz) for the internal sections of the CMX7031/CMX7041. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose Timer, the signal processing block and the RF Synthesisers. In particular, it should be noted that in IDLE mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX7031/CMX7041 defaults to the settings appropriate for a 6.144MHz Xtal, however if other frequencies are to be used (to facilitate commonality of Xtals between the RF synthesisers and the CMX7031/CMX7041 for instance) then the Program Block registers P3.2 to P3.6 will need to be programmed appropriately at power-on. A table of common values is provided in Table 2.

See:

- Program Block 3 – AuxDAC, RAMDAC and Clock Control:

7.17.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 26. Note that at power-on, these pins provide, by default:

CMX7031: XTAL clk
CMX7041: no signal (off)

See:

- SYSCLK 1 and 2 PLL Data – $AB, $AD write
- SYSCLK1 and 2 REF – $AC and $AE write

7.18. GPIO

Two pins on the CMX7031 or four pins on the CMX7041 are provided for GPIO purposes. GPIO 1 and 2 are driven by the CMX7031/CMX7041 to follow the state of the Rx and Tx Mode bits in the Mode register, $C1:

$C1 Mode	b1	b0	TXENA	RXENA
IDLE	0	0	1	1
Rx	0	1	1	0
Tx	1	0	0	1
reserved	1	1	1	1

With FI-1.3.8.2 onwards and on the CMX7041 only, GPIO A and B are available as outputs controlled by the host using the GPIO write function of the Audiotone register, $CD. This function is provided to maintain compatibility for applications which can dual boot the CMX7141 FI-1 functionality. At power-on their default state is high impedance.

7.19. Signal Level Optimisation

The internal signal processing of the CMX7031/CMX7041 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) – (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. Compared to the reference level of 308mV rms, this is a signal of +8.69dB. This should not be exceeded at any stage. The various level adjustment facilities are shown in Figure 27.

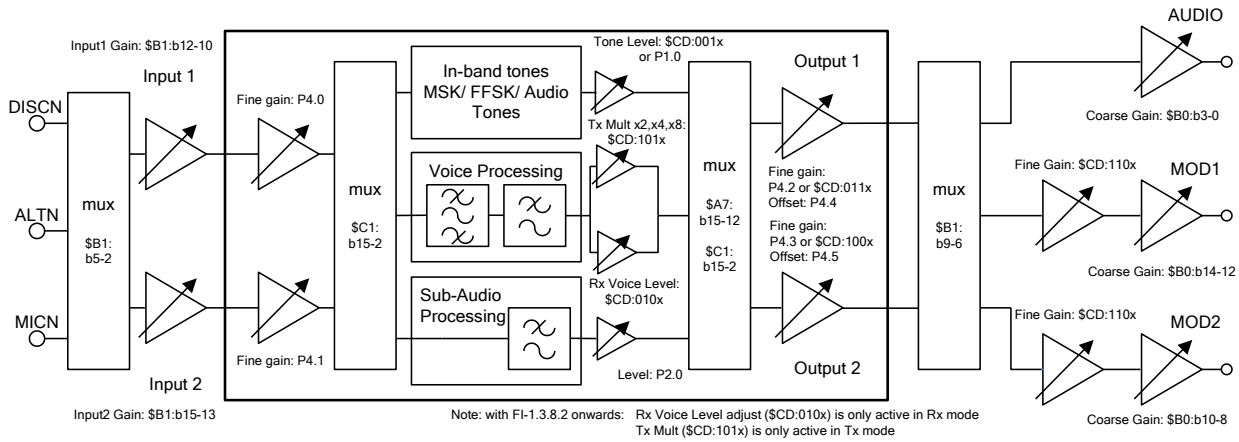


Figure 27 Level Adjustments

7.19.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output level adjustments are set to 0dB. The sub-audio level is normally set to 31mVrms ±1.0dB, which means that the output from the soft limiter must not exceed 803mV rms. If pre-emphasis is used, an output signal at 3000Hz will have three times the amplitude of a signal at 1000Hz, so the signal level before pre-emphasis should not exceed 268mVrms. If the compressor is also used, its 'knee' is at 100mVrms, which would allow a signal into the compressor of 718mVrms, which is less than the maximum signal level. The Fine Input level adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input level adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the MicFB pin would be 54mVrms. With the lowest gain setting (0dB), the maximum allowable input signal level at the MicFB pin would be 718mVrms.

7.19.2 Receive Path Levels

For the maximum signal output from the AUDIO gain/attenuator stage, the signal level at the output of the Analogue Routing block should not exceed +8.69dB, assuming both fine and coarse output level adjustments are set to 0dB. In this case, there is no sub-audio signal to be added, so the maximum signal level remains at 838mVrms. If de-emphasis is used, an output signal at 300Hz will have three and a third times the amplitude of a signal at 1000Hz, so the signal level before de-emphasis should not exceed 251mVrms. If the expander is also used, its 'knee' is at 100mVrms, which would allow a signal into the expander of 158mVrms. The Fine Input level adjustment has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Input level adjustment has a variable gain of up to +22.4dB and no attenuation. If the highest gain setting were used, then the maximum allowable input signal level at the DiscFB pin would be 12.0mV rms. With the lowest gain setting (0dB), the maximum allowable input signal level at the DiscFB pin would be 158mVrms. The signal level of +8.69dB (838mVrms) is an absolute maximum, which should not be exceeded anywhere in the signal processing chain if severe distortion is to be avoided.

7.20. C-BUS Register Summary

Table 14 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC and TX MOD Mode	16
$A8	W	AuxDAC Control/Data	16
$A9	R	AuxADC1 Data/Checksum 2 hi	16
$AA	R	AuxADC2 Data/Checksum 2 lo	16
$AB	W	SYSCLK1 PLL Data	16
$AC	W	SYSCLK1 Ref	16
$AD	W	SYSCLK2 PLL Data	16
$AE	W	SYSCLK2 Ref	16
$AF		Reserved	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Output Signal Routing	16
$B2	W	RF Channel Data	16
$B3	W	RF Channel Control	16
$B4	R	RF Channel Status	8
$B5	W	AuxADC Threshold Data	16
$B6	W	Modem Rx Address	16
$B7		Reserved	
$B8	R	Checksum 1 hi	16
$B9	R	Checksum 1 lo	16
$BA		Reserved	
$BB	R	NWR Status and Data	16
$BC		Reserved	
$BD		Reserved	
$BE		Reserved	
$BF		Reserved	
$C0	W	Power-Down Control	16
$C1	W	Mode Control	16
$C2	W	Audio Control	16
$C3	W	Tx Inband Tones	16
$C4		Reserved	
$C5	R	Rx Data 1	16
$C6	R	Status	16
$C7	W	Modem Control	16
$C8	W	Programming	16
$C9	R	Rx Data 2 and XTCSS	16
$CA	W	Tx Data 1	16
$CB	W	Tx Data 2 and XTCSS	16
$CC	R	Tone Status	16
$CD	W	Audio Tone	16
$CE	W	Interrupt Mask	16
$CF		Reserved	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

7.20.1 Interrupt Operation

The CMX7031/CMX7041 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the Status register, except the Programming Flag (bit 0) and the RF Channel Status Flag (bit 1), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. The Programming Flag bit is set to 1 only when it is permissible to write a new word to the Programming register. See:

- Status – $C6 read
- Interrupt Mask – $CE write

7.20.2 General Notes

In normal operation, the most significant registers are:

- Mode Control – $C1 write
- Status – $C6 read
- Analogue Output Gain – $B0 write
- Input Gain and Output Signal Routing – $B1 write
- Audio Control – $C2 write

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed, whilst setting the Mode register to IDLE will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in IDLE mode.

Under normal circumstances the CMX7031/CMX7041 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

8. Performance Specification

8.1. Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
RFV_{DD}- RFV_{SS}	–0.3	4.5	V
CPV_{DD}- RFV_{SS}	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Voltage on any pin to RFV_{SS} (excluding CPV_{DD})	–0.3	RFV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS}, CPV_{DD}, RFV_{DD} or RFV_{SS})	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD}	0	0.3	V
DV_{SS} and AV_{SS} or RFV_{SS}	0	50	mV
AV_{SS} and RFV_{SS}	0	50	mV

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1690	mW
… Derating	–	16.9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	3500	mW
… Derating	–	35.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1600	mW
... Derating	–	16.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
CPV_{DD} – RFV_{SS}		3.0	3.6	V
RFV_{DD} – DV_{SS}	13	2.25	2.75	V
V_{DEC} – DV_{SS}	12	2.25	2.75	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using a Xtal)	11	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	11	3.0	24.576	MHz

Notes:
11 Nominal XTAL/CLK frequency is 6.144MHz.
12 The V_{DEC} supply is automatically created from DV_{DD} by the on-chip voltage regulator.
13 The RFV_{DD} supply can be supplied from the V_{DEC} supply, if preferred.

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.01% (100ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} = 3.0V to 3.6V; RFV_{DD} = 2.25V to 2.75V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device when loaded with FI 1.5 only. The use of other Function Images™, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	100	µA
AI_{DD} (AV_{DD} = 3.3V)		–	4	20	µA
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	4	20	µA
IDLE Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	1.1	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	250	–	µA
Rx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	4.8	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	3.0	–	mA
Tx Mode	22				
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	6.1	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	3.0	–	mA
Additional Current for each RF Synthesiser	23				
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	2.5	4.5	mA
Additional Current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	500	–	µA
Additional Current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	5	–	µA
Additional Current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes:
21 Tamb = 25°C, Not including any current drawn from the device pins by external circuitry.
22 System Clocks, RF, Auxiliary circuits, audio scrambler, compander and pre/de-emphasis disabled, but all other digital circuits (including the Main Clock PLL) enabled. A single analogue path is enabled through the device.
23 When using the external components shown in Figure 24 and when supplying the current for RFV_{DD} from the regulated 2.5V digital (V_{DEC}) supply. The latter is derived from DV_{DD} by an on-chip voltage regulator.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	25				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	21	–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 120µA)		90%	–	–	DV_{DD}
(I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = 360µA)		–	–	10%	DV_{DD}
(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current	21	–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
RDATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes: 25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' pulse width		31	15	–	–	ns
'Low' pulse width		31	15	–	–	ns
Input Impedance (at 6.144MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
Auxiliary SYSCLK1/2 Outputs						
XTAL/CLK Input to CLOCK_OUT Timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' pulse width		33	76	81.38	87	ns
'Low' pulse width		33	76	81.38	87	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)						
Input Impedance		34	–	1	–	MΩ
Maximum Input Level (pk-pk)		35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)			80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mVrms at 100Hz)			–	60	–	dB
Unity Gain Bandwidth			–	1.0	–	MHz
Programmable Input Gain Stage		36				
Gain (at 0dB)		37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)		37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz XTAL fitted and 6.144MHz output selected.

34 With no external components connected.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB OR MICFB.

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD 1, MOD 2, AUDIO)					
Power-up to outputs stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance		–	10	–	MΩ
Capacitance		–	5	–	pF
Zero Error (input offset to give ADC output = 0)		0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error (output offset from a DAC input = 0)		0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
RF Synthesisers – Phase Locked Loops					
Reference Clock Input					
Input Logic '1'	62	70%	–	–	RFV_{DD}
Input Logic '0'	62	–	–	30%	RFV_{DD}
Frequency	64,66	5.0	19.2	40.0	MHz
Divide Ratios (R)	63	2	–	8191	
Each RF Synthesiser	69				
Comparison Frequency		–	–	500	kHz
Input Frequency Range	67	100	–	600	MHz
Input Level		−14	–	0	dBm
Input Slew Rate		14	–	–	V/µs
Divide Ratios (N)		1088	–	1048575	
1Hz Normalised Phase Noise Floor	68	–	−197	–	dBc/Hz
Charge Pump Current (high)	65	±1.88	±2.5	±3.3	mA
Charge Pump Current (low)	65	±470	±625	±820	µA
Charge Pump Current – voltage variation		–	10%	–	per V
Charge Pump Current – sink to source match		–	5%	–	of ISET

Notes:

62 Square wave input.

63 Separate dividers are provided for each PLL.

64 For optimum performance of the synthesiser subsystems, a common master clock should be used for the RF Synthesisers and the baseband sections. Using unsynchronised clocks is likely to result in spurious products being generated in the synthesiser outputs and in some cases difficulty may be experienced in obtaining lock in the RF Synthesisers.

65 External ISET resistor (R31) = 0Ω (Internal ISET resistor = 9k6Ω nominally).

66 Lower input frequencies may be used subject to division ratio requirements being maintained.

67 Operation outside these frequency limits is possible, but not guaranteed. Below 150MHz, a square wave input may be required to provide a fast enough slew rate.

68 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop by:

Phase Noise (in-band) = $PN1Hz + 20\log_{10}(N) + 10\log_{10}(f_{comparison})$

69 It is recommended that RF Synthesiser 1 be used for the higher frequency use (eg: RF 1st LO) and RF Synthesiser 2 be used for lower frequency use (eg: IF LO).

8.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 6.144MHz ±0.003% (30ppm)[§]; Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} = 3.0V to 3.6V; RFV_{DD} = 2.25V to 2.75V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.
All figures quoted in this section apply to the device when loaded with FI 1.5 only. The use of other Function Images™, can modify the parametric performance of the device.

AC Parameters (cont.)		Notes	Min.	Typ.	Max.	Unit
Receiver Signal Type Identification						
Probability of correctly identifying signal type (SNR = 12dB)			–	>>99.9	–	%
CTCSS Detector						
Sensitivity	(Pure Tone)	71	–	−26	–	dB
SINAD opening		72	–	5	–	dB
Response Time	(Composite Signal)	72	–	225	250	ms
De-response Time	(Composite Signal)	72, 75	–	210	250	ms
Dropout Immunity		75	–	160	–	ms
Falsing		72	–	1	–	
Frequency Range			60	–	260	Hz
Inband Tone Detector						
Sensitivity	(Pure Tone)	73	–	−26	–	dB
Response Time	(Good Signal)		–	35	–	ms
De-response Time	(Good Signal)		–	–	45	ms
Drop-out Immunity		76	–	–	20	ms
Frequency Range	(Inband Tone)		288	–	3000	Hz
DCS Decoder						
Sensitivity		71	44	–	–	mVp-p
Bit-Rate Sync Time			–	2	–	edges
MSK/FFSK Decoder						
Signal Input Dynamic Range		74	100	–	800	mVrms
Bit Error Rate	(SNR = 20dB)	74	–	<1	–	10^{-8}
Receiver Synchronisation	(SNR = 12dB)					
Probability of bit 16 being correct			–	>99.9	–	%
FSK/DSC Decoder						
Signal Input Dynamic Range		74	100	–	800	mVrms
Bit Error Rate	(SNR = 8dB)	74	–	<1	–	10^{-2}
Co-channel Rejection			–	10	–	dB

Notes:

§ To meet DSC specifications, a 30ppm xtal, or better, is required.

71 Sub-Audio Detection Level threshold set to 16mVrms (CTCSS) or 44mVpk-pk (DCS).

72 Tested as per TIA-603 C.

73 Inband Tone Detection Level threshold set to 16mV.

74 AV_{DD} = 3.3V, for a "101010101 … 01" pattern measured at the input amplifier feedback pin. Signal level scales with AV_{DD}.

75 With sub-audio dropout time (P2.5) set to default. The typical dropout immunity is approximately 40ms more than the programmed dropout time. The typical de-response time is approximately 90ms longer than the programmed dropout time. See section 9.2.3, P2.5 in the CMX7031/CMX7041 User Manual.

76 Immunity to signal drop-outs of up to the specified duration.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
DTMF Decoder					
Sensitivity		–	-22	+3	dB
Response Time		–	35	–	ms
De-response Time		–	–	45	ms
Falsing Rate (per 30min Voice input)		–	10	–	
Frequency Tolerance		–	±2.5	–	%
Twist		-10	–	+10	dB
NWR Decoder					
Sensitivity		–	TBD	–	dB
Audio Compandor					
Attack Time		–	4.0	–	ms
Decay Time		–	13	–	ms
0dB-point	84	–	100	–	mVrms
Compression/Expansion Ratio		–	2:1	–	
CTCSS Encoder					
Frequency Range		60.0	–	260	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	81	−1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%
Inband Tone Encoder					
Frequency Range		288	–	3000	Hz
Tone Frequency Accuracy		–	–	±0.3	%
Tone Amplitude Tolerance	83	−1.0	0	+1.0	dB
Total Harmonic Distortion	82	–	2.0	4.0	%
DCS Encoder					
Bit Rate		–	134.4	–	bps
Amplitude Tolerance	81	−1.0	0	+1.0	dB
DTMF Encoder					
Output Signal Level (2dB twist)		–	360	775	mVrms
Output Level Variation					dB
Output Distortion		–	–	5	%
MSK/FFSK Encoder					
Output Signal Level		–	775	–	mVrms
Output Level Variation		−1.0	0	+1.0	dB
Output Distortion		–	–	5	%
3rd Harmonic Distortion		–	–	3	%
Logic 1 Frequency 1200baud and 2400baud		1198	1200	1202	Hz
Logic 0 Frequency 1200baud		1798	1800	1802	Hz
2400baud		2398	2400	2402	Hz
Isochronous Distortion (0 to 1 and 1 to 0)		–	–	40	µs
PSK Encoder					
Bit Rate		–	559.2	–	bps
Carrier Frequency		–	1398	–	Hz

Notes:
81 AV_{DD} = 3.3V and Tx Sub-Audio Level set to 88mV p-p (31mVrms).
82 Measured at MOD 1 or MOD 2 output.
83 AV_{DD} = 3.3V and Tx Audio Level set to 871mV p-p (308mVrms).
84 AV_{DD} = 3.3V.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
FSK/DSC Encoder					
Output Signal Level		–	775	–	mVrms
Output Distortion		–	–	5	%
3rd Harmonic Distortion		–	–	3	%
Logic 1 Frequency		–	1300	–	Hz
Logic 0 Frequency		–	2100	–	Hz
Baud Rate		–	1200	–	bps
Pre-emphasis (per octave)		–	6	–	dB
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Received Audio	91	300	–	3300	Hz
12.5kHz Channel Transmitted Audio	92	300	–	2550	Hz
25kHz Channel Transmitted Audio	93	300	–	3000	Hz
Pass-band Gain (at 1.0kHz)		–	0	–	dB
Pass-band Ripple (wrt gain at 1.0kHz)		−2.0	0	+0.5	dB
Stop-band Attenuation		33.0	–	–	dB
Residual Hum and Noise Tx	96	–	−47	–	dBm
Residual Hum and Noise Rx	96	–	−74	–	dBm
Pre-emphasis	94	–	+6	–	dB/oct
De-emphasis	95	–	−6	–	dB/oct
Audio Scrambler					
Inversion Frequency		–	3300	–	Hz
Pass-band		320	–	2900	Hz
Audio Expandor					
Input Signal Range	97	–	–	0.55	Vrms

Notes:

91 The receiver audio filter complies with the characteristic shown in Figure 10. The high pass filtering removes sub-audio components from the audio signal.

92 The 12.5kHz channel filter complies with the characteristic shown in Figure 14.

93 The 25kHz channel filter complies with the characteristic shown in Figure 13.

94 The pre-emphasis filter complies with the characteristic shown in Figure 15

95 The de-emphasis filter complies with the characteristic shown in Figure 12.

96 Psophometrically weighted. Pre/de-emphasis, Compandor and 25kHz channel filter selected.

97 AV_{DD} = 3.3V.

8.2. C-BUS Timing

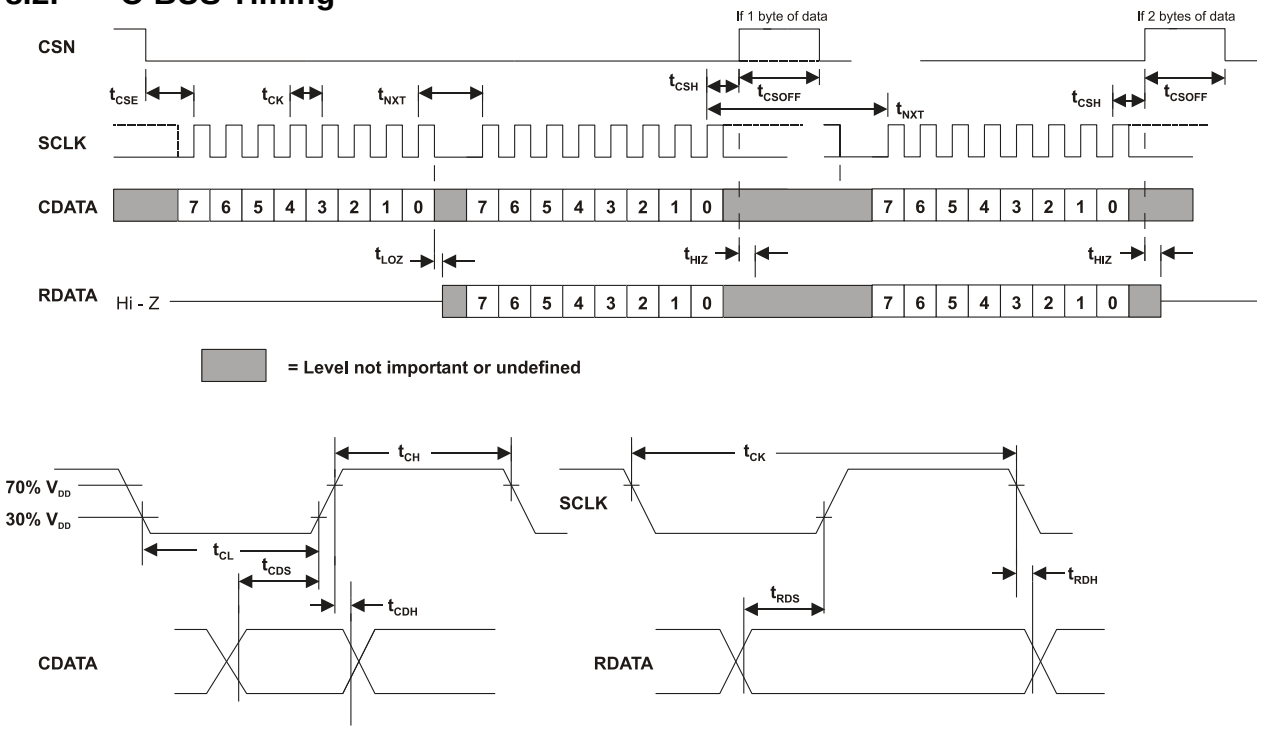


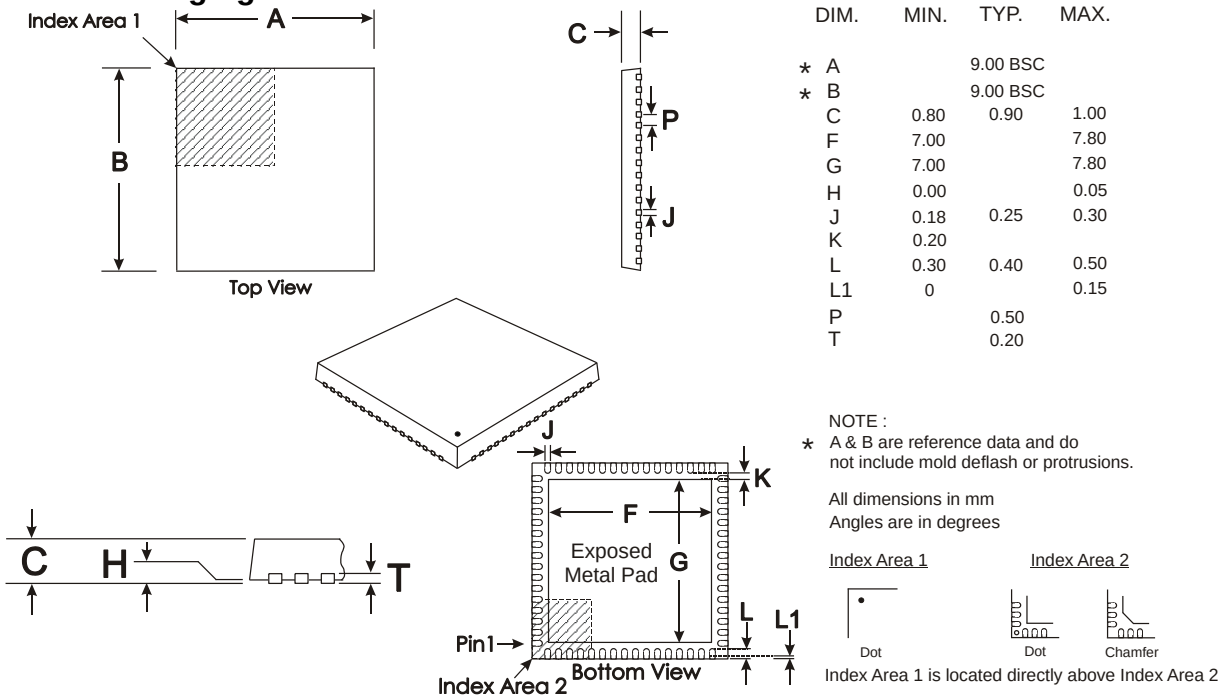
Figure 28 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7031/CMX7041 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

8.3. Packaging



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

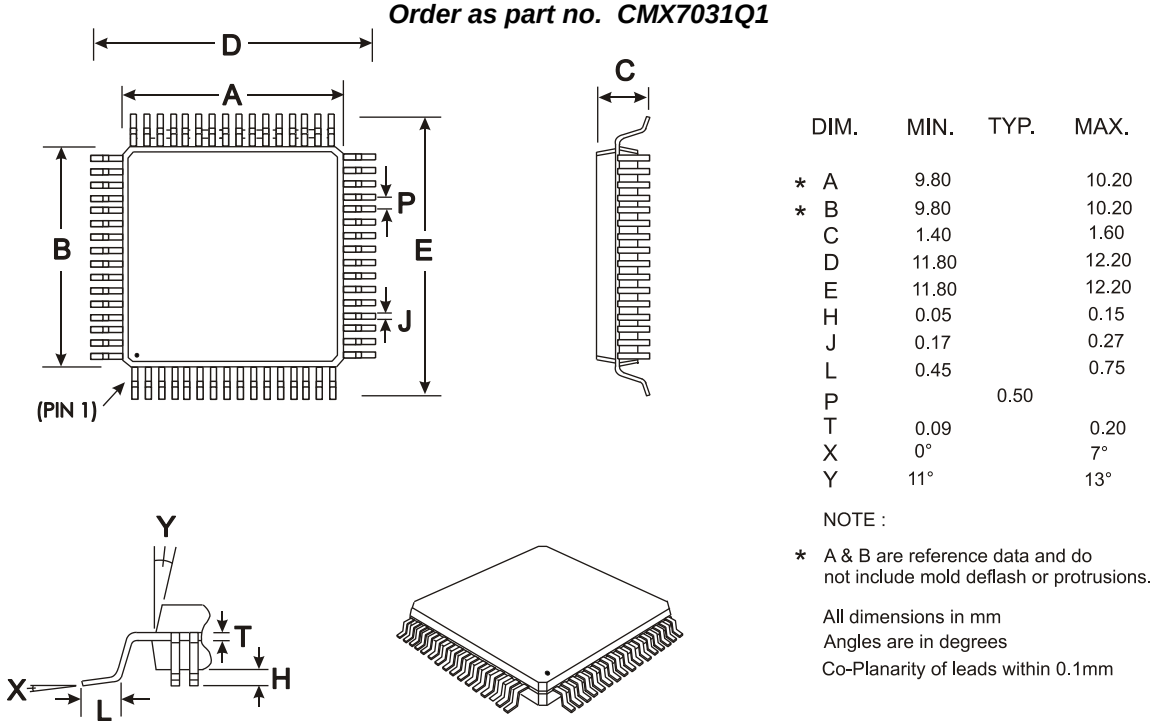
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 29 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7031Q1



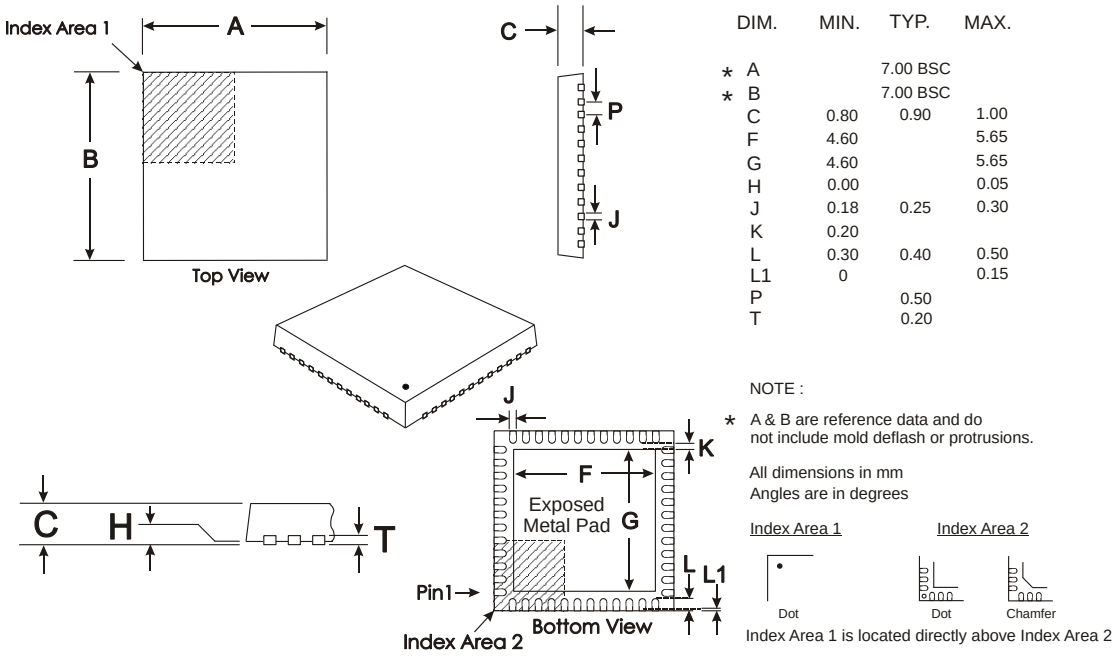
DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 30 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7031L9



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

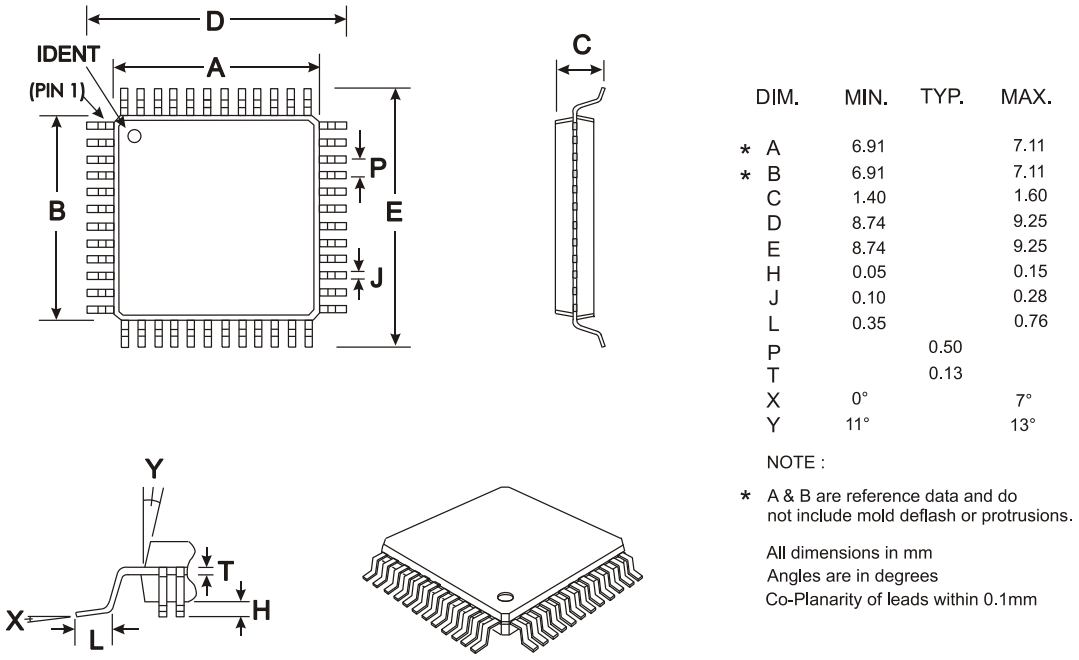
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 31 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7041Q3



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 32 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7041L4

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support area of the CML website: [http://www.cmlmicro.com/].

Infinite Capabilities . . .
FirmASIC®
. . . Maximum Flexibility

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

CML Microcircuits (UK) Ltd COMMUNICATION SEMICONDUCTORS	CML Microcircuits (USA) Inc. COMMUNICATION SEMICONDUCTORS	CML Microcircuits (Singapore) Pte Ltd COMMUNICATION SEMICONDUCTORS
Tel: +44 (0)1621 875500 **Fax:** +44 (0)1621 875600 **Sales:** sales@cmlmicro.com **Tech Support:** techsupport@cmlmicro.com	**Tel:** +1 336 744 5050 800 638 5577 **Fax:** +1 336 744 5054 **Sales:** us.sales@cmlmicro.com **Tech Support:** us.techsupport@cmlmicro.com	**Tel:** +65 62 888129 **Fax:** +65 62 888230 **Sales:** sg.sales@cmlmicro.com **Tech Support:** sg.techsupport@cmlmicro.com
- www.cmlmicro.com -		

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for RF Wireless Misc ***category:***

Click to view products by CML Microcircuits ***manufacturer:***

Other Similar products are found below :

R415720000 HMC598-SX RX98-4 MABT-011000-14235P W2SW0001-SHLD HMC1110-SX HMC579-SX R417703118 MA4BN1840-1 HMC443LP4ETR HMC561LP3ETR STHVDAC-253MF3 ADL5390ACPZ-REEL7 ADA4304-2ACPZ-R7 ADA4304-3ACPZ-R2 ADA4304-4ACPZ-R2 ADA4304-4ACPZ-R7 ADA4304-3ACPZ-R7 HMC760LC4B HMC577LC4B HMC370LP4E HMC444LP4E HMC445LP4E HMC448 HMC1096LP3ETR HMC573LC3BTR HMC575LP4 HMC575LP4E HMC576 HMC576LC3B HMC576LC3BTR HMC578 HMC578LC3B HMC578LC3BTR HMC578-SX HMC579 HMC598 HMC695LP4E HMC814 HMC814LC3B HMC814LC3BTR HMC814-SX SML1 MAX2045ETJ+ CMX882E1 CMX881E1 SA606DK/01,118 MAX1005CEE+ MAX2046ETJ MAX9990ETP+