CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7262
TWELP Vocoder

D/7262_FI-1.x/4 August 2013

DATASHEET

Advance Information

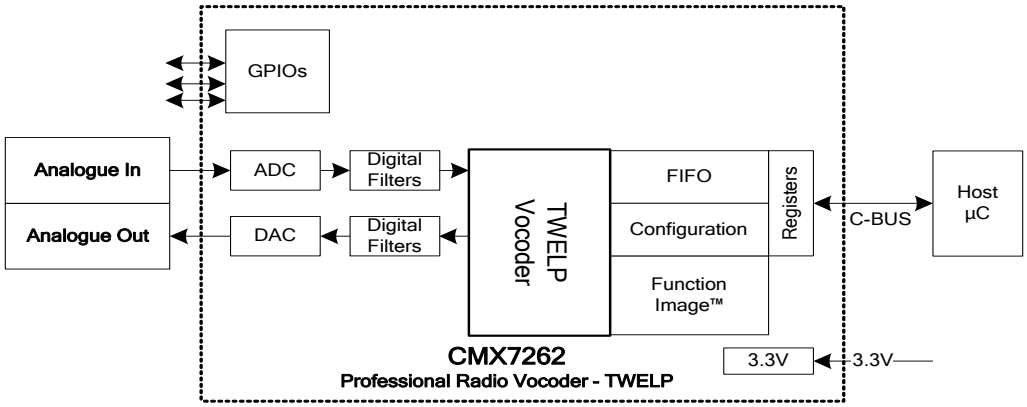
7262 FI-1.x Professional Radio Vocoder

Features

- High-performance, low bit rate vocoder using TWELP (Tri-wave Excited Linear Prediction) technology
- Crystal clear voice and excellent performance in real-life radio operation
- Excellent performance providing natural-sounding speech and high quality non-voiced signals such as emergency services sirens
- Half-duplex operation
- FEC built in to each vocoder frame
- Noise Reduction
- Integral voiceband audio codec (No external DSP or codecs required)
- C-BUS host serial interface
  - Streaming input and output registers to streamline transfers and relax host service latency
- Signal routing:
  - Choice of input sources – C-BUS transfer from host, analogue audio input
  - Choice of output sources – C-BUS transfer to host, analogue audio output
- Auxiliary functions
  - GPIOs
  - Two differential audio outputs
  - Single-ended speaker output
  - Analogue input/output gain adjustment
  - Analogue input multiplexer
  - Analogue output multiplexer
- Low power 3.3V operation with powersave functions
- Small 64-pin VQFN package

Applications

- Half duplex digital radio systems
- Personal area network voice links
- Secure digital voice communications
- Secure door access
- Wireless PBX
- VoIP applications
- Digital Software Defined Radio (SDR)



1 Brief Description

The CMX7262 TWELP Vocoder IC is a device supporting a Tri-Wave Excited Linear Prediction (TWELP) vocoder functionality in a single chip. The CMX7262 is capable of encoding analogue voice into TWELP-encoded frames. It is capable of decoding TWELP-encoded frames back to analogue voice.

Input and output signals may be passed through the C-BUS interface, or the on-chip analogue-to-digital and digital-to-analogue converters (ADC/DAC).

The CMX7262 is designed to be flexible. However, it interfaces directly to the CMX7141 modem and the two can used together to build a dPMR radio.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from a host microcontroller over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7262 operates from a 3.3V supply and includes selectable power saving modes. It is available in a 64-VQFN (Q1) and 64-LQFP (L9) packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This Data Sheet is the first part of a two-part document.

CONTENTS

Table Page

Figure Page

Information in this data sheet should not be relied upon for final product design. It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
4	Initial Encoder Delay added: • Section 6.14: (register summary table) updated • Section 8.1: (register details) updated • Section 8.1.13: register description (Initial Encoder Delay $59) added • Section 9.2: Function Images updated • Miscellaneous typographical and editorial changes	30/08/2013
3	Decoder Noise Gate added: • Section 2.1: (block diagram) updated • Section 6.11: (Noise Gate) added • Section 6.14: (register summary table) updated • Section 8.1: (register details) updated • Section 8.1.16: new register description (Noise Gate Configuration $5E) • Section 9.2: Function Images updated	17/04/2013
2	Test Mode added: • Section 6.13 (register summary table) updated • Section 8.1 (register details) updated • Section 8.1.9, new register description (Frequency Control $52) added • Section 8.1.19 (description for VCTRL register) updated to include Test Mode • Section 9.2, Function Images updated Miscellaneous typographical and editorial changes Added advice about connection to the exposed metal pad in Q1 package.	06/09/2012
1	• First approved version	26/07/2012

2 Block Diagram

2.1 TWELP Vocoder

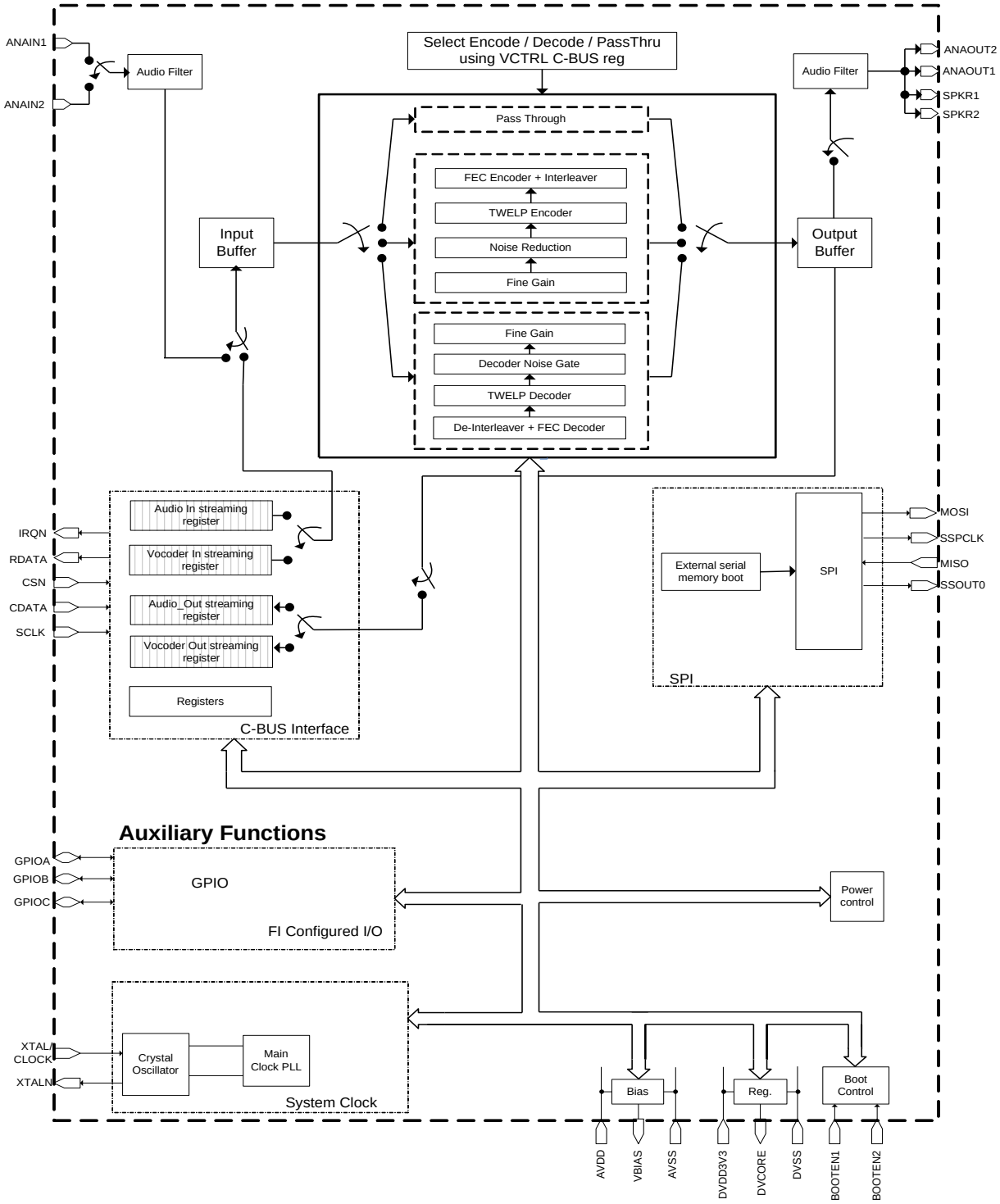


Figure 1 Block Diagram

3 Signal List

64-pin L9/Q1	Pin		Description
Pin No.	Name	Type	
1	NC	NC	Reserved - Do not connect.
2	BOOTEN1	IP+PD	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determines the Function Image™ load interface.
3	BOOTEN2	IP+PD	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determines the Function Image™ load interface.
4	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
5	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
6	GPIOA	BI	General Purpose I/O.
7	RESETN	IP	Logic input used to reset the device (active low).
8	GPIOB	BI	General Purpose I/O.
9	GPIOC	BI	General Purpose I/O.
10	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
11	SPKR2	OP	Single-ended output for speaker.
12	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuits Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
13	SPKR1VSS	PWR	Negative supply rail (ground) for the on-chip speaker driver circuit.
14	SPKR1P	OP	Low-impedance differential driver to the external speaker; ‘P’ is positive, ‘N’ is negative. Together these are referred to as the SPKR1 output.
15	SPKR1N	OP	
16	SPKR1VDD	PWR	Positive supply rail for the on-chip speaker driver circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to SPKR1VSS by capacitors mounted close to the device pin.
17	ANAOUT1P	OP	Differential outputs for main audio; ‘P’ is positive, ‘N’ is negative. Together these are referred to as ANAOUT1.
18	ANAOUT1N	OP	
19	ANAOUT2P	OP	Differential outputs for monitor audio; ‘P’ is positive, ‘N’ is negative. Together these are referred to as ANAOUT2.
20	ANAOUT2N	OP	
21	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
22	DACREF	PWR	DAC reference voltage, connect to AVSS.

64-pin L9/Q1	Pin		Description
Pin No.	Name	Type	
23	ANAIN2P	IP	Input (IP) and feedback (FB) connections to single-ended audio input 2. Gain and filtering circuitry can be constructed around these pins. Together these are referred to as ANAIN2.
24	ANAIN2FB	OP	
25	NC	NC	Do not connect.
26	NC	NC	Do not connect.
27	VBIAS	OP	Internally-generated bias voltage of approximately AVDD/2. If VBIAS is power saved this pin will present a high impedance to AVDD. This pin must be decoupled to AVSS by a capacitor mounted close to the device pins; no other connections should be made.
28	ANAIN1P	IP	Differential inputs for main audio; 'P' is positive, 'N' is negative. Together these are referred to as ANAIN1.
29	ANAIN1N	IP	
30	ADCREF		ADC reference voltage; connect to AVSS.
31	NC	NC	Reserved - Do not connect.
32	NC	NC	Reserved - Do not connect.
33	NC	NC	Reserved - Do not connect.
34	NC	NC	Reserved - Do not connect.
35	NC	NC	Reserved - Do not connect.
36	NC	NC	Reserved - Do not connect.
37	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
38	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits.
39	NC	NC	Reserved - Do not connect.
40	NC	NC	Reserved - Do not connect.
41	NC	NC	Reserved - Do not connect.
42	NC	NC	Reserved - Do not connect.
43	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
44	DVCORE1	PWR	Digital core supply, nominally 1.8V. By default, this will be supplied by an on-chip regulator, although an option is available to use an external regulator. This pin should be decoupled to DVSS by capacitors mounted close to the device pins and connected with a power supply track to DVCORE2. For details see programming register P1.19 in section in 9.1.2 Program Block 1 – Clock Control.

64-pin L9/Q1	Pin		Description
Pin No.	Name	Type	
45	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
46	NC	NC	Reserved - Do not connect.
47	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
48	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits.
49	XTALN	OP	Output from the on-chip xtal oscillator inverter.
50	XTAL/CLOCK	IP	Input to the oscillator inverter from the xtal circuit or external clock source.
51	NC	NC	Reserved - Do not connect.
52	NC	NC	Reserved - Do not connect.
53	SCLK	IP	C-BUS serial clock input from the microcontroller.
54	RDATA	TS OP	3-state C-BUS serial data output to the microcontroller. This output is high impedance when not sending data to the microcontroller.
55	CDATA	IP	C-BUS serial data input from the microcontroller.
56	CSN	IP	C-BUS chip select input from the microcontroller.
57	IRQN	OP	'wire-Orable' output for connection to the Interrupt Request input of the microcontroller. This output is pulled down to DVSS when active and is high impedance when inactive. An external pull-up resistor is required.
58	DVCORE2	PWR	Digital core supply, nominally 1.8V. By default, this will be supplied by the on-chip regulator, although an option is available to use an external regulator. This pin should be decoupled to DVSS by capacitors mounted close to the device pins and connected with a power supply track to DVCORE1. For details see programming register P1.19 in section in 9.1.2 Program Block 1 – Clock Control.
59	MOSI	OP	SPI: Master Out Slave In.
60	NC	NC	Reserved - Do not connect.
61	MISO	IP	SPI: Master In Slave Out.
62	SSOUT0	OP	SPI: Slave Select Out 0.
63	SSPCLK	OP	SPI: Serial Clock.
64	NC	NC	Do not connect.
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on the Q1 package only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connection is permitted.**

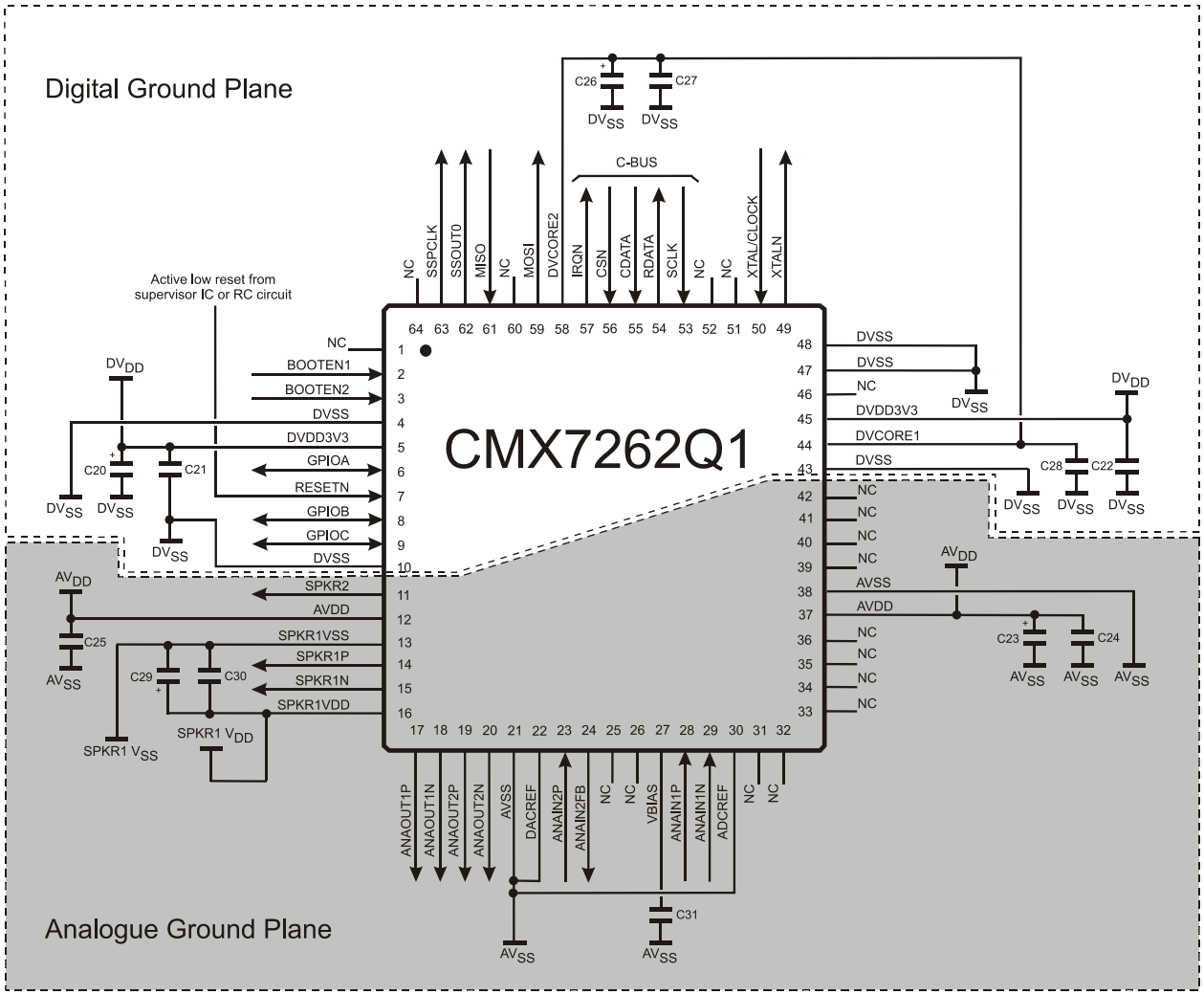
Notes: IP = Input (+ PU/PD = internal pull-up / pull-down resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{DD3v3}	DVDD3V3	3.3V positive supply rail for the digital on-chip circuits
DV_{SS}	DVSS	Ground for all digital circuits
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
DV_{CORE}	DVCORE1, DVCORE2	Power for digital core voltage of approximately 1.8V

4 PCB Layout Guidelines and Power Supply Decoupling



C20	10µF	C26	22µF
C21	10nF	C27	10nF
C22	10nF	C28	10nF
C23	10µF	C29	10µF
C24	10nF	C30	10nF
C25	10nF	C31	100nF

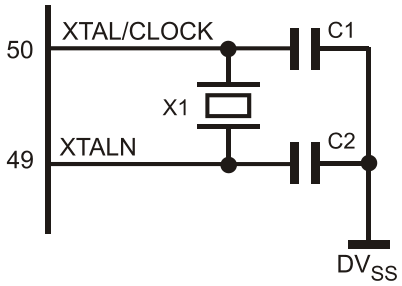
Figure 2 CMX7262 Power Supply and De-coupling

Notes:

To achieve good noise performance, V_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX7262 area to provide a low-impedance connection between the VSS pins and the V_{DD} and V_{BIAS} decoupling capacitors.

5 External Components

5.1 Xtal Interface



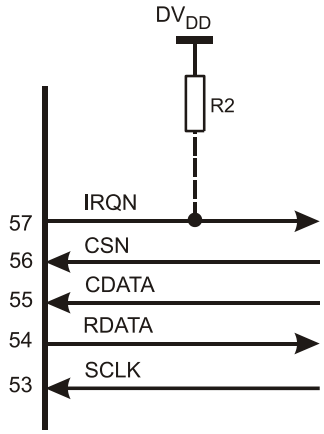
X1 For frequency range see section 7.1.2 Operating Limits
C1 22pF Typical
C2 22pF Typical

Figure 3 Recommended External Components – Xtal Interface

Notes:

- The clock circuit can operate with either a xtal or external clock generator. If using an external clock generator it should be connected to the XTAL/CLOCK pin and the xtal and other components are not required. For external clock generator frequency range see section 7.1.2 Operating Limits. When using an external clock generator the XTAL oscillator circuit may be disabled to save power, see 9.1.2 Program Block 1 – Clock Control for details.
- The tracks between the xtal and the device pins should be as short as possible to achieve maximum stability and best start up performance. It is also important to achieve a low-impedance connection between the xtal capacitors and the ground plane.
- The DV_{SS} supply to the xtal oscillator capacitors C1 and C2 should be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up. For correct values of capacitors C1 and C2 refer to the manufacturer's documentation for the xtal used.

5.2 C-BUS Interface



R2 10kΩ - 100kΩ

Figure 4 Recommended External Components – C-BUS Interface

Note: If the IRQN line is connected to other compatible pull-down devices only one pull-up resistor is required on the IRQN node.

5.3 Serial Port Interface

The CMX7262 can also load its Function Image™ from an external serial memory. Pins 59, 61, 62 and 63 act as serial port pins. For more information refer to section 3 Signal List.

Figure 5 below shows the connections required for interfacing CMX7262 to a typical external serial memory for booting from a Function Image™.

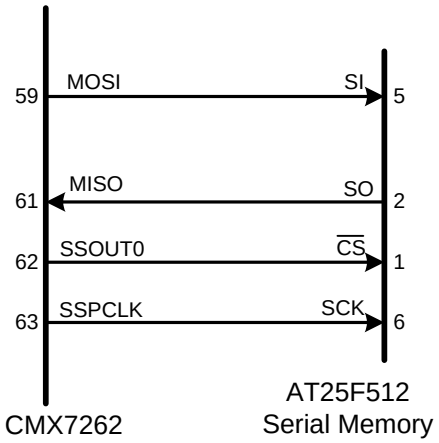


Figure 5 Interfacing the CMX7262 to Serial Memory

Hardware design must ensure that, when booting from external serial memory, no device other than the external serial memory drives the serial port interface pins.

5.4 Audio Output

5.4.1 Audio Output Routing

The CMX7262 has four possible analogue outputs: two differential outputs – ANAOUT1 and ANAOUT2, a low-impedance differential output speaker driver – SPKR1 and, a single-ended output – SPKR2 that can drive a headset/earpiece.

The CMX7262's DAC (ANAOUT DAC) can output analogue waveforms on any or all of the four outputs (ANAOUT1, ANAOUT2, SPKR1 and SPKR2) under the control of four C-BUS registers. Figure 6 Analogue Audio Output Routing, shows the analogue output signal routing and control.

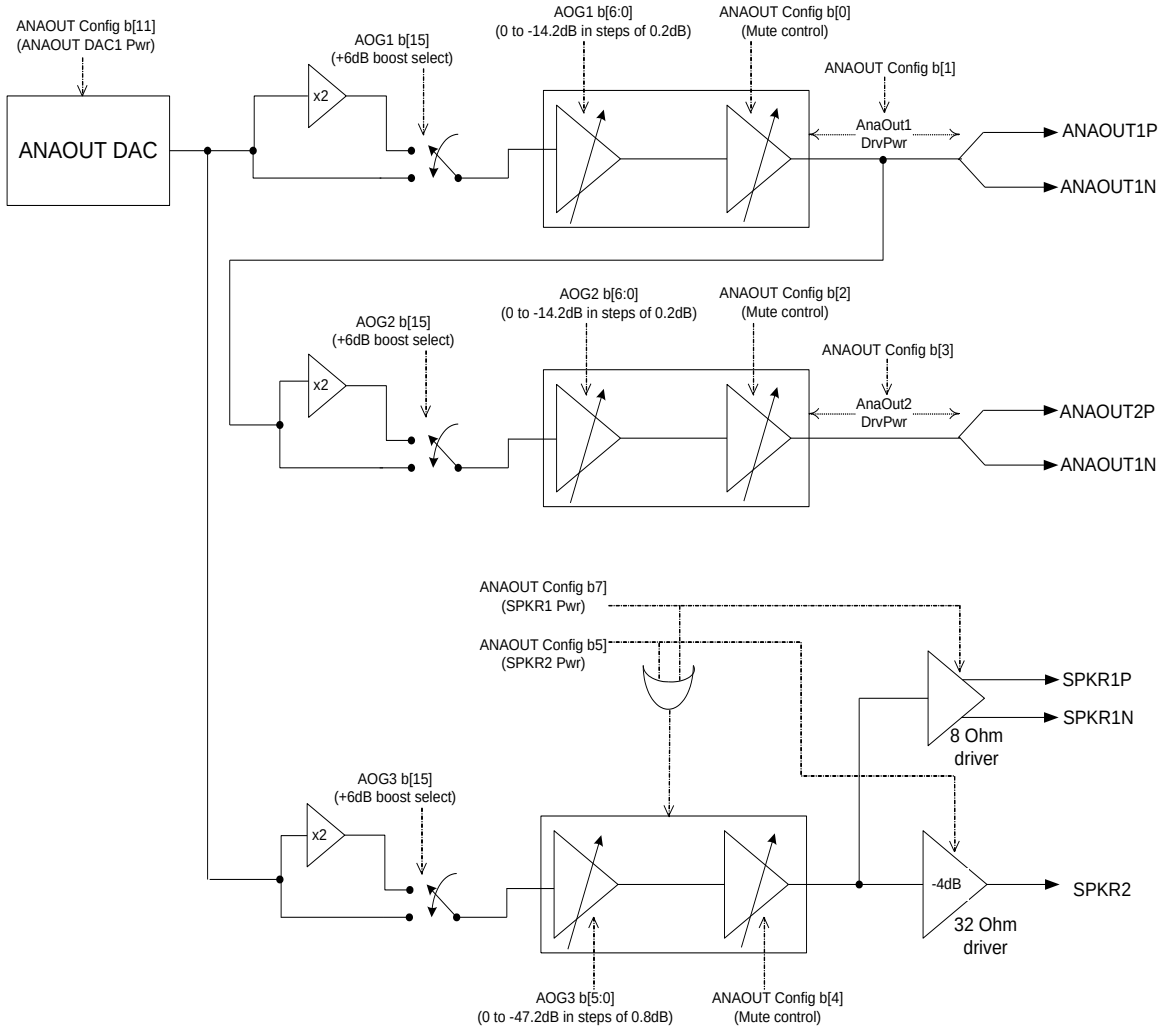


Figure 6 Analogue Audio Output Routing

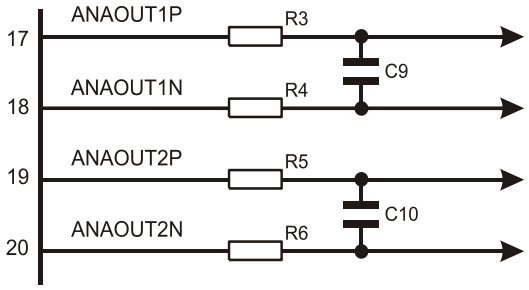
The registers that control the analogue audio output routing are:

- 8.1.25 ANAOUT Config - $B3 write
- 8.1.26 AOG1 - $B4 write
- 8.1.27 AOG2 - $B5 write
- 8.1.28 AOG3 - $B6 write

NOTE: If lower operating current is desired, it is recommended that unused outputs be powered down using the ANAOUT Config - $B3 write register.

5.4.2 Audio Output Reconstruction Filter

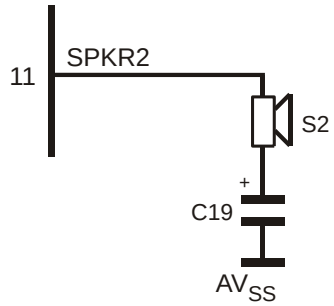
The CMX7262 ANAOUT1 and ANAOUT2 outputs provide internal reconstruction filtering. To complete the reconstruction filter, the external RC network shown in Figure 7 should be used for each of the differential outputs. The SPKR1 and SPKR2 outputs do not need any external reconstruction filter.



Bandwidth (kHz)	R3-R6 (kOhms)	C9-C10 (pF)
12.5	22	270

Figure 7 Recommended External Components – ANAOUT1/ANAOUT2 Reconstruction Filter

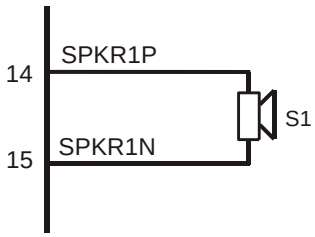
The CMX7262 SPKR2 output provides a single-ended audio output that can be used to drive an earpiece or headphone, as shown in Figure 8.



S2 32Ω nominal
C19 100µF

Figure 8 Recommended External Components – SPKR2 Output

The CMX7262 SPKR1 output can be used to drive a speaker as shown in Figure 9.



S1 8Ω nominal

Figure 9 Recommended External Components – SPKR1 Output

Care should be taken to avoid shorting any of the speaker outputs to one another or to V_{SS} or V_{DD}. An external RC filter may be added across SPKR1P and SPKR1N pins if clock noise needs further reduction.

5.5 Audio Input

5.5.1 Audio Input Routing

The CMX7262 has two possible analogue inputs: a differential input – ANAIN1 and a single-ended input – ANAIN2.

The CMX7262's ADC can sample either of the two analogue inputs. Figure 10 shows the analogue input signal routing and control.

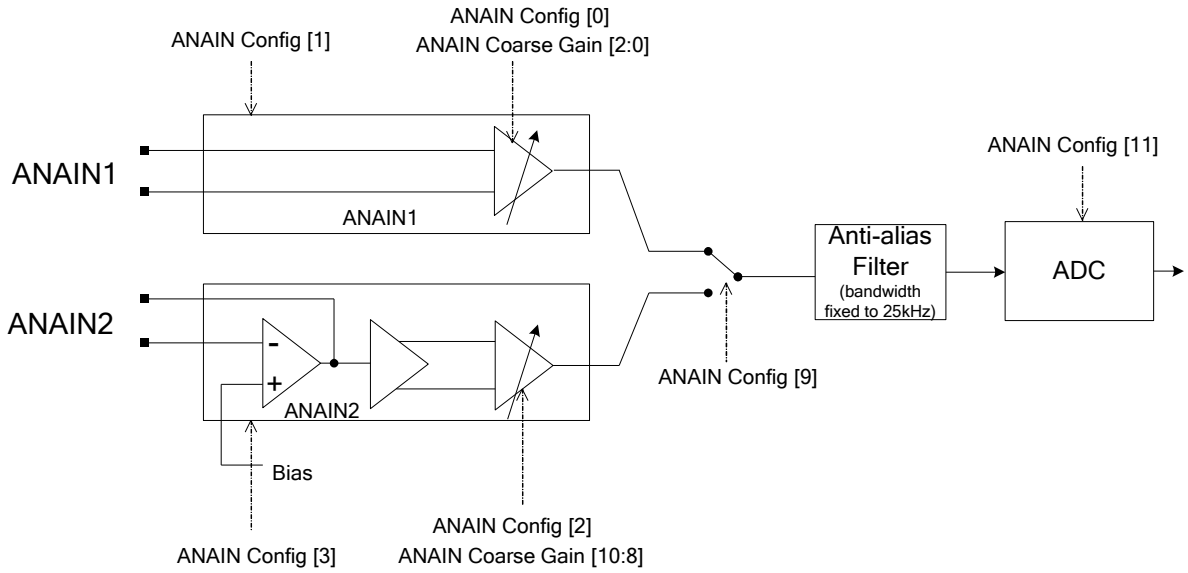


Figure 10 Analogue Audio Input Routing

The registers that control the analogue audio input routing are:

- 8.1.23 ANAIN Config - $B0 write
- 8.1.24 AIG - $B1 write

NOTE: If lower operating current is desired, it is recommended that unused inputs be powered down using the ANAIN Config - $B0 write register.

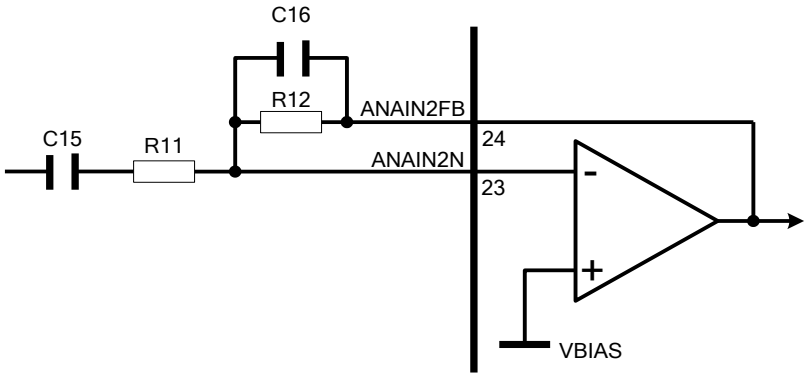
5.5.2 Differential Audio Input

The device has an anti-alias filter in the analogue audio input path which should be sufficient for most applications. However, if additional filtering is required, it can be done at the input to the device.

The input impedance of the ANAIN1 pins varies with the input gain setting, see section 7.1.3 Operating Characteristics.

5.5.3 Single-Ended Audio Input Interface

A single-ended input can be connected to the CMX7262 using the ANAIN2 pins. Gain and filtering circuitry can be constructed around these pins, as shown in Figure 11.



C15	See below
C16	100pF
R11	See below
R12	100kΩ

Figure 11 Recommended External Components – Single-Ended Audio Input Interface

R11 should be selected to provide the required DC gain (assuming C15 is not present) as follows:

$$\left|GAIN_{ANAIN2}\right| = 100k\Omega / R11$$

The gain should be such that the resultant output at the pins is within the input signal range.

C15 should be selected to maintain the lower frequency roll-off of the ANAIN2 input as follows:

$$C15 \geq 0.1\mu F \times \left|GAIN_{ANAIN2}\right|$$

The high frequency cut off $= \left(\frac{1}{2\pi.R12.C16}\right)$

The low frequency cut off $= \left(\frac{1}{2\pi.R11.C15}\right)$

5.6 GPIO Pins

All GPIO pins are configured as inputs with an internal bus-hold circuit, after the Function Image™ has been loaded. This avoids the need for users to connect external termination (pullup/pulldown) resistors to these inputs. The bus-hold is equivalent to a 75kΩ resistor either pulling up to logic 1 or pulling down to logic 0. As the input is pulled to the opposite logic state by the user, the bus-hold resistor will change, so that it also pulls to the new logic state. The internal bus-hold can be disabled or re-enabled using programming register P1.20 in Program Block 1 – Clock Control.

6 General Description

6.1 CMX7262 Features

The CMX7262 is a half-duplex TWELP Vocoder chip that performs encoding of linear PCM samples / analogue audio into TWELP-coded packets or, decoding of TWELP-coded data into linear PCM samples / analogue audio. CMX7262 contains on-chip ADC and DAC which can be used to sample and output analogue waveforms.

A flexible power control facility allows the device to be placed in its optimum power save mode when not actively processing signals.

The device includes a crystal clock generator, with phase-locked loop to enable operation from a range of reference xtal frequencies.

A block diagram of the device is shown in Figure 1.

Encoder Functions:

- Analogue voice / 16-bit linear PCM samples to TWELP-coded packets.
- Input filtering – when processing the CMX7262's analogue audio input.
- Noise Reduction processing on the input signal before encoding.
- FEC encoder with interleaver for protection against channel errors.

Decoder Functions:

- TWELP decoding to analogue voice or 16-bit linear PCM samples.
- Output filtering– when processing the CMX7262's analogue audio output.
- The decoder processes either hard or soft decision bits from the modem.
- FEC decoder and de-interleaver.

Repeater Functions:

- The FEC alone can be decoded and re-applied without having to voice decode and voice re-encode, allowing the CMX7262 to be used in repeater systems.

Interface:

- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer.
- Input data can emanate from the analogue audio input or C-BUS.
- Output data can be sent to the analogue audio output and/or C-BUS.
- Open drain IRQ to host.
- Three GPIO pins.
- Serial memory or C-BUS (host) boot mode.

6.2 Signal Interfaces

Figure 12 shows the CMX7262 input and output interfaces. The CMX7262's output can be sent to either one or both of its outputs simultaneously – C-BUS (for transfer to the host microcontroller) and/or, analogue audio output. Input to the CMX7262 must come from one of the two input ports – C-BUS (input data from the host controller) or the analogue audio input.

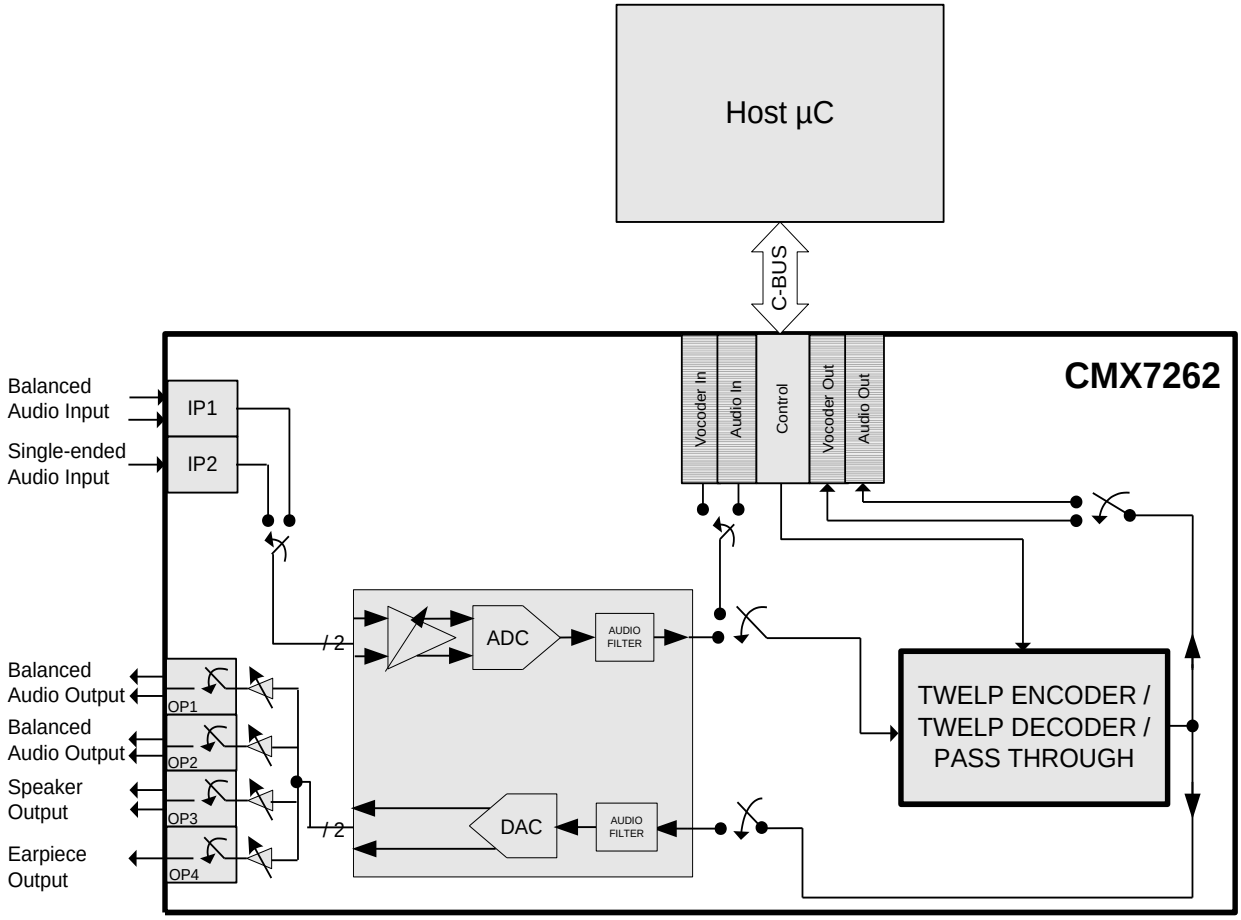


Figure 12 CMX7262 Inputs and Outputs

6.3 System Design

A number of system architectures can be supported by the CMX7262. The most highly-integrated solution uses a CMX7262 Vocoder under full control of the CMX7141. In this mode, audio codec functions can be provided by the on-chip ADC and DAC in the CMX7262. It is also possible to use the audio codec functions of the CMX7141 and use CMX7262 as a digital vocoder co-processor. In both these modes the CMX7262 will be under the full control of CMX7141.

Figure 13 shows the configuration using CMX7262's internal audio codec. In this configuration the CMX7141 uses its SPI port to interface with CMX7262's C-BUS port to control and to transfer data to/from CMX7262. Using the on-chip converters of CMX7262, allows the system designer to exploit the variety of analogue inputs and outputs that CMX7262 offers. For more details, see Section 5.4 and 5.5.

When CMX7141 is used in analogue mode, the CMX7262 can be configured to pass-through mode where it samples analogue waveforms and transfers the linear PCM samples to the CMX7141 or, it receives linear PCM samples from the CMX7141 and outputs the result as an analogue waveform.

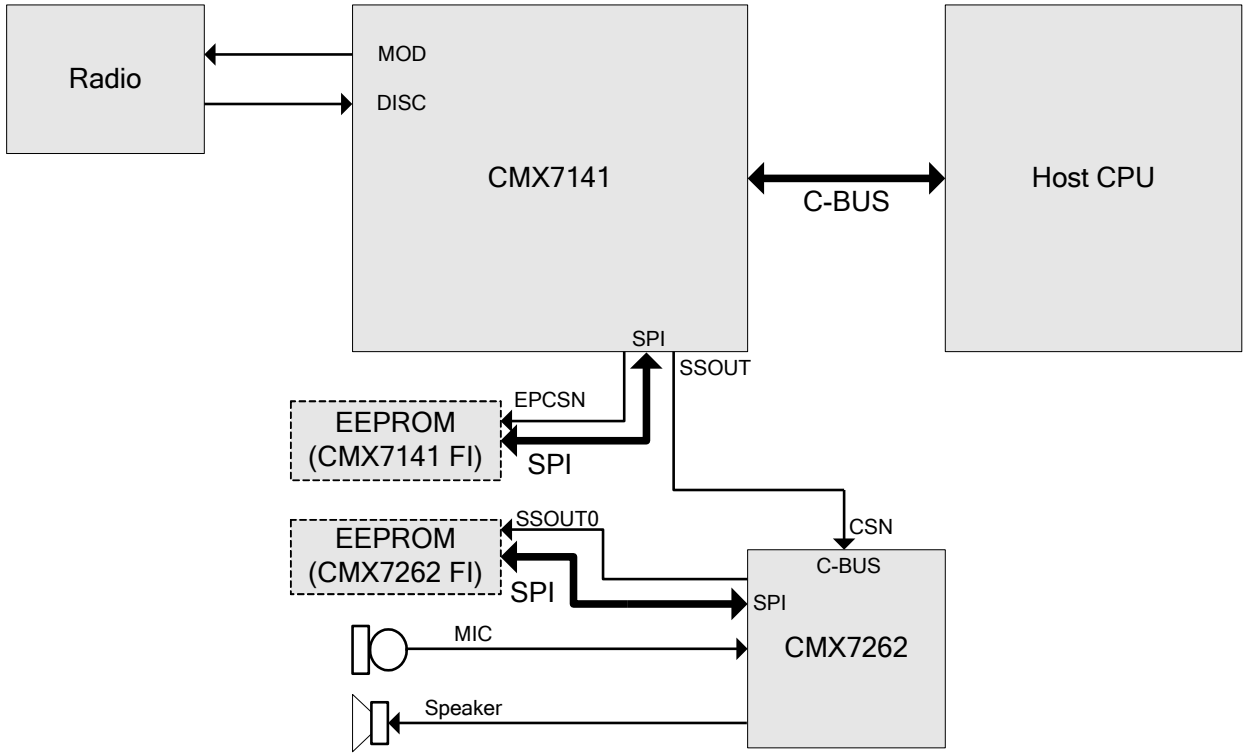


Figure 13 CMX7262 Using Internal Audio Codec Interfaced With CMX7141

Figure 14 shows the interface between the CMX7262 and CMX7141 when using the audio codecs on the CMX7141. In this configuration, the CMX7141 uses its SPI port to interface with CMX7262's C-BUS port to control and transfer data to/from the CMX7262.

In this mode, the CMX7262 is fed linear PCM samples by the CMX7141 and it returns TWELP-coded packets. Or, the CMX7262 is fed TWELP-coded packets by CMX7141 and it returns decoded linear PCM samples. The CMX7141 has full control of analogue inputs and outputs.

The CMX7262 can work with other modem ICs or a host microcontroller, in a similar manner.

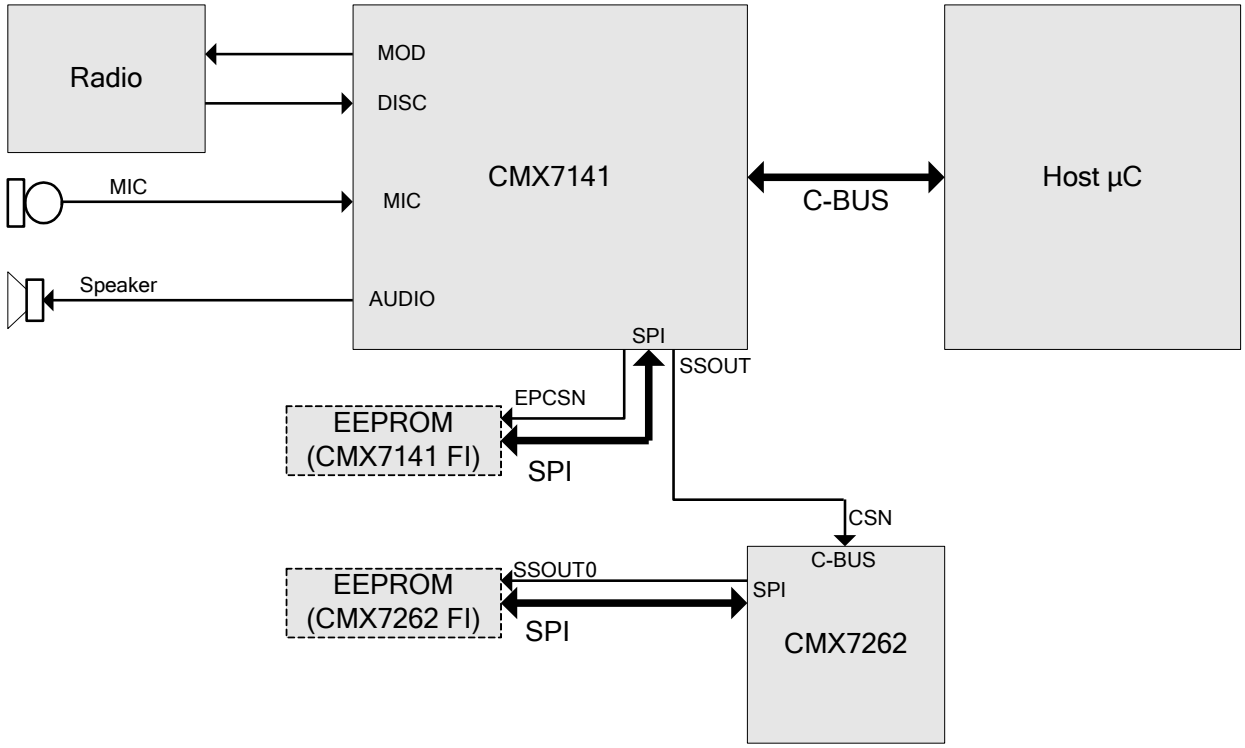


Figure 14 CMX7262 Interfaced With CMX7141 Using CMX7141's Audio Codec

6.4 Xtal Frequency

The CMX7262 is designed to work with a xtal or an external frequency oscillator within the ranges specified in section 7.1.2. Block 1 of the Programming Block (refer to the User Manual) must be loaded with the correct values to ensure that the device will work to specification with the user-selected clock frequency. A list of configuration values can be found in Table 7, supporting a sampling rate of 8kHz for a range of xtal or external oscillator frequencies.

6.5 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7262 and the host microcontroller; this interface is compatible with Microwire™, SPI™, and other similar interfaces. Interrupt signals notify the host microcontroller when a change in status has occurred; the microcontroller should read the Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see Section 6.12.5.

6.5.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7262 internal registers and the host microcontroller over the C-BUS serial bus. Single register transactions consist of a single Register Address byte sent from the microcontroller, which may be followed by a data word sent from the microcontroller to be written into one of the CMX7262's write only registers, or a data word read from one of the CMX7262's read only registers. Streaming C-BUS transactions consist of a single register address byte followed by many data bytes being written to, or read from, the CMX7262. All C-BUS data words are multiples of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the microcontroller, no data transfer being required. The operation of the C-BUS is illustrated in Figure 15.

Data sent from the microcontroller on the CDATA (command data) line is clocked into the CMX7262 on the rising edge of the SCLK input. Data sent from the CMX7262 to the microcontroller on the RDATA (reply data) line is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common microcontroller serial interfaces and may also be easily implemented with general purpose microcontroller I/O pins controlled by a simple software routine. Section 7.2 (C-BUS Timing) gives detailed C-BUS timing requirements.

Note that, due to internal timing constraints, there may be a de*l*ay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

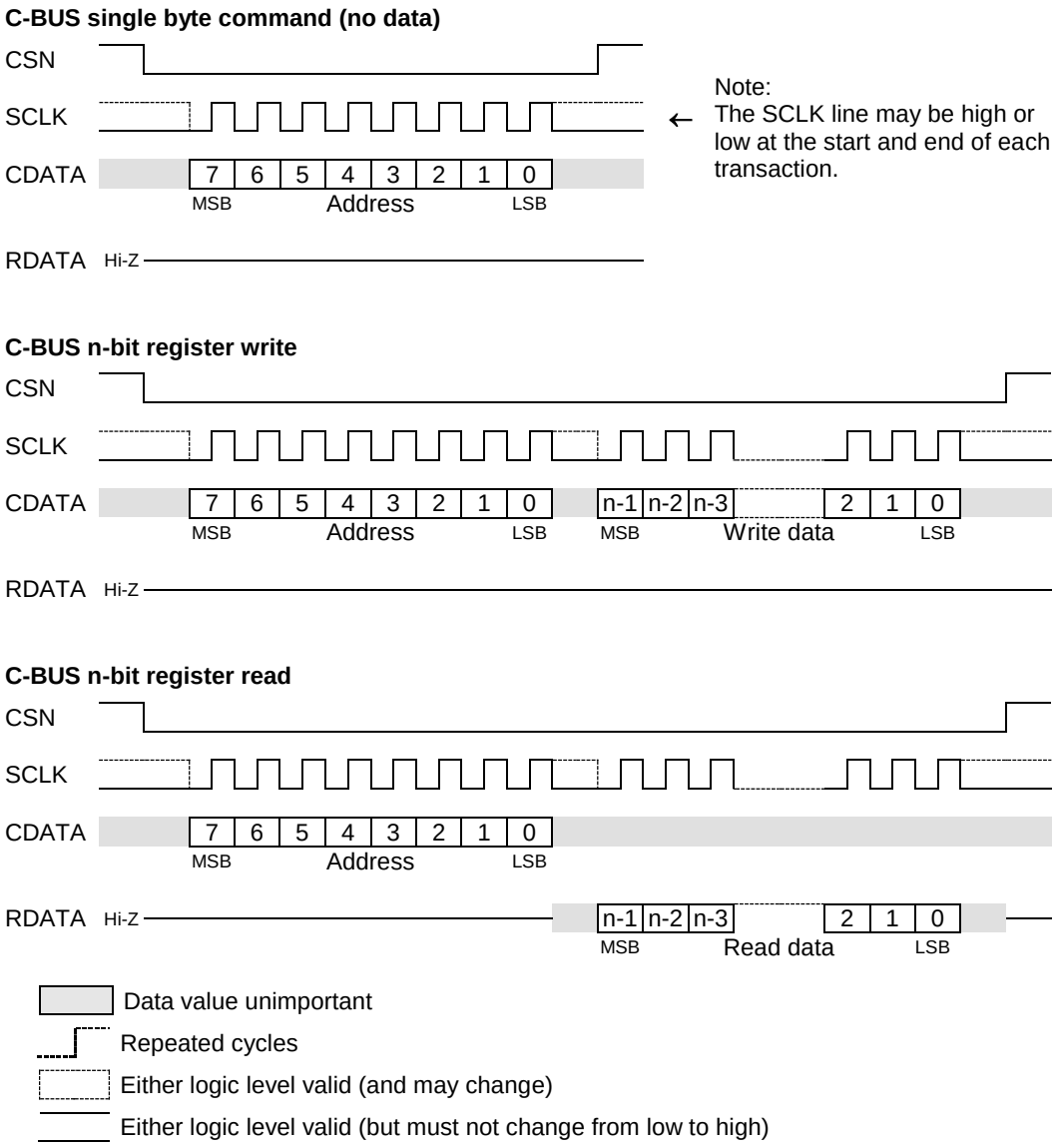
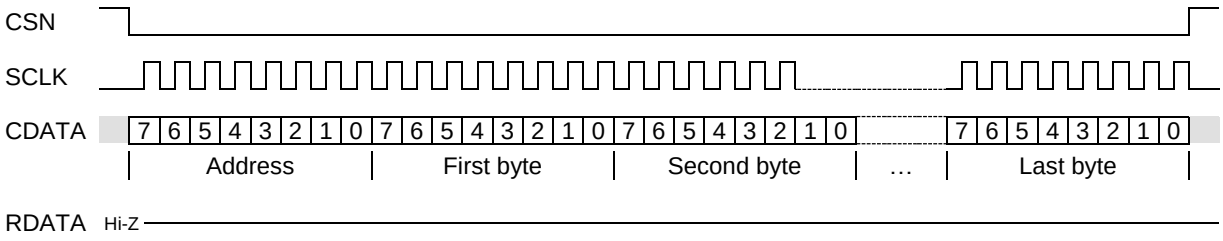


Figure 15 Basic C-BUS Transactions

To increase the data bandwidth between the microcontroller and CMX7262, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 16.

Example of C-BUS data-streaming (8-bit write register)



Example of C-BUS data-streaming (8-bit read register)

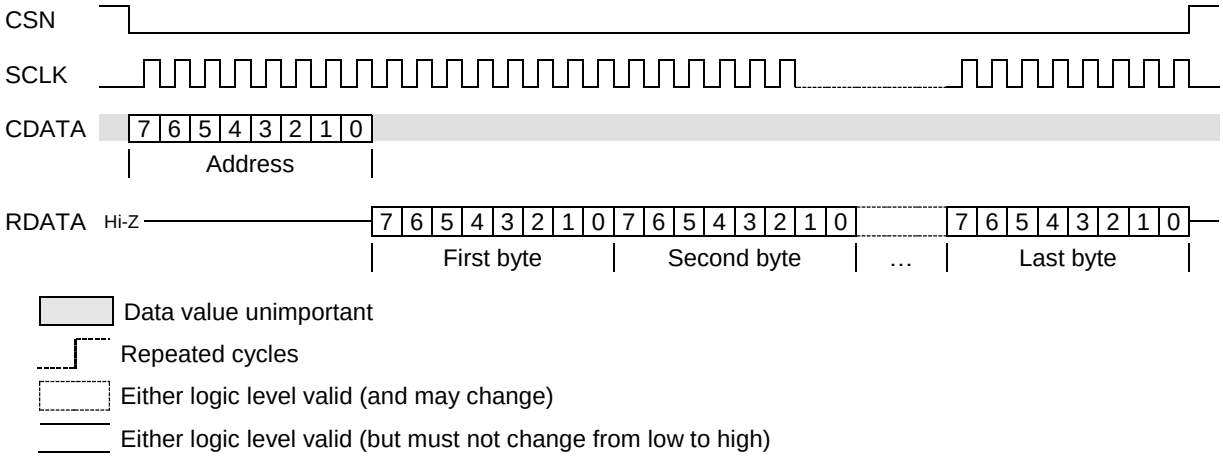


Figure 16 C-BUS Data-Streaming Operation

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional; the host may insert gaps or concatenate the data as required.

6.6 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file, which can be included into the host controller software or programmed into an external serial memory. The Function Image™ size can never exceed 128kbytes, although a typical FI will be considerably less than this. Note that the BOOTEN1, 2 pins are only read at power-on, when the RESETN pin goes high, or following a C-BUS General Reset, and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN1, 2 pins are ignored by the CMX7262 until the next power-up or Reset.

The BOOTEN 1, 2 pins are both fitted with internal low current pull-up devices.

For serial memory load operation, BOOTEN2 should be pulled low by connecting it to DV_{SS} either directly or via a 47kΩ resistor (see Table 2).

Whilst booting, the boot loader will return the checksum of each block loaded in the C-BUS Audio Out data word streaming register. The checksums can be verified against the published values to ensure that the FI has loaded correctly.

Once the FI has been loaded, the CMX7262 performs these actions:

(1) The product identification code is reported in the C-BUS Audio Out data word streaming register.
(2) The FI version code is reported in the C-BUS Audio Out data word streaming register.

Table 2 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS host load	1	1
Reserved	1	0
Serial Memory load	0	1
Reserved	0	0

6.6.1 FI Loading from Host Controller

The FI can be included in the host controller software build and downloaded into the CMX7262 at power-up over the C-BUS interface, using the Audio In streaming register. For Function Image™ load, the CMX7262 accepts raw 16-bit Function Image™ data using the Audio In Data Word - $49 write register. The BOOTEN 1, 2 pins must be set to the C-BUS load configuration, the CMX7262 powered or Reset, and then data can then be sent directly over the C-BUS to the CMX7262.

If the host detects a brownout, the BOOTEN 1, 2 pins should be set to re-load the FI. A General Reset should then be issued or the RESETN pin used to reset the CMX7262 and the appropriate FI load procedure followed.

Streaming C-BUS may be used to load the Audio In Data Word - $49 write register with the Function Image™, and the Input Level - $4B read register used to ensure that the Audio In streaming register is not allowed to overflow during the load process.

NOTE: The Input Level - $4B read register and the Output Level - $4F read register are valid only when booting and must not be accessed at any other time.

The download time is limited by the clock frequency of the C-BUS; with a 5MHz SCLK it should take less than 250ms to complete even when loading the largest possible Function Image™.

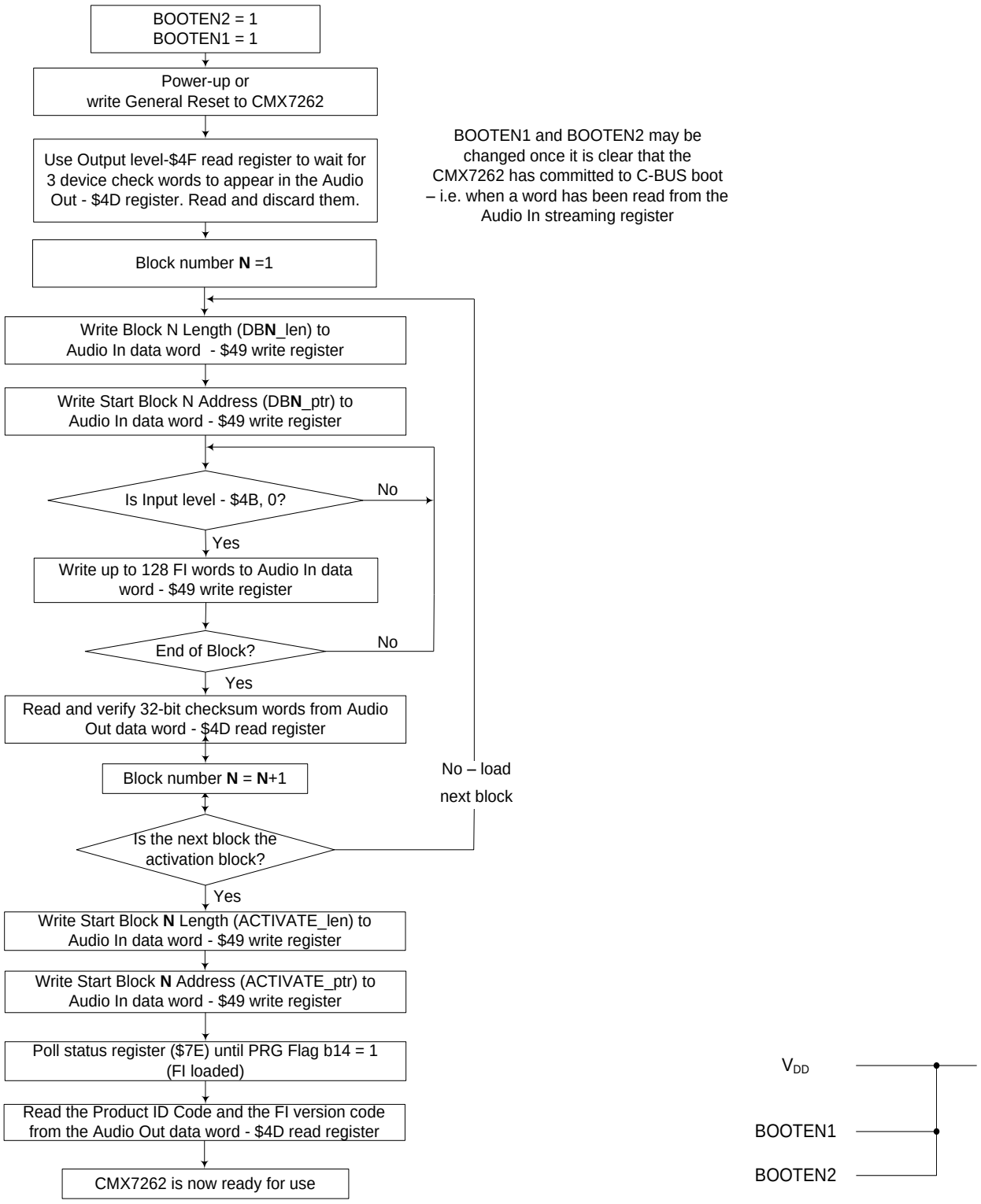


Figure 17 FI Loading from Host

6.6.2 FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory by either the host or an external programmer. The serial memory should contain the same data stream as written to the Audio In streaming register as shown in Figure 17. The most significant byte of each 16-bit word should be stored first in serial memory.

The serial memory should be interfaced to the CMX7262 using SSOUT0 as the chip select and PCM port pins, which act as an SPI port whilst booting (refer Section 3). Section 5.3 Serial Port Interface, shows the connections required for interfacing a typical device such as the AT25F512 Serial Flash memory with the CMX7262.

The CMX7262 needs to have the BOOTEN pins set to serial memory load, and then on power-on, following the RESETN pin becoming high, or following a C-BUS General Reset, the CMX7262 will automatically load the data from the serial memory without intervention from the host controller.

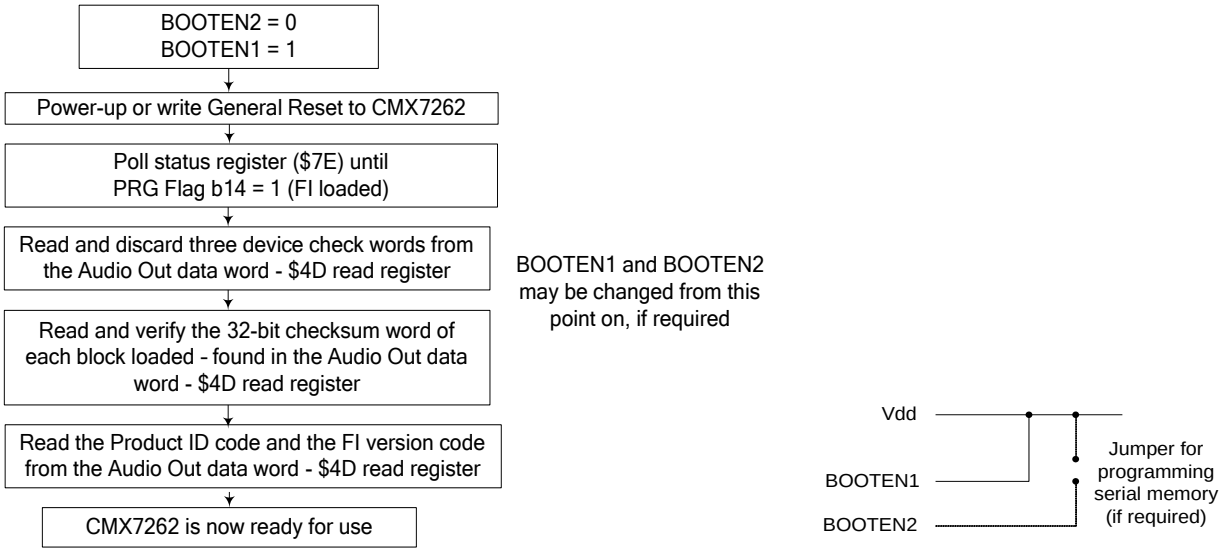


Figure 18 FI Loading from Serial Memory

The CMX7262 has been designed to function with the AT25F512 Serial Flash memory, however other manufacturers' parts may also be suitable. The time taken to load the FI should be less than 500ms even when loading the largest possible Function Image™.

6.7 TWELP Coding Format [1]

This section provides a brief description about the TWELP voice coding standard. The motivation behind the TWELP voice coding standard is to compress analogue voice in order to reduce the bandwidth required to transmit it.

TWELP converts linear PCM data at 8 ksamples/s, into a 2.4 kbps coded bitstream (without FEC) or into a 3.6 kbps coded bitstream (with FEC). The coded bitstream is packed into bytes for efficient transfer to the host, over the C-BUS interface.

TWELP technology uses unique proprietary signal decomposition and parameter encoding methods, ensuring high quality voice at high compression ratios.

The TWELP Vocoder operates on a frame-by-frame basis. A frame is 20ms of voice data. Each 20ms frame of voice data consists of 160 linear 16-bit PCM samples, sampled at 8kHz. Each frame of voice data is converted into 48 bits of TWELP-coded frame (without FEC) or into 72 bits of TWELP-coded frame (with FEC). 1, 2, 3 or 4 frames can be encoded at once. Interleaving is supported, with interleaver size selectable from 1, 2, 3 or 4 frames.

When FEC is used, the integral FEC decoder can optionally use “soft-decision” metrics to improve its decoding ability if the input can be applied as a 4-bit representation of the received demodulated signal. The FEC can also be used on its own, so that data can be decoded/error-corrected then re-encoded and forwarded on. This allows the CMX7262 to be used in in digital voice repeater systems.

6.8 Vocoder Frame / Packet Sizes

Packets of both raw and FEC-protected vocoder data are transferred between the device and the host over the byte wide streaming C-BUS registers (Vocoder In and Vocoder Out registers).

TWELP *Frame*:
A frame is 20ms of voice data. It could be 160 linear PCM samples or, 6 bytes of raw TWELP-coded data or, 9 bytes of TWELP-coded data with FEC.

TWELP *Packet*:
A packet is a combination of one or more frames. The CMX7262 can handle packets of up to 4 frames.

Packets of raw vocoder frames:
During raw encoding, each 20ms of audio is encoded into 48-bits of TWELP-coded frame. These bits are packed into bytes for transfer over C-BUS. For details see Section 6.9 Data Transfer Using C-BUS Interface. Table 3 shows all allowed packet sizes handled by the CMX7262. This is the amount of data that the host should expect to read from the Vocoder Out register for each packet size, when encoding. This is also the amount of data that CMX7262 expects to read from the Vocoder In register when decoding.

Packets of FEC-protected vocoder frames:
The CMX7262 has a built-in FEC system to protect the vocoder frames when transported over an error prone channel. When FEC is enabled, data interleaving is automatically set to match the packet size. Interleaving provides good performance over a channel with burst errors, typical in wireless applications. FEC and interleaving is applied on a packet basis. Therefore, a complete packet must be presented in the Vocoder In register for the decoder to start decoding.

When FEC is enabled, each 20ms of audio is encoded into 72-bits of TWELP-coded frame. These bits are packed into bytes for transfer over C-BUS. For details see section 6.9 Data Transfer Using C-BUS Interface. Table 3 shows all allowed packet sizes handled by the CMX7262. This is the amount of data that

[1] The TWELP™ voice coding technology is provided by DSP Innovations, Inc. www.dspini.com, www.twelp.pro

the host should expect to read from the Vocoder Out register for each packet size, when encoding. This is also the amount of data that the CMX7262 expects to read from the Vocoder In register when decoding.

The FEC decoder provides the possibility to operate with both “hard decision and “soft decision” inputs.

Hard Decision Input (Hard bits):
Hard bits are represented by one bit per bit. These are packed into 9 bytes for a single TWELP-coded frame. For details see section 6.9 Data Transfer Using C-BUS Interface. A TWELP-coded packet consists of 1/2/3/4 frames. Table 3 lists the number of bytes of hard bits for each packet size.

Soft Decision Input (Soft bits):
Each information bit in soft decision mode is represented by 4 bits:

Decision value (Binary)	Interpretation
0000	Most confident 0
…	…
0111	Least confident 0
1000	Least confident 1
...	…
1111	Most confident 1

In this case a TWELP-coded frame will be represented using 72x4 = 288 bits. These are packed into 36 bytes for a single TWELP-coded frame. For details see section 6.9 Data Transfer Using C-BUS Interface. A TWELP-coded packet consists of 1, 2, 3 or 4 frames. Table 3 lists the number of bytes of soft bits for each packet size.

Packet size (as number of frames)	FEC Enabled	Encoder output written to the Vocoder Out register		Decoder input that CMX7262 expects to read from Vocoder In register			Number of linear PCM samples (corresponding to the packet size)
		Bytes	Produced every	Hard bits (bytes)	Soft bits (bytes)	Produced every	
1	No	6	20ms	6	-NA-	20ms	160
1	Yes	9	20ms	9	36	20ms	160
2	Yes	18	40ms	18	72	40ms	320
3	Yes	27	60ms	27	108	60ms	480
4	Yes	36	80ms	36	144	80ms	640

Table 3 Packet Sizes

6.8.1 TWELP Packed Data Format

The CMX7262 handles 16-bit linear PCM samples as well as TWELP-coded data frames. Each TWELP-coded data frame is 48-bits (without FEC) or 72-bits (with FEC). The TWELP-coded bitstream is packed into bytes for efficient transfer into/out of CMX7262.

Raw Vocoder Packets

Without FEC, the TWELP encoder compresses 160 samples (20ms of audio at 8kHz sampling rate) into 48-bits. Groups of 8-bits are packed into data bytes. 6 packed bytes make a frame of TWELP-coded bits. For data input to the CMX7262, packed bytes are written to the Vocoder In Data Byte - $48 write register in the following order:

The byte at the top is the first out of the Vocoder Out register for the encoder and the first into the Vocoder In register for the decoder. The bits in a packet are named D0 through D47. The bits should be transmitted in order starting with D0 and ending with D47.

Beginning of a TWELP frame:	B7	B6	B5	B4	B3	B2	B1	B0
1st byte written to Vocoder In register	D0	D1	D2	D3	D4	D5	D6	D7
	Intervening bits follow the same pattern							
6th byte written to Vocoder In register **End of TWELP Frame**	D40	D41	D42	D43	D44	D45	D46	D47

FEC Protected Vocoder Packets

Hard Decision Packets

With FEC enabled, the TWELP encoder compresses 160 samples (20ms of audio at 8kHz sampling rate) into 72-bits. Groups of 8-bits are packed into data bytes. With hard decision decoding, where each information bit is represented using a single bit, 9 packed bytes make a frame of TWELP-coded bits.

For data input to the CMX7262, packed bytes are written to the Vocoder In Data Byte - $48 write register in the following order:

The byte at the top is the first out of the Vocoder Out register for the encoder and the first into the Vocoder In register for the decoder. Groups of 1, 2, 3 or 4 frames make a TWELP-coded packet. The bits in a packet are named D0 through D287 (for maximum packet size of 4 frames). The bits should be transmitted in order starting with D0 and ending with D287.

Beginning of a TWELP frame:	B7	B6	B5	B4	B3	B2	B1	B0
1st byte written to Vocoder In register	D0	D1	D2	D3	D4	D5	D6	D7
	Intervening bits follow the same pattern							
9th byte written to Vocoder In register **End of Frame-1**	D64	D65	D66	D67	D68	D69	D70	D71
For 2 frame packets, the sequence continues…	Intervening bits follow the same pattern							
18th byte written to Vocoder In register **End of Frame-2**	D136	D137	D138	D139	D140	D141	D142	D143
For 3 frame packets, the sequence continues…	Intervening bits follow the same pattern							
27th byte written to Vocoder In register **End of Frame-3**	D208	D209	D210	D211	D212	D213	D214	D215
For 4 frame packets, the sequence continues…	Intervening bits follow the same pattern							
36th byte written to Vocoder In register **End of Frame-4**	D280	D281	D282	D283	D284	D285	D286	D287

Soft Decision Packets
With FEC enabled, the TWELP encoder compresses 160 samples (20ms of audio at 8kHz sampling rate) into 72-bits. Groups of 8-bits are packed into data bytes. With soft decision decoding, where each information bit is represented using 4 bits, 36 packed bytes (9x4) make a frame of TWELP-coded bits.

For data input to the CMX7262, packed bytes are written to the Vocoder In Data Byte - $48 write register in the following order:

The byte at the top is the first out of the Vocoder Out register for the encoder and the first into the Vocoder In register for the decoder. Groups of 1, 2, 3 or 4 frames make a TWELP-coded packet. The bits in a packet are named D0 through D287 (for maximum packet size of 4 frames). The bits should be transmitted in order starting with D0 and ending with D287. The bits of a nibble are shown as n3 to n0, with n3 being the most significant and n0 being the least significant.

Beginning of a TWELP frame:	B7	B6	B5	B4	B3	B2	B1	B0
	n3	n2	n1	n0	n3	n2	n1	n0
1st byte written to Vocoder In register	D0				D1			
	Intervening bits follow the same pattern							
36th byte written to Vocoder In register **End of Frame-1**	D70				D71			
For 2 frame packets, the sequence continues…	Intervening bits follow the same pattern							
72th byte written to Vocoder In register **End of Frame-2**	D142				D143			
For 3 frame packets, the sequence continues…	Intervening bits follow the same pattern							
108th byte written to Vocoder In register **End of Frame-3**	D214				D215			
For 4 frame packets, the sequence continues…	Intervening bits follow the same pattern							
144th byte written to Vocoder In register **End of Frame-4**	D286				D287			

The above ordering/packing also applies when the host is reading TWELP-coded frames from the Vocoder Out Data Byte - $4C read register.

Linear PCM Samples
Linear PCM samples are always transferred using one 16-bit word per sample. Input is through the Audio In Data Word - $49 write register. Output is through the Audio Out Data Word - $4D read register.

6.9 Data Transfer Using C-BUS Interface

Data transferred over the C-BUS interface between CMX7262 and host is either TWELP-coded packets or linear PCM samples. There are two sets of streaming registers to handle the two different data types:

- Audio In and Audio Out streaming registers (word wide) – to handle 16-bit linear PCM samples.
- Vocoder In and Vocoder Out streaming registers (byte wide) – to handle 8-bit TWELP-coded data.

Transfer of linear PCM samples:
Linear PCM samples are transferred to and from the host via the Audio In and Audio Out registers. The Audio In and Audio Out registers are word wide streaming registers.

The Audio In and Audio Out streaming registers can hold one packet of linear PCM samples. A packet may consist of one or more 20ms audio frames. The packet size is selectable using the VCFG - $55 write register. Table 3 shows the number of linear PCM samples associated with each packet size.

The only exception is “Pass-through” mode, where a packet is defined as a single frame of 16 samples, for both input and output.

Each Audio In / Audio Out word is 16-bits. The Audio In Data Word - $49 write and Audio Out Data Word - $4D read registers can be accessed as a single read/write or using streaming C-BUS.

Transfer of vocoder data:
TWELP-coded packets are transferred to and from the host via the Vocoder In and Vocoder Out registers. The Vocoder In and Vocoder Out registers are byte wide streaming registers.

The Vocoder In and Vocoder Out streaming registers can hold one packet of TWELP-coded data. A packet may consist of one or more 20ms audio frames. The packet size is selected using the VCFG - $55 write register. Table 3 shows the number of coded bytes produced for various packet sizes.

Each Vocoder In / Vocoder Out word is 8-bits. The Vocoder In Data Byte - $48 write and Vocoder Out Data Byte - $4C read registers can be accessed as either a single read/write or using streaming C-BUS.

The Audio In data word register and Vocoder In data byte register are collectively referred to as the Input Registers or C-BUS Input. Similarly, the Audio Out data word register and Vocoder Out data byte register are collectively referred to as the Output Registers or C-BUS Output.

At any time only one input streaming register (Audio In OR Vocoder In register) can be used, along with one output streaming register (Audio Out OR Vocoder Out register).

When operating in encode or decode mode the CMX7262 will actively copy the contents of the Audio In / Vocoder In input registers into an internal buffer, called the “Input Buffer”. The Input Buffer has space for one packet of data. Similarly, there is an internal “Output Buffer” which has space for one packet of data, and is connected to the Audio Out / Vocoder Out registers.

On reset or on entry to any active mode (Encode / Decode / Pass-through / Enc-Dec / FEC Loop) the CMX7262 Input and Output buffers will be empty – this means that initially two packets of data can be written to the Audio In / Vocoder In input register and may be stored by the CMX7262. Similarly, there is space in the CMX7262 for two output packets – one in the Audio Out / Vocoder Out output register and one in the Output Buffer. Once this storage is full, the CMX7262 will stop processing data and will flag a “Data Overflow” error using the Status - $7E read register.

The registers that affect data transfer to/from C-BUS interface are:

- Vocoder In Data Byte - $48 write
- Audio In Data Word - $49 write
- Vocoder Out Data Byte - $4C read
- Audio Out Data Word - $4D read
- Status - $7E read

The remainder of this section explains data transfer to and from the host using the C-BUS interface.

Operational Details when Decoding:

1. At the start of an active operating mode, the host may initially write up to two packets of data without handshaking.
2. When decoding, a whole packet must be received before processing can begin.
3. When decoding the decoded result will become available once the entire packet has been processed.
4. When decoding, the availability of the entire decoded packet in the Audio Out register may be determined using the Output Data Available (ODA) bit in the Status - $7E read register.

Operational Details when Encoding:

1. At the start of an active operating mode, the host may initially write up to two packets of data in without handshaking.
2. When encoding (regardless of the number of frames per packet) encoding will begin as soon as one frame is received.
3. When encoding the encoded result will become available once a whole packet is processed.
4. When encoding, the availability of a whole packet in the Vocoder Out register may be determined using the Output Data Available (ODA) bit in the Status - $7E read register.
5. During encoding, when the CMX7262 begins processing the last frame in a packet, the Input Data Wanted (IDW) bit is set in the Status - $7E read register to indicate that the Audio In / Vocoder In input register is free to accept more input packets.

When the input data source is C-BUS:

1. The operating mode (Encode / Decode / Pass-through / Enc-Dec / FEC Loop) must be selected using the VCTRL - $6B write register. Any write to the VCTRL - $6B write register will cause the Audio In and Vocoder In input registers and Input Buffer, along with the Audio Out and Vocoder Out output registers and the Output Buffer, to be flushed.
2. The Audio Source field in the Audio Routing - $5D write register must be set to indicate that audio input is through the C-BUS interface.
3. The host writes a packet of data to the Audio In / Vocoder In register (see Audio In Data Word - $49 write, Vocoder In Data Byte - $48 write registers).
4. Once a packet of data has been read by the CMX7262, the host will be signalled using the IDW (Input Data Wanted) bit in the Status - $7E read register. Initially it is possible to write two packets of data to the CMX7262 but after this time the host must wait until IDW is set before writing another packet of input data.

When the input data source is analogue audio input and the output data destination is C-BUS:

When the Audio Source is set to analogue audio, input data from the analogue audio input will be loaded into the internal Input Buffer, without the host having to intervene in the data transfer process. The Audio Source may be set to analogue audio input only when the CMX7262 is in Encode / Enc-Dec / Pass-through mode.

If the audio source is the analogue audio input, and the audio destination is C-BUS, the host must read the output data quickly enough to maintain real-time constraints. Once started, the analogue audio input will operate at an 8kHz sample rate regardless of the host C-BUS access rate. If the Vocoder Out register is not read quickly enough by the host a data overflow will occur, which the CMX7262 will indicate to the host using the Status - $7E read register.

When the output data destination is C-BUS:

1. The operating mode (Encode / Decode / Pass-through / Enc-Dec / FEC Loop) must be selected using VCTRL - $6B write register. Any write to this register will cause the Audio In and Vocoder In input registers and Input Buffer, along with the Audio Out and Vocoder Out output registers and the Output Buffer, to be flushed.
2. Once a packet of input has been processed, the CMX7262 places the output data in the Audio Out / Vocoder Out register and signals the host using the ODA (Output Data Available) bit in the Status - $7E read register, On ODA being set, the host can read an entire packet from the Audio Out / Vocoder Out register.

When the output data destination is - analogue audio output and audio source is C-BUS:

When the Audio Destination is set to analogue audio output, the data in the output buffer will be sent to the analogue audio output, without the host having to intervene in the data transfer process. The audio destination may be set to analogue audio output only when the CMX7262 is in Decode / Enc-Dec / Pass-through mode.

If the audio destination is analogue audio output, and the audio source is C-BUS, the host must provide input data to the C-BUS quickly enough to maintain real-time constraints. Once started, the analogue audio output will operate at an 8kHz sample rate regardless of the host C-BUS access rate. If the C-BUS Vocoder In register is not written quickly enough by the host a data underflow will occur, which the CMX7262 will indicate to the host using the Status - $7E read register.

Figure 19 illustrates operation when data is transferred into the CMX7262 using C-BUS input. Figure 20 illustrates operation when data is transferred from the CMX7262.

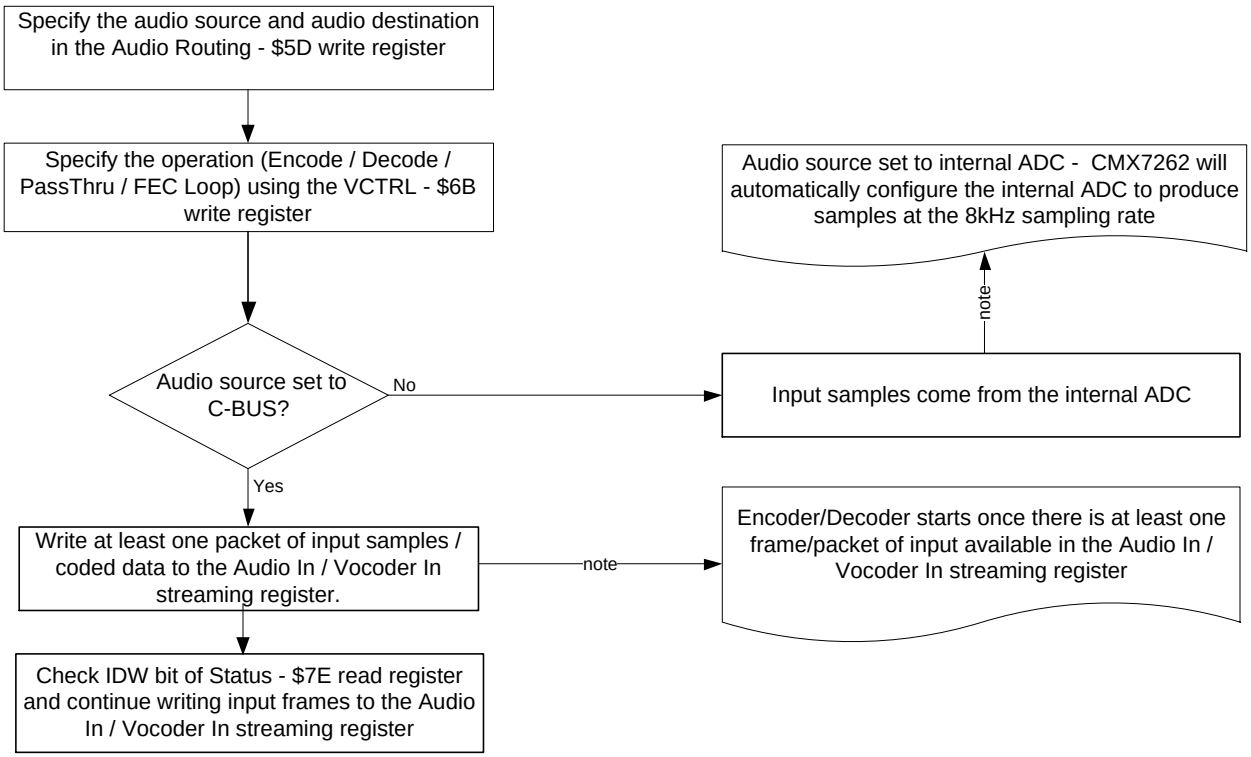


Figure 19 Input Data Transfer into the CMX7262

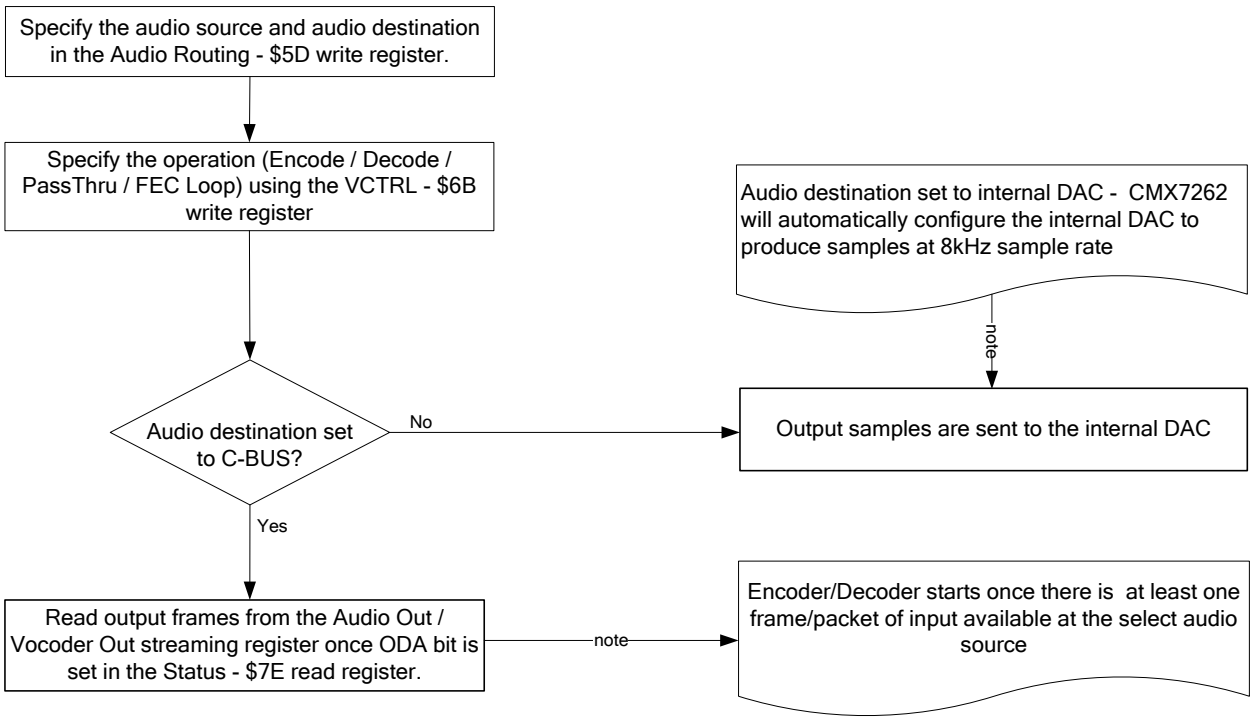


Figure 20 Output Data Transfer from the CMX7262

6.10 Noise Reduction

The TWELP Encoder in CMX7262 contains a built-in propriety noise suppression algorithm that can be activated optionally. The level of noise suppression can be controlled using the Noise Suppression - $53 write register.

6.11 Noise Gate

The output from the TWELP decoder may optionally be passed through a noise gate that fully mutes the audio output signal while it is below a configurable amplitude threshold. Noise suppression is different and complementary; it is an encoder process that significantly reduces, but may not completely eliminate, background noise. Accordingly the decoder noise gate and encoder noise suppression functions work well in conjunction.

Noise Gate is active in Decode and Enc-Dec modes only.

The noise gate is controlled by the Threshold and Delay fields in the Noise Gate Configuration - $5E write register.

6.12 Device Control

Once the Function Image™ is loaded, the CMX7262 can be set to one of its operating modes using the VCTRL - $6B write register:

- Idle mode – for configuration or low-power operation.
- Encode mode – for encoding from linear PCM into TWELP-coded frames.
- Decode mode – for decoding from TWELP-coded frames into linear PCM samples.
- Enc-Dec mode – a test mode which encodes linear PCM to TWELP audio format and then decodes it again – providing the ability to evaluate audio quality.
- Pass Thru – simply passes the audio from source port to destination port. Source and destination ports are set using VCTRL - $6B write register.
- FEC Loop – for decoding just the FEC in a TWELP-coded packet, in order to correct any bit errors, and re-apply the FEC on the error corrected bit stream.

These modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers or, for parameters that are not likely to change during operation, using the Programming Register - $6A write in idle mode.

To conserve power when the device is not actively processing a signal, place the device into idle mode. Additional power saving can be achieved by disabling unused hardware blocks. However, most of the hardware power saving is automatic. Note that the BIAS block must be enabled to allow any of the Analogue Input or Output blocks to function. It is only possible to write to the Programming register whilst in Idle mode. See:

- Programming Register - $6A write
- VCTRL - $6B write
- Programming Register Operation
- Bias Control - $B7 write.

6.12.1 Normal Operation Overview

In normal operation (after the CMX7262 is configured), the required mode must be selected and correctly formatted data input and read out. This process is carried out by specifying the input audio source and output audio destination and selecting the type of operation (Encode/Decode/Enc-Dec/Pass-through/FEC Loop). Such options are required to be configured correctly before encoding/decoding can begin.

For continuous operation, data must be transferred into and out of the CMX7262. Audio transfer into the CMX7262 can be through the analogue audio input or, the host can feed in the data using C-BUS streaming registers. Similarly, the output can be transferred out of the CMX7262 using the analogue audio output or, to the host using the C-BUS streaming registers.

C-BUS transfers use the Audio In/Vocoder In streaming registers to transfer data into the CMX7262, and the Audio Out/Vocoder Out streaming registers to transfer data out of the CMX7262. The Status register is used to indicate that the data has been dealt with, or if more data is wanted. The CMX7262 can be configured to interrupt the host when it is ready to accept more data or when there is a packet of data ready to be read.

During active operation, the most significant registers are:

- VCTRL - $6B write
- Status - $7E read
- IRQ Enable - $6C write
- Audio In Data Word - $49 write
- Vocoder In Data Byte - $48 write
- Audio Out Data Word - $4D read
- Vocoder Out Data Byte - $4C read

6.12.2 Vocoder Operation

The CMX7262 has many features which allows the device to offer significant flexibility. However, basic encoding or decoding can be carried out by understanding the operation of just a few registers.

Basic Operation

Example: The following table explains the process involved in encoding linear PCM samples to TWELP-coded frames when the input comes from Audio In FIFO and the output is sent to the Vocoder Out FIFO:

Step No.	C-BUS Operation	Action	Description
1	Write $0011 to the Audio Routing - $5D write register.	Specify Audio Source and Audio Destination.	Input port is set to Audio In streaming register and output port is set to Vocoder Out streaming register.
2	Write $0031 to VCFG - $55 write register.	Configure the vocoder parameters.	Set vocoder frame length to 1 frame, set hard decision decoding and enable FEC.
3	Write $0002 to the VCTRL - $6B write register.	Put the device in encoder mode.	Commands the CMX7262 to start the encoding operation. Any write to VCTRL - $6B write register will flush the Audio In, Vocoder In, Audio Out, Vocoder Out registers along with the Input and Output Buffers. Handshaking to acknowledge that the effect of writing to VCTRL - $6B write register has completed, is provided by the Reg Done bit in Status - $7E read register. On this signal the host may start writing input data. The CMX7262 will wait until it has enough data to start encoding.
4	Write a frame of input data (160 LPCM samples) to the Audio In register – see Audio In Data Word - $49 write register.	Provide input data.	This provides a frame's worth of data for the CMX7262 to start the encoding operation.
5	Check the Status - $7E read register for bits 3 and 4 – the Output Data Available and Input Data Wanted flags respectively.	ODA	The input data has been encoded into the desired format, and the host can now read a packet of data from the Vocoder Out register
		IDW	There is now space for a new packet of data to be written to the Audio In register. This should be done promptly to ensure uninterrupted encoding.
6	Continue encoding		Repeat step 5 as required.

The procedure described above can be adapted, to achieve different Decoding / Pass-through / FEC Loop modes, with different input and output ports. Encoding from the linear PCM samples to TWELP-coded frames will continue as long as there is enough input data and the mode bits (b2-0) of VCTRL - $6B write register have not changed. The registers used for basic operation are:

- VCTRL - $6B write
- VCFG - $55 write
- Status - $7E read
- Audio In Data Word - $49 write
- Vocoder Out Data Byte - $4C read

The basic encoding operation described above is illustrated by Figure 21.

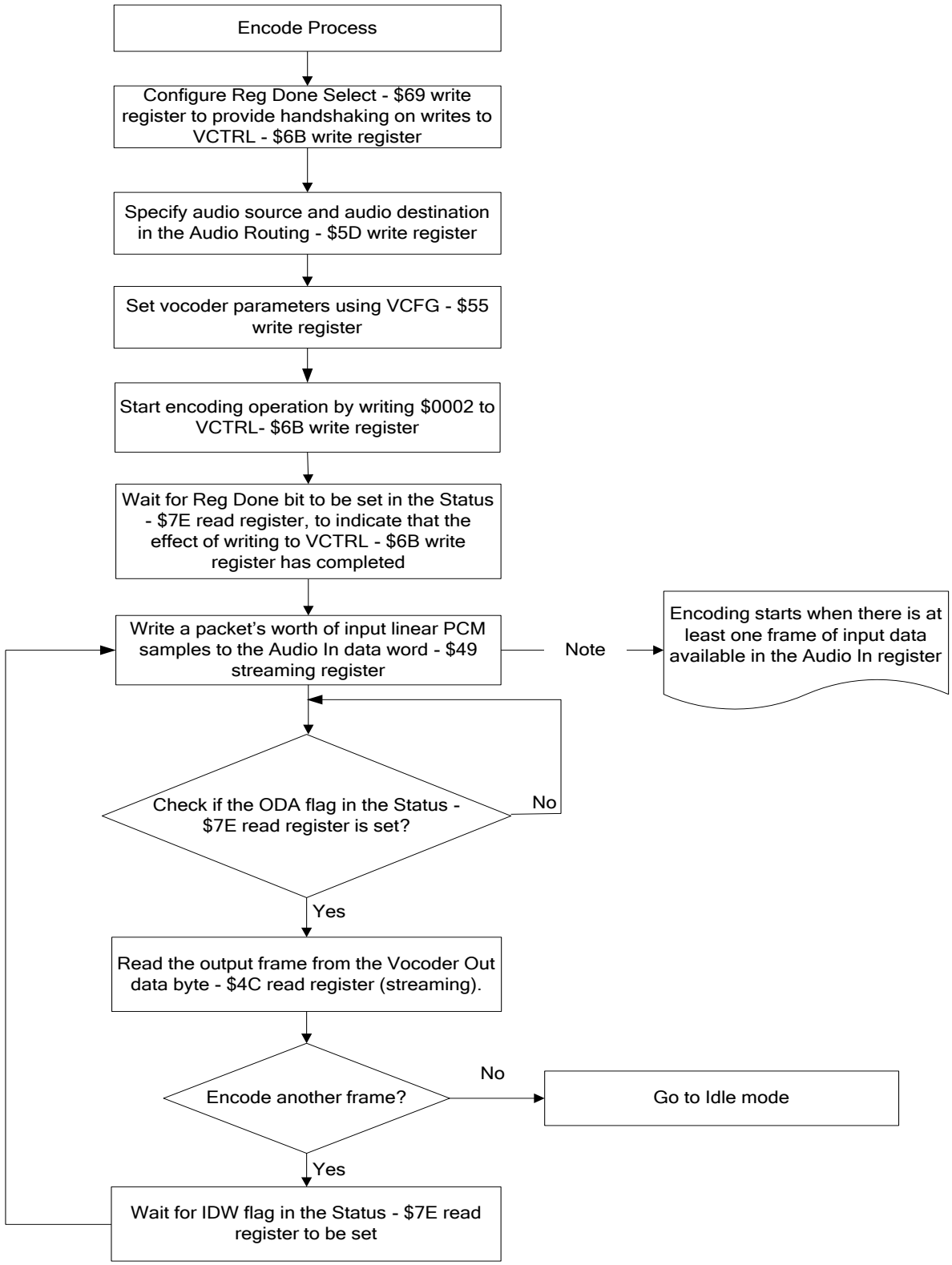


Figure 21 TWELP Encoder Operation Flowchart

6.12.3 Device Configuration (Using the Programming Register)

While in idle mode the Programming register becomes active, providing access to the Program Blocks. Program Blocks allow additional configuration of the CMX7262. Features that can be configured include:

- Configuration of the CMX7262 to operate with a non-default XTAL input frequency.

Full details of how to configure the programming register are given in Section 9 in the User Manual.

6.12.4 Device Configuration (Using dedicated registers)

Some device features may be configured using dedicated registers. This allows for configuration when the device is not in idle mode. Configuration of the following features is possible:

- Gain, power saving and muting of the analogue audio output
- Gain, power saving and muting of the analogue audio input
- Gain and muting of linear PCM signals. i.e., the input signal in Encoder / Enc-Dec / Pass-through modes OR the output signal in Decoder mode
- Decoder Noise Gate – noise threshold and gate activation delay

The registers that allow configuration of these features are:

- AIG - $B1 write
- AOG1 - $B4 write
- AOG2 - $B5 write
- AOG3 - $B6 write
- ANAOUT Config - $B3 write
- ANAIN Config - $B0 write.
- Fine Gain - $5B write
- Noise Gate Configuration - $5E write

6.12.5 Interrupt Operation

The CMX7262 can produce an interrupt output when various events occur. Examples of such events include when the vocoder has finished processing and has the output data available, or when the vocoder is ready to accept more input data or an output overflow when processing audio data.

Each event has an associated Status register bit and an Interrupt Mask register bit. The Interrupt Mask register is used to select which status events will trigger an interrupt on the IRQN line. Events can be masked using the IRQ mask bit (bit 15) or individually masked using the Interrupt Mask register. Enabling an interrupt by setting a mask bit ($0 \rightarrow 1$) after the corresponding Status register bit has already been set to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the Status register reflects the IRQN line state.

All interrupt flag bits in the Status register are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. See:

- Status - $7E read
- IRQ Enable - $6C write.

6.13 Signal Level Optimisation

The internal signal processing of the CMX7262 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V supply, the signal range which can be accommodated without distortion is specified in 7.1.3 Operating Characteristics. Signal gain and dc offset can be manipulated as follows:

6.13.1 Audio Output Path Levels

The signals output from ANAOUT DAC have independent gain controls. The Fine Output adjustment has a maximum attenuation of 6dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 14.2dB and 6dB gain.

The ANAOUT signals may be independently inverted. Inversion is achieved by selecting a negative value for the (linear) Fine Output adjustment.

See:

- Fine Gain - $5B write.
- ANAOUT Config - $B3 write.
- AOG1 - $B4 write
- AOG2 - $B5 write.
- AOG3 - $B6 write.

6.13.2 Audio Input Path Levels

The Coarse Input has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the ANAIN pins is specified in section 7.1.3 Operating Characteristics.

A Fine Input level adjustment is provided, although the CMX7262 should operate correctly with the default level selected. Inversion is achieved by selecting a negative value for the (linear) Fine Input gain adjustment.

It should be noted that if the maximum allowable signal input level is exceeded, signal distortion will occur regardless of the internal attenuation.

See:

- Fine Gain - $5B write.
- ANAIN Config - $B0 write
- AIG - $B1 write.

6.14 C-BUS Register Summary

ADDR. (hex)	Read/ Write	REGISTER	Word Size (bits)	User Manual Page	Section
$01	W	General Reset	0	57	8.1.2
$48	W	Vocoder In Data Byte	8	58	8.1.3
$49	W	Audio In Data Word	16	58	8.1.4
$4B	R	Input Level	8	58	8.1.5
$4C	R	Vocoder Out Data Byte	8	59	8.1.6
$4D	R	Audio Out Data Word	16	59	8.1.7
$4F	R	Output Level	8	59	8.1.8
$52	W	Frequency Control	16	59	8.1.9
$53	W	Noise Suppression	16	60	8.1.10
$55	W	VCFG	16	60	8.1.11
$58	W	Signal Control	16	61	8.1.12
$59	W	IED	16	61	8.1.13
$5A	W	IDD	16	61	8.1.14
$5B	W	Fine Gain	16	62	8.1.15
$5D	W	Audio Routing	16	62	8.1.16
$5E	W	Noise Gate Configuration	16	63	8.1.17
$64	W	GPIO Control	16	63	8.1.18
$79	R	GPIO Input	16	70	8.1.31
$69	W	Reg Done Select	16	64	8.1.19
$6A	W	Programming Register	16	64	8.1.20
$6B	W	VCTRL	16	65	8.1.21
$6C	W	IRQ Enable	16	66	8.1.22
$71	R	PLEVEL	16	69	8.1.30
$7E	R	Status	16	71	8.1.32
$7F	R	MVCTRL	16	72	8.1.33
$B0	W	ANAIN Config	16	67	8.1.23
$B1	W	AIG	16	67	8.1.24
$B3	W	ANAOUT Config	16	68	8.1.25
$B4	W	AOG1	16	69	8.1.26
$B5	W	AOG2	16	69	8.1.27
$B6	W	AOG3	16	69	8.1.28
$B7	W	Bias Control	16	69	8.1.29

Table 4 C-BUS Registers

All other C-BUS addresses are reserved and must not be accessed.

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
DV_{DD} - DV_{SS}	-0.3	4.0	V
DV_{CORE} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
SPKR1 V_{DD} – SPKR1 V_{SS}	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Current into or out of any pin, except power supply pins, SPKR1P and SPKR1N	-20	20	mA
Current into or out of power supply pins, SPKR1P and SPKR1N	-120	120	mA

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25C		3500	mW
... Derating		35.0	mW/C
Storage Temperature	-55	+125	C
Operating Temperature	-40	+85	C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
DV_{DD} - DV_{SS}	3.0	3.3	3.6	V
DV_{CORE} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
SPKR1 V_{DD} – SPKR1 V_{SS}	3.0	3.3	3.6	V
Operating Temperature	-40	–	+85	C
Xtal Frequency	4.0	–	12.288	MHz
External Clock Frequency	9.6	–	24.576	MHz

Notes:

DV_{DD} = AV_{DD} = SPKR1 V_{DD} = "IOV_{DD}"
DV_{SS} = AV_{SS} = SPKR1 V_{SS} = "V_{SS}"

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Section 5, External Components.
Maximum load on digital outputs = 30pF.
Xtal Frequency = 9.6MHz ±0.01% (100ppm); T_{AMB} = –40C to +85C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device only when loaded with CMX7262 FI-1.0.0.0. Current consumption may vary with Function Image™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	20				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		-40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	22	-1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current	22	-1.0	–	1.0	µA
V_{BIAS}	21				
Output Voltage Offset w.r.t. $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	50	–	kΩ

Notes:

20 Characteristics when driving the XTAL/CLK pin with an external clock source.

21 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Section 5 External Components.

22 T_{AMB} = 25C, not including any current drawn from the device pins by external circuitry.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		30	15	–	–	ns
'Low' Pulse Width		30	15	–	–	ns
Input Impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Single-Ended ANAIN2 Input						
Input Impedance		31	–	> 10	–	MΩ
Input voltage range		34	–	–	20 to 80	%AV_{DD}
Load resistance (on pin 24)			47	–	–	kΩ
Amplifier open loop voltage gain (I/P = 1mV rms at 100Hz)			–	80	–	dB
Unity gain bandwidth			–	1.0	–	MHz
Differential ANAIN Input						
Input Impedance, enabled		31	10	–	140	kΩ
Input Impedance, muted or powersaved			–	200	–	kΩ
Input Voltage Range		32	–	–	20 to 80	%AV_{DD}
Programmable Input Gain Stage						
Gain (at 0dB)		33	-0.5	0	+0.5	dB
Cumulative Gain Error (w.r.t. attenuation at 0dB)		33	-1.0	0	+1.0	dB

Notes:

30 Timing for an external input to the XTAL/CLOCK pin.

31 With no external components connected.

32 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

33 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

34 Voltage range at the feedback pin to ensure input buffer does not limit.

AC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
Differential ANAOUT Output					
Power-up to Output Stable	40	–	50	100	µs
ANAOUT Output Coarse Gain Attenuator					
Attenuation (at 0dB)		-0.2	0	+0.2	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		-0.6	0	+0.6	dB
Output Impedance	41	–	600	–	Ω
Output Voltage Range	43	0.3	–	AV_{DD}-0.3	V
Load Resistance		20	–	–	kΩ
SPKR1 Speaker Output, SPKR2 Earpiece Output					
Power-up to Output Stable	40	–	50	100	µs
SPKR1, SPKR2 Output Coarse Gain Attenuator					
Attenuation (at 0dB)		-0.5	0	0.5	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		-1.0	0	1.0	dB
Output Power (SPKR1 Outputs)	44	–	–	140	mW
Output Voltage Range (SPKR1 Outputs)	45, 46	0.75	–	AV_{DD} – 0.75	V
Output Voltage Range (SPKR2 Outputs)	47	0.5	–	AV_{DD} – 0.5	V
Resistance					
SPKR1 Speaker Output	41	8	–	–	Ω
SPKR2 Earpiece Output	41	32	–	–	Ω

Notes:

40 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

41 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25C.

43 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

44 Differential power output into a 8Ω load at AV_{DD} = 3.0V.

45 For each output pin.

46 With respect to the outputs driving a differential load of 8Ω.

47 With respect to the output driving a 32Ω load to $AV_{DD}/2$.

7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in section 5.
Maximum load on digital outputs = 30pF.
Clock source = 19.2MHz ±0.01% (100ppm) external clock input; T_{AMB} = –40C to +85C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference signal level = 308mV rms at 1kHz with AV_{DD} = 3.3V
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device only when loaded with CMX7262 FI-1.0.0.0.
The use of other Function Images™ can modify the parametric performance of the device.
Current consumption may vary with Function Image™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	50				
Idle mode					
DI_{DD}	51	–	670	–	µA
AI_{DD}	52	–	17	–	µA
Transcoding mode					
TWELP Decoder (raw)	53	–	8.2	–	mA
TWELP Encoder (raw)	53	–	23.4	–	mA
TWELP Encoder (with FEC)	53		23.5		mA
TWELP Decoder (with FEC, soft decision)	53		10.1		mA
TWELP Decoder (with FEC, hard decision)	53	-	9.9	-	mA
FEC Loop (hard decision)	53	-	4.15	-	mA
FEC Loop (soft decision)	53	-	4.22	-	mA
Additional current for activating Analogue In port					
DI_{DD}		–	4.5	–	mA
AI_{DD}		–	3.3	–	mA
Additional current for activating Analogue Out port					
DI_{DD}		–	0.7	–	mA
AI_{DD}	54	–	4	–	mA

Notes:

50 T_{AMB} = 25C, not including any current drawn from the device pins by external circuitry.

51 Using external clock input, XTAL oscillator circuit powered down, and all GPIOs set to output and low using the GPIO Control - $64 write register.

52 All analogue sections are powered down by setting both ANAIN Config - $B0 write and ANAOUT Config - $B3 write registers to 0.

53 Input and output is through CBUS interface using Audio In, Audio Out, Vocoder In, and, Vocoder Out registers. Input is fed at the rate of 160 samples every 20ms. All analogue sections are powered down.

54 Only ANAOUT1 is enabled. If ANAOUT2 and, SKPR2 are also enabled, this figure increases to 8.3mA.

7.2 C-BUS Timing

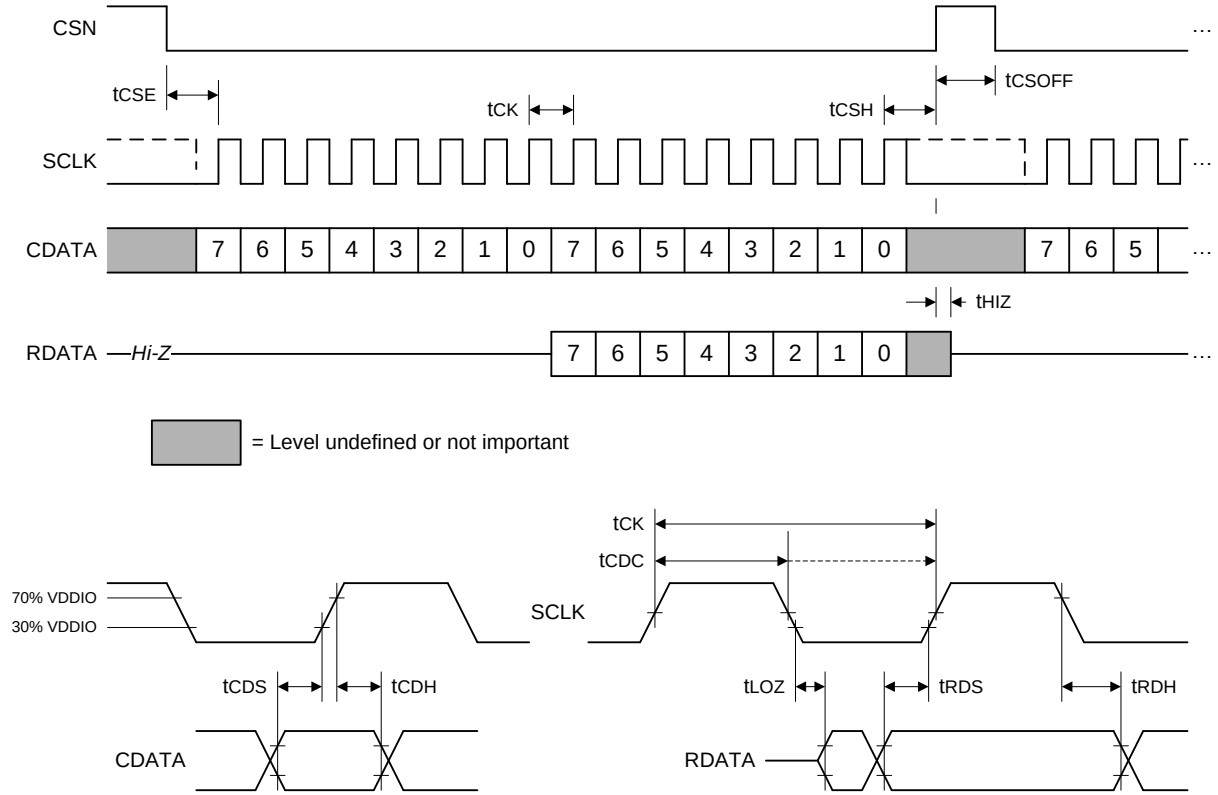


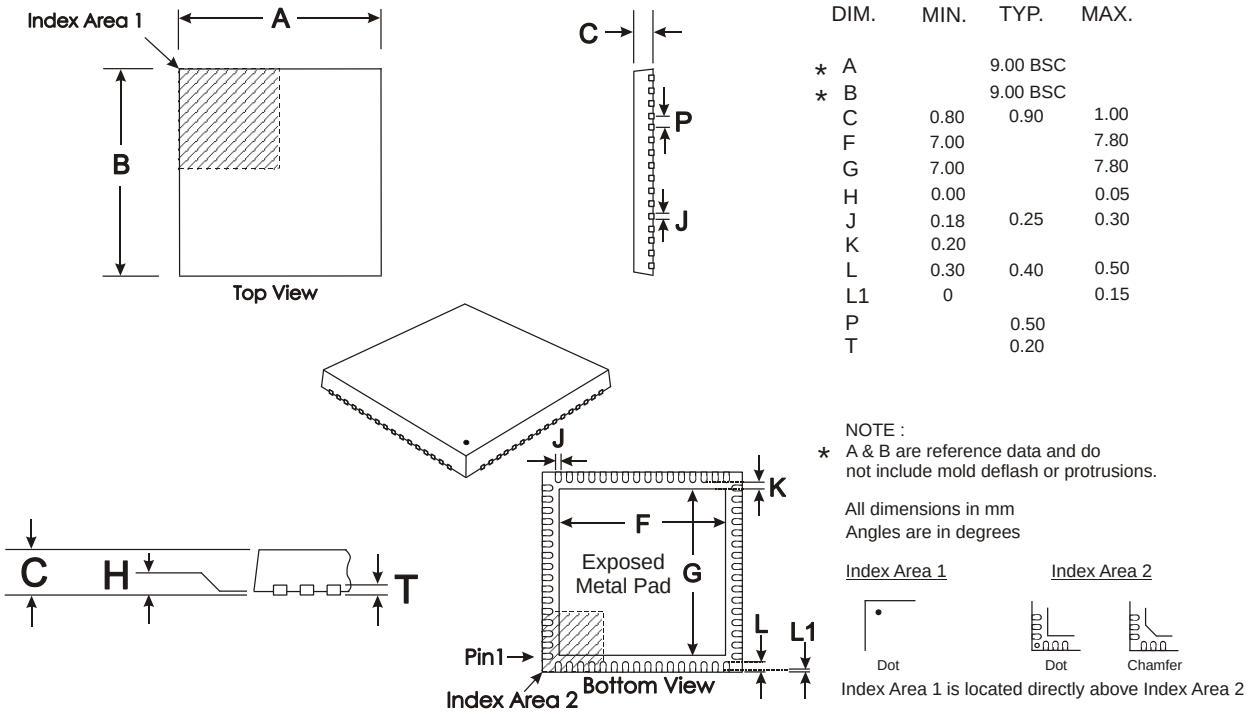
Figure 22 C-BUS Timings

AC Parameters	Notes	Min.	Typ.	Max.	Unit
C-BUS Timing	61, 62, 63				
Input pin rise/fall time (10% - 90% of VDDIO)		–	–	3	ns
Capacitive load on RDATA and IRQN		–	–	30	pF
t_{CSE} CSN enable to SCLK high time		40	–	–	ns
t_{CSH} Last SCLK high to CSN high time		40	–	–	ns
t_{LOZ} SCLK low to RDATA output enable time		0	–	–	ns
t_{HIZ} CSN high to RDATA high impedance		–	–	40	ns
t_{CSOFF} CSN high time between transactions		50	–	–	ns
t_{CK} SCLK cycle time		100	–	–	ns
t_{CDC} SCLK duty cycle		40	–	60	%
t_{CDS} CDATA setup time		25	–	–	ns
t_{CDH} CDATA hold time		25	–	–	ns
t_{RDS} RDATA setup time		25	–	–	ns
t_{RDH} RDATA hold time		0	–	–	ns

Notes: 61. Depending on the command, 1, 2 or more bytes of CDATA are sent to CMX7262 MSB first, LSB (Bit 0) last. RDATA is read from CMX7262 MSB first, LSB (Bit 0) last.
62. Commands are acted upon between the last rising edge of SCLK of each command and the rising edge of the CSN signal.
63. The CMX7262 is able to work with SCLK pulses starting and ending at either polarity.

These timings are for the latest version of streaming C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7262 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.3 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A		9.00 BSC	
*	B		9.00 BSC	
	C	0.80	0.90	1.00
	F	7.00		7.80
	G	7.00		7.80
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

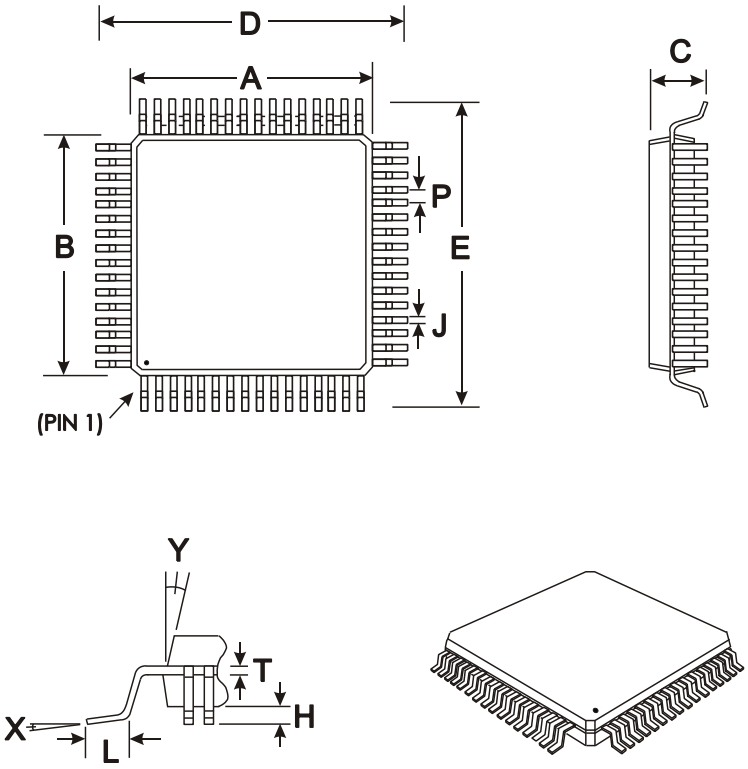
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 23 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7262Q1



	DIM.	MIN.	TYP.	MAX.
*	A	9.80		10.20
*	B	9.80		10.20
	C	1.40		1.60
	D	11.80		12.20
	E	11.80		12.20
	H	0.05		0.15
	J	0.17		0.27
	L	0.45		0.75
	P		0.50	
	T	0.09		0.20
	X	0°		7°
	Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 24 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7262L9

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

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