CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX971
Quadrature Modulator

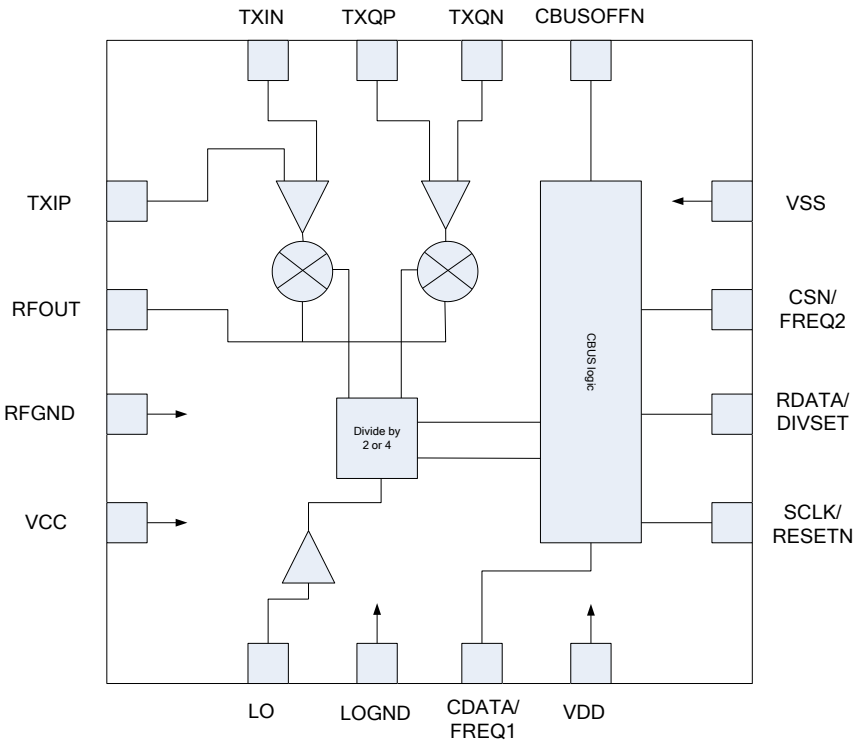
D/971/5 February 2019 Provisional Issue

Features

- 20 – 1000MHz RF Output
- 0dBm Output
- 25MHz I/Q Bandwidth
- Serial Bus or Direct Control Operation
- Low Power 3.0V – 3.6V Operation
- Small 16-lead VQFN Package

Applications

- Wireless Data Terminals
- HF/VHF and UHF Mobile Radio
- Avionics Radio Systems



1 Brief Description

The CMX971 is a high performance quadrature modulator featuring a wide operating frequency range and attractive power consumption. Control of the CMX971 may be either by serial bus or by direct control (with reduced functionality). Programmable features include the local oscillator divider ratio (2 or 4). The small, RF-optimised VQFN package and minimal external components make the device ideal for space-constrained applications.

CONTENTS

1.1 History

Version	Changes	Date
5	• CMX971A Introduced • Section 9.1.3.3: CMX971 typical equivalent output IP3 specification changed from 21 dBm to 14 dBm	05/02/19
4	• Added Smith Chart for LO input impedance, as section 8.1.1	17/2/15
3	• Information added on modulator harmonics (section 8.2.3).	25/2/13
2	• Clarification of Front Page, sections 5.2 and 7.0. • Additional information on FREQ bit settings, section 5.2.1 • Updated parametric information, after further characterisation	17/5/12
1	• First Issue	23/3/12

2 Block Diagram

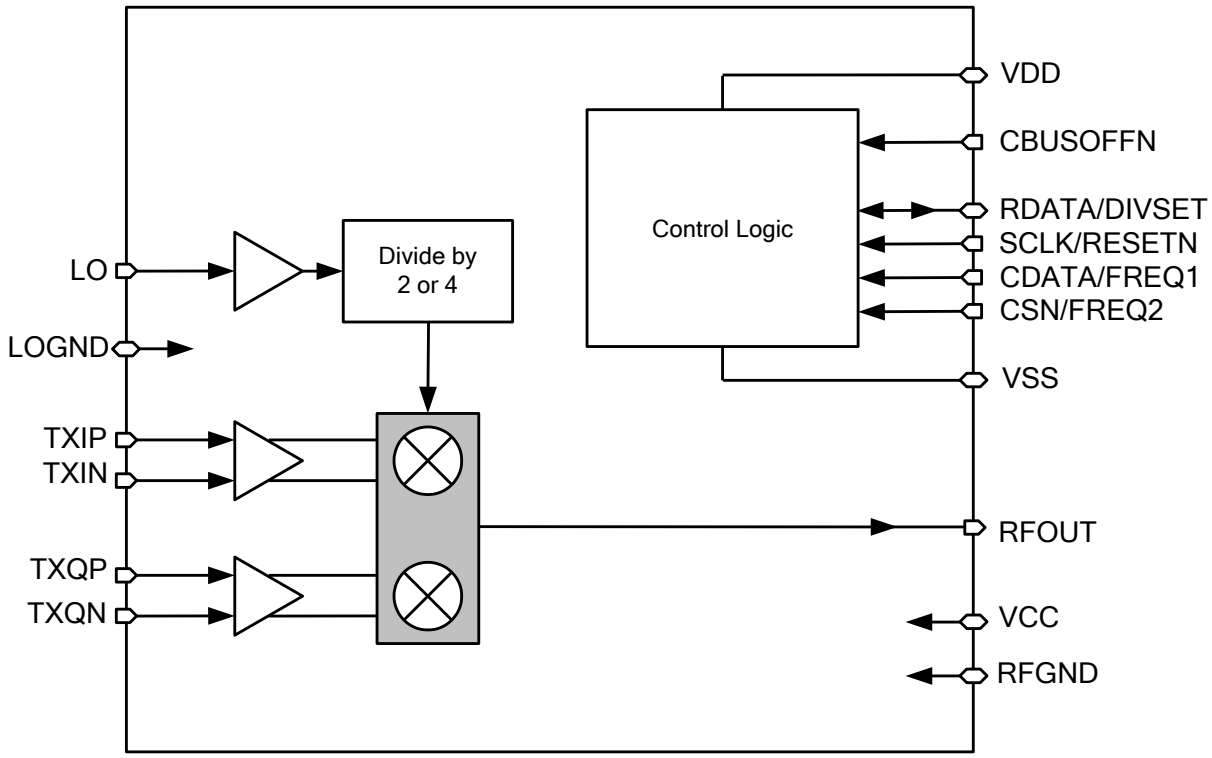


Figure 1 Block Diagram

3 Pin and Signal List

3.1 Main Functions

Pin	Name	Type	Signal Description
1	TXIP	IP	Input for baseband transmit I signal (positive)
2	RFOUT	OP	RF output
3	RFGND	PWR	Analogue and RF ground
4	VCC	PWR	Analogue and RF supply
5	LO	IP	Input for local oscillator
6	LOGND	PWR	LO Buffer ground
7	CDATA / FREQ1*	IP	C-BUS data-in
8	VDD	PWR	C-BUS and digital supply
9	SCLK / RESETN*	IP	C-BUS clock input
10	RDATA / DIVSET*	OP or IP*	C-BUS data output
11	CSN / FREQ2*	IP	C-BUS chip select
12	VSS	PWR	C-BUS and digital ground
13	CBUSOFFN	IP	Disable pin for C-BUS operation. If held low, direct control pin functions are selected as described in Table 2 and it enables modulator sections (equivalent to General Control Register b4 and b0 = '1', see section 6.2.1). Internal ≈1MΩ pullup resistor.
14	TXQN	IP	Input for baseband transmit Q signal (negative)
15	TXQP	IP	Input for baseband transmit Q signal (positive)
16	TXIN	IP	Input for baseband transmit I signal (negative)
~	EXPOSED METAL PAD	PWR	Substrate. Connect to Analogue and RF ground
* Direct control functions for these pins selected if CBUSOFF pin = '0', see Table 2.			

Table 1 Main Pin Functions

Notes: IP = Input
OP = Output
PWR = Power Connection
NC = No connection – should NOT be connected to any signal

3.2 Direct Control Functions

When C-BUS is held disabled, pins 7, 9, 10 and 11 have the following functions (Table 2). Every time the CBUSOFFN pin is held low the registers of the device are placed in the RESET state (section 6.1.1) except ENBIAS and TXEN (see section 6.2.1) which are active. The functions listed in Table 2 are then controlled by the appropriate pins.

Pin	Function
7	**FREQ1** – in combination with FREQ2 sets frequency range (see bit 0 of Tx Control register, section 6.3.1 and section 7.)
9	**RESETN** – When low puts the device into low power mode. No internal pullup resistor.
10	**DIVSET** – if low sets mixer input to local oscillator divide by two, if high sets mixer input to local oscillator divide by four (equivalent to the inverse of bit 6 of General Control Register, section 6.2.1)
11	**FREQ2** – in combination with FREQ1 sets frequency range (see bit 1 of Tx Control register, section 6.3.1 and section 7.)

Note: local oscillator divide by two and local oscillator divide by four will hereafter be referred to as LO/2 and LO/4 respectively.

Table 2 Direct Control Pin Functions

4 External Components

4.1 Power Supply Decoupling

The CMX971 has separate supply pins for the RF, analogue and digital circuitry; a 3.3V nominal supply is recommended for all circuits. It is recommended that the digital supply be decoupled from the RF and analogue supply; an example of such decoupling is shown in Figure 2.

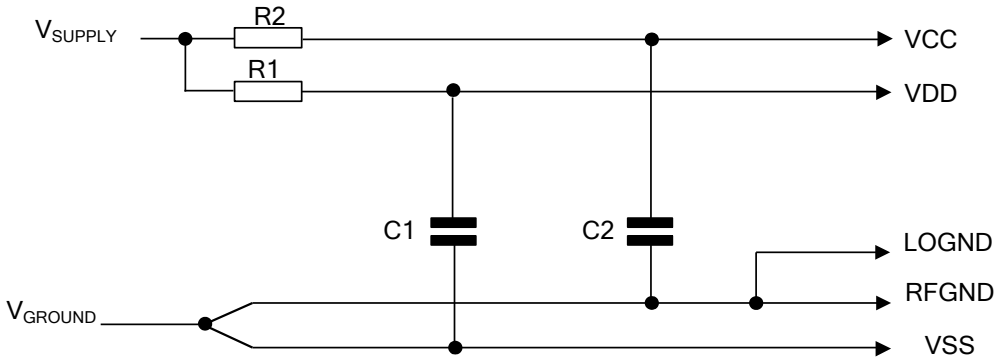


Figure 2 Power Supply Connections and Decoupling

C1	10nF	R1	10Ω
C2	10nF	R2	3.3Ω

Resistors ±1%, capacitors ±20%

Table 3 Power Supply Component Values

Note:

It is expected that low frequency interference on the 3.3V supply will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well. This may be achieved cost effectively using the resistor as shown. The use of resistors results in small dc voltage drops. Choosing resistor values approximately inversely proportional to the dc current requirements of each supply pin ensures the dc voltage drop on each supply is reasonably matched. In any case, the dc voltage change that results are well within the design tolerance of the device. If higher impedance resistors are used then greater care will be needed to ensure that the supply voltages are maintained within tolerance, including when parts of the device are enabled or disabled.

4.2 Quadrature Modulator

A typical circuit for the quadrature modulator output is shown in Figure 3 / Table 4.

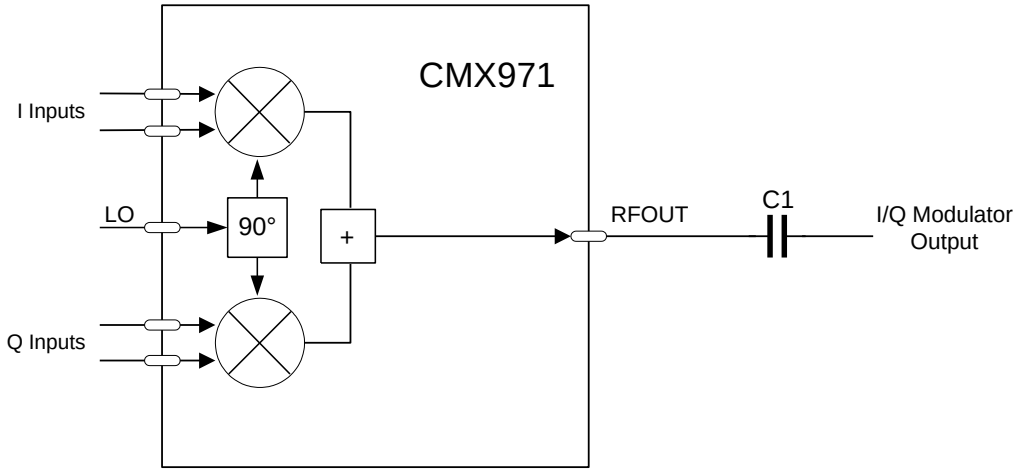


Figure 3 Modulator Output External Components (30MHz to 1GHz)

C1	1nF

Table 4 Quadrature Modulator Output Components

4.3 Local Oscillator (LO) Input

The CMX971 has a single ended LO input. Users should be aware that the presence of high levels of harmonics in the signal applied to the LO Input might degrade quadrature accuracy.

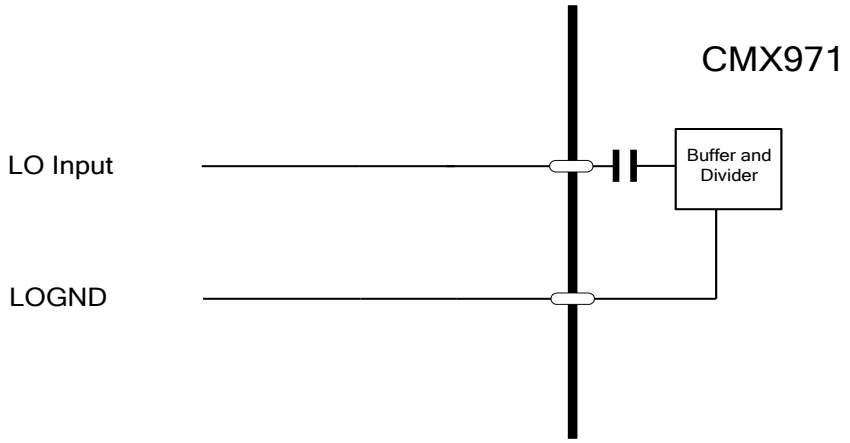


Figure 4 LO Input Configuration

A separate ground pin (LOGND) is used for the LO buffer to allow routing of the ground feed to the device such that any coupling, via the ground plane, between the LO signal and the RF signal can be minimised. In most cases it will be sufficient to just connect this to the RFGND ground plane, although it may be advantageous to supply LOGND from the ground supply for the LO generator or to star-connect the LO generator ground and the LOGND at a single point on the ground plane.

5 General Description

The CMX971 device is an RF integrated circuit providing a quadrature modulator. A detailed block diagram for the device is shown in Figure 1. The device can support a wide range of modulation formats and standards. The following sections describe its functionality.

5.1 Programmable Data Interface

The CMX971 may be controlled via its C-BUS serial interface (see section 6). Alternatively, the device can be used in direct control mode with reduced programmability; this can be advantageous in systems without a host controller (see section 7).

5.2 Quadrature Modulator

The quadrature modulator provides translation from baseband I/Q signals to a modulated RF signal. The wideband inputs can be driven in a differential or single-ended configuration. In the case of single ended operation a reference voltage equal to the nominal dc level of the modulation must be supplied on the unused input pin.

5.2.1 DC Offsets and Carrier Leakage

The modulator inputs (TXIN / TXIP and TXQN / TXQP) are differential and require a common dc level or common mode voltage. Differences in the bias voltages on the pins will result in an increased level of carrier present at the output. Care should be taken to minimise offsets, thereby minimising carrier leakage.

5.3 Local Oscillator

The LO pin is a single-ended input for the modulator local oscillator signal. Internal ac coupling is provided so an external dc blocking capacitor is not required, see Figure 4. Note that the LO should be at two or four times the desired RF output frequency.

6 C-BUS Interface and Register Description

The C-BUS serial interface supports the transfer of control and status information between the CMX971's internal registers and an external host. Each C-BUS transaction consists of the host sending a single Register Address byte, which may then be followed by zero or one data byte that is written into the corresponding CMX971 register, as illustrated in Figure 5.

Data sent from the host on the Command Data (CDATA) line is clocked into the CMX971 on the rising edge of the Serial Clock (SCLK) input. The C-BUS interface is compatible with common µC/DSP serial interfaces and may also be easily implemented with general purpose I/O pins controlled by a simple software routine. Section 9.1.3.5 gives the detailed C-BUS timing requirements.

Whether a C-BUS register is of read or write type is fixed for a given C-BUS register address, thus one cannot both read and write the same C-BUS register address.

In order to provide ease of addressing when using this device with other CML RF devices the C-BUS addresses below are arranged so as not to overlap those used on the existing CML RF Devices. Thus, a common chip select (CSN) signal can be used, as well as common CDATA, RDATA and SCLK signals. Also note that the General Reset ($1A) command on the CMX971 differs from other CML devices (such as CMX991 / CMX992 / CMX993 / CMX998), which use $01 or $10 for this General Reset function.

The C-BUS functions can be disabled in the CMX971 by using the CBUSOFFN pin, see section 3 for details. The CBUSOFFN pin should be tied high to enable C-BUS operation.

The following C-BUS register addresses are used:

Write Only register;	
General Reset Register (Address only, no data)	Address $1A
General Control Register, 8-bit write only.	Address $1B
Control Register, 8-bit write only.	Address $1E
Read Only register;	
General Control Register, 8-bit read only.	Address $EB
Control Register, 8-bit read only.	Address $EE

Notes:

- All registers will retain data if the VDD pin is held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices, the VDD pin must be maintained in its normal operating range otherwise ESD protection diodes may cause a problem with loading signals connected to SCLK, RDATA and CDATA pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.

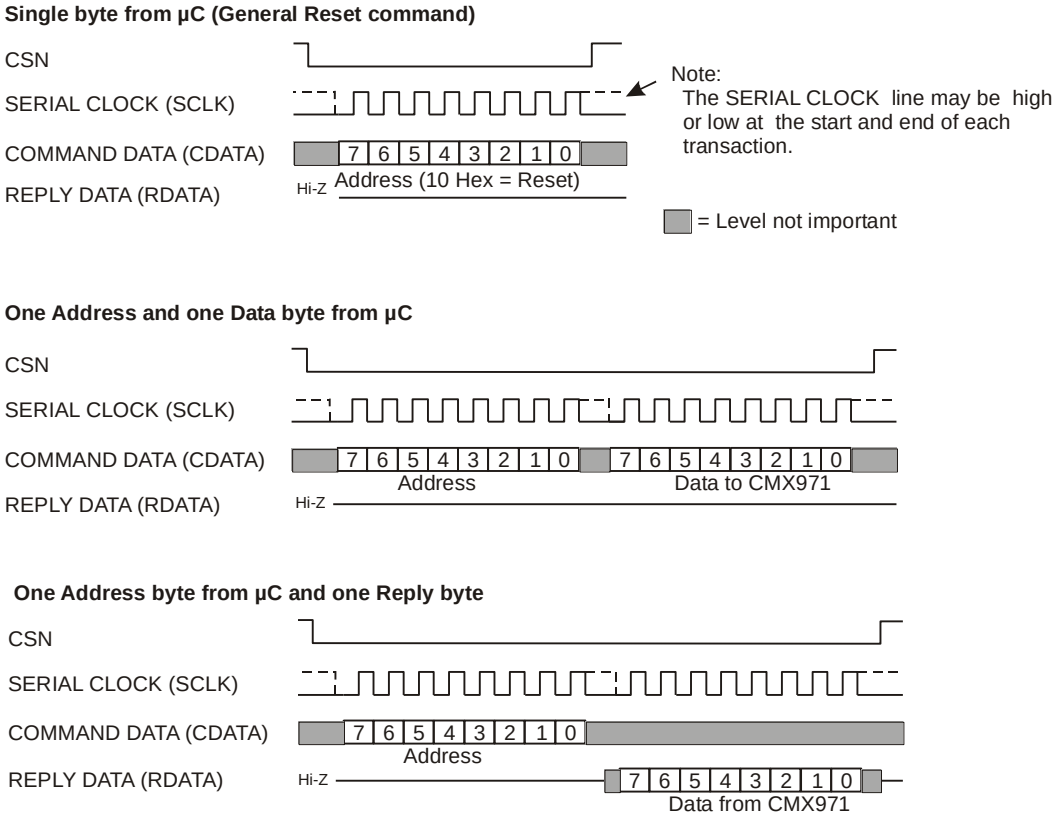


Figure 5 C-BUS Transactions

6.1 General Reset Command

6.1.1 General Reset Command C-BUS address $1A (no data)

This command resets the device and clears all bits of all registers. The General Reset command places the device into Powersave mode.

Whenever power is applied to the VDD pin, a built in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. If the C-BUS is disabled, the RESETN pin on the device will also place the device into the same state whilst the pin is held low.

6.2 General Control Register
8-bit write-only

6.2.1 General Control Register: C-BUS address $1B
This register controls general features such as powersave.

All bits of this register are cleared to ‘0’ during a General Reset command.

Note:
b0 (TXEN) and b4 (ENBIAS) are high if pin CBUSOFFN is low.

Bit:	7	6	5	4	3	2	1	0
	0	TXDIV	0	ENBIAS	0	0	0	TXEN

General Control Register b6, b4 and b0

Writing b6 = ’1’ the LO is divided by 2; writing b6 = ’0’ the LO is divided by 4.
Writing b4 = ‘1’ Enables the internal bias current supplies.
Writing b0 = ‘1’ Enables the quadrature modulator

All other bits are reserved and must be set to ‘0’ for correct operation.

6.2.2 General Control Register C-BUS address $EB
8-bit read-only
This register reads the value in register $1B, see section 6.2.1 for details of bit functions.

6.3 Control Register

6.3.1 Control Register: C-BUS address $1E
8-bit write-only
This register controls transmitter features.

All bits of this register are cleared to ‘0’ by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	0	0	0	0	F3	F2	F1	F0

Control Register b7 – b4
These bits are reserved and must be set to ‘0’ for correct operation.

Control Register b3 - b0
These bits optimise the performance of the Transmitter LO path. The best intermodulation performance is achieved at the lowest control setting (‘0000’) and the best wideband noise can be achieved at the highest setting (‘1111’).

Bit:	b3	b2	b1	b0	
	0	0	0	0	best intermodulation
	0	0	0	1	intermediate value
	0	0	1	0	intermediate value
	0	0	1	1	intermediate value
	0	1	0	0	intermediate value
	0	1	0	1	intermediate value
	0	1	1	0	intermediate value
	0	1	1	1	intermediate value
	1	0	0	0	intermediate value
	1	0	0	1	intermediate value
	1	0	1	0	intermediate value
	1	0	1	1	intermediate value
	1	1	0	0	intermediate value
	1	1	0	1	intermediate value
	1	1	1	0	intermediate value
	1	1	1	1	best wideband noise

6.3.2 Control Register C-BUS address $EE

8-bit read-only

This read-only register mirrors the value in register $1E; see section 6.3.1 for details of bit functions.

7 Direct Control Option

As an alternative to the C-BUS method of controlling the device, the CMX971 has the option of using a direct method to control some of the device settings. This is particularly useful in systems that do not require a microcontroller. The settings are limited to being able to reset the device, set the LO divider to LO/2 or LO/4 and set the LO path frequency setting to 1 of 4 values to minimise quadrature error (see section 6.3.1).

The Direct Control Option is selected by holding the CBUSOFFN pin low. This changes the function of the C-BUS pins (CDATA, SCLK, RDATA and CSN) to those defined in Table 2 (these are FREQ1, RESETN, DIVSET and FREQ2 respectively). Other register settings adopt a default value. Note that the FREQ1 and FREQ2 pins have no frequency-dependent properties.

The device behaviour with CBUSOFFN = 0 is as follows:

RESETN, if asserted by taking the pin low, behaves like a C-BUS General Reset in that all registers will go to an all zero state and the device will go into a low power mode.

When RESETN is de-asserted (taken high) the device comes out of low power mode and enters its active state. In the active state the FREQ1, RESETN, DIVSET and FREQ2 pins have the following functionality.

Function	Pin at VDD	Pin at VSS
RESETN	Active mode	Low power mode, device reset
DIVSET	Divide by 4	Divide by 2

The FREQ1 and FREQ2 pins are decoded so as to give four values at which the quadrature accuracy is optimised. This is important in the LO divide-by-2 mode if the input oscillator mark-space ratio is not sufficiently close to 1. The value is a guide only – see section 6.3.1. The best intermodulation performance is achieved at the lowest setting (‘00’) and the best wideband noise can be achieved at the highest setting (‘11’).

FREQ1	FREQ2	
0	0	best intermodulation
1	0	intermediate value
0	1	intermediate value
1	1	best wideband noise

The C-BUS registers will be automatically configured as follows:

General Control Register: C-BUS address $1B

b7	b6	b5	b4	b3	b2	b1	b0
	TXDIV		ENBIAS				TXEN
0	See below	0	1	0	0	0	1

If DIVSET is low, b6 = 1 and the LO is divided by 2
If DIVSET is high, b6 = 0 and the LO is divided by 4

Control Register: C-BUS address $1E

b7	b6	b5	b4	b3	b2	b1	b0
				F3	F2	F1	F0
0	1	1	1	See below			

FREQ1	FREQ2	b3	b2	b1	b0
0	0	0	0	0	0
1	0	0	1	0	1
0	1	1	0	1	0
1	1	1	1	1	1

Note: It is unimportant that b6-b4 are set to ‘1’ rather than ‘0’ when using the Direct Control Option.

8 Application Notes

8.1 Impedance Matching Information

8.1.1 LO Input

The impedance to the LO input (LO pin) is shown in Figure 6.

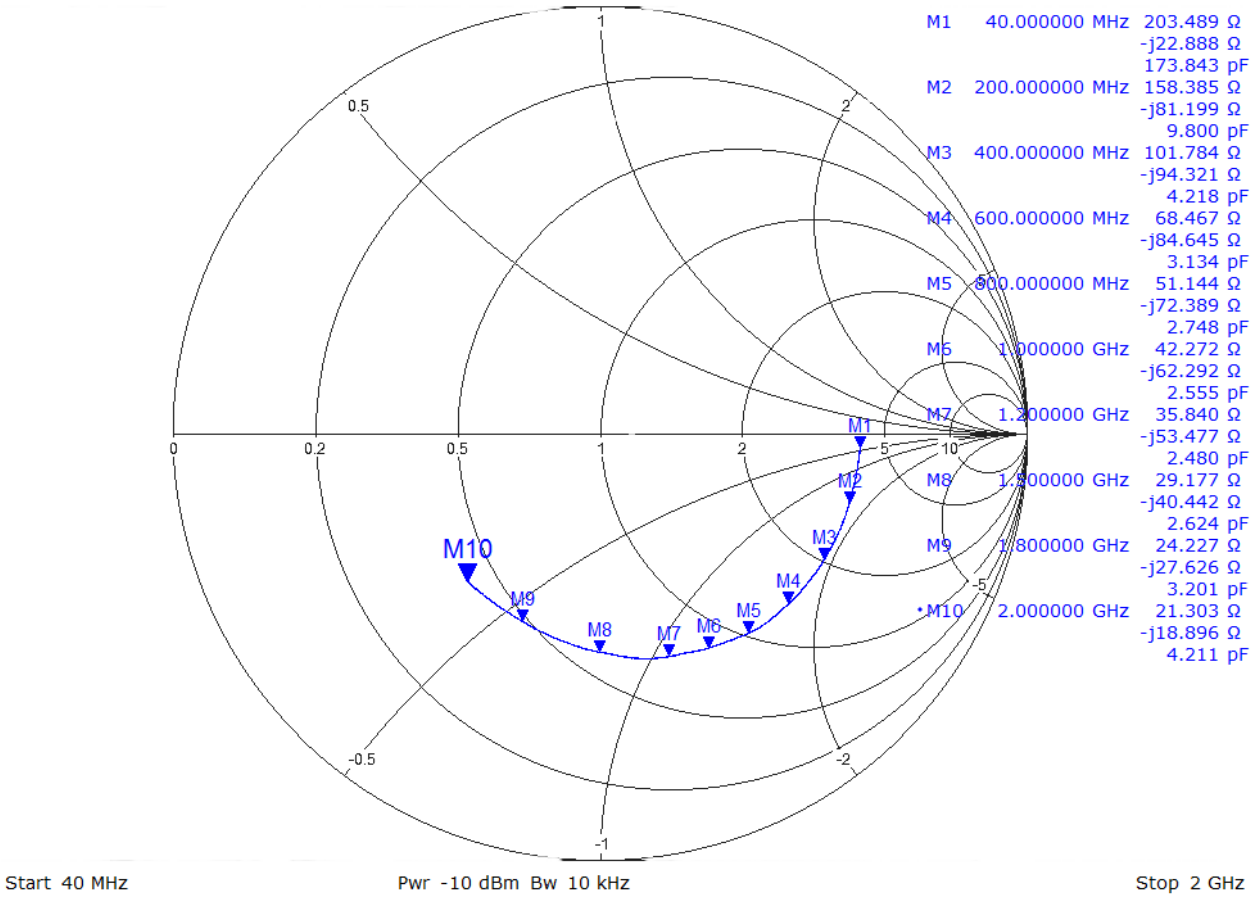


Figure 6 LO Impedance

8.2 Modulator Operation

This quadrature modulator is designed to operate with a maximum I/Q input level of 1Vp-p for either single-ended or differential operation. The device offers excellent modulation accuracy with accurate phase and amplitude balance and also low carrier leakage.

The variation in output level with frequency is typically 2dB, as shown in Figure 7, where the output level is shown for an I/Q input of 1Vp-p 7kHz sine and cosine waves. The LO input level is -10dBm.

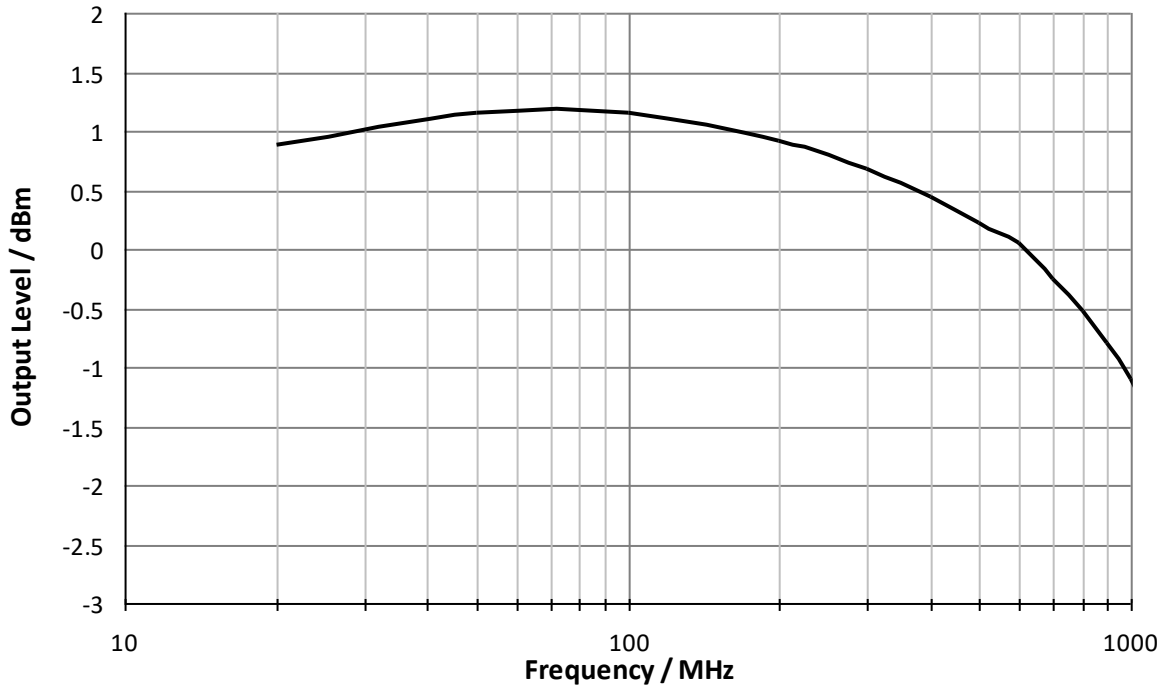


Figure 7 Typical Variation in Modulator Output Level with Frequency

8.2.1 Quadrature Accuracy

The modulation accuracy is excellent and consistent with frequency. The I/Q phase and amplitude balance can be measured as a combined result in terms of image suppression when sine and cosine waves are applied to the I and Q channels. Typical results for 7kHz I/Q signals are shown in Figure 8.

The CMX971A can be used to generate a wide range of modulations including those with stringent adjacent channel requirements, for example C4FM modulation for the APCO P25 system – see Figure 9. In this figure, the I/Q input level was 700mVp-p and the measured adjacent channel power is -70dB.

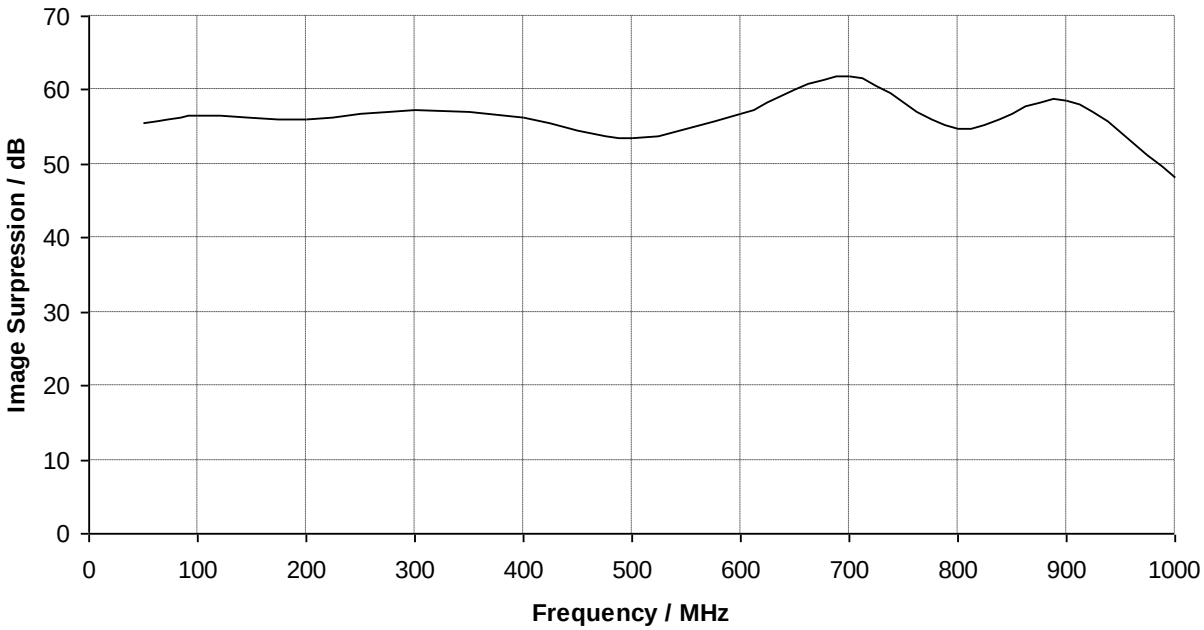


Figure 8 Modulator Accuracy with Frequency

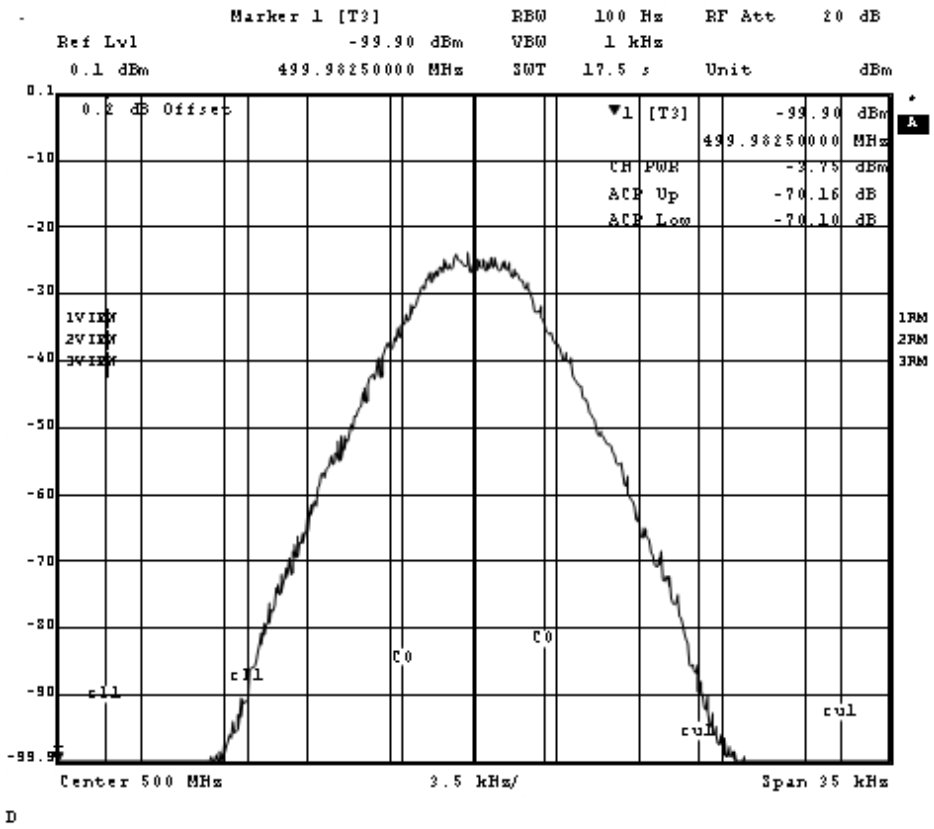


Figure 9 Typical Spectrum with APCO C4FM, (TIA/EIA 102.CAAB-B) at 500MHz

8.2.2 Wideband Noise

The CMX971 noise floor does not vary significantly with LO input level: with LO levels between -5dBm and -15dBm, less than 0.5dB of variation from the typical value of -150dBm/Hz can be expected.

For optimum wideband noise during modulation the F bits in the Control Register ($1E, b3-b0) should be set to '1111'. Wideband noise during modulation measured at a 5MHz offset from a 390MHz signal is shown in Table 5.

Freq Setting ($1E, b3-b0)	Output Level (dBm)	Noise at 5 MHz offset (dBc/Hz)
'0000'	3.9	-143.7
'1111'	4.2	-146

Table 5 Typical Wideband Noise at 5MHz Offset with Different Frequency Control Settings

8.2.3 Harmonics

The typical levels of modulator harmonics are summarised in Table 6 for an I/Q modulator output level of circa 0dBm; the LO level was -10dBm.

Variation of the LO level +/-10dB does not change the CMX971 modulator harmonic levels significantly. Whether the divide-by-2 or divide-by-4 mode is used also does not materially effect the level of the harmonics.

Harmonic	100MHz / dBc	400MHz / dBc	500MHz / dBc	1GHz / dBc
2nd	-37	-37	-36	-34
3rd	-10	-15	-17	-28
4th	-40	-36	-39	-47
5th	-15	-27	-33	-46
6th	-41	-48	-53	-57
7th	-19	-40	-51	-59
8th	-42	-55	-61	-68
9th	-23	-51	-64	
10th	-45	-66	-74	

Table 6 Typical Modulator Harmonic Levels for Given Output Frequency

9 Performance Specification

9.1 Electrical Performance

9.1.1 Absolute Maximum Ratings (CMX971 & CMX971A)

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS}), (V_{CC} - V_{RFGND}) or (V_{CC} – V_{LOGND})	-0.3	+4.0	V
Voltage on any pin to V_{RFGND}, V_{SS} or V_{LOGND}	-0.3	V_{DD} + 0.3	V
Voltage between V_{SS}, V_{RFGND} and V_{LOGND}	-50	+50	mV
Current into or out of RFGND, VSS, LOGND, VCC or VDD pins	-75	+75	mA
Current into or out of any other pin	-30	+30	mA

Q7 Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	2060	mW
... Derating (see Note below)	–	20.6	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Note: Junction-to-ambient thermal resistance is dependent on board layout and mounting arrangements. The derating factor stated will be better than this with good connection between the device and a ground plane or heat sink.

9.1.2 Operating Limits (CMX971 & CMX971A)

	Notes	Min.	Max.	Units
Analogue Supply (V_{CC} – V_{RFGND})		3.0	3.6	V
Digital Supply (V_{DD} – V_{SS})		3.0	3.6	V
Operating Temperature (see Note above)		-40	+85	°C

9.1.3 Operating Characteristics

9.1.3.1 DC Parameters CMX971 & CMX971A

For the following conditions unless otherwise specified:
$V_{DD} = V_{CC} = 3.3V$; $V_{SS} = V_{RFGND} = V_{LOGND} = 0V$. LO Level = -10dBm and T_{AMB} = +25ºC.

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption	1				
Powersave mode	2	–	7	70	µA
Bias only	3	–	1.7	2.0	mA
Operating	5	–	63	75	mA
Logic '1' Input Level		70%	–	–	V_{DD}
Logic '0' Input Level		–	–	30%	V_{DD}
Logic Input Leakage Current (Vin = 0 to V_{DD})		-1.0	–	+1.0	µA
Output Logic '1' Level (I_{OH} = 0.6 mA)		80%	–	–	V_{DD}
Output Logic '0' Level (I_{OL} = -1.0 mA)		–	–	+0.4	V
Power-up Time					
Voltage Reference	4	–	–	0.5	ms
All blocks except Voltage Reference	4	–	–	10	µs

Notes:

1. Total current, V_{DD} and V_{CC}.
2. Powersave mode includes the case after general reset with all analogue and digital supplies applied and also the case with V_{DD} applied but with all analogue supplies disconnected (i.e. in this latter scenario power from V_{DD} will not exceed the specified value, whatever the state of the registers). At T_{AMB} = 25ºC, not including any current drawn from device pins by external circuitry.
3. Only BIAS section active.
4. Time from the rising edge of the last serial clock input following CSN being asserted for a write to the appropriate control register.
5. Tx and Bias sections active, TXDIV = 0, F3-F0 = 0000.

9.1.3.2 AC Parameters CMX971 & CMX971A

For the following conditions unless otherwise specified:
$V_{DD} = V_{CC} = 3.3V$; $V_{SS} = V_{RFGND} = V_{LOGND} = 0V$. LO Level = -10dBm and T_{AMB} = +25ºC.

AC Parameters	Notes	Min.	Typ.	Max.	Units
Local Oscillator Input					
Frequency Range	6	40	–	2000	MHz
LO Input Impedance	7	–	–	–	Ω
LO Input Level		–	-10	–	dBm

Notes:

6. Local oscillator input frequency twice or four times the required operating frequency.
7. See section 8.1.1

9.1.3.3 AC Parameters – Modulator CMX971

For the following conditions unless otherwise specified:
$V_{DD} = V_{CC} = 3.3V$; $V_{SS} = V_{RFGND} = V_{LOGND} = 0V$. LO Level = -10dBm and $T_{AMB} = +25ºC$.

Quadrature Modulator	Notes	Min.	Typ.	Max.	Units
I/Q Input Common Mode Voltage		–	1.6	–	V
I/Q Mixer Input Voltage		–	–	1	Vp-p
Modulator Input Bandwidth		–	25	–	MHz
Gain from I/Q Input to Output	11	–	-4	–	dB(V/V)
Output Frequency Range		20	–	1000	MHz
Transmit Output Power (PEP)	8	–	0	–	dBm
Noise Floor	10	–	-150	–	dBm/Hz
Wideband Noise During Modulation	12	–	-146	–	dBc/Hz
Image Suppression					
At 100MHz		–	50	40	dB
At 500MHz		–	52	–	dB
At 1000MHz		–	44	40	dB
I/Q Gain Matching Error		–	–	0.5	dB
I/Q Phase Matching Error		–	–	1	degree
Carrier Suppression					
At 100MHz		–	-50	-40	dBm
At 500MHz		–	-50	–	dBm
At 1000MHz		–	-49	-40	dBm
Equivalent Output IP3	8, 13, 14	–	14	–	dBm
Load Impedance		–	50	–	Ω
Discrete Unwanted Emissions (other than harmonics of the output) in the Frequency Range 9kHz –12.75GHz.	9	–	-	-70	dBc

Notes:

8. Output power and OIP3 is achieved with the input drive level stated on I and Q channels, operation at 500MHz (sine and cosine waveforms on I and Q respectively).
9. With a spurious-free LO input and -10dBm output level.
10. Measured with TXIN, TXIP, TXQN, TXQP connected to 1.6V with 10Ω resistors decoupled by 33nF capacitors; measured at 20MHz offset from the operating frequency of 380 MHz.
11. Voltage gain measured from modulator input to output using 7kHz sine/cosine waves on TXIN/TXQN, at 500MHz.
12. Control Register ($1E), b3-b0 = ‘1111’.
13. Control Register ($1E), b3-b0 = ‘0000’.
14. Optimum performance for I/Q signals up to 2 MHz.

9.1.3.4 AC Parameters – Modulator CMX971A

The CMX971A offers guaranteed linearity performance and is therefore recommended for the most demanding applications.

Parameters as section 9.1.3.3 are applicable plus the following additional items.

For the following conditions unless otherwise specified:
$V_{DD} = V_{CC} = 3.3V$; $V_{SS} = V_{RFGND} = V_{LOGND} = 0V$. LO Level = -10dBm and $T_{AMB} = +25ºC$.

Quadrature Modulator	Notes	Min.	Typ.	Max.	Units
Equivalent Output IP3 -	13, 14, 15				
100 MHz		15	-	–	dBm
500 MHz		13	-	-	dBm
1 GHz		7	-	-	dBm
Single tone third order product	13,16	–	–	-42	dBc

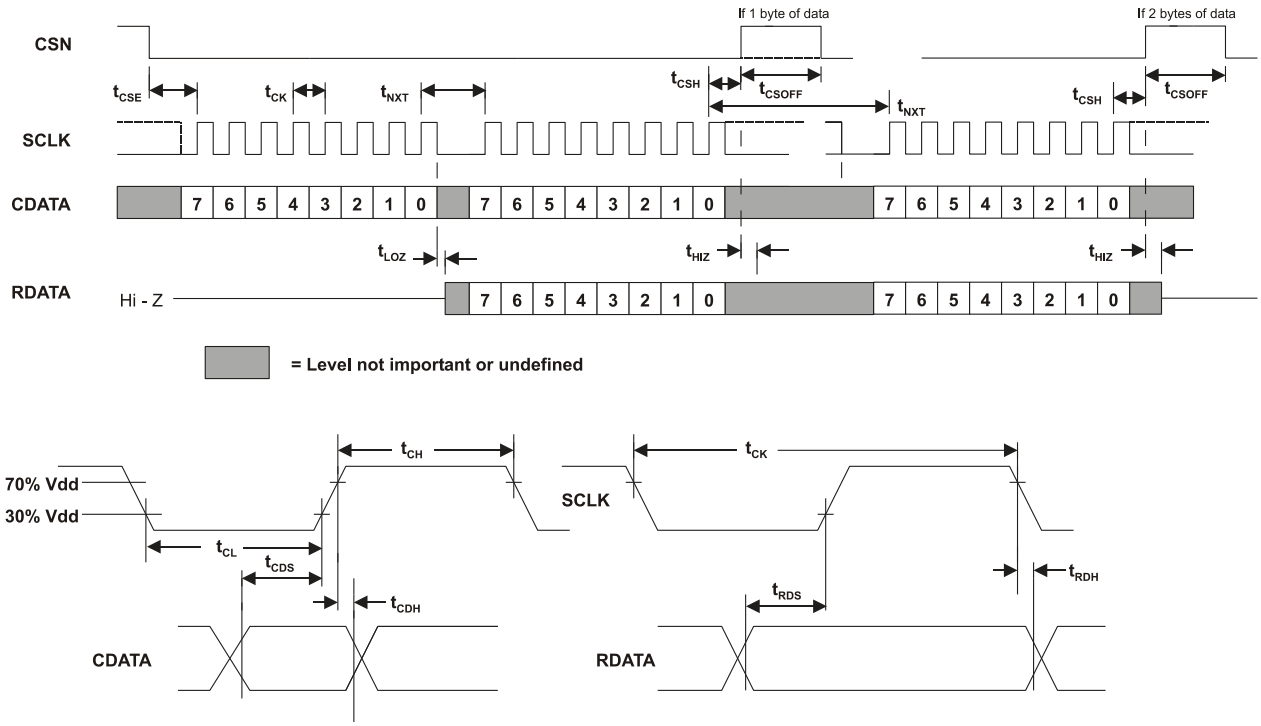
Notes:

15. Input drive level on I and Q channels, 1Vp-p differential.
16. Single tone input of 1 kHz, differential on I/Q adjusted to achieve -5 dBm wanted signal at 999.999 MHz; product at 1000.003 MHz measured relative to wanted signal.

9.1.3.5 C-BUS CMX971 & CMX971A

C-BUS Timings (See Figure 10)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-enable to clock-high time		100	–	–	ns
t_{CSH}	Last clock-high to CSN-high time		100	–	–	ns
t_{LOZ}	Clock-low to reply output enable time		0.0	–	–	ns
t_{HIZ}	CSN-high to reply output 3-state time		–	–	1.0	µs
t_{CSOFF}	CSN-high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	Clock-cycle time		200	–	–	ns
t_{CH}	Serial clock-high time		100	–	–	ns
t_{CL}	Serial clock-low time		100	–	–	ns
t_{CDS}	Command data set-up time		75.0	–	–	ns
t_{CDH}	Command data hold time		25.0	–	–	ns
t_{RDS}	Reply data set-up time		50.0	–	–	ns
t_{RDH}	Reply data hold time		0.0	–	–	ns

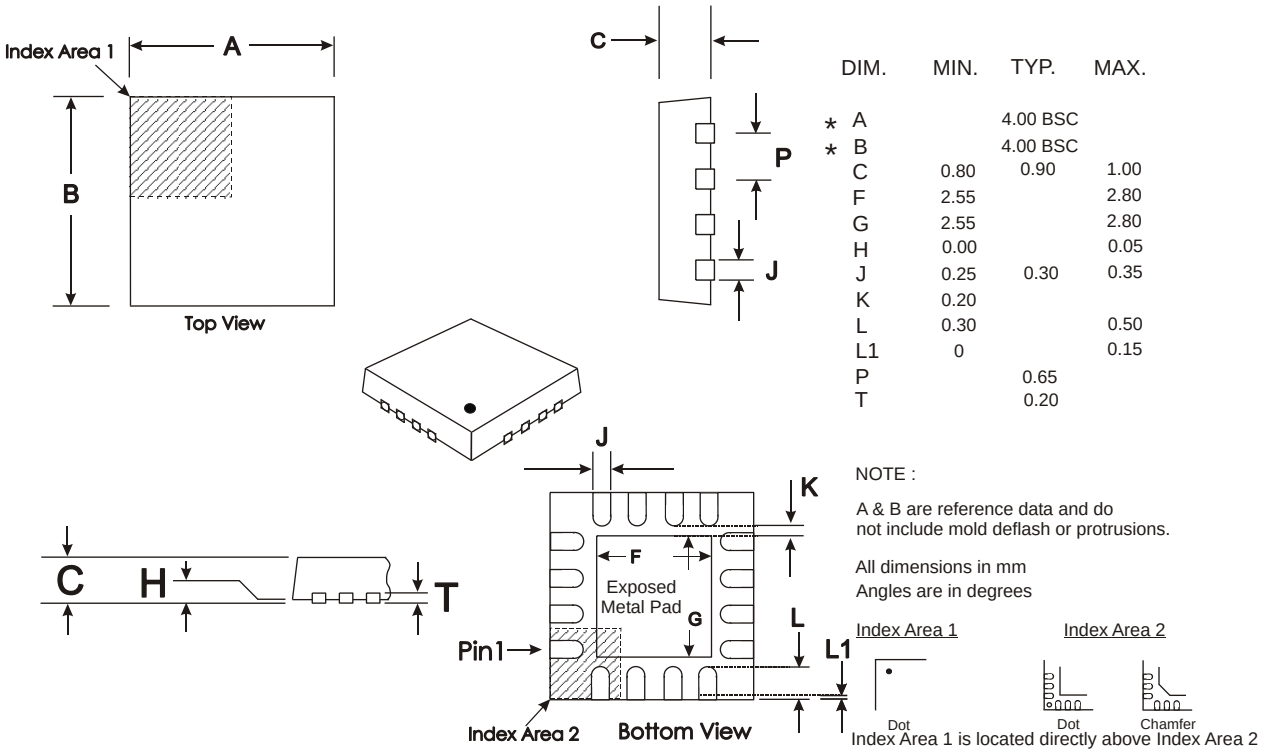
Maximum 30pF load on each C-BUS interface line.



Note: *Only 1 byte of data is used in C-BUS transactions.*

Figure 10 C-BUS Timing

9.2 Packaging



Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 11 Q7 Mechanical Outline: *Order as part no. CMX971Q7*

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