

Evaluation Board Quick Start

EV9830

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Introduction 1

Thank you for your interest in the EV9830 Evaluation Board.

This quick start guide will help you get started with your EV9830 evaluation. The respective datasheet and user manual provide full details on the board, but this "quick start" guide consolidates information from multiple sources to accelerate your testing.

This guide walks the user through the following steps:

- Downloading necessary files
- Connecting the EV9830, HB9830, and PE0003
- Installing PE0003 USB driver .
 - Using EV9830 graphical user interface (GUI) to:
 - Configure CMX983 frac-N synthesizers for 901MHz and 2.1GHz 0
 - Configure CMX983 main ADC (Rx) and DAC (Tx) channels for 75ksps 0
 - Configure CMX983 Rx/Tx serial ports for data capture to/from PE0003 microSD card 0

2 **History**

Version	Changes	Date
2	Modified Tx/Rx GUI settings	15-02-26
1	Initial release	15-01-29

Table of Contents

1	Intro	duction	. 1
2	Histo	Dry	. 1
3	Prep	aration for Operation	.2
	3.1	Download of Documents and Software	.2
	3.2	Test Equipment	.2
	3.3	Basic Connections	.2
	3.4	PE0003 Installation	.3
4	EV98	830 Graphical User Interface	.3
	4.1	Save State and Load State	.4
5	CMX	(983 Frac-N Synthesizer Operation	.4
6	CMX	(983 Rx and Tx Channel Operation	. 5
	6.1	PE0003 microSD Card	.5
	6.2	Rx Channel Operation	.7
	6.3	Tx Channel Operation	. 8
	6.4	Helpful Hints.	. 8

3 Preparation for Operation

3.1 Download of Documents and Software

Please visit the CML website (www.cmlmicro.com) and download the following files:

- CMX983 Datasheet
- EV9830 User Manual
- EV9830 Schematic
- EV9830 Evaluation Software package
- PE0003 Driver
- PE0003 User Manual

3.2 Test Equipment

The following test equipment will be needed:

- PC with Windows 8 or earlier.
- +/-6V supply (rated for 500mA) for PE0003 and EV9830.
- Baseband IQ signal generator
- RF spectrum analyzer
- Oscilloscope (for generic signal viewing if desired)

3.3 Basic Connections

Connect HB9830 to "Host Port" port on PE0003 (Do not use PE0003 C-BUS ports!).



Figure 1: HB9830 Connected to PE0003 Host Port

• Connect 20-pin ribbon cable between EV9830 "Host Port" and HB9830.



Figure 2: EV9830 Host Port Connected to HB9830

• Apply +6V to PE0003 and +/-6V to EV9830.



Figure 3: Power Supply Connections

3.4 PE0003 Installation

The following steps will install the PE0003 on your PC:

- Connect PE0003 to PC with USB cable.
- The PC will ask for a USB driver the first time a PE0003 is connected. When prompted, load the USB driver from the unzipped PE0003 Driver package.
- Your PC may attempt to use "Windows Update" to find the PE0003 USB driver. Cancel the "Windows Update" search. On your PC click "Start" button, right click on "Computer" and select "Properties". Select "Device Manager". Right click "PE0003 Evaluation Kit" and choose "Update driver software". Choose "Browse my computer" and locate the PE0003 driver you downloaded earlier. Click "Install anyway" if you get a driver warning message.

4 EV9830 Graphical User Interface

The EV9830 graphical user interface (GUI), named "ES9830xx.exe" (xx=version number), is available in the unzipped EV9830 Evaluation Software package.

- Double-click the executable file to launch the GUI.
- Click "Init Board" to activate CMX983 internal clock generation.



Figure 4: Location of "Init Board" in ES9830 GUI

4.1 Save State and Load State

Clicking "Save State" allows the creation of a user-named ".sta" file that contains all ES9830 GUI selections. These selections can be recalled by clicking "Load State" and selecting the appropriate ".sta" file from your computer. Please note that loading a ".sta" file does not automatically cause the GUI selections to be written to CMX983; the "Write" button on each GUI tab must be clicked in order for the GUI selections to be written to CMX983.

ES9830 Evaluation Kit Software		ES9830 Evaluation Kit Software	
CEUS Control Frac-N 1 Frac-N 2 Rx Channel Wite a Register G Stat. Register Address (5) C 16bit. Register Data (5) Wae.	Tx Ohannel Re/Tx Pots Sorgt Hender Read a Register G Baa Register Address (0) C 16bit Register Data (0) Register Data	CBUSControl Frac-N 2 Rocharnel Tx Wite a Register (c Bob Register Address (b) C 1564 Register Data (b)	Channel Re/Tx Pots Scipt Hander Read a Register G Solt Register Address (5) G 16bt Register Data (5) Register Data (5)
System Dock Generator System Cock Generator MLK frequency 192 VMLK mouthing 192 Use PLL Use PLL CLKPL CON1 2603 CLKPLL CON1 0604	Topologic PLI. NR Divides Required Finite 38.8 MHz. N = 8 dec Comparison Finite 4800 MHz. N = 4 dec Reference Finite 13.2 MHz. N = 4 dec Reference Finite 13.2 MHz. VCD 200- 0.00 MLX N = VCD/2 LinzRes 4.4 1500-0605 Alog: Childres Childres Childres	- System Clock Generator MCLK/requery 192 MHz PL System Clock 192 MHz C P MCLK ampliter P MCLK ampliter CLK/CON 2860 CLK/PLL_CON 6640 CLKPLL_CON 6404	L, N/E, Divides 38.4 MHz, N * 6 dec squited Fireq 38.4 MHz, N * 6 dec operation Fireq 4500 kHz, R * 4 dec ofference Fireq 19.2 MHz, N * 6 dec Objection Kr 7.000+007 Hz/V / VC/V2/2 Rate 4 1.500+005 Hz - Octand 11 Fprex (1250+005 Hz -
Select Target Board Sa	ve settings n all GUI tabs	Select Target Board © C&US Header 1 C C&US Hea	(must click "Write" on individual tabs)

Figure 5: Save State and Load State

5 CMX983 Frac-N Synthesizer Operation

The EV9830 includes external VCO circuits to allow demonstration of frac-N synthesizer operation at 900MHz and 2.1GHz.

• Click "Frac-N 1" tab in GUI, make the following selections, and click "Write Frac-N 1" to enable the frac-N 1 synthesizer to generate 901.2MHz. Output is available on 900MHZ (J101) SMA connector.

ES9830 Evaluation Kit Software	
ES933 Evaluation Kit Schware CBUS Contral Free-N1 [Free-N2] Rx Channel Tx O PLLR RVF Divides VPLLEnable	
MCLK Frequency 192 MHz Comparison free 4.8 MHz R = 4 dec I = 188 dec F = 4194303 dec	Pagites PL1_SON(\$48) 0909 PL1_RON(\$52) 04 PL1_SON(\$48) 0000 PL1_DON(\$53) 000C PL1_SON(\$51) 00 PL1_SON(\$52) 000 PL1_SON(\$52) 000 PL1_SON(\$53) 000C PL1_SON(\$52) 000 PL1_SON(\$55) 000 PL_CFG(\$CE) 0000 PL1_SON(\$55) 00 Free-N1
	Save State Load State Options Close

Figure 6: Frac-N 1 Configured for 901.2MHz

• Click "Frac-N 2" tab in GUI, make the following selections, and click "Write Frac-N 2" to enable the frac-N 2 synthesizer to generate 2096.45MHz. Output is available on 2G1HZ (J6) SMA connector.

ES9830 Evaluation Kit Software	
C-BUS Control Frac-N 1 Frac-N 2 Rx Channel Tx Ch	nannel Rx/Tx Ports Script Handler
PLL, R/I/F Dividers	Bleed Current (\$51) F Enable Bleed Current Coarse 0 Fine 0
Mode Frac-N div (3rd Order) Charge Pump Current 250uA	Fast Lock
Dividers	Timer Coarse Divide 0 Timer Fine Divide 0 Current Multiply 4x •
VC0 Frequency 2096.45 MHz MCLK Frequency 19.2 MHz Comparison Freq 4.8 MHz R = 4 dec I = 437 dec	Registers PLL2_CONIS57 0593 PLL2_RDIVIS58) 04 PLL2_RCKIS59 0000 PLL2_DIVIS50 0185 PLL2_BLEED(SM) 00 PLL2_FOVIS5D) AA48 PLL_CFG(SE) 0000 PLL2_FOVIS5D) C2
F = 4013541 dec	Frac-N 2 Serve State Load State Options Occe

Figure 7: Frac-N 2 Configured for 2096.45MHz

6 CMX983 Rx and Tx Channel Operation

6.1 PE0003 microSD Card

A Class 10 microSD card is required in the PE0003 for proper data transfer to/from CMX983 serial ports. The microSD card is located on PE0003 bottom.

Ensure that the PE0003 microSD card has been partitioned with a large unformatted area for EV9830 data storage. A file system on the microSD card slows down EV9830 data transfer, so serial port data must be stored in the unformatted area of the microSD card. Here is an example of a 32GB card with a 4GB partition:

SD Card (F:) F	roperties	per disk.	×
Security	ReadyBoost	Quota	Customize
General	Tools	Hardware	Sharing
SD			
Type:	Removable Disk		
File system:	NTFS		
Used space	e: 94,2	12,096 bytes	89.8 MB
Free space	e: 4,031,9	30,368 bytes	3.75 GB
Capacity:	4,126,1	42,464 bytes	3.84 GB
	Driv	e F:	
Compress this drive to save disk space Mow files on this drive to have contents indexed in addition to file properties			d in addition to
	ОК	Cancel	Apply

Figure 8: Example of Reduced Size Partition in 32GB SD Card

If you need to establish a partition on a microSD card, insert card into PC and do the following:

- 1) Backup the files on the SD card by copying them to a separate drive.
- 2) At a command prompt, type: diskpart.
- 3) Use LIST DISK command and identify the disk number that the SD card is mounted as.
- 4) Use SELECT DISK command to select the SD card disk e.g. SELECT DISK 3.
- 5) Double check the correct disk is selected by using the **LIST DISK** command again. The selected disk should have * character in front of it. This step is very important as the wrong selection could result in corruption and data loss of other drives.
- 6) Use CLEAN command to clear all the information off the disk (all data will be lost).
- 7) Use CREATE PARTITION PRIMARY command to create a new partition.
- 8) Select the partition using **SELECT PARTITION 1**.
- 9) Shrink the partition by the required amount where the size is specified in Megabytes e.g. to shrink by 500MB use **SHRINK DESIRED=500**.
- 10) Format the partition as required e.g. **FORMAT fs=NTFS QUICK** (skip this step if the type is already NTFS).
- 11) Use **FILESYSTEM** command to list properties of drive if desired.
- 12) Use EXIT command to quit the diskpart tool.
- 13) Copy files onto the SD card from the backup, if necessary.

Every time new data is written to the microSD card the old data is erased, so only one "file" can be on the card's non-partitioned area at a time.

The microSD card data is in decimal format with I and Q values on the same line, separated by a comma.



Figure 9: Example of microSD Card IQ Data Format

6.2 Rx Channel Operation

Signal flow for Rx channel operation is:

EV9830 Rx input -> CMX983 ADC -> CMX983 Rx Serial Port -> HB9830 -> PE0003 microSD card

EV9830 Rx inputs can be single-ended or differential. Considerations include the following:

- Single-ended inputs -> Ensure signal source has 50ohm output impedance and inputs are biased at 0V. Ensure jumpers are installed on RX I/Q header (J12, 1-2, 3-4, 7-8, 9-10).
- Differential inputs -> Remove jumpers on RX I/Q header (J12). Ensure inputs are biased at AV_{DD}/2.

The maximum CMX983 ADC input amplitude, after internal gain, is 20%-80% AV_{DD}. For Vbias=1.65V (AV_{DD}=3.3V) and with 0dB CMX983 internal gain, this translates to:

- Single-ended: 0.99V_{PP}, centered on 0V. (EV9830 single-ended input signal path provides +6dB of gain.)
- Differential: +/-0.99 V_{PP} on each of IRXP, IRXN, QRXP, and QRXN, centered on $AV_{DD}/2$.

Click "Rx Channel" GUI tab, make the following selections, and click "Write Rx" to activate CMX983 Rx ADCs at 75ks/s sample rate:

C-BUS Control FraceN 1 FraceN 2 RX Channel Tx Channel RX Fx Pots Sort Hander Othermal Figure Figure	ES9830 Evaluation Kit Software PE0003 Name	
Auto Load Filter	ES930 Evolution Kit Software PE0003 Name C-BUS Cotrol Frac-N 1 Frac-N 2 Fx Channel Tx Cha Fx Channel Frac-N 1 Frac-N 2 Fx Channel Tx Cha O'hannel Frac-N 1 Frac-N 2 Fx Channel Tx Cha Fan A [048 •] Invert A O'hannel Frac-N 1 Frac-N 2 Fx Channel Tx Cha Fan A [048 •] Invert A O'hannel Frac-N 1 Frac-N 2 Fx Channel Tx Cha Fan B [048 •] Invert A Sinc Rine Tx Cha Sinc Rin 32 B Ind Beel T7 Atta Beel 17 Ver Phase A 0 FIR Filter TX Atta Beel 17 Ver Phase A 0 CAL T Tx Atta Beel 77 Ka/s RAURINGTION GHR RX_CONIGS1F) 08 RX_VINPUT[0310) GHR RX_CONIGS1F) 08 RXPORT_CONIG400 64 RX_CONIG520 1220 RXPORT_CONIG411 18 RX_CONIGS212 2001	TX
	Auto Load Filter	Write Rx Save State Load State Options Close

Figure 10: Rx ADC Configuration

The following figure illustrates how to capture CMX983 ADC output to PE0003 microSD card:

ES9830 Evaluation Kit Software	
CBUS Control Frace N 1 Frace N 2 Rk Channel Tx Chan Rk Pot Number of Samples 500000 Enable Rk Inou Trigger (PE0003 GPI00) Receive Re PC File	Net Re/Tk Potr Soge Header RECEIVE (1) Enter desired number of samples (2) Click "Receive" to start signal capture (3) Select PC storage location (4) Save file to PC
	Save State Load State Options Oose

Figure 11: Signal Capture Process

6.3 Tx Channel Operation

Signal flow for Tx channel operation is:

PE0003 microSD card -> HB9830 -> CMX983 Tx Serial Port -> CMX983 Tx DAC -> EV9830 outputs

EV9830 Tx outputs can be single-ended or differential:

- Single-ended -> Outputs are biased at 0V with 50ohm output impedance. Ensure jumpers are installed on TX I/Q header (J7, 1-2, 3-4, 7-8, 9-10).
- Differential -> Remove jumpers on TX I/Q header (J7). Outputs are biased at AV_{dd}/2.

Click "Tx Channel" GUI tab, make the following selections, and click "Write Tx" to activate CMX983 Tx DACs at 75ks/s sample rate:

ES9830 Evaluation Kit Software PE0003 Name:TX	
C-BUS Control Frac-N 1 Frac-N 2 Rk Channel Tx Ohmmel Implify Bitable Implify A Brable Implify A Brable Implify Bitable Implify A Brable Implify A Brable FIR Filter Implify Implify A Brable Implify A Brable FIR R Coeff Implify Implify Implify A Brable Implify B Bitsel 0 A Brable 0 Implify Implify CT2 Tmplify Tmplify Ke/s Implify Implify	N Rx/Tx Parts Scopt Handler FIR Riter Load
Registers TX_CON0830} TX_CON0830 VBIAS_CON(\$10) 02 TX_CON18310 TX_CON2534 TX_CON2534	08 TXPORT_CON0(\$48) 04 0401 TXPORT_CON1(\$49) 0F 0605 Tx Port Freq 4800.00 kHz kHz
Sa	ve State Load State Options Close

Figure 12: Tx DAC Configuration

The following figure illustrates how to write data from the PE0003 microSD card to the CMX983 Tx DAC inputs:

ES9830 Evaluation Kit Software	
C-BUS Control Frac-N 1 Frac-N 2 Rx Channel Tx Ch	annel Rx/Tx Ports Script Handler
TRANSMIT (3) Enter desired number of samples	Tx Pot 500000 F Evable Tx Output Trgger (PE0003 GPI01)
(4) Click "Transmit" to start signal generation	Transmit
(1) Select PC file location	
(2) Load data to PE0003 SD card	Load
	Save State Load State Options Close

Figure 13: Signal Generation Process

6.4 Helpful Hints

Detailed PE0003 driver installation information can be found in the PE0003 User Manual. For Win7 and Win8 driver signing issues see the FAQ tab on the CML website's PE0003 Product page.

Keep a reasonable space between RF evaluation boards to avoid RF coupling issues.

Keep RF leads routed away from the boards and other RF sources when making precise measurements. This will avoid signal coupling affecting the results.

The PE0003 generates high spurious noise typical of high speed processors and this may be coupled into the RF circuits. While every care has been taken to avoid issues, optimum performance will be achieved with a production design that includes overall shielding and consideration of the layout with respect to the processor speed and proximity.

Please contact CML Technical Support if you have any questions or require further assistance.

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