CML Microcircuits

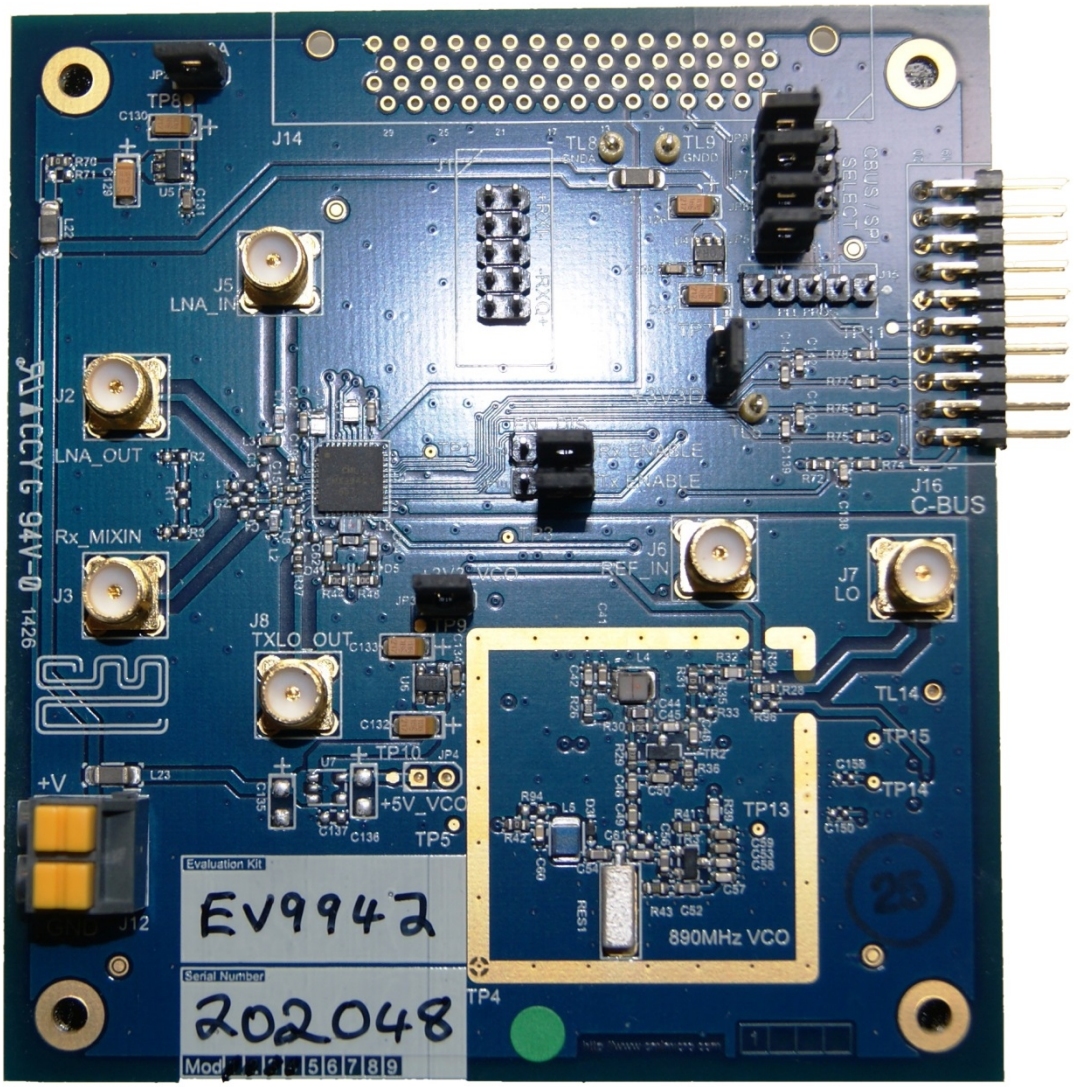
COMMUNICATION SEMICONDUCTORS

EV9942/EV9942A/ EV9942E Evaluation Kit User Manual

UM9942/5 September 2015 Provisional Issue

Features

- CMX994 Evaluation
- Receiver:
  - LNA
  - I/Q Output
  - Selectable Filters
- Transmit LO Output
- Integer-N PLL
- 19.2MHz VCTCXO
- Flexible External VCO on PCB
- On-board Voltage Regulators
- PC Control Interface Available
- Interfaces to PE0601, EV9810 or EV9100 Evaluation Kits
- 448MHz Default Operation
- 100MHz to 940MHz (1000MHz for CMX994A /CMX994E)



1. Brief Description

The EV9942/EV9942A/EV9942E allows the user to investigate all aspects of the CMX994 integrated circuit, which implements a high-performance direct conversion receiver. The evaluation kit also includes additional circuits that may be used to evaluate system performance, a high-frequency VCO and an optional Fractional-N PLL.

Access is provided to all CMX994 RF, baseband and control signals by either connector or test points. Test access points are available to accept common test equipment's, such as RF and baseband signal generators and spectrum analysers. All signal paths are matched by suitable components. The overall frequency range of this evaluation kit is for RF frequencies between 100MHz and 940MHz, with default operation at 448MHz.

The CMX994 is controlled via its C-BUS serial interface. The PE0003 Interface Card is available separately to support PC-based control of the EV9942/EV9942A/EV9942E. The PE0003 uses **ES9942xx.exe** PC software, part of the **ES9942xx.zip** file, which is available from the CML website.

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It is recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

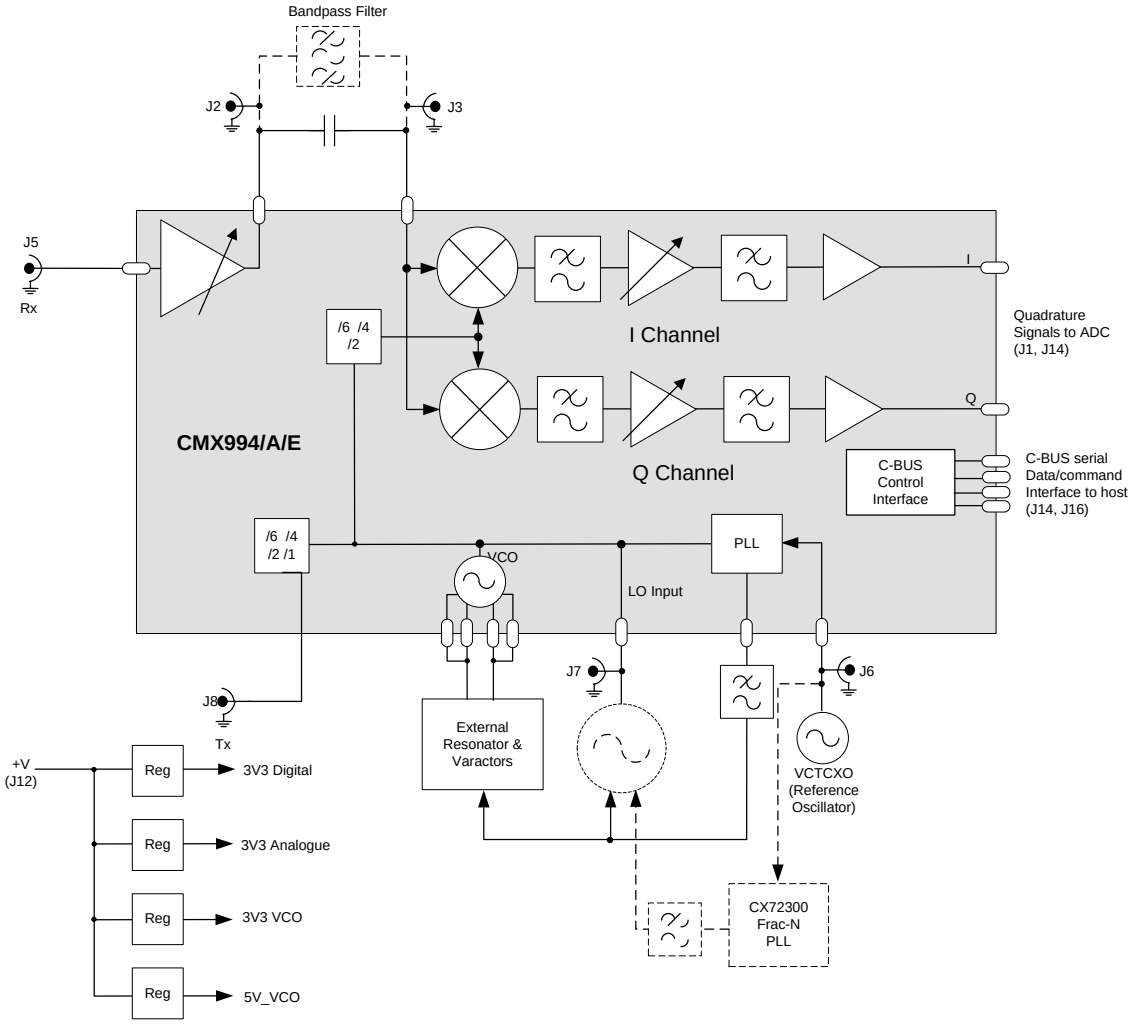

Figure 1 Block Diagram

2. Preliminary Information

The EV9942/EV9942A/EV9942E provides a platform for evaluation of the CMX994/CMX994A/CMX994E integrated circuits. The EV9942 provides a platform for evaluation of the CMX994 integrated circuit, the EV9942A provides a platform for evaluation of the CMX994A integrated circuit and the EV9942E provides a platform for evaluation of the CMX994E integrated circuit.

To use the EV9942/EV9942A/EV9942E a PC interface or micro-controller is required to control the CMX994/CMX994A/CMX994E via its C-BUS interface. This controller is not part of the EV9942/EV9942A/EV9942E kit. A separate CML product (PE0003) is available which provides the controller functionality and interfaces to a standard PC by means of a USB cable.

A PC application is available for C-BUS communication, **ES9942xx.exe**.

Glossary

ACR	Adjacent Channel Rejection
ADC	Analogue to Digital Converter
B/B	Baseband
BER	Bit Error Rate
C-BUS	4-Wire control interface, see CMX994 datasheet
CW	Continuous Wave
DAC	Digital to Analogue Converter
LNA	Low Noise Amplifier
LO	Local Oscillator
NF	Not Fitted
PC	Personal Computer
PCB	Printed Circuit Board
PER	Packet Error Rate
PLL	Phase Locked Loop
RF	Radio Frequency
Rx	Receiver
TBD	To Be Decided
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Controlled, Temperature Controlled Xtal Oscillator
VGA	Variable Gain Amplifier

2.1. Laboratory Equipment

The following laboratory equipment is recommended for use with this evaluation kit:

- Power Supply (Dual Power Supply if using PE0003)
- RF Signal Generator(s) (100MHz to 2GHz)
- RF Spectrum Analyser (up to 1GHz)
- Oscilloscope
- Personal Computer + PE0003 or other C-BUS microcontroller

For more detailed design or investigation work, other RF test equipment may be required.

2.2. Power Supply

The supply input voltage to the PCB is 7.2V (5.25V to 8V acceptable). On-board regulators are provided to generate all voltage rails used on the PCB (3.3V and 5V rails are used). The 7.2V supply should be rated at 1A.

NOTE:

1. **Care should be exercised with the power supplies, as they are not protected for reverse polarity.**
2. **When using the EV9942/EV9942A/EV9942E kit with a PE0003 kit, power is not supplied to the PE0003 via the C-BUS connector (J16). The PE0003 must be connected to a separate +5V regulated power supply.**

2.3. Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation:

2.3.1. Static Protection

This product uses circuits that can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

2.3.2. Contents - Unpacking

Please ensure that you have received all the items on the separate information sheet (EK9942??) and notify CML within seven working days if the delivery is incomplete.

2.4. Approvals

This evaluation kit is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements which may apply to this product and the radio frequency signals that may emanate from it.

3. Quick Start

This section provides instructions, in three steps, for users who wish to experiment immediately with the evaluation kit at 448MHz. This is the default frequency of the kit's hardware configuration. A more complete description of the kit and its uses appears later in this document. The EV9942/EV9942A/EV9942E includes a CMX994/CMX994A/CMX994E integrated circuit**.** Accordingly, before using the EV9942/EV9942A/EV9942E, the user should read the current CMX994/CMX994A/CMX994E datasheet.

This Quick Start configuration assumes the user has a CML PE0003 Evaluation Kit Interface Card available and that the PE0003 provides the interface between EV9942/EV9942A/EV9942E and a controlling PC.

3.1. First – Initial Setup

3.1.1. Make External Connections and Apply Power

Perform the following steps in sequence:

1. Connect test leads as shown below in Figure 2.
2. Connect a controller to C-BUS interface J16 (PE0003 can be used – see Figure 3. Note: J3 or J5 can be used on PE0003, but ensure the correct C-BUS port is selected when programming data: Figure 3 shows PCB connected using port 2).
3. Install PE0003 hardware/software and apply power to PE0003 – see section 3.1.2
4. If not already applied, power should be provided to the main EV9942/EV9942A/EV9942E supply (7.2V nominal).

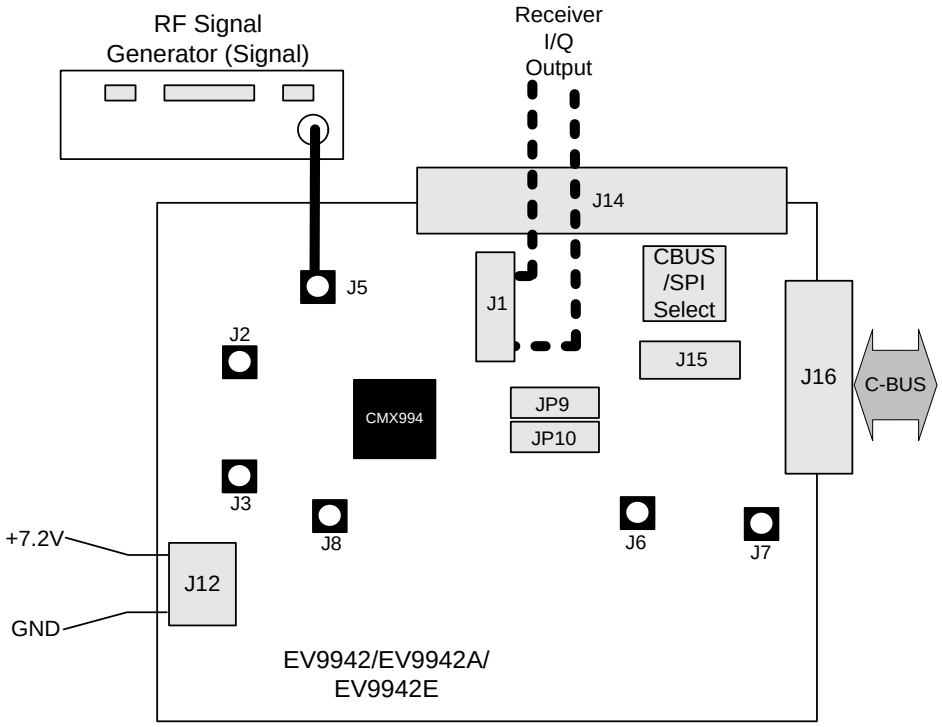

Figure 2 Typical Evaluation Connections for EV9942/EV9942A/EV9942E

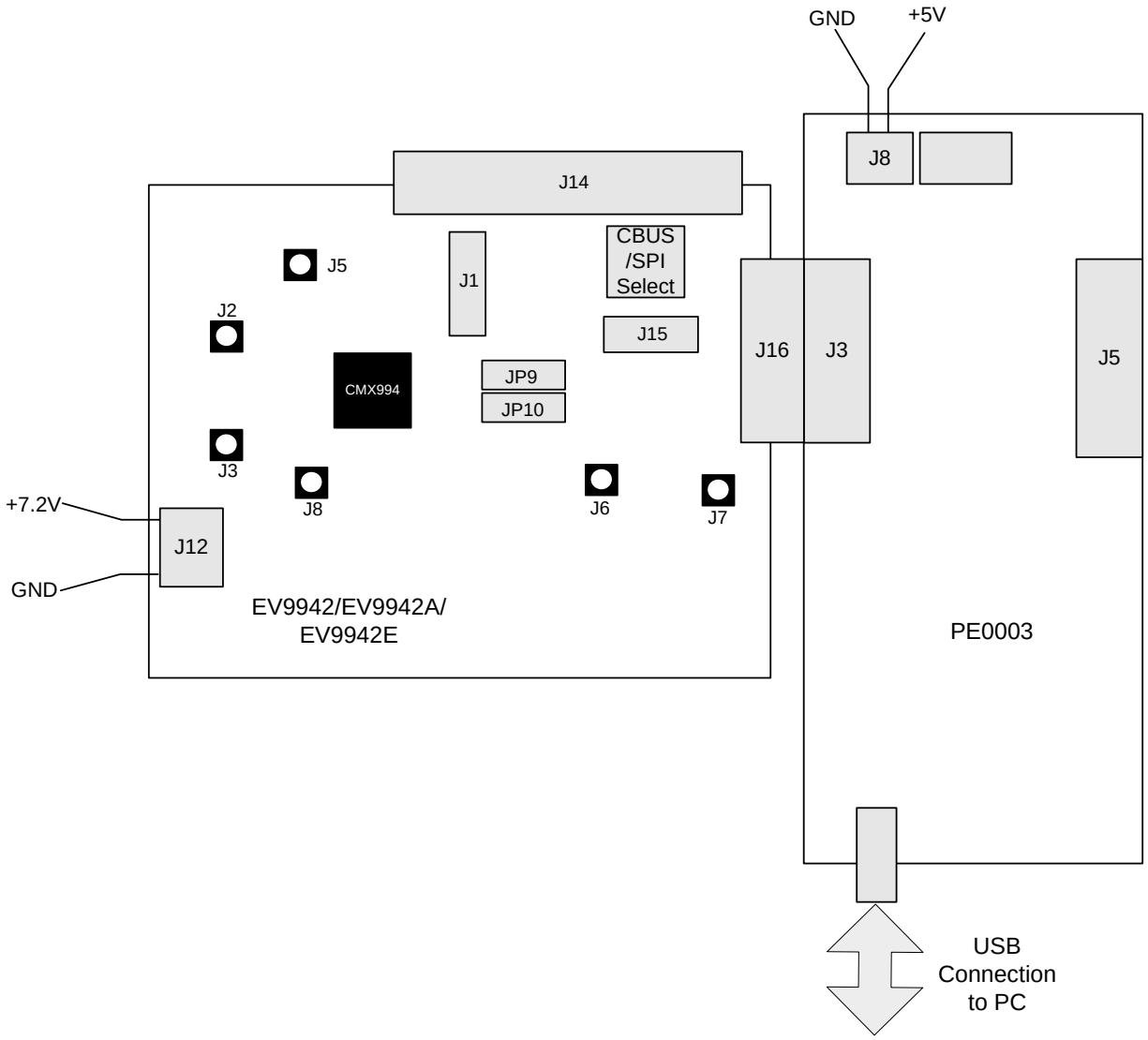

Figure 3 EV9942/EV9942A/EV9942E Connection to PC Using PE0003

3.1.2. Hardware/Software Installation (for PE0003)

- Copy the file '**ES9942xx.zip**', which is downloaded from the CML website following registration, to the hard drive of your host PC.
- Extract the files to the hard drive of your host PC.
- Connect a 5V dc supply to the PE0003 Interface.
- Connect a 7.2V dc supply to the EV9942/EV9942A/EV9942E.
- Attach a USB cable from connector J2 of the PE0003 Interface Card to the PC USB port.
- Turn on the power supply to the PE0003. The PE0003 power-on indicator D8 will light.
- Install the USB driver when requested. The driver is in the same folder where the '**ES9942xx.zip**' files were extracted to, in directory '.\Driver'. Follow instructions on the screen to install the USB driver. Click 'Install this driver software anyway' when the Message Box in Figure 4 is shown.

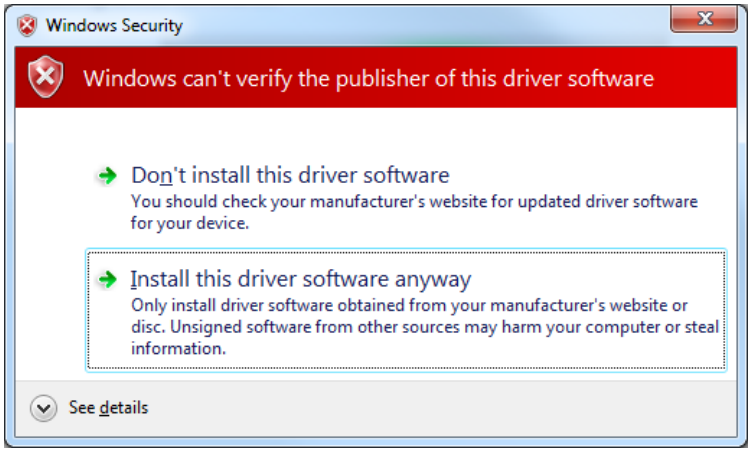

Figure 4 USB Driver Installation Message Box

3.2. Second – Configure

In this second step the EV9942/EV9942A/EV9942E is configured for Rx operation at 448MHz input frequency.

3.2.1. EV9942/EV9942A/EV9942E Configuration

The following steps should be undertaken to configure the EV9942/EV9942A/EV9942E to receive at 448MHz with an I/Q output. Set the applied signals and register values as shown in the following table.

Note: Setting the CMX994/CMX994A/CMX994E registers requires the use of the PE0003 host connected as above. The CMX994/CMX994A/CMX994E datasheet give details of the registers and commands.

Signal or Register	Setting	Note
LNA_IN (J5)	448.001MHz	The input level here may be user defined: for example an input signal of –60dBm at J5 the typical single-ended output level would be ~440mVp-p at J1 pin 2. The output should be 1kHz sine and cosine waves on I and Q when the configuration in this table is completed.
General Reset register ($10)	To ensure the device and hardware are in known states issue the General Reset command	Use RESET script, see section 6.3 for details.
General Control register ($11)	The General Control register should be set to enable the following: • Bias generator • PLL • Rx	Write $86 to register $11. The value $84 may be used if the RXEN pin is used to enable the CMX994.
VCO Control register ($25)	Enable the LO input [b4]	Write $10 to register $25.

Signal or Register	Setting	Note
Rx Control register ($12)	Select the LO/2 mode and enable the following: • Rx Mixer and divider • LNA • B/B Differential Amps and filters The filter bandwidth is selected in this register [b4 and b3].	Write $10 to register $12, this enables LO divide by 2 mode, all Rx Circuits on and maximum filter bandwidth.
Rx Offset register ($13) (or Extended Rx Offset ($17) for CMX994A/ CMX994E)	The value written to this register will vary between devices. A good starting point is $88.	Write $88 to register $13 and then check the dc levels on J1 (I and Q) to ensure the voltage difference between the differential pins of both I and Q channels is less than 25mV; adjust the value written to $13 as required.
Rx Gain register ($16)	Set Rx Gain to maximum.	Write $00 to register $16.
LNA IM Control register ($14)	For optimal IMD performance a value of $3F is recommended.	Write $3F to register $14. The value written to this register can be adjusted to give the optimal IMD performance.
PLL M Divider registers ($20-22) and R divider register ($23-24)	Enable the following: • Charge pump • PLL The default settings for the LO are as follows: • Required frequency = 896MHz • Comp frequency = 12.5kHz • Ref frequency = 19.2MHz	The default values would be M = 71680 and R = 1536. Write the following to the relevant register (note that the divider values are updated when register $22 is written so $20 and $21 need to be written first, therefore $23 needs to be written before $24); $22 = $A1, $21 = $18 and $20 = $00 $24 = $06 and $23 = $00 Note: If an external LO is to be used (see 6.2.3) the PLL circuitry (b2 in register $11) and the NR amplifier (b1 in register $25) should be disabled. The LO Input(b4 in register $25) should be enabled.
RXI/Q (J1)	Rx I/Q output.	The differential I and Q signals can be taken from J1.

3.3. Third – Operate

Following the configuration procedures given in sections 3.1 and 3.2, the EV9942/EV9942A/EV9942E should be operating as a receiver at 448MHz. Various evaluation tests can now be performed.

4. Signal Lists

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1	1, 3, 7, 9	NC	Baseband	Not connected
J1	2	RXI+	Baseband	I channel positive output
J1	4	RXI-	Baseband	I channel negative output
J1	5, 6	GNDA	DC	Ground (analogue)
J1	8	RXQ-	Baseband	Q channel negative output
J1	10	RXQ+	Baseband	Q channel positive output
J2	N/A	LNA_OUT	RF	Test connector to observe LNA output. To use this connector C7 must be fitted; C1 and C15 not fitted.
J3	N/A	Rx_MIXIN	RF	Test connector to allow direct input to the I/Q down-converter mixers (no LNA). To use this connector C8 must be fitted; C2 and C15 not fitted.
J5	N/A	LNA_IN	RF	LNA input
J6	N/A	REFIN	RF	Input for external reference source for PLL. To use this input C34 needs to be fitted to the PCB and C31, R16 removed.
J7	N/A	LO	RF	Main LO input or external VCO output
J8	N/A	TXLO_OUT	RF	Tx LO Output
J12	2	+V	DC	7.2V power supply input
J12	1	GND	DC	Power supply ground
J14	1 – 62			See Table 3
J15	1, 5	GNDD	DC	Ground (digital)
J15	2	RF_MOSI	Logic	Data input for PLL programming interface
J15	3	RF_SCLK	Logic	Clock for PLL programming interface
J15	4	RF_CSN	Logic	Latch/Enable for PLL programming interface
J16	1 – 20	C-BUS Interface	Logic	C-BUS interface from PE0003 or host controller. See schematics, CMX994/CMX994A/CMX994E Datasheet and Table 2 for details.

Table 1 Signal List

CONNECTOR PINOUT for J16			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
1	RESETN	I/P	General RESET (RESET active low)
2	CSN	I/P	C-BUS Enable.
3	-	-	Spare pin. Leave unconnected.
4	CDATA	I/P	C-BUS Data Input.
5	-	-	Spare pin. Leave unconnected.
6	SCLK	I/P	C-BUS Clock.
7	-	-	Spare pin. Leave unconnected.
8	RDATA	O/P	C-BUS Data Output.
9	-	-	Spare pin. Leave unconnected.
10	IRQN	I/P	Interrupt request - if required. Not used, so remains unconnected on EV9942/EV9942A/EV9942E.
11	GNDD	Power	Connection to Digital Ground.
12	GNDD	Power	Connection to Digital Ground.
13	-	-	Spare pin. Leave unconnected.
14	-	-	Spare pin. Leave unconnected.
15	-	-	Spare pin. Leave unconnected.
16	-	-	Spare pin. Leave unconnected.
17	-	-	Spare pin. Leave unconnected.
18	-	-	Spare pin. Leave unconnected.
19	-	-	Spare pin. Leave unconnected.
20	-	-	Spare pin. Leave unconnected.

Table 2 C-BUS Interface

Notes: I/P = Input
O/P = Output

CONNECTOR PINOUT for J14			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
1	RF_MOSI	I/P	Data input for PLL programming interface
2	RF_SCLK	I/P	Clock for PLL programming interface
3	MOSI	I/P	SPI Command Data (Master Out Slave In)
4	MISO	O/P	SPI Read Data (Master In Slave Out)
5	GNDD	GND	Digital ground
6	GPIO13	I/P	Not connected
7	SSOUT	I/P	SPI Chip Select
8	GNDD	GND	Digital ground
9	GPIO11	I/P	Not connected
10	GNDD	GND	Digital ground
11	NC	-	Not used on EV9942/EV9942A/EV9942E – do not connect to this pin
12	+V_EXT	I/P	+5V (nominal) power (not used on EV9942/EV9942A/EV9942E)
13	+V_EXT	I/P	+5V (nominal) power (not used on EV9942/EV9942A/EV9942E)
14	GNDA	GND	Analogue ground
15	19M2_TCXO	BI	19.2MHz VCTCXO input (To use, fit C36 and R79. Do not fit C31 and R16)
16	AUXDAC0	I/P	Not connected
17	AUXDAC2	I/P	Not connected
18	GNDA	GND	Analogue ground
19	AUXADC3	O/P	Not connected
20	AUXADC1	O/P	Not connected
21	GNDA	GND	Analogue ground
22	IP1	O/P	Not connected
23	IP2	O/P	Not connected
24	SPKR_2_OP	O/P	Not connected
25	MOD1P	I/P	Not connected
26	MOD1N	I/P	Not connected
27	EXT_VBIAS	I/P	Not connected
28	NC	-	Not connected
29	MOD2P	I/P	Not connected
30	MOD2N	I/P	Not connected
31	GNDA	GND	Analogue ground
32	J14_RXI+	O/P	Rx I channel positive output

CONNECTOR PINOUT for J14 (cont'd)			
Connector Pin No.	**Signal Name**	**Signal Type**	**Description**
33	J14_RXI-	O/P	Rx I channel negative output
34	GNDA	GND	Analogue ground
35	GNDA	GND	Analogue ground
36	GNDA	GND	Analogue ground
37	GNDA	GND	Analogue ground
38	J14_RXQ+	O/P	Rx Q channel positive output
39	J14_RXQ-	O/P	Rx Q channel negative output
40	GNDA	GND	Analogue ground
41	AUXADC0	O/P	Not connected
42	AUXADC2	O/P	Not connected
43	GNDA	GND	Analogue ground
44	AUXDAC3	I/P	Not connected
45	AFC	I/P	AFC input (AUXDAC1)
46	GNDA	GND	Analogue ground
47	GNDA	GND	Analogue ground
48	GNDA	GND	Analogue ground
49	+V_EXT	I/P	+5V (nominal) power (not used on EV9942/EV9942A/EV9942E)
50	NC	-	Not used on EV9942/EV9942A/EV9942E – do not connect to this pin
51	GNDD	GND	Digital ground
52	GPIO10	I/P	Not used on EV9942/EV9942A/EV9942E – do not connect to this pin
53	GNDD	GND	Digital ground
54	RX_EN	I/P	GPIO4 – Rx Enable on the EV9942
55	TX_EN	I/P	GPIO0 – Rx Enable on the EV9942
56	GNDD	GND	Digital ground
57	GPIO5	I/P	Not connected
58	CLK/CLK0	I/P	SPI Clock
59	RF_CSN	I/P	Latch/Enable for PLL programming interface
60	GPIO1	-	Not connected
61	NC	-	Not connected
62	NC	-	Not connected

Table 3 Control Interface (Connector J14)

TEST LOOPS		
Test Loop Ref.	**Default Measurement**	**Description**
TL5	-	C-BUS Serial Data Input
TL8	0V	Analogue ground
TL9	0V	Digital ground
TL14	-	Optional serial ‘Mod_in’ data for the CX72300 PLL

Table 4 Test Loops

Notes:

I/P	=	Input
O/P	=	Output
BI	=	Bidirectional
TL	=	Test Loop
TP	=	Test Point

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP1	3.3V	VDDIO
TP3	-	AFC (Automatic Frequency Control) to VCTCXO, U2
TP4	0V	Analogue ground
TP5	-	PLL Loop filter output/VCO control voltage
TP7	3.3V	3.3V regulator output for digital circuits
TP8	3.3V	3.3V regulator output for analogue circuits
TP9	3.3V	3.3V regulator output for VCO/PLL circuits
TP10	5.0V	5.0V regulator output for VCO/PLL circuits
TP11	-	IRQN (C-BUS IRQN, not used on EV9942)
TP13	-	CX72300 (U8) PLL Loop filter output
TP14	-	CX72300 (U8) Lock Detect output pin
TP15	-	CX72300 (U8) 'Mux_Out' pin
TP16	-	IFLT1N Receiver post mixer monitoring point (I channel)
TP17	-	IFLT1P Receiver post mixer monitoring point (I channel)
TP18	-	QFLT1N Receiver post mixer monitoring point (Q channel)
TP19	-	QFLT1P Receiver post mixer monitoring point (Q channel)

Table 5 Test Points

JUMPERS/LINKS			
Link Ref.	**Positions**	**Default Position**	**Description**
JP1	1-2	1-2	Connects on-board regulator (1-2) or allows an external power supply to be connected (NF), +3V3D
JP2	1-2	1-2	Connects on-board regulator (1-2) or allows an external power supply to be connected (NF), +3V3A
JP3	1-2	1-2	Connects on-board regulator (1-2) or allows an external power supply to be connected (NF), +3V3_VCO
JP4	1-2	NF	Connects on-board regulator (1-2) or allows an external power supply to be connected (NF), +5V_VCO
JP5	1-2	NF	Selects SPI MISO from Host (1-2), if required
JP6	1-2/2-3	NF	Selects between SPI CSN (1-2) or PLL programming CSN (2-3)
JP7	1-2/2-3	NF	Selects between SPI CLK (1-2) or PLL programming CLK (2-3)
JP8	1-2/2-3	NF	Selects between SPI MOSI (1-2) or PLL programming MOSI (2-3)
JP9	1-2/2-3	2-3	Rx Enable, can select between +3V3D (1-2) and GNDD (2-3)
JP10	1-2/2-3	2-3	Tx Enable, can select between +3V3D (1-2) and GNDD (2-3)

Table 6 Jumper Links

5. Circuit Schematics and Board Layouts

For clarity, circuit schematics for each board variant are available as separate high-resolution files. These can be obtained via the CML website, files: '**DWG9942A04.pdf**', '**DWG9942AA01.pdf**'. and '**DWG9942EA01.pdf**'. By default, the CX72300 is not fitted. If the customer chooses to fit the CX72300, then it can be programmed via TL14 and J14. To do this, a wire link should be fitted on the PCB between R84/R85 and J14 pin 6.

The layout on each side of the PCB is shown in Figure 5 and Figure 6.

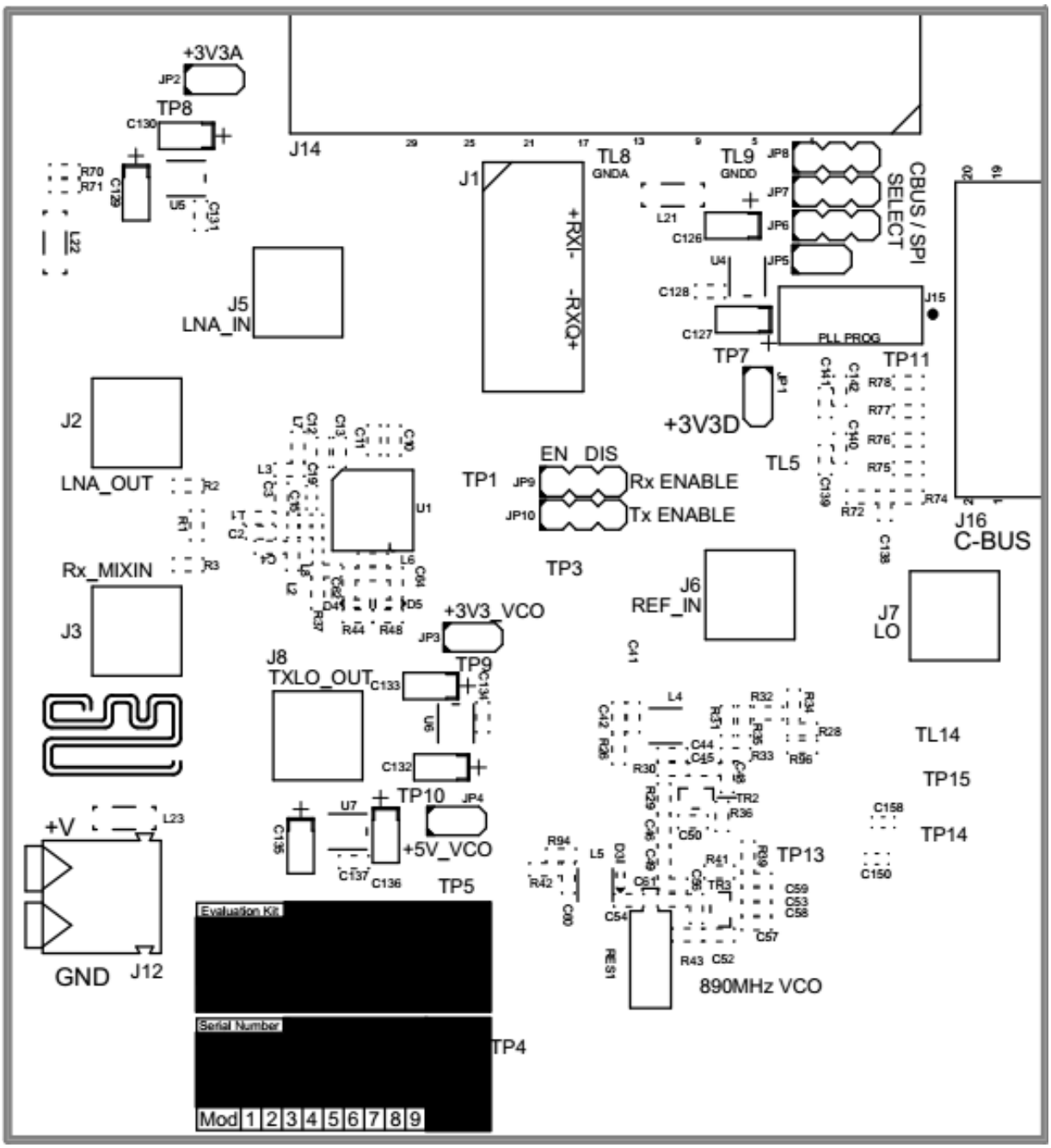

Figure 5 PCB Layout: top

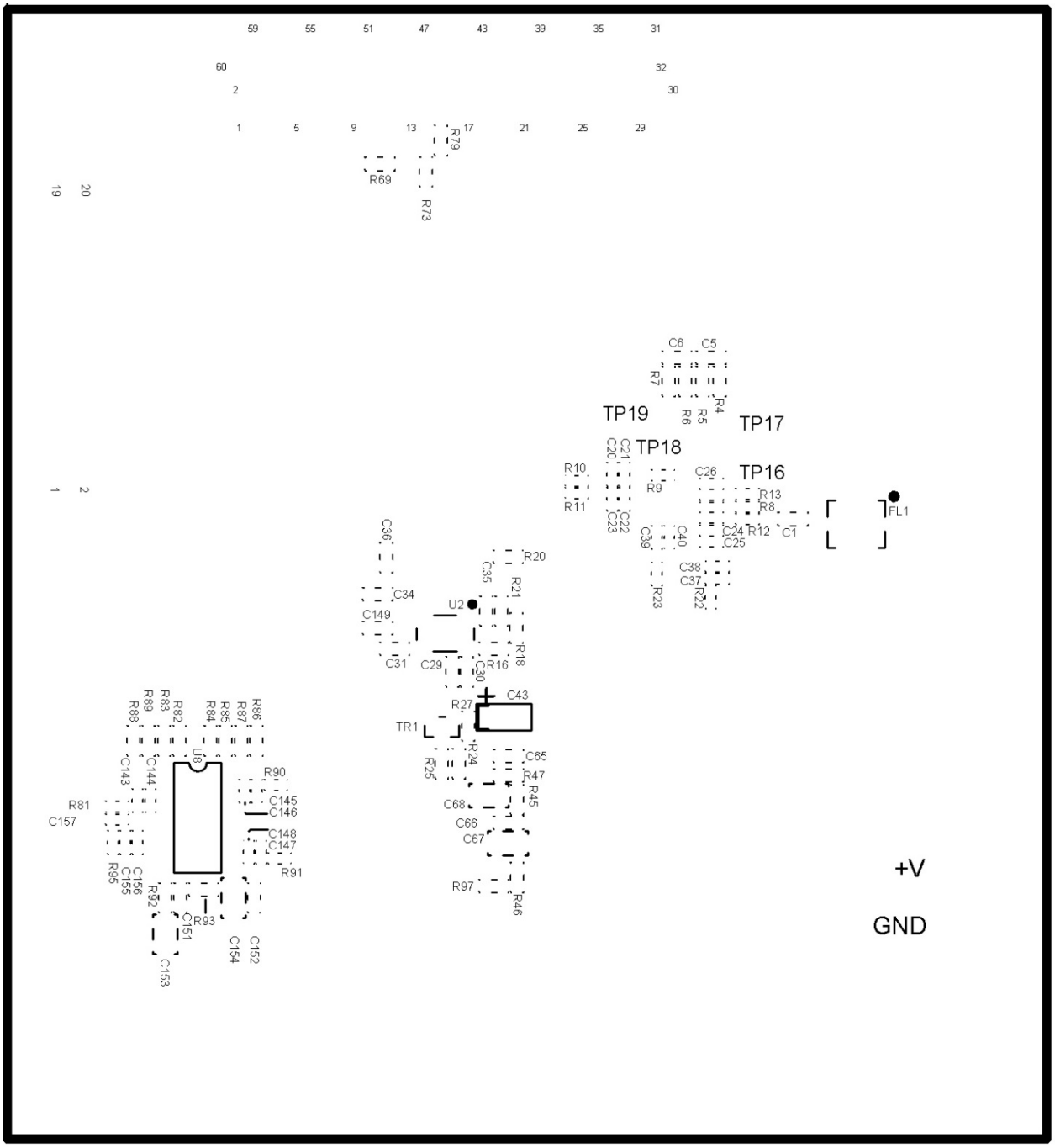

Figure 6 PCB Layout: bottom

6. Detailed Description

Refer to the CMX994/CMX994A/CMX994E datasheet for a detailed description of the device.

The EV9942/EV9942A/EV9942E functionality includes:

- Demonstration of a linear direct conversion receiver from RF input to output in I/Q format including:
    - LNA with gain control
    - I/Q mixers
    - first baseband filters
    - first baseband amplifiers
    - second baseband filters
    - second baseband amplifiers
- VCO, Integer-N PLL and divider.
- Tx LO Output.
- Operation 100MHz to 940MHz (448MHz = default configuration).
- 19.2MHz VCTCXO.
- On-board linear regulators for all necessary power rails.
- The C-BUS Interface that allows the card to be connected to a host µController. A PC Interface board is separately available and allows control of all device functions, to support initial test and customer evaluation.
- Interface to CMX7163 or CMX7164 evaluation boards (PE0601-7163 / PE0601-7164, not included) to allow demonstration/test of QAM and 2-FSK / 4-FSK demodulation.
- Interface to CMX910 evaluation card (EV9100, not included) to allow demonstration/test with GMSK demodulation.
- Interface to CMX981 evaluation card (EV9810, not included) allows demonstration of:
    - Linear receiver
    - Pi/4-DQPSK

In summary, the EV9942/EV9942A/EV9942E allows the user to create experiments to investigate all aspects of the CMX994 device. The EV9942/EV9942A/EV9942E is designed to allow user modification, to support the detailed investigation of the user's specific and different applications. The evaluation platform also includes additional circuits that may be used to evaluate system performance, for example a fractional-N PLL (U8) and a high-frequency VCO (TR2/TR3).

6.1. Hardware Description

6.1.1. Receiver

The EV9942/EV9942A/EV9942E demonstrates the CMX994/CMX994A/CMX994E advanced direct conversion receiver ICs, which are capable of supporting a range of digital radio systems of both constant envelope and linear modulation types. The applied input signal, typically applied at J5, will be amplified by the on-chip LNA. The output of the LNA may be either matched to the input of the I/Q down-conversion mixers by C7, L1, C15 and C8, or passed through an external filter FL1. Alternatively, the signal may be passed to test connector J2 for detailed LNA test and measurement purposes.

The I/Q down-conversion mixers can be accessed from test connector J3 or driven from the LNA, as previously described. The mixers convert the received signal to I/Q baseband format, where C10 and C12 combine with on-chip components to remove off-channel signals. The signal is then amplified before further filtering is provided to remove adjacent channel signals. A final amplifier stage completes the receiver line-up, providing differential I/Q outputs.

The typical performance of the CMX994 is that the overall receiver gain and noise figure for the default configuration is ~63dB and 4.5dB respectively. The Rx input third-order intercept point achieved is ~ -3dBm.

6.1.1.1. LNA

The CMX994/CMX994A/CMX994E includes a broadband LNA. The design has a single-ended input and output. This minimises cost and board area, as balun transformers are not required. The LNA can be evaluated using J5 (input) to J2 (output). The plots in Figure 7, 8 and Figure 9 are with the LNA input and output matched to 450MHz.

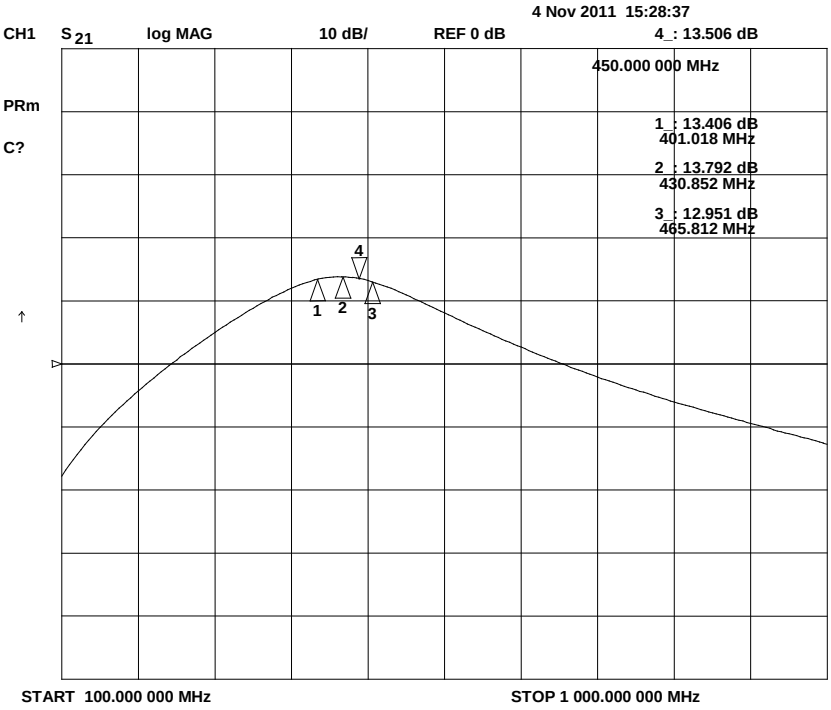

Figure 7 LNA S_{21} 400 – 465MHz

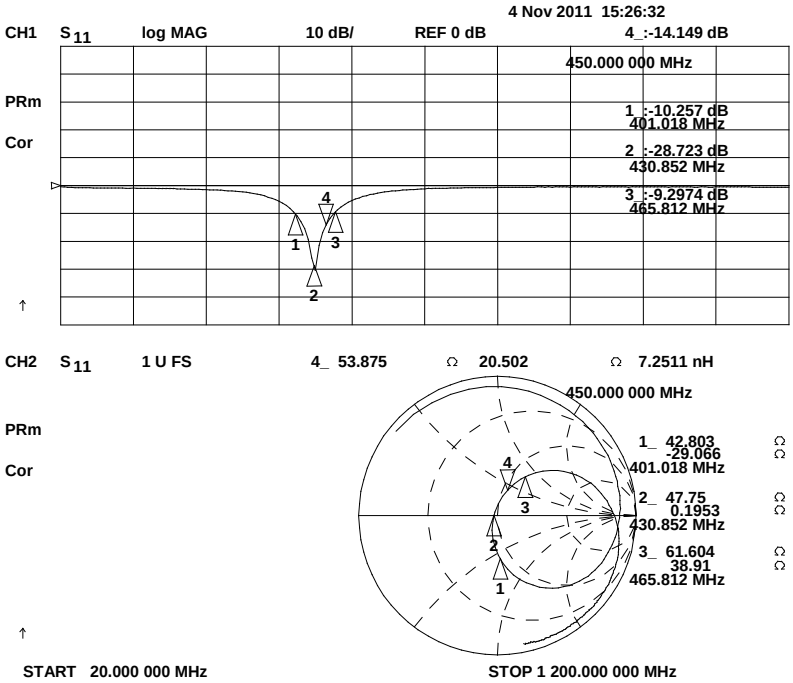

Figure 8 Typical LNA S_{11} response 400- 465MHz

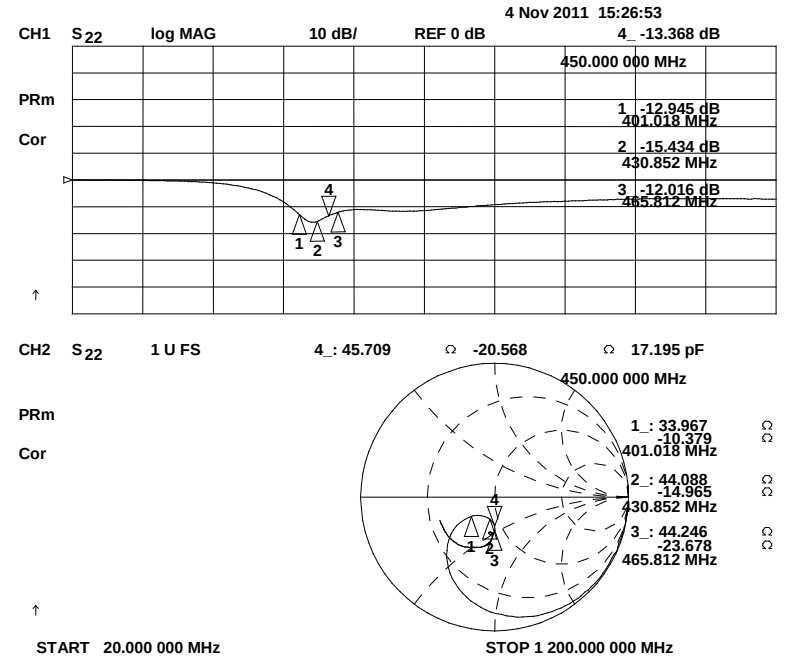

Figure 9 Typical LNA S_{22} response 400 – 465MHz

6.1.1.2. Rx Direct Conversion Mixers and Filtering

The Rx I/Q Mixers have a single-ended input with a nominal input frequency range of 100MHz to 940MHz for CMX994 or 100MHz to 1000MHz for CMX994A/E. If the mixer is connected to the LNA, a simple match is required at the default frequency of operation (448MHz) and different matches are required for other frequencies of operation, typical values for 150MHz are shown in Table 7 and typical values for 900MHz are shown in Table 8. The mixer has selectable LO input dividers: these are /2, /4 and /6.

The output of the I/Q mixers is baseband; the two capacitors (C10, C12) together with on-chip components determine the break point of a first stage of baseband filtering, intended to attenuate off-channel signals such as blockers and signals used in intermodulation testing.

After the filters, a variable gain amplifier is provided, followed by a further stage of filtering. Again, external capacitors (C11, C13) set the response of the filter. Resistor R9 is provided to act as a reference to ensure the accuracy of the filter response. For details of the filter configurations and how to adjust the values see the CMX994/CMX994A/CMX994E datasheet. The filter bandwidth can be scaled on a ratio of 1:2:4, typical results are shown in Figure 10, again see the CMX994/CMX994A/CMX994E datasheet for further details.

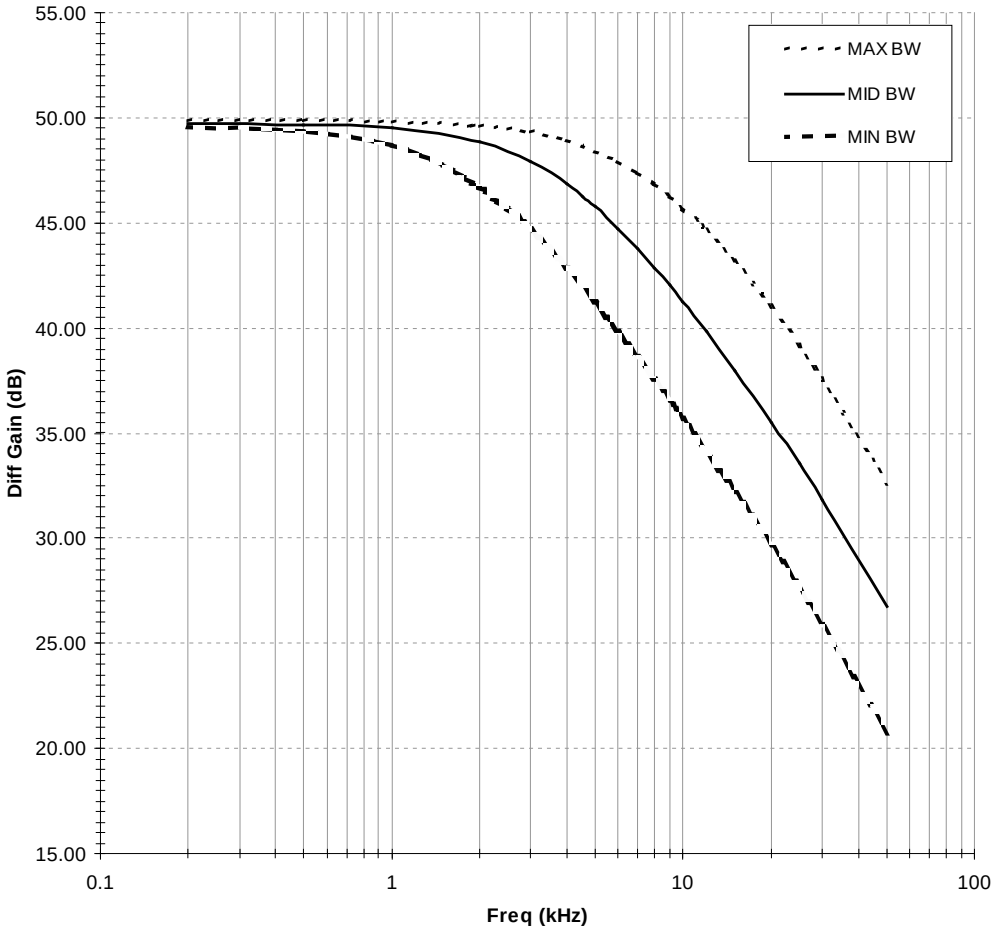

Figure 10 ACR Filter Response With Different Bandwidth Settings

The I/Q chain is completed by a final stage of amplification, which drives the differential output pins on the CMX994/CMX994A/CMX994E IC (RXIP, RXIN, RXQP, RXQN). These outputs are available on the EV9942/EV9942A/EV9942E board as RXI+, RXI-, RXQ+ and RXQ-.

6.1.1.3. DC Offset Correction

The EV9942/EV9942A/EV9942E does not provide direct compensation of DC offsets in the I/Q outputs from the receiver, however the CMX994/CMX994A/CMX994E does allow a coarse DC offset compensation to be applied to maximise receiver dynamic range; this assumes that the I/Q signals are measured externally to calculate the required compensation. See the CMX994/CMX994A/CMX994E datasheet for further details.

6.1.2. Local Oscillator (LO)

6.1.2.1. CMX994 VCO and PLL

The EV9942/EV9942A/EV9942E provides components to use the VCO amplifier and PLL contained within the CMX994/CMX994A/CMX994E IC. As supplied, the resonator circuit (L6, C63, C62, C64, D4, D5) is configured for 440MHz operation with a tuning sensitivity of approximately 20MHz/V. The component values used for the PLL loop filter provide a bandwidth of approximately 1kHz. The oscillator is usable up to about 1GHz, for further details consult the CMX994/CMX994A/CMX994E datasheet, see also section 6.2.3.

6.1.2.2. EV9942/EV9942A/EV9942E Alternative VCO

The EV9942/EV9942A/EV9942E PCB includes an external VCO (TR2/TR3) for improved phase noise operation. The external VCO uses a ceramic resonator (RES1) and is thus flexible in its operation. The default components give an operating frequency at around 896MHz, allowing operation of the IC at 448MHz when the Rx divider is in /2 mode. This VCO is connected to the CMX994/CMX994A/CMX994E LO input (LOP, pin 12). To allow testing at frequencies not directly supported by the VCOs on the PCB, an external LO signal may be applied to J7. If an external LO is used it is recommended that the on-chip and on-board VCOs are disabled (e.g. by ensuring R24 and R25 are not fitted).

6.1.2.3. EV9942/EV9942A/EV9942E Alternative PLL

Some CMX994/CMX994A/CMX994E applications may require a Fractional-N PLL, therefore to allow such evaluation a Skyworks SKY72300/CX72300 (Fractional-N Frequency Synthesiser) IC can be fitted at position U8.

6.1.2.4. Reference Oscillator

A 19.2MHz VCTCXO is fitted on the EV9942/EV9942A/EV9942E. An external reference oscillator applied to J6 may be used by fitting C34 with 1nF and removing C31 and R16. Alternatively, an external oscillator may be connected using J14, in which case C36 should be fitted as 1nF and C34, C31 and R16 should all be unfitted (NF).

6.1.3. Power Supply

The input to the PCB is nominally 7.2V (5.25V to 8V is acceptable). On board regulators are provided to generate voltage rails used on the EV9942/EV9942A/EV9942E.

6.2. Adjustments and Controls

The user has the facility to configure the EV9942/EV9942A/EV9942E for a number of different operational scenarios.

6.2.1. Operation on other Frequency Bands and Configurations

The default operating frequency is 448MHz. The following components (see Table 7) need to be changed at the LNA input and output to enable the EV9942/EV9942A/EV9942E receiver to operate at 150MHz as a complete chain. The LO input frequency will also need to be considered in order to operate at 150MHz. The 896MHz VCO (default) could still be used if the Rx divider is put into /6 mode (i.e.896MHz/6 = 149.33MHz), otherwise another LO source will need to be provided (for example the internal VCO could be used).

Ref. Designator	Values for 150MHz
L7	150nH
L3	2.7pF
C7	18pF
C15	0R
C8	1nF
L2	150nH

Table 7 Components for Complete Rx Chain Operation at 150MHz

In Table 8 are a set of values for operation at 900MHz, this involves value changes at the input and output of the LNA. Again consideration will have to be given to the LO source which will have to be provided from an external source and applied to J7, typically 1.8GHz at -10dBm. To allow J7 to be used it is recommended to power down the external VCO by not fitting R25, also R32 should be not fitted, R28 and R34 should be changed to 0R.

Ref. Designator	Values for 900MHz
L7	12nH
L3	8.7nH
C19	100pF
C7	4.7pF
C15	0R
C8	100pF
L2	5.6nH

Table 8 Components for Complete Rx Chain Operation at 900MHz

6.2.2. Rx I/Q Mixer Input Match (when using J3 input)

For test purposes it may be useful to connect directly to the I/Q down-conversion mixers. This can be done by using J3, the default values for C4 and L2 are for operation at 450MHz as a complete chain. To use J3 it is necessary to remove C15. The values shown in Table 9, Table 10 and Table 11 are for operation at 450MHz, 100MHz and 900MHz respectively. These values provide a match to 50 Ohms.

Ref. Designator	Values for 450MHz
C4	4.7pF
L2	18nH
C8	1nF

Table 9 Components for Direct Input to I/Q Mixer at 450MHz

Ref. Designator	Values for 100MHz
C4	22pF
L2	150nH
C2	1nF

Table 10 Components for Direct Input to I/Q Mixer at 100MHz

Ref. Designator	Values for 900MHz
C4	4.7pF
L2	5.6nH
C2	100pF

Table 11 Components for Direct Input to I/Q Mixer at 900MHz

6.2.3. Internal/External LO

The EV9942/EV9942A/EV9942E has four options for the Local Oscillator. The default configuration of the EV9942/EV9942A/EV9942E is to use the external VCO (TR3/TR2) along with the CMX994/CMX994A/CMX994E internal PLL. The second option is to use the CMX994/CMX994A/CMX994E internal VCO, this can be used for VHF applications in its default configuration. The third option for the EV9942/EV9942A/EV9942E is to apply an external LO using J7. The final option is to use the external VCO with the Fractional-N Synthesiser[1] (U8), see Table 13 for some typical values (also see section 5).

To use the CMX994/CMX994A/CMX994E internal VCO the following modifications (Table 12) are required. With this configuration the VCO should operate at circa 440MHz.

Ref. Designator	Values to use CMX994 VCO
D3 and D4	SMV1705-079LF[2] (as fitted)
L6	8.2nH (as fitted)
C63	8.2pF (as fitted)
C62 and C64	22pF (as fitted)
R46	0R
R42	NF
C65	150nF
C66	15nF
C68	1000nF
R45	2.4kΩ
R47	1.5kΩ

Table 12 Components for use CMX994/CMX994A/CMX994E VCO at 440MHz

To use the external LO connector (J7), R24 and R25 should not be fitted (NF), to disable the on-board external VCO. The CMX994/CMX994A/CMX994E VCO buffer and negative resistance amplifier should be disabled using the General Control Register or the VCO Control Register.

To use the internal VCO the external VCO should be disabled (R24 and R25 should not be fitted) and VCO Negative Resistance amplifier and VCO buffer enabled (e.g. VCO Control Register ($25) set to 0x03, see CMX994/CMX994A/CMX994E datasheet for details).

The LO input should be enabled when using an external source (e.g. VCO Control Register ($25) set to 0x10, see CMX994/CMX994A/CMX994E datasheet for details).

[1] SKY72300 (U8) is now obsolete (2015)
[2] JDV2S08S fitted to EV9942 with modification state 2 and below; this diode has been made obsolete by the manufacturer.

Ref. Designator	Values to use Frac N PLL and ext VCO
U8	SKY72300-21 (CX72300)
R81, R95, R90, R91	10R
C143, C146, C148,C156, C158	33pF
C144, C145, C147, C155	10nF
C157	100pF
C150	1nF
R82, R86, R94	0R
R88	4.7k
R89	10k
R93	1k
R92	360R
C152	6.8nF
C151	5.6nF
C153	330nF
R42, R34	DNF
R96	18R

Table 13 Components for use with External VCO and Skyworks Frac N PLL

6.3. PC Control Software

The EV9942/EV9942A/EV9942E itself does not require any embedded firmware, however, it does require C-BUS control from an external microcontroller. The CML product, PE0003, can be used with the EV9942/EV9942A/EV9942E and PC software files '**ES9942xx.zip**'. To use the software, connect the EV9942/EV9942A/EV9942E as shown in Figure 3. First ensure the drivers supplied for the PE0003 are installed correctly. The executable must be in the same folder on the PC as the '**EF0003xx.bin**' file. Run the '**ES9942xx.exe**' and the main application window will open with a progress bar for the initialisation process. Once the initialisation process is complete, the appropriate GUI for the EV9942, EV9942A or EV9942E will be automatically loaded and the first screen will be displayed. One of four tabs can be selected.

To perform a General Reset on the CMX994/CMX994A/CMX994E, a single write to register $10 is required. The following script, which may be used with the **ES9942xx** software, is recommended.

```
;General Reset.pes
;This script will send a C-BUS General reset.
;Reset C-BUS (assigns register RESET a zero length parameter to get a single 8-bit write)
;format: register <device (1 or 2)> <C-BUS address> <# parameter bytes (0 to 2)>

RESET const $10
        register 1 RESET 0
        copy 0 *RESET

;If using C-BUS port 2 then use the following lines
;       register 2 RESET 0
;       device 2
;       copy 0 *RESET
```

There are three tabs that represent a particular set of registers or a particular function of the CMX994/CMX994A/CMX994E. To select a tab simply click on the corresponding name in the row at the top of the program window. Setting or clearing the check box associated with a bit of a register will cause that bit to be set or cleared when the register is next written to. If the 'Auto

Write' check box is set a register will be written whenever a check box or list box associated with it is modified. This removes the need to click the 'Write' button associated with that register. The program can be closed at any time by clicking the 'Close' button or by pressing 'Alt' and 'F4' keys simultaneously.

Note: The C-BUS Control tab and Script Handler tab displays are the same for all three devices. Therefore a single screen shot has been included for these tabs. Separate screen shots are shown for the Reg 1 and Reg 2 tabs, to show the differences.

6.3.1. The C-BUS Control Tab

The C-BUS Tab allows the user to read from or write to any register plus issue a General Reset command, see Figure 11. Also on this tab, the Hardware Reset command can be issued and the C-BUS header to be used can be selected.

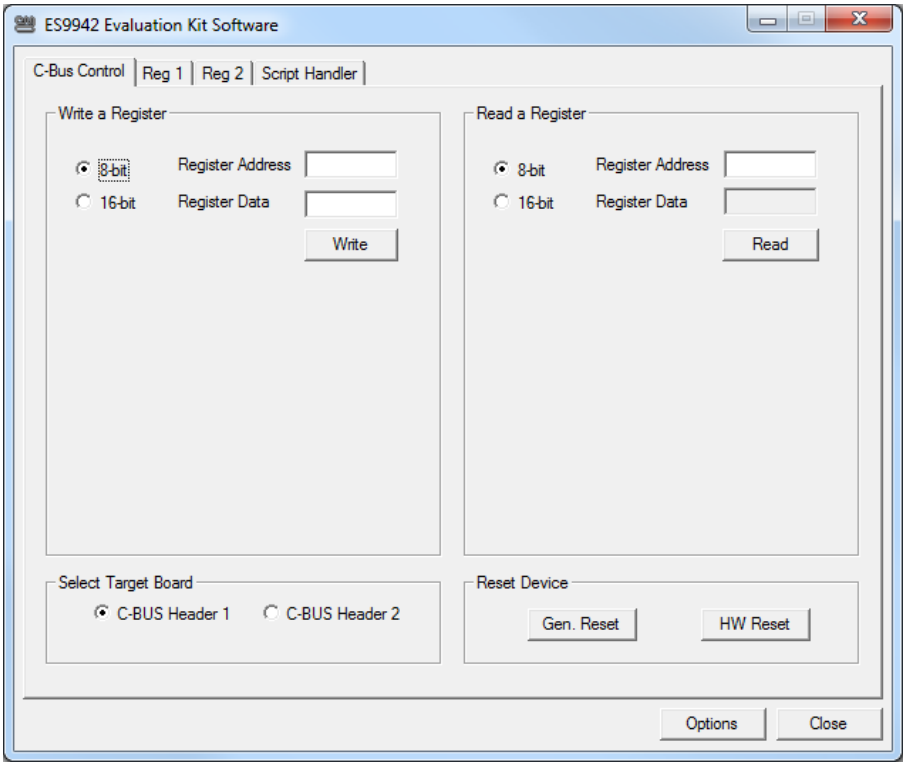

Figure 11 The C-BUS Control Tab (EV9942/EV9942A/EV9942E)

6.3.2. The Reg 1 Tab

The Reg 1 tab gives the user access to the General Control register, Rx Control register, Rx Offset register, Intermodulation Control register, the Rx Gain register plus the Extended Offset register and Options register on the EV9942A and EV9942E, see Figure 12 for the EV9942, Figure 13 for the EV9942A and Figure 14 for the EV9942E. All registers can be written to individually, or as a whole mass register write (Write All bottom left hand corner of window). If Auto Write is checked, the register is changed as the user makes changes to the register window.

In the case of the Rx Offset and Intermodulation registers, slide bars have been used to allow easy control during operation.

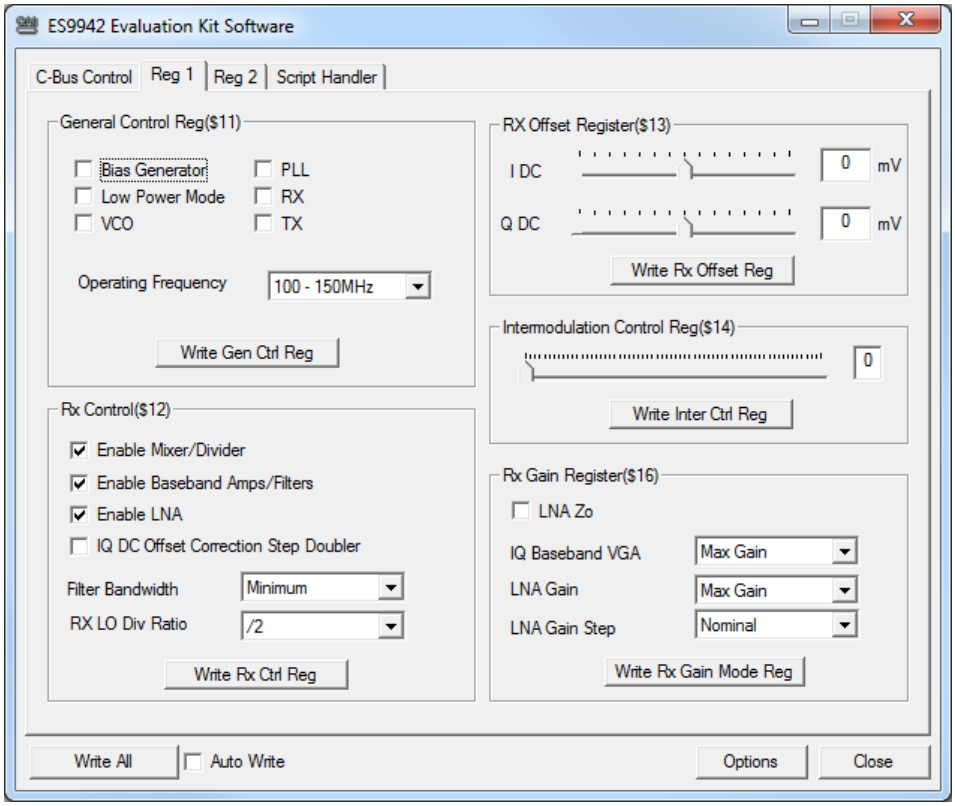

Figure 12 The Reg 1 Tab (EV9942)

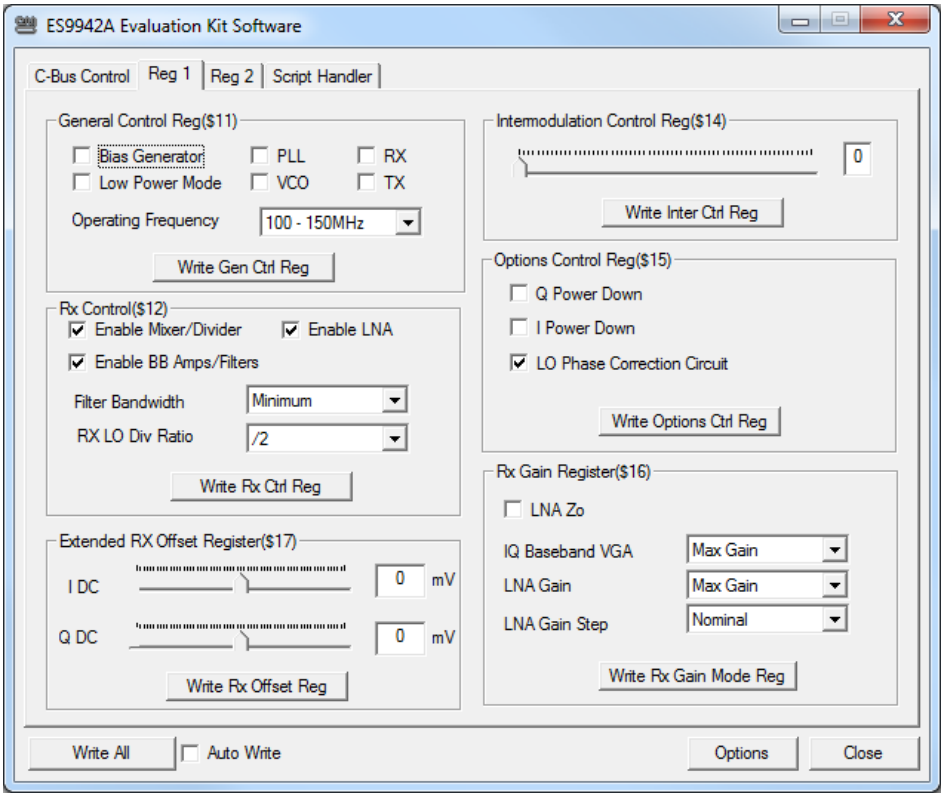

Figure 13 The Reg 1 Tab (EV9942A)

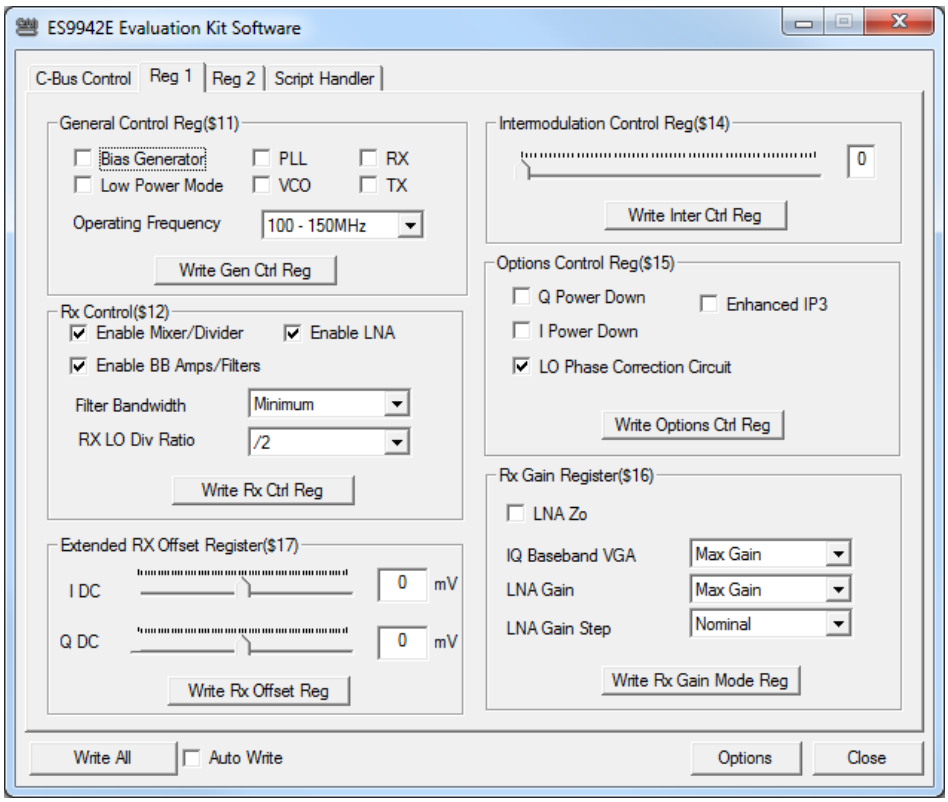

Figure 14 The Reg 1 Tab (EV9942E)

6.3.3. The Reg 2 Tab

The Reg 2 tab gives the user access to the PLL M/R Divider registers and the VCO Control register. All register states can be read with one button press, see Figure 15. All registers can be written to individually, or as a whole mass register write (Write All bottom left hand corner of window). If Auto Write is checked, the register is changed as the user makes changes to the register. See Figure 16 for the EV9942A and EV9942E. These have more read-back registers than the EV9942.

The PLL M/R Divider register window has a box which indicates the PLL lock detect states. The lock detect is read each time the PLL divider values are written and the status updated. The box will be blank to indicate PLL is out of lock and when the PLL is in lock the box will have an L in it, as shown in Figure 15.

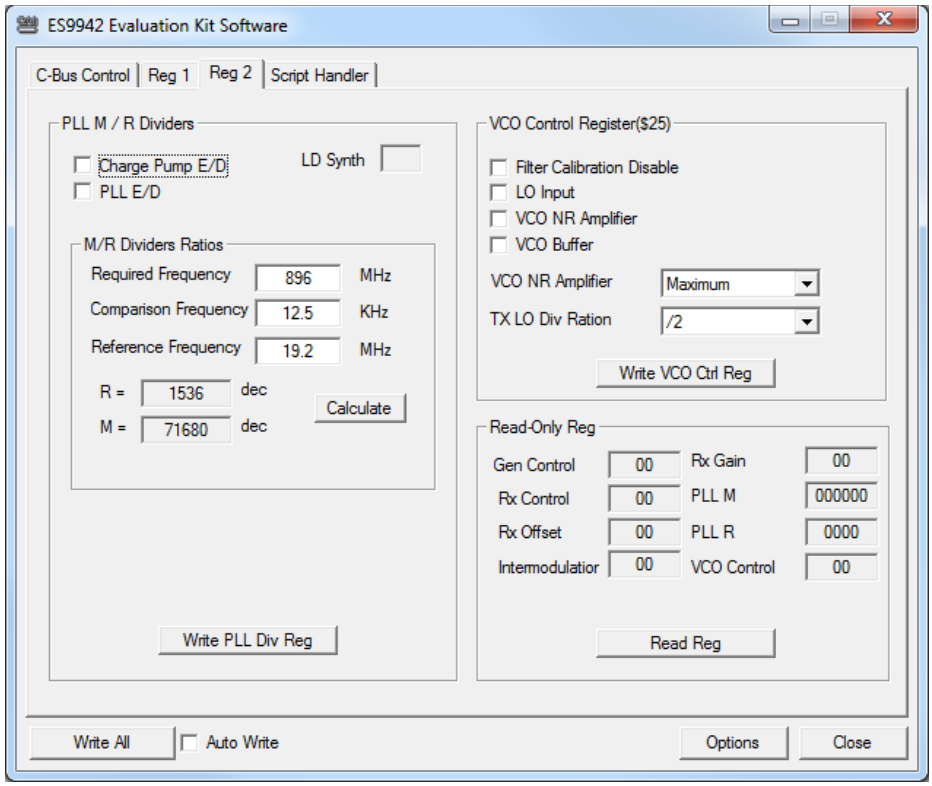

Figure 15 The Reg 2 Tab (EV9942)

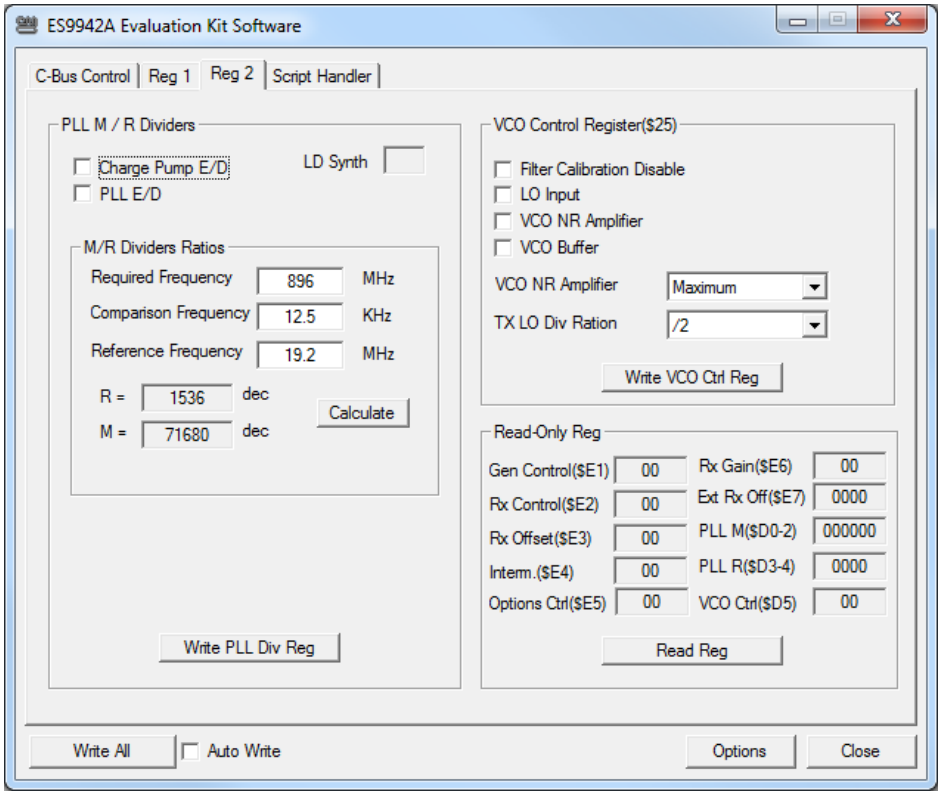

Figure 16 The Reg 2 Tab (EV9942A/EV9942E)

6.3.4. The Script Handler Tab

The Script Handler Tab (shown in Figure 17) allows the execution of script files consisting of register write, read, and delay commands. These are plain text files on the PC, which are compiled via the GUI but executed by the LPC4330 microprocessor on the PE0003 board. The script language is documented separately in the "Script Language Reference" document, which can be downloaded with the PE0003 support package from the CML website. Control of the EV9942 does not require the use of script files.

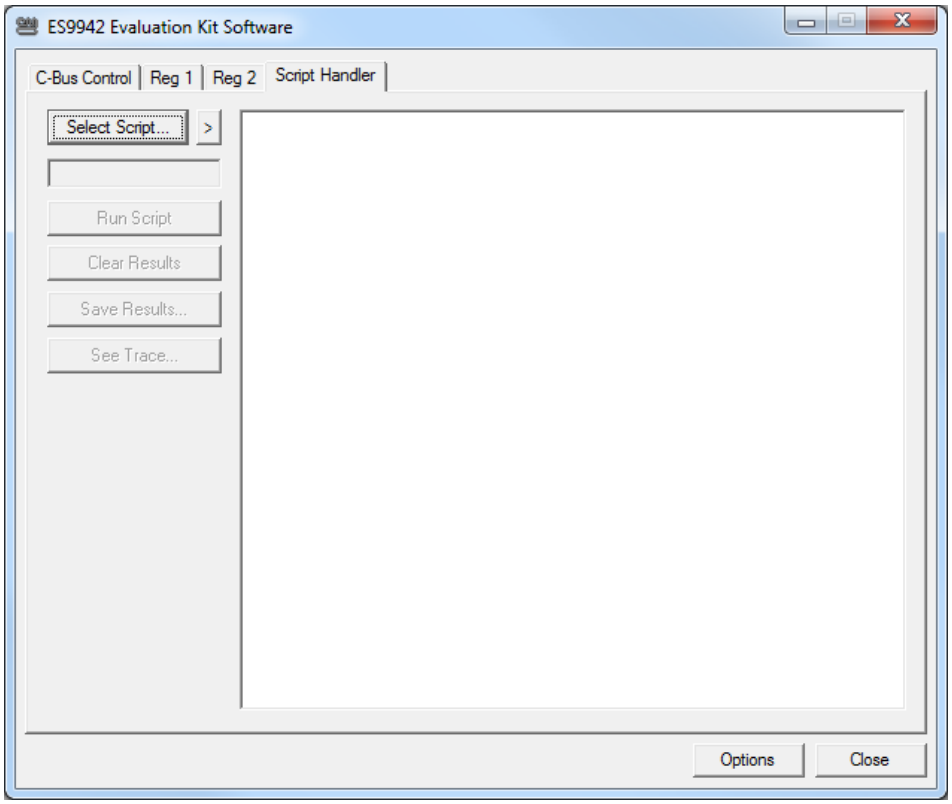

Figure 17 The Script Handler Tab (EV9942/EV9942A/EV9942E)

To select a script file, click on the 'Select Script' button. The Open File Dialog is displayed. Browse and select the script file. The folder that contains the script file will be the working folder of the script (i.e. all the files referenced in the script will be searched in this folder). Alternatively, select a script file from the recent files list. Click on the '>' button to display the list.

The results window displays the values returned by the script. These results can be saved to a text file or discarded by clicking on the 'Save Results' or 'Clear Results' buttons, respectively. When a script file is being executed the 'Run Script' button will change to the 'Abort' button, the rest of the tab will be disabled and the other tabs cannot be selected.

After a script has finished running and when trace data is available, the 'See Trace…' button will be enabled. Up to 131072 C-BUS transactions can be logged in the PE0003 board. Click in the 'See Trace…' button to display the Trace dialog box. Note that the C-BUS transactions are only logged if the feature has been enabled in the script. See the "Script Language Reference" document for details.

6.4. Application Information

6.4.1. Rx Testing the CMX994/CMX994A/CMX994E with the CMX7164 via the PE0601[3]

The EV9942/EV9942A/EV9942E has an I/Q interface which may be connected to a PE0601 through J14. This connector also allows the CMX994/CMX994A/CMX994E to be programmed via the SPI of the CMX7164. This allows evaluation of the CMX994 receiver with 4-FSK and QAM modulation (4, 16 and 64QAM). The following results have been taken based on measurement methods and limits taken from EN 301 166 (6.25kHz channels), EN 300 113 (25kHz channels, 4-FSK) and EN 302 561 (QAM).

6.4.2. Results with 4-FSK

6.4.2.1. Typical Performance 4-FSK, 3kHz Deviation, 19 200bps

The following performance is considered typical of CMX994/CMX994A/CMX994E operation in a 25kHz RF channel.

Sensitivity	
Input Level (dBm)	BER
-109	6.87E-07
-110	4.58E-06
-112	1.59E-04
-114	1.96E-03
-116	7.69E-03
-117	1.44E-02

Table 14 Typical Sensitivity Performance (4-FSK, 3kHz Deviation, 19 200bps)

Intermodulation	
Separation (dB)	BER
65	2.22E-03
65.5	6.11E-03
66	1.34E-02

Table 15 Typical Intermodulation Performance (4-FSK, 3kHz Deviation, 19 200bps)

The Intermodulation rejection (Table 15) is typically better than 65dB for <1% BER, with a wanted signal at -107dBm and interfering signals spaced at 50/100kHz (tested as EN 300 113).

Blocking results (Table 16) were taken with an unmodulated interferer at +/-1MHz offset. Typical blocking measurements are between 86dB and 93dB, depending on offset and measurement method (TIA or ETSI).

[3] Versions of the PE0601 are available for the CML products CMX7163 and CMX7164, which are both compatible with EV9942/EV9942A/EV9942E.

Blocking	
Separation (dB)	Wanted signal at -110dBm BER
87	6.85E-04
88	1.31E-03
89	2.55E-03
90	5.38E-03

Table 16 Typical Blocking Performance (4-FSK, 3kHz Deviation, 19 200bps)

Adjacent Channel Rejection Wanted at -110dBm		
Separation (dB)	On-Board VCO BER	External LO BER
60	3.66E-04	
62	1.07E-03	
64	3.44E-03	
65	5.88E-03	
66	9.61E-03	
67	1.58E-02	
68		
70		1.14E-05
71		2.47E-05
72		2.98E-05
73		1.02E-02

Table 17 Typical ACR Performance (4-FSK, 3kHz Deviation, 19 200bps)

Table 17 shows the on-board VCO is limiting the ACR measurement and the measurements with an external LO show that the receiver is capable of achieving >70dB adjacent channel performance. The CMX994 maximum filter bandwidth was used when taking these results. The positive and negative offsets have very similar performance.

Spurious response test results (Table 18) were measured with a FM modulated interferer at +50kHz.

Spurious Response Rejection	
Separation (dB)	Wanted signal at -110dBm BER
75	4.69E-05

Table 18 Typical Spurious Response Rejection Performance (4-FSK, 3kHz Deviation, 19200bps)

6.4.2.2. Typical Performance 4-FSK, 1.05kHz Deviation, 4800bps

The following performance is considered typical of CMX994 operation in a 6.25kHz RF channel. These measurements were taken with the on-board VCO and the CMX994/CMX994A/CMX994E minimum filter bandwidth selected. The positive and negative offsets have very similar performance.

Sensitivity	
Input Level (dBm)	BER
-114	2.29E-06
-116	3.89E-05
-118	5.68E-04
-120	3.94E-03
-121	8.77E-03
-122	1.55E-02

Table 19 Typical Sensitivity Performance (4-FSK, 1.05kHz Deviation, 4 800bps)

Adjacent Channel Rejection Wanted at -104dBm	
Separation (dB)	BER
54	1.13E-03
56	5.25E-03
57	8.15E-03
58	1.36E-02

Table 20 Typical ACR Performance (4-FSK, 1.05kHz Deviation, 4 800bps)

6.4.3. Results with QAM

The following results were all taken with the CMX994/CMX994A/CMX994E ACR filter set at its maximum setting and the on-board LO at 896MHz. The input was at 448MHz and the baud rate in all cases was 18ksymbols/s. The plot in Figure 18 compares the sensitivity curves of the three different QAM types.

6.4.3.1. 4QAM, 18ksymbols/s

Input Level (dBm)	**BER**
-113	4.58E-06
-114	4.40E-05
-115	2.57E-04
-116	1.14E-03
-117	4.30E-03
-118	1.18E-02

Table 21 Typical 4QAM Sensitivity Performance

6.4.3.2. 16QAM, 18ksymbols/s

Input Level (dBm)	BER
-105	1.37E-06
-106	6.87E-06
-107	4.53E-05
-108	2.28E-04
-109	9.51E-04
-110	2.51E-03
-111	5.67E-03
-112	1.11E-02

Table 22 Typical 16QAM Sensitivity Performance

6.4.3.3. 64QAM, 18ksymbols/s

Input Level (dBm)	BER
-98	5.95E-06
-99	1.92E-05
-100	9.16E-05
-101	2.74E-04
-102	7.99E-04
-103	2.50E-03
-104	4.97E-03
-105	9.69E-03
-106	1.59E-02

Table 23 Typical 64QAM Sensitivity Performance

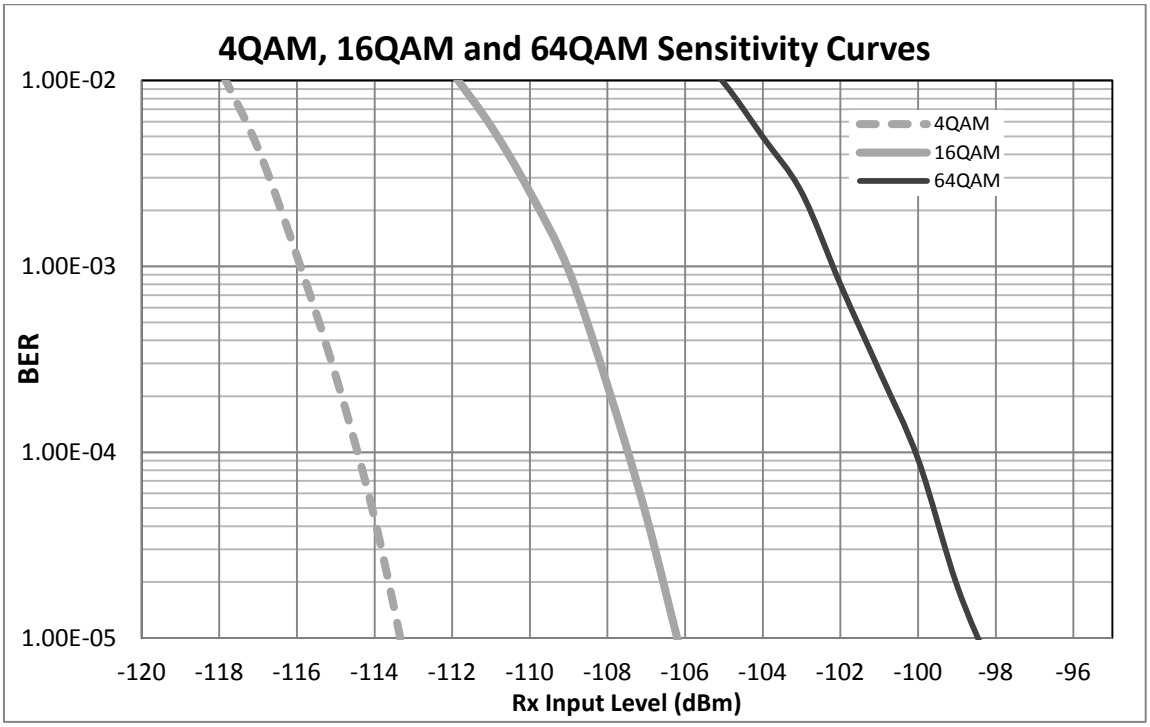

Figure 18 4QAM, 16QAM and 64QAM Sensitivity Curves

6.5. Troubleshooting

The CMX994/CMX994A/CMX994E is a complex RF system. If incorrectly programmed or modified, results will be at variance from datasheet performance. Please study the IC datasheet, this user manual and the associated schematics and layout drawings carefully when troubleshooting.

This section provides some suggestions to help users resolve application issues they might encounter.

6.5.1. General

Error Observed	Possible Cause	Remedy
'**ES9942xx.exe**' software fails to run correctly and reports an error during start up.	Faulty USB port or cable.	Check USB cable to your PC.
	PE0003 or EV9942/EV9942A/EV9942E is not powered up during start up.	Power up PE0003 (5.0V) and EV9942/EV9942A/EV9942E (7.2V).
	Incorrect software for PE0003.	Contact: techsupport@cmlmicro.com
Programming data to EV9942/EV9942A/EV9942E does not appear to work.	The data is being programmed to the wrong C-BUS port on PE0003.	Check whether EV9942/EV9942A/EV9942E is connected to PE0003 Port 1 (J5) or Port 2 (J3) and ensure the correct window is used for programming data. (See PE0003 user manual for further information).

Table 24 Possible General Errors

6.5.2. Receiver Operation

Error Observed	Possible Cause	Remedy
No output from the receiver.	The receiver has not been enabled by either the RXEN pin or the C-BUS Rx enable ($11, b1).	Set C-BUS Rx enable ($11, b1='1') or set RXEN (pin 23) high.
No output from the receiver.	The PCB does not have the LNA connected to the down-converter mixers using C7, C15, C8 etc or filter FL1.	Check hardware configuration and ensure received signal is present at pin 9.
No output from the receiver.	The RF input is connected to the wrong connector. Note: Input is J5.	Check hardware configuration and ensure received signal is present at pin 6.
Adjacent channel performance is not the same on +ve offset and –ve offset.	The VCTCXO control line has not been setup to ensure the PLL frequency is centred on the channel. Note: the default configuration of the EV9942/EV9942A/EV9942E is that the control voltage to the VCTCXO is fixed by means of R18 and R21.	Apply a suitable signal to AFC, which can be monitored on TP3.
PLL does not lock. (Lock detect bit = '0').	VCO is not enabled. LO Input is not enabled. M and R Divider setting are incorrect.	Check values of PLL registers $20, $21, $22, $23 and $24.
	VCO has been programmed to a frequency outside its operating range.	Check VCO control voltage on CMX994/CMX994A/CMX994E signal DO (pin 20 or TP5). If the voltage is at either supply rail, try a different frequency and observe the effect.

Table 25 Possible Receiver Errors

6.5.3. Transmitter and PLL Operation

Error Observed	Possible Cause	Remedy
No output from the transmit LO path.	The transmitter has not been enabled by either the TXEN pin or the C-BUS Tx enable ($11, b0).	Set C-BUS Tx enable ($11, b0='1') or set TXEN (pin 22) high.
No output from the transmit LO path.	The wrong Tx divider ratio has been selected ($25, b5 & b6)	Check CMX994/CMX994A/CMX994E Datasheet for details on register $25 to ensure correct divider ratio selected.
PLL does not lock. (Lock detect bit = '0').	VCO is not enabled. LO Input is not enabled. M and R Divider setting are incorrect.	Check values of PLL registers $20, $21, $22, $23 and $24.
	VCO has been programmed to a frequency outside its operating range.	Check VCO control voltage on CMX994/CMX994A/CMX994E signal DO (pin 20 or TP5). If the voltage is at either supply rail, try a different frequency and observe the effect.

Table 26 Possible Transmitter Errors

7. Performance Specification

7.1. Electrical Performance

7.1.1. Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the evaluation kit.

	Min.	Max.	Units
Supply Voltage (V_{IN} - V_{SS})	0	8.0	V
Current into or out of VIN and VSS pins	0	+2.0	A
Current into or out of any other connector pin	-20	+20	mA

7.1.2. Operating Limits

Correct operation of the evaluation kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply Voltage (V_{IN} - V_{SS})		5.25	8.0	V

7.1.3. Operating Characteristics

Characteristics apply to all versions (EV9942/EV9942A/EV9942E) unless otherwise specified.
For the following conditions unless otherwise specified: V_{IN} - V_{SS} = 7.2V, Tamb = +25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (CMX994/CMX994A/CMX994E Powersaved)	2, 3	–	16	–	mA
I_{DD} (CMX994/CMX994A/CMX994E Rx Enabled, PLL and VCO)	2	–	95	–	mA
I_{DD} (CMX994/CMX994A/CMX994E Tx Enabled, PLL and VCO)	2	-	50	-	mA
I_{DD} (CMX994E Rx Enabled, PLL and VCO)	2,11	–	103	–	mA
AC Parameters					
Receiver Input					
Input Impedance		–	50	–	Ω
Input Level		–	–	0	dBm
Frequency Range (Default Components)	10	446	448	450	MHz
Frequency Range (With FL1 Fitted)	10		446		MHz
Frequency Range (With External LO)		440		460	MHz
Filter Bandwidth	4	–	2 / 4 / 8	–	kHz
I/Q Output Signal					
Amplitude	5	–	440	–	mVp-p
DC Level		–	1.6	–	Vdc
LO Input (J7)					
Input Impedance		–	50	–	Ω
Frequency Range		200	–	2000	MHz
Input Level		–	-13	–	dBm
Frequency Reference (U2)					
Frequency		–	19.2	–	MHz
Stability		–	1.5	–	ppm
448MHz Rx Operation					
Gain	7	62.5	63	64.5	dB
Noise Figure		–	4.5	6	dB
Input Third Order Intercept Point		-4	-2	–	dBm
Enhanced Input Third Order Intercept Point	11	2	4	–	dBm
Input Second Order Intercept Point	8	45	55	–	dBm
Sensitivity	6	–	-116	–	dBm
Tx Operation					
Output Level	9	-5	-3.5	–	dBm
Frequency Range (CMX994)		100	–	940	MHz
Frequency Range (CMX994A/CMX994E)		100	–	1000	MHz
C-BUS Interface					
See CMX994 Datasheet					

Notes:

2. Total PCB current consumption, not current consumption of the CMX994 alone.
3. Current consists of TR2/TR3 VCO (15mA); VCTCXO (1mA).
4. Bandwidth is selectable in the CMX994 IC, see CMX994 datasheet for details.
5. 448MHz input at –60dBm at J5.
6. 4-FSK modulation, 3kHz deviation, 19 200 bits/s at a BER of $1x10^{-2}$.
7. Gain is measured from RF input (assumed to be 50 Ohm source /load) to differential voltage measured at output of I or Q channels.
8. Measured at +1MHz offset.
9. Measured at 448MHz.
10. Operating range set by tuning range of 892MHz VCO.
11. CMX994E (EV9942E only) in Enhanced mode ($15, b7='1')

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