

# CMS100N04H8-HF

**N-Channel**  
**RoHS Device**  
**Halogen Free**

## Features

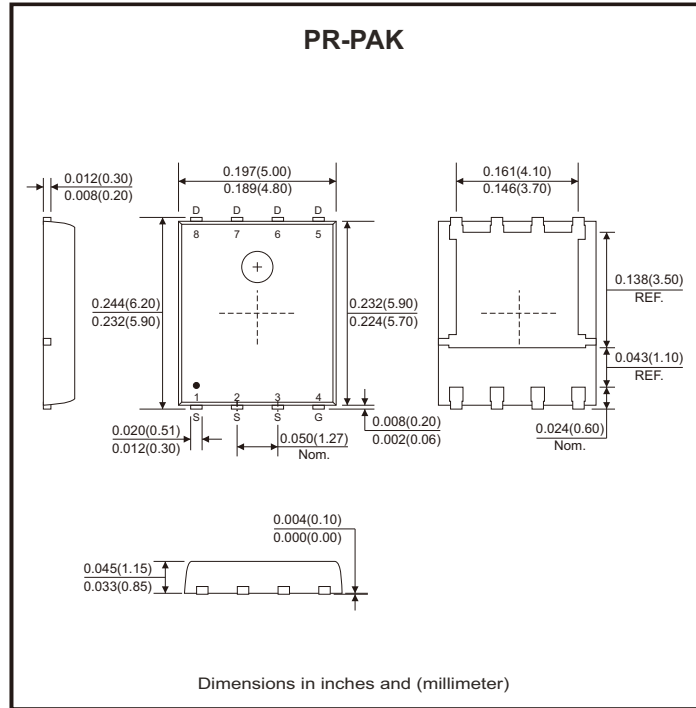
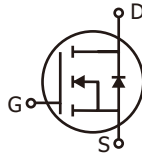
- Advanced DMOS trench technology.
- Fast switching.
- Improve dv/dt capability.
- 100% EAS and Rg guaranteed.
- Green device available.

## Mechanical data

- Case: PR-PAK

## Circuit Diagram

- G : Gate
- S : Source
- D : Drain



## Maximum Ratings

Parameter	Conditions	Symbol	Value	Unit
Drain-source voltage		$V_{DS}$	40	V
Gate-source voltage		$V_{GS}$	$\pm 20$	V
Continuous drain current (Note 1)	$T_C = 25^\circ\text{C}$	$I_D$	100	A
	$T_C = 100^\circ\text{C}$	$I_D$	63	
Pulsed drain current (Note 1, 2)		$I_{DM}$	400	A
Total power dissipation (Note 4)	$T_C = 25^\circ\text{C}$	$P_D$	135	W
	$T_A = 25^\circ\text{C}$	$P_D$	2	
Single pulse avalanche energy, $L=0.1\text{mH}$ (Note 3)		$E_{AS}$	312	mJ
Single pulse avalanche current, $L=0.1\text{mH}$ (Note 3)		$I_{AS}$	79	A
Operating junction and storage temperature range		$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Thermal resistance junction-ambient (Note 1)	Steady state	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal resistance junction-case (Note 1)	Steady state	$R_{\theta JC}$	0.92	$^\circ\text{C/W}$

- Notes: 1. The data tested by surface mounted on a 1inch<sup>2</sup> FR-4 board with 2oz copper.  
 2. The data tested by pulsed, pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 3. The EAS data shows max. rating. The test condition is  $V_{DD}=25\text{V}$ ,  $V_{GS}=10\text{V}$ ,  $L=0.1\text{mH}$ ,  $I_{AS}=79\text{A}$ .  
 4. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature.

## Electrical Characteristics (at T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	40			V
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.6	2.5	V
Gate-source leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V			±100	nA
Drain-source leakage current (T <sub>J</sub> =25°C)	I <sub>DSS</sub>	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V			1	μA
Drain-source leakage current (T <sub>J</sub> =125°C)		V <sub>DS</sub> = 32V, V <sub>GS</sub> = 0V			10	
Static drain-source on-resistance (Note 2)	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A		2.2	2.8	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 12A		2.6	3.5	
Total gate charge (Note 2)	Q <sub>g</sub>	I <sub>D</sub> = 10A, V <sub>DS</sub> = 20V, V <sub>GS</sub> = 4.5V		44.4		nC
Gate-source charge	Q <sub>gs</sub>			9.6		
Gate-drain ("miller") charge	Q <sub>gd</sub>			16		
Turn-on delay time (Note 2)	t <sub>d(on)</sub>	V <sub>DD</sub> = 20V, I <sub>D</sub> = 1A V <sub>GS</sub> = 10V, R <sub>G</sub> = 6Ω		28		nS
Rise time	t <sub>r</sub>			3.2		
Turn-off delay time	t <sub>d(off)</sub>			89		
Fall time	t <sub>f</sub>			14		
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz		4940		pF
Output capacitance	C <sub>oss</sub>			425		
Reverse transfer capacitance	C <sub>rss</sub>			170		
Gate resistance	R <sub>g</sub>	f = 1MHz		1.4		Ω
<b>Source-drain diode</b>						
Diode forward voltage (Note 2)	V <sub>SD</sub>	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C			1.2	V
Continuous source current (Note 1, 4)	I <sub>S</sub>	V <sub>G</sub> = V <sub>D</sub> = 0V, Force current			100	A
Pulsed source current (Note 2, 4)	I <sub>SM</sub>				200	A
<b>Guaranteed avalanche characteristics</b>						
Single pulse avalanche energy (Note 3)	EAS	V <sub>DD</sub> = 25V, L = 0.1mH, I <sub>AS</sub> = 40A	80			mJ

- Notes: 1. The data tested by surface mounted on a 1inch<sup>2</sup> FR-4 board with 2oz copper.  
 2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%.  
 3. The min. value is 100% EAS tested guarantee.  
 4. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

## Rating and Characteristic Curves (CMS100N04H8-HF)

Fig.1 - Typical Output Characteristics

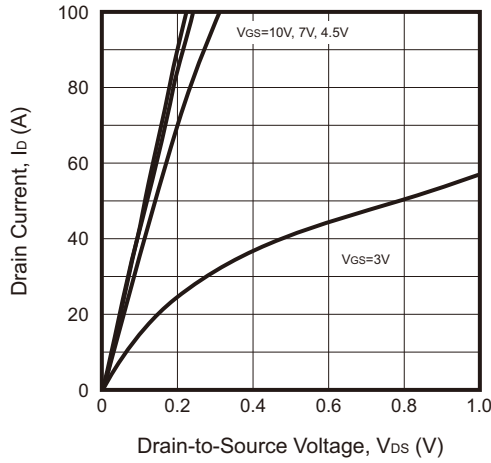


Fig.2 - On-Resistance vs. G-S Voltage

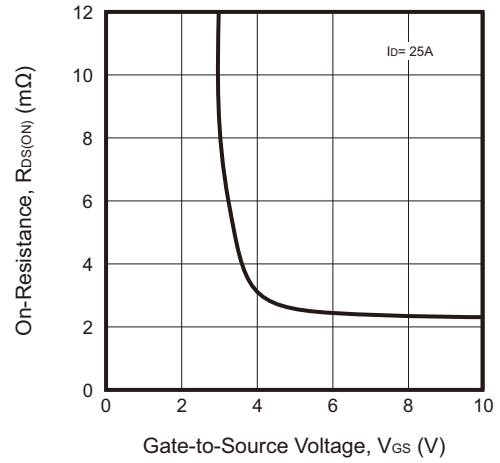


Fig.3 - On-Resistance vs. Drain Current

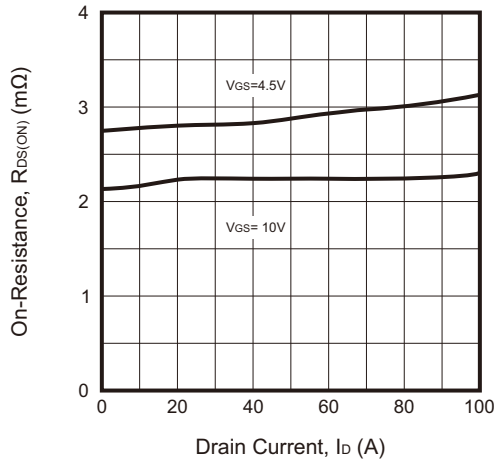


Fig.4 - Normalized  $R_{DS(ON)}$  vs.  $T_J$

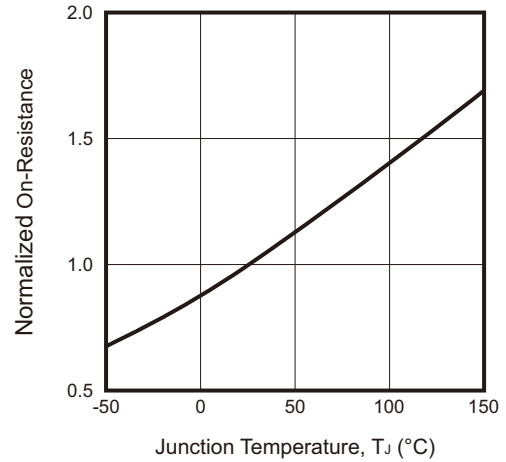


Fig.5 - Normalized  $V_{GS(th)}$  vs.  $T_J$

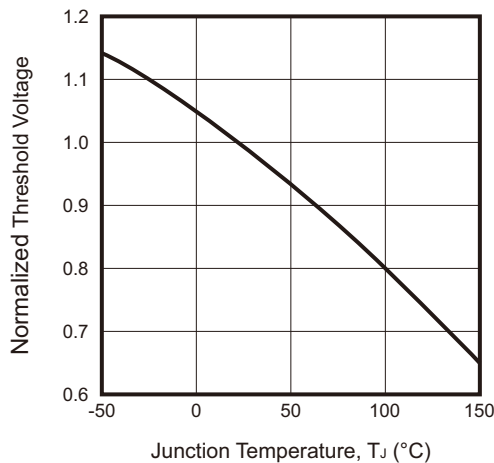
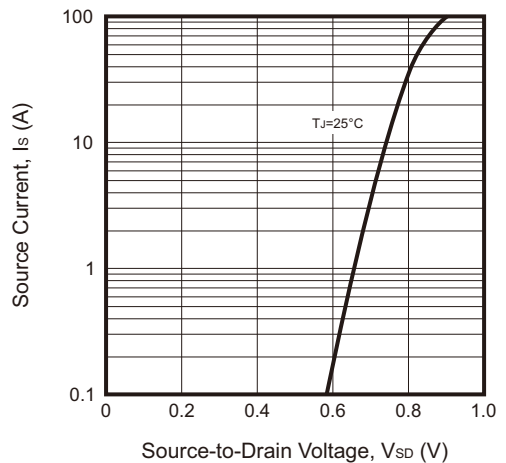


Fig.6 - Forward Characteristics of Reverse



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## Rating and Characteristic Curves (CMS100N04H8-HF)

Fig.7 - Gate Charge Characteristics

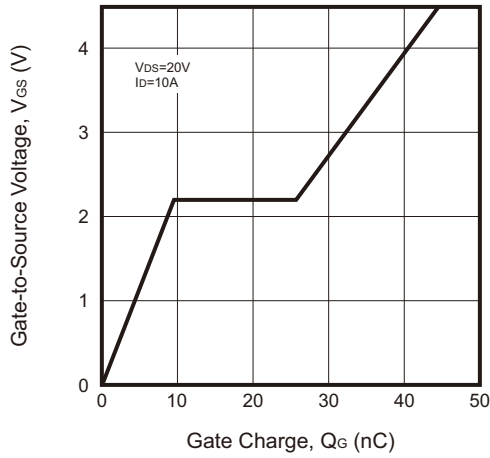


Fig.8 - Drain Current vs.  $T_c$

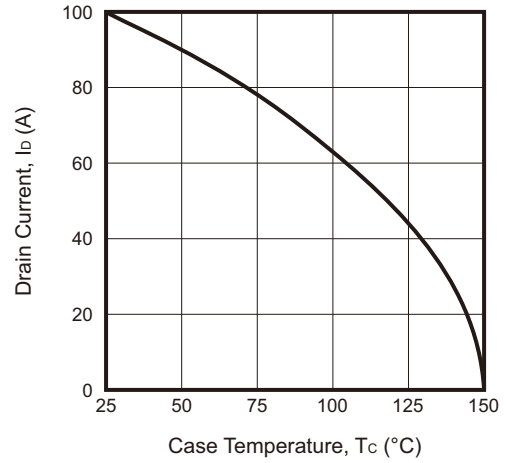
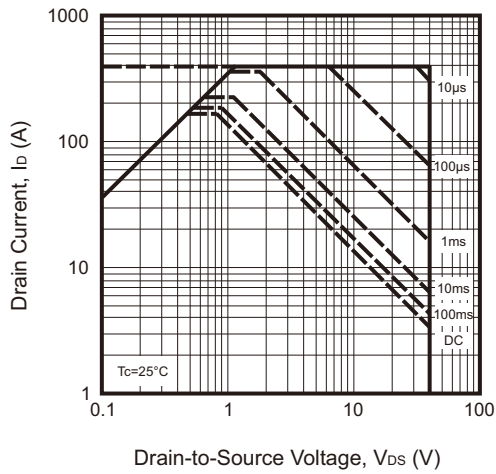
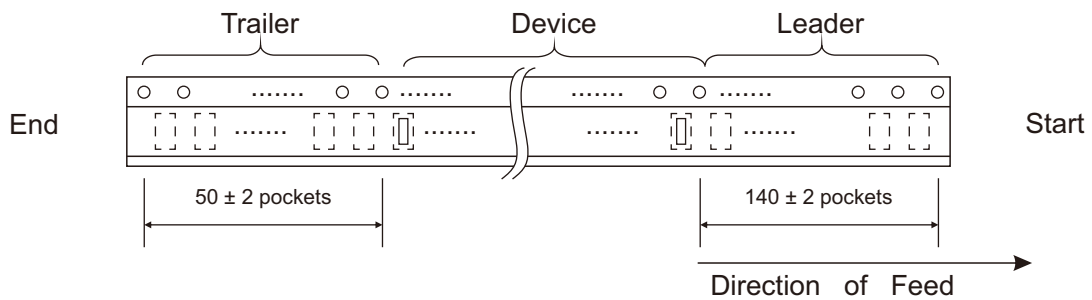
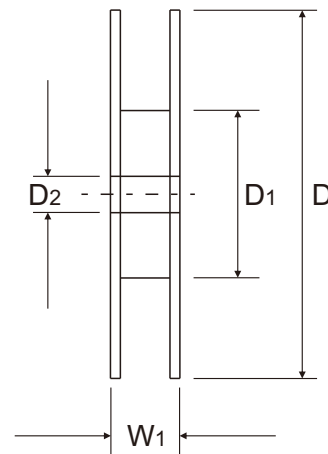
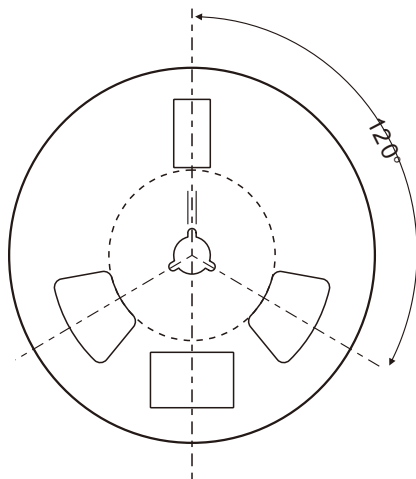
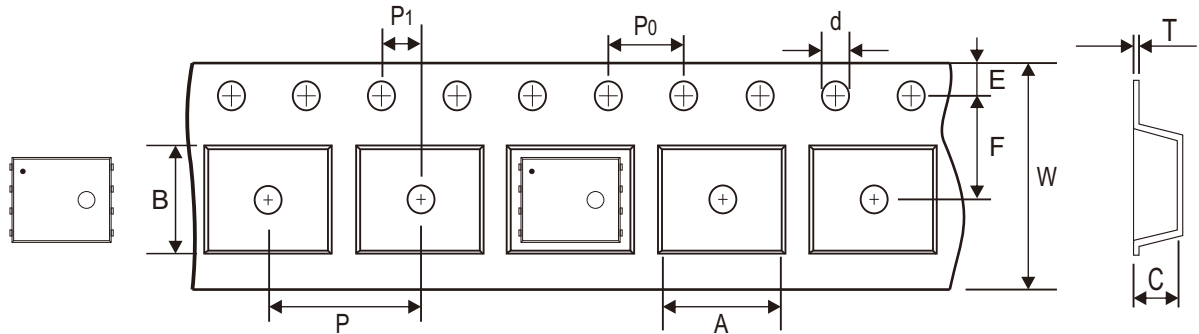


Fig.9 - Safe Operating Area



Reel Taping Specification



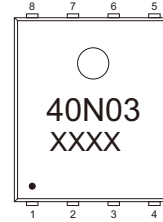
PR-PAK	SYMBOL	A	B	C	d	D	D1	D2
	(mm)	6.50 ± 0.10	5.30 ± 0.10	1.40 ± 0.10	1.50 + 0.10 - 0.00	330.00 ± 1.00	178.00 + 0.00 - 2.00	13.00 min.
	(inch)	0.256 ± 0.004	0.209 ± 0.004	0.055 ± 0.004	0.059 + 0.004 - 0.000	12.992 ± 0.039	7.008 + 0.000 - 0.079	0.512 min.

PR-PAK	SYMBOL	E	F	P	P0	P1	T	W	W1
	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05	12.00 ± 0.30	18.40 ref.
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.012 ± 0.002	0.472 ± 0.012	0.724 ref.

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## Marking Code

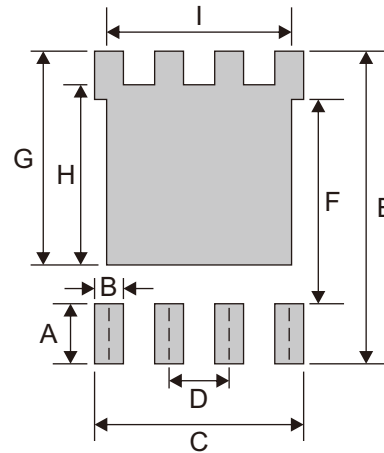
Part Number	Marking Code
CMS100N04H8-HF	40N03 XXXX



XXXX = Control code

## Suggested PAD Layout

SIZE	PR-PAK	
	(mm)	(inch)
A	1.27	0.050
B	0.61	0.024
C	4.42	0.174
D	1.27	0.050
E	6.61	0.260
F	4.32	0.170
G	4.52	0.178
H	3.81	0.150
I	3.91	0.154



Note: 1. The pad layout is for reference purposes only.

## Standard Packaging

Case Type	REEL PACK	
	REEL ( pcs )	Reel Size (inch)
PR-PAK	3,000	13

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