

## FEATURES

- Intel Cyclone V - U672 SoC
  - **Up To Dual ARM Cortex- A9 MPU**
  - 925MHz Max clock speed
  - Dual NEON SIMD Coprocessors
  - 32 KB L1 Program Cache (per core)
  - 32 KB L1 Data Cache (per core)
  - 512 KB L2 Cache (shared)
  - 64 KB on-chip RAM
  - ECC Support
  - **Up To 133 User FPGA I/O Pins**
  - **44 CPU I/O Pins**
  - **6 High speed transceivers (SX only)**
- **Cyclone V Processor Choices**
  - Cyclone V SX (3.125 Gbps transceivers)
  - Cyclone V SE
- **Memory**
  - Up To 2GB DDR3 CPU RAM  
x32 bits + ECC
  - Up To 512MB DDR3 FPGA RAM  
x8 bits (optional)
  - Up To 272MB QPSI NOR FLASH
- Integrated Power Management
- JTAG connector on-module
- **FPGA Fabric**
  - Up To 110K Logic Elements (LE)
  - 460Mhz Global Clock
  - Up To 5.1Mb M10K Memory
  - Up To 621Kb MLAB Memory
  - Up To 112 DSP Blocks
  - Up To 6 FPGA PLLs
  - Fractional PLL Outputs on each PLL
- Low Power Serial Transceivers (**SX only**)
  - 3.125Gbps Transceivers
  - PCIe Hard IP Block  
(Gen1.1 x1 or x4)
- Power, Reset and Clock Management



- **Mechanical**
  - 314-Pin Card Edge Connector
  - Small 82mm (3.2") x 39mm (1.5") size
- **Hard Processor System (HPS)**
  - Selection of boot sources
  - Up to 2 10/100/1000 Mbps Ethernet MACs
  - Up to 2 USB 2.0 OTG Ports
  - Up to 2 CAN Interfaces
  - Up to 2 UARTs
  - 1 MMC/SD/SDIO
  - Up to 4 I2C controllers
  - Up to 2 master/2 slave SPI
  - 3 HPS PLLs

## APPLICATIONS

- Machine Vision
- Test and Measurement
- Embedded Instrumentation
- Industrial Automation and Control
- Industrial Instrumentation
- Medical Instrumentation
- Closed Loop Motor Control

## BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- Rich User Interfaces
- High System Integration
- High Level OS Support
  - Embedded Linux
  - Micrium uC/OS (via 3<sup>rd</sup> Party)
  - Android (via 3<sup>rd</sup> Party)
  - QNX (via 3<sup>rd</sup> Party)

## DESCRIPTION

The MitySOM-5CSx series of highly configurable, small form-factor System-on-Modules (SoM) feature an Intel Cyclone V System-on-Chip (SoC). Additionally, the module includes on-board power supplies, NOR FLASH and DDR3 RAM memory subsystems. A MitySOM-5CSx provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The MitySOM-5CSX is available with either a Cyclone V SX or Cyclone V SE which provide up-to Dual-core Cortex-A9 32-bit RISC processors with dual NEON SIMD coprocessors. This MPU is capable of running a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux, Micrium uC/OS, Android and QNX.

### MitySOM 5CSx System On Module Block Diagram

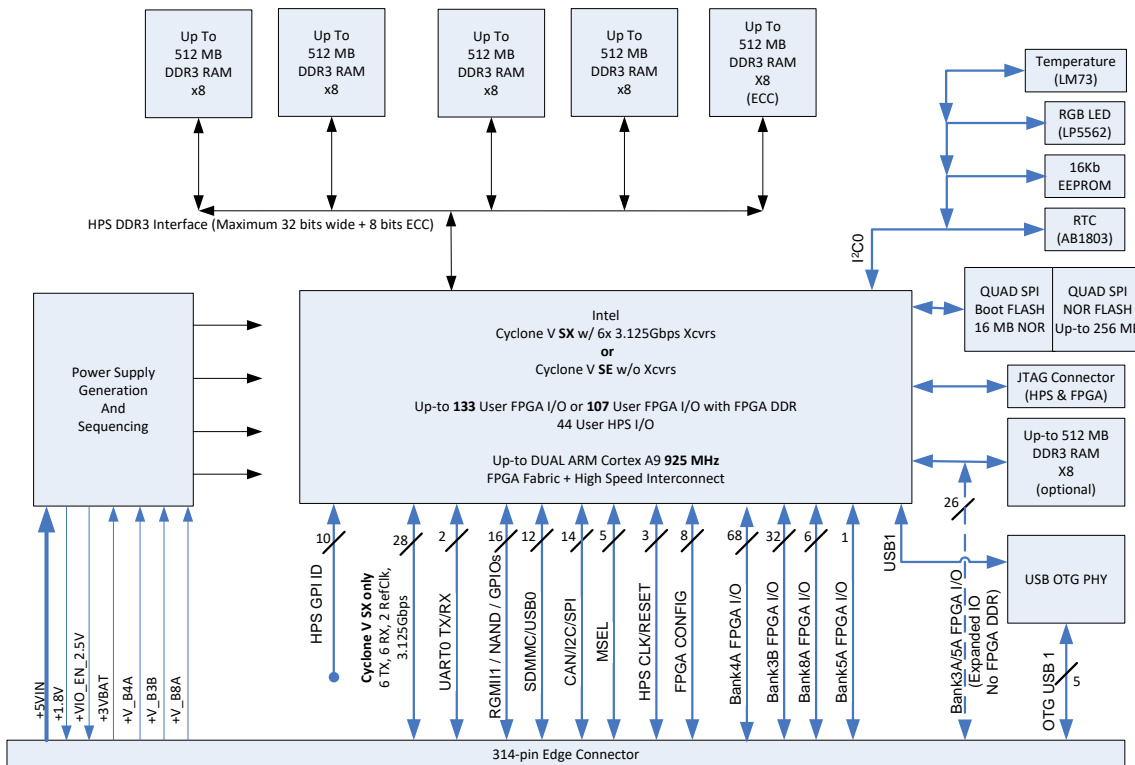


Figure 1 MitySOM-5CSx Block Diagram

Figure 1 provides a top-level block diagram of the MitySOM-5CSx processor card. As shown in the figure, the primary interface to the MitySOM-5CSx is through a 314-Pin card edge interface. Details of the edge connector interface are included in the Card Edge Interface Description section.

## **MitySOM-5CSx Onboard Storage**

### **DDR3 Memory – HPS Memory**

The MitySOM-5CSx includes one dedicated 40-bit DDR3 memory interface. The memory interface can be up-to 40-bits wide including 8-bits for ECC. A maximum of 2GB of DDR3 RAM with ECC is supported by the MitySOM-5CSx module.

The standard MitySOM-5CSx includes 1GB of DDR3 RAM with ECC (40-bits wide) integrated on the module.

The lowest KLE variant of the MitySOM-5CSE includes 512MB of DDR3 RAM without ECC (16-bits wide) integrated on the.

This HPS DDR3 memory is available for both the HPS (Cortex-A9 ARM core(s)) as well as the FPGA fabric through either the AXI or Avalon high speed interfaces internal to the Cyclone V.

The MitySOM-5CSx family adheres to Intel's Cyclone V maximum memory speeds. At this time the HPS memory clocked at 400Mhz as the maximum and a slower speed may be selected, if desired, down to 300MHz. This may change if Intel makes changes to their Silicon/recommendations.

See Table 10: Standard Model Numbers for additional details.

### **DDR3 Memory – FPGA Memory (Optional)**

The MitySOM-5CSx modules can also include up to 512MB of DDR3 connected directly to the Cyclone V FPGA fabric through a 8-bit bus. This memory is exclusively for the use of the FPGA fabric for buffering and local storage and is available through a high speed, low latency direct connect.

A total of 26 additional FPGA I/O is available through the card edge connector in models that do not feature the FPGA DDR3 memory. See Table 10: Standard Model Numbers for additional details.

### **HPS-FPGA AXI**

The high bandwidth HPS-FPGA AXI bridges provided by Intel in the Cyclone V SoC allow masters in the FPGA fabric to communicate with slaves in the HPS logic and vice versa. These bridges can be configured for 32, 64, or 128 bit widths.

For example, designers can instantiate additional memories or peripherals in the FPGA fabric, and master interfaces belonging to components in the HPS logic can access them. Designers can also instantiate components such as a Nios® II processor in the FPGA fabric and their master interfaces can access memories or peripherals in the HPS logic, including DDR3 Memory – HPS Memory.

### **NOR FLASH**

A maximum of 272MB (1 x 16MB and 1 x 256MB) of on-board NOR FLASH memory is connected to the Cyclone V using a Quad Serial Peripheral Interface (QSPI SS0 and SS1). This is a reliable flash memory that can be used as a boot media for the module as well as configuration information if needed for custom applications.

### **Configuration EEPROM**

MitySOM-5CSx modules contain a 2048 x 8-bit EEPROM that is used to hold configuration data for the module. The EEPROM is connected to the Cyclone V using the I2C0 interface. This EEPROM contains information such as the module type, Serial Number, MAC addresses for the Ethernet interface(s) and additional information as required by Critical Link.

Note that this memory shall not be used except for Critical Link factory configuration information and its contents may change as required by Critical Link.

## On-board Interfaces

The following on-board interfaces were chosen to provide the most flexibility for end user applications. As many HPS MUX options as possible were left available for the user. These interfaces should not be muxed external to the module on other pins.

### Console Serial port

The console serial port (UART0) is supported on pins 2 (RX) and 4 (TX) of the 314-Pin Card Edge Connector with a simple TX/RX interface. By default, the flow control signals are not enabled but can be added to the console serial interface if desired.

Please reference the Card Edge Pin-Out for specific Cyclone V pin-connections.

### I2C0 Interface

The I2C0 peripheral is consumed local to the module. It is used for the Real Time Clock, Temperature Sensor, Configuration EEPROM, and to control a PWM LED driver for status and debug.

**Table 1: I2C0 Peripherals**

Address	Device	Feature
1000010	AS3668	LED Driver for RGB Status LED (D1) and a Green LED (D5)
1010XXX	FT24C16A	16Kbit EEPROM for Critical Link factory configuration parameters
1101001	AB1805-T3	Real Time Clock
1001100	LM73CIMK-1	Temperature sensor

For application information about each of these I2C devices, including drivers and example code, please visit our support site at <https://support.criticallink.com/>.

### QuadSPI Interface

The QUADSPI peripheral is wired to Bank 7B and is used for the NOR FLASH interface on the module. Both Slave select 0 and slave select 1 have been utilized for this NOR memory.

**Table 2: QSPI Slave Selects**

Slave Select	Feature	Memory Sizing
0	Boot flash	128Mb –x4 width - 16MB max
1	Additional flash	128Mb –x4 width (not populated on 16MB NOR modules) – 256MB max

### USB-2.0 OTG Phy

The USB1 interface of the Cyclone V processor is connected directly to a USB 2.0 OTG phy on the module itself. The necessary USB ID, power and data pins are available at the edge connector of the module.

Please see Table 8 for the specific pin locations.

### Debug Interface

The JTAG interface signals for the Cyclone V processor have been brought out to a 31 pin Hirose connector (DF9-31P-1V(32)), J2, which is intended for use with available Critical Link breakout adapters. For JTAG interfacing please utilize the Critical Link JTAG Debug Adapter, part number 80-000616.

The interface on the module allows for both HPS (ARM processor(s)) and FPGA debug. Below is the pin-out of the J2 connector on the MitySOM-5CSx module.

#### *Debug Interface Connector Description (J2)*

**Table 3 J2 Hirose Connector**

Pin	I/O	Signal	Pin	I/O	Signal
1	-	GND	2	I/O	HPS_RST_N
3	I	MICTOR_TRACE_PRSNT*	4	I	HPS_GPI10_SYSCON
5	-	GND	6	I	JTAG_HPS_TCK
7	-	GND	8	-	NC
9	I/O	MICTOR_TRACE_D0*	10	O	JTAG_HPS_TDO
11	I/O	MICTOR_TRACE_D1*	12	-	VCC (3.3V)
13	I/O	MICTOR_TRACE_D2*	14	I	JTAG_HPS_TDI
15	I/O	MICTOR_TRACE_D3*	16	I	JTAG_HPS_TRST
17	I/O	MICTOR_TRACE_D4*	18	I	JTAG_HPS_TMS
19	I/O	MICTOR_TRACE_D5*	20	-	GND
21	I/O	MICTOR_TRACE_D6*	22	-	+VPD_3A5A5B
23	I/O	MICTOR_TRACE_D7*	24	I	JTAG_FPGA_TMS
25	-	GND	26	I	JTAG_FPGA_TCK
27	-	GND	28	O	JTAG_FPGA_TDO
29	I/O	MICTOR_TRACE_CLK*	30	I	JTAG_FPGA_TDI
31	-	GND			

\*For TRACE support please contact your Critical Link representative for further information

A debug breakout adapter is not included with individual modules but the JTAG adapter is included with each Critical Link MitySOM-5CSx Development Kit that is ordered. If an adapter is needed please contact your Critical Link representative. The JTAG debug adapter from Critical Link is compatible with the Intel FPGA Download Cable and Download Cable II [Intel Download Cables](#)<sup>[3]</sup>.

Note that this header, J2, can be removed for production units; please contact your Critical Link representative for details.

## External Interfaces

The Cyclone V makes extensive use of functional pin multiplexing to provide a highly configurable device that can be tailored to a multitude of applications.

## HPS Interfaces

A list of the interfaces/functions that are available to the user from the HPS is provided below.

- Up to 2 Universal Serial Bus (USB) 2.0 High-Speed On-The-Go (OTG) port
  - USB1 features an on SoM TI TUSB1211 USB Phy
  - USB0 ULPI interface pins available at edge connector, no Phy on SoM
- 2 Controller-Area Network (CAN) ports
- Up to 2 Gigabit Ethernet MAC's (10/100/1000 Mbps)
  - EMAC1 through HPS or FPGA fabric
  - EMAC0 through FPGA fabric
- 1 MMC/SD/SDIO ports
- 4 Serial Peripheral (SPI) ports
  - 2 Master
  - 2 Slave
- 2 Universal Asynchronous Receive/Transmit (UART) ports
- 4 Inter-Integrated Circuit (I2C) ports
  - I2C0 is connected to the on-board EEPROM, Temperature Sensor, RTC and LED Driver
- JTAG/Debugger port
- RTC Battery Input (+3VBAT)

Additionally, most of the pin multiplexed signals can be configured as general purpose I/O signals with interrupt capability.

## FPGA Interfaces

### *GPIO*

Up to 133 FPGA Input/Output pins are available externally to a module that does not contain FPGA memory and 107 FPGA Input/Output pins are available externally for modules that feature the FPGA memory.

### *3.125 Gbps Transceivers (Cyclone V SX based modules only)*

A total of six (6) 3.125Gbps transceivers are available on the module for supporting high speed serial interfaces. This feature is only available on Cyclone V SX based modules.

## Configuration and Boot Modes

The Cyclone V has two groups of pins, documented below, that are read during reset to determine which media to boot from for the HPS and one group of pins that is used to configure the FPGA.

Please see Table 8 for the specific pin locations.

### HPS Configuration pins

The BSEL and CSEL pins determine which memory interface has the bootloader and how to clock the interface. For booting the HPS, the BSEL and CSEL pins details are covered in [CV-5400A](#)<sup>[1]</sup>.

#### *BSEL[0:2] (HPS Boot Select at Reset)*

The MitySOM-5CSx module can boot from a number of devices and identified in Table 4 below. Pull-ups and pull-downs must be included in the base-board design to select the correct boot option; please consult the MitySOM-5CSx Carrier Board Design Guide for details.

Table 4 lists the BSEL values that could be used on a MitySOM-5CSx design. The necessary BSEL configuration pins are all exposed to the edge connector for their HPS peripheral functions, Table 8.

**Table 4: BSEL Values**

BSEL Value	Boot device
0x0	Reserved
0x1	FPGA (HPS-to-FPGA bridge)
0x2	1.8V NAND flash memory
0x5	3.0V SD/MMC flash memory with external transceiver
0x6	1.8V SPI or Quad SPI flash memory (16MB bootable QSPI NOR)

#### *CSEL[0:1] (HPS Clock Select at Reset)*

The HPS signals that include the two CLKSEL boot configuration options are exposed on the module's edge connector pins. The default setting recommended by Critical Link is b'00'. These need to be pulled to the desired clock select option for your design. The default is to use the MitySOM-5CSx module's included 25MHz clock source into the osc1\_clk pin. Please consult the MitySOM-5CSx Carrier Board Design Guide for details.

The CSEL settings allow some of the HPS peripherals to run from a different clock source than the main HPS reference. Refer to [CV-5400A](#)<sup>[1]</sup> for the CSEL setting details.



### FPGA Configuration Pins

The FPGA MSEL configuration input pins are dedicated inputs that should be connected directly to either power or ground. These define where the FPGA configuration boot stream will come from and the master that will clock the interface. Please see [Cyclone V Device Handbook CV-52007<sup>\[2\]</sup>](#) for details on what value to use for the MSEL connections and the MitySOM-5CSx Carrier Board Design Guide for further recommendations.

#### *MSEL[0:4] (FPGA Configuration Mode Select at Power-On-Reset)*

The MSEL should be set to FPPx16 if the design is going to use the FPGA Manager. With MSEL set to FPP, the HPS will be able to load the FPGA using the FPGA manager. This works in both FPPx16 and FPPx32 modes, but partial reconfiguration only works if set to FPPx16. The MSEL may be internally adjusted in the future using the HPS when it is configured first, the initial devices are not able to exercise this functionality. The default MSEL values recommended are b'00000'.

For modules that include the optional DDR memory connected to the FPGA fabric I/Os the FPP configuration modes are not supported because the Bank 3A pins are consumed by the DDR interface. If the FPGA needs to be loaded first, the serial configuration modes are available, but the HPS will not be able to use the FPGA Manager to reconfigure the logic.

When configuring the FPGA through the HPS, MSEL can be:

- FPPx16 or FPPx32 (required for FPGA Manager to function properly)
- FPPx16 mode required to support partial reconfiguration
- Set MSEL to boot peripheral image. Can be from a prom or from the HPS pre-loader.
- Using the internal HPS FPGA Manager

#### Supported MSEL Options

- FPP – Fast Passive Parallel (Modules without FPGA DDR only)

FPP configuration is expected to work on the future module without FPGA DDR and FPPx16 is the default mode to use for booting from HPS.

- PS – Passive Serial

1bit @ 125MHz Max – 10000 and 10001

- AS – Active Serial

1bit or 4bit @ 100MHz Max – 10010 and 10011

- CVP – Config via Protocol (over the PCI Express bus)

This mode is supported for production Cyclone V silicon, but not for the modules shipped with early silicon. These early silicon modules are identified with a -X indicator at the end of their Critical Link model number, Table 10.

Because the MSEL connections are dedicated inputs that should be tied directly to a power supply or ground, they are arranged on the edge connector to help isolate clock signals from crosstalk. They are also used for return current paths to improve signal integrity. To get this benefit, there are 1000pF capacitors on each of these signals on the module. The baseboard design must also include these caps to get the additional return current path benefits if they are not directly connected to ground.

### **Debug LEDs**

There are 5 debug LEDs on the MitySOM-5CSx module. Three of them are on/off status LEDs tied to a specific condition and the other two are controlled by software through the LED controller on the I2C0 interface, Table 1.

The LEDs have been identified in Figure 2.

### ***General Status LED's***

#### **Trace Debug**

D3 indicates that the JTAG/TRACE adapter board has been inserted into J2 of the module and was detected.

#### **Power OK**

D4 indicates the MitySOM-5CSx on-module +3.3V supply is operating.

#### **Configuration Debug**

D2 indicates that FPGA configuration is not complete by lighting a yellow LED. This is only a warning rather than an error because the HPS can still boot and load the FPGA.

### ***I2C Controllable LED's***

#### **Status Feedback**

The first LED, D1, is an RGB LED which is controlled when using the UBoot image provided by Critical Link.

The second LED, D5, is a green LED that is also controlled by the LED controller on the I2C0 interface.

### Software and Application Development Support

Users of the MitySOM-5CSx are encouraged to develop applications using the MitySOM-5CSx software development kit provided by Critical Link LLC. The SDK is an expansion of the Intel platform support package for the Cyclone V and includes an implementation of a Yocto Project-compatible board support package providing an Angstrom based Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger. Additional embedded Linux support is available from TimeSys, Inc. Please visit <https://support.criticallink.com/> to utilize our support resources.

### Growth Options

The MitySOM-5CSx has been designed to support several upgrade options. These options include a range of speed grades, FPGA DDR memory, I/O, main DDR memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact a Critical Link sales representative.

### Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

**Table 5: Absolute Maximum Ratings**

Maximum Supply Voltage (+5VIN)	5.2V
Storage Temperature Range	-55°C to 150°C

### Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-5CSx. For specifications not contained in this table please contact a Critical Link sales representative. Please see the Thermal Management section below concerning ambient/operating temperature recommendations.

**Table 6: Module Component Temperature Ratings (minimum)**

Temperature Range	Component Ratings
Commercial (-RC)	0°C to 70°C
Industrial (-RI)	-40°C to 85°C

## Thermal Management

The MitySOM-5CSx module requires careful consideration of thermal management. Depending on processor load, thermal management may be required for operation at room temperatures and above. The primary thermal concern is with the Cyclone V SoC device. Even when idle, case temperature on this device rises significantly. Additional processing activity will require more power consumption and more heat dissipation.

Critical Link has operated the MitySOM-5CSx module without a heat sink or air flow on bench tops at room temperatures for long periods of time without issue.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-5CSx into an end product.

Critical Link has developed a sample heat-spreader that is compatible with the MitySOM-5CSx. Please contact your Critical Link representative for further details.

Every end product is different and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications. We recommend that customers utilize Intel's Early Power Estimator (EPE) for the Cyclone V. This utility will assist in estimating the potential power usage of the processor for a given application. Details can be found on the [PowerPlay EPE<sup>\[4\]</sup>](#) page at Intel.com. In order to achieve reliable operation at the maximum specified operating temperatures it has been determined that heat dissipation will likely be required.

## Example Thermal Dissipation Scenarios

By utilizing the PowerPlay EPE for the Cyclone V SoC Critical Link has provided some example scenarios detailing the effects of different cooling fin and airflows. Please be advised these are only estimations based on the Intel modeling tool that are only being used to illustrate the effect of different heat dissipation techniques and are not tested conditions by Critical Link.

Table 7: Example EPE Based Scenarios

Cyclone V Power	Fin Size	Airflow	Max Ambient
2.90W	23 mm	200 LFM	71°C
4.25W	15 mm	None	49°C
4.25W	15 mm	100 LFM	55°C
4.25W	15 mm	400 LFM	65°C
4.25W	23 mm	200 LFM	65°C
4.25W	28 mm	400 LFM	67°C

### Card-Edge Interface Description

The primary interface connector for the MitySOM-5CSx is the 314-pin card edge interface which contains 7 classes of signals:

- Power (**PWR**)
  - Input – Input power to the module
  - Output – Voltage supply from the module
  - Enable – Voltage enable signal from the module for sequencing on carrier boards
- Bank IO Power to the module (**PWR\_VIO**)
- FPGA Bank Power (**PWR\_FPGA**)
- Dedicated signals mapped to the Cyclone V SoC HPS / FPGA pins (5CSx\_D)
- Multi-function signals mapped to the Cyclone V SoC HPS pins (5CSx\_HPS)
- General purpose I/O pins mapped to the Cyclone V SoC FPGA pins (5CSx\_IO)
- General purpose I/O pins available on expanded IO modules; no FPGA DDR memory present on the module (5CSx\_EIO)
- Dedicated 3.125Gbps Transceiver signals mapped to the Cyclone V SoC (5CSX\_GXB). Only available on Cyclone V SX based modules.

Table 8 contains a summary of the MitySOM-5CSx pin-mapping.

### Card-Edge Mating Connector

The MitySOM-5CSx module mates with a single connector that contains all of the power and I/O for the module. The mating socket is a 314-pin MXM 3.0 type connector. An example connector is a JAE - MM70-314-310B1-1-R300 which is available from distributors such as DigiKey and Mouser.

More information is available in the MitySOM-5CSx Carrier Board Design guide from Critical Link.

**Table 8: MitySOM-5CSx Edge Connector Pin-Out**

Module Pin Number	Class	SCH NET Name	Bank Number	Cyclone V 5CSXFC6 U672	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin
1	PWR - Input	+5VIN	-	-			
2	5CSx_HPS	UART0_RX	7A	B19	CAN0_RX	UART0_RX	SPIM1_
3	PWR - Input	+5VIN	-	-			
4	5CSx_HPS	UART0_TX,CLKSELO	7A	C16	CAN0_TX,CLKSELO	UART0_TX,CLKSELO	SPIM1_
5	PWR - Input	+5VIN	-	-			
6	5CSx_HPS	UART0_RTS/SPIM0_MOSI/I2C1_SCL/HPS_GPIO58	7A	C17	SPIM0_MOSI	I2C1_SCL	UART0_
7	PWR - Input	+5VIN	-	-			
8	5CSx_HPS	UART0_CTS/SPIM0_CLK/I2C1_SDA/HPS_GPIO57	7A	A18	SPIM0_CLK	I2C1_SDA	UART0_
9	PWR - Input	+5VIN	-	-			
10	5CSx_HPS	CAN0_TX,CLKSEL1/HPS_GPIO62	7A	H17	UART0_TX,CLKSEL1	CAN0_TX,CLKSEL1	SPIM1_
11	PWR	GND	-	-			
12	5CSx_HPS	CAN0_RX/SPIM0_SS1/HPS_GPIO61	7A	A17	UART0_RX	CAN0_RX	SPIM0_
13	PWR	GND	-	-			
14	5CSx_HPS	CAN1_TX,BOOTSELO/SPIM0_SS0/HPS_GPIO60	7A	J17	SPIM0_SS0	CAN1_TX,BOOTSELO	UART1_
15	PWR	GND	-	-			
16	5CSx_HPS	CAN1_RX/SPIM0_MISO/HPS_GPIO59	7A	B18	SPIM0_MISO	CAN1_RX	UART1_
17	PWR	GND	-	-			
18	PWR - Input	+3VBAT	-	-			
19	5CSx_D	B7A_HPS_CLK2	7A	D20			
20	5CSx_HPS	TRACE_D7/SPI1_MISO/HPS_GPIO56	7A	C18	TRACE_D7	SPI1_MISO	I2C0_SC
21	5CSx_D	nPERSTL1/B5A_RX_R6n	5A	W15			
22	5CSx_HPS	TRACE_D6/SPI1_SS0/HPS_GPIO55	7A	A19	TRACE_D6	SPI1_SS0	I2C0_SD
23	5CSx_D	HPS_nRST	7A	A23			
24	5CSx_HPS	TRACE_D5/SPI1_MOSI/CAN1_TX/HPS_GPIO54	7A	J18	TRACE_D5	SPI1_MOSI	CAN1_T
25	5CSx_D	HPS_nPOR	7A	H19			
26	5CSx_HPS	TRACE_D4/SPI1_CLK/CAN1_RX/HPS_GPIO53	7A	A20	TRACE_D4	SPI1_CLK	CAN1_F
27	5CSx_D	B3B_FPGA_DCLK	3A	AA8			
28	5CSx_HPS	TRACE_D3/SPI0_SS0/I2C1_SCL/HPS_GPIO52	7A	K18	TRACE_D3	SPI0_SS0	I2C1_SC
29	5CSx_D	MSEL0	9A	J10			
30	5CSx_HPS	TRACE_D2/SPI0_MISO/I2C1_SDA/HPS_GPIO51	7A	A21	TRACE_D2	SPI0_MISO	I2C1_SD
31	5CSx_D	B3B_FPGA_D3	3A	AB6			
32	5CSx_HPS	TRACE_D1/SPI0_MOSI/HPS_GPIO50	7A	B21	TRACE_D1	SPI0_MOSI	UART0_
33	5CSx_D	B3B_FPGA_D2	3A	AC5			
34	5CSx_HPS	TRACE_D0/SPI0_CLK/HPS_GPIO49	7A	A22	TRACE_D0	SPI0_CLK	UART0_
35	5CSx_D	B3B_FPGA_D1	3A	AC6			
36	5CSx_D	MSEL4	9A	K9			
37	5CSx_D	B3B_FPGA_D0	3A	AD7			
38	5CSx_HPS	TRACE_CLK/HPS_GPIO48	7A	C21	TRACE_CLK		
39	5CSx_D	nCONFIG	9A	F7			
40	PWR	GND	-	-			
41	5CSx_D	nSTATUS	9A	H8			
42	5CSx_EIO	B5A_TX_R5_P/NC with FPGA DDR Memory	5A/NC	AC24			
43	5CSx_D	nCSO	3A	AA6			
44	5CSx_EIO	B5A_TX_R5_N/NC with FPGA DDR Memory	5A/NC	AB23			
45	5CSx_D	MSEL1	9A	H9			
46	PWR-Enable	VIO_ENABLE_2V5	-	-			

Module Pin Number	Class	SCH NET Name	Bank Number	Cyclone V 5CSXFC6 U672	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin
47	5CSx_EIO	B5A_TX_R1_P/NC with FPGA DDR Memory	5A/NC	AF26			
48	PWR_VIO	+VIO_4A	-	-			
49	5CSx_EIO	B5A_TX_R1_N/NC with FPGA DDR Memory	5A/NC	AE26			
50	PWR	GND	-	-			
51	5CSx_D	MSEL2	9A	G6			
52	5CSx_IO	B4A_TX_B80p/DQ8B/B_DM_4	4A	AF27			
53	5CSx_EIO	B5A_TX_R3_P/NC with FPGA DDR Memory	5A/NC	AE25			
54	5CSx_IO	B4A_TX_B80n/DQ8B/B_DQ_39	4A	AF28			
55	5CSx_EIO	B5A_TX_R3_N/NC with FPGA DDR Memory	5A/NC	AD26			
56	5CSx_IO	B4A_TX_B77p/DQ8B/B_DQ_38	4A	AG28			
57	5CSx_D	MSEL3	9A	K10			
58	5CSx_IO	B4A_TX_B77n/DQ8B/GND	4A	AH27			
59	PWR	GND	-	-			
60	5CSx_IO	B4A_TX_B76n/DQ8B/B_DQ_35	4A	AH26			
61	5CSx_IO	B4A_RX_B78p/DQ8B/B_DQ_37	4A	AF25			
62	5CSx_IO	B4A_TX_B73p/DQ8B/B_DQ_34	4A	AG26			
63	5CSx_IO	B4A_RX_B78n/DQ8B/B_DQ_36	4A	AG25			
64	5CSx_IO	B4A_TX_B72p/DQ7B/B_DM_3	4A	AG24			
65	5CSx_IO	B4A_RX_B75p/DQS8B/B_DQS_4	4A	AC22			
66	5CSx_IO	B4A_TX_B72n/DQ7B/B_DQ_31	4A	AH24			
67	5CSx_IO	B4A_RX_B75n/DQSn8B/B_DQS#_4	4A	AC23			
68	5CSx_IO	B4A_TX_B69p/DQ7B/B_DQ_30	4A	AH23			
69	5CSx_IO	B4A_RX_B74p/DQ8B/B_DQ_33	4A	AE24			
70	5CSx_IO	B4A_TX_B69n/DQ7B/GND	4A	AH22			
71	5CSx_IO	B4A_RX_B74n/DQ8B/B_DQ_32	4A	AE23			
72	PWR	GND	-	-			
73	5CSx_IO	B4A_RX_B70p/DQ7B/B_DQ_29	4A	AG23			
74	5CSx_IO	B4A_TX_B68n/DQ7B/B_DQ_27	4A	AH21			
75	5CSx_IO	B4A_RX_B70n/DQ7B/B_DQ_28	4A	AF23			
76	5CSx_IO	B4A_TX_B65p/DQ7B/B_DQ_26	4A	AG21			
77	5CSx_IO	B4A_RX_B67p/DQS7B/B_DQS_3	4A	AD23			
78	5CSx_IO	B4A_TX_B64p/DQ6B/B_DM_2	4A	AF20			
79	5CSx_IO	B4A_RX_B67n/DQSn7B/B_DQS#_3	4A	AE22			
80	5CSx_IO	B4A_TX_B64n/DQ6B/B_DQ_23	4A	AG20			
81	PWR	GND	-	-			
82	5CSx_IO	B4A_TX_B61p/DQ6B/B_DQ_22	4A	AG19			
83	5CSx_IO	B4A_RX_B66p/DQ7B/B_DQ_25	4A	AF22			
84	5CSx_IO	B4A_TX_B61n/DQ6B/GND	4A	AH19			
85	5CSx_IO	B4A_RX_B66n/DQ7B/B_DQ_24	4A	AF21			
86	5CSx_IO	B4A_TX_B60p/B_RESET#	4A	AG18			
87	5CSx_IO	B4A_RX_B62p/DQ6B/B_DQ_21	4A	AE20			
88	5CSx_IO	B4A_TX_B60n/DQ6B/B_DQ_19	4A	AH18			
89	5CSx_IO	B4A_RX_B62n/DQ6B/B_DQ_20	4A	AD20			
90	5CSx_IO	B4A_TX_B57p/DQ6B/B_DQ_18	4A	AF18			
91	5CSx_IO	B4A_RX_B59p/DQS6B/B_DQS_2	4A	AA19			
92	PWR	GND	-	-			
93	5CSx_IO	B4A_RX_B59n/DQSn6B/B_DQS#_2	4A	AA18			
94	5CSx_IO	B4A_TX_B56p/DQ5B/B_DM_1	4A	AH17			
95	5CSx_IO	B4A_RX_B58p/DQ6B/B_DQ_17	4A	AE19			

Module Pin Number	Class	SCH NET Name	Bank Number	Cyclone V 5CSXFC6 U672	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin
96	5CSx_IO	B4A_TX_B56n/DQ5B/B_DQ_15	4A	AH16			
97	5CSx_IO	B4A_RX_B58n/DQ6B/B_DQ_16	4A	AD19			
98	5CSx_IO	B4A_TX_B53p/DQ5B/B_DQ_14	4A	AG15			
99	5CSx_IO	CLK3p/B4A_RX_B55p	4A	Y15			
100	5CSx_IO	B4A_TX_B53n/DQ5B/B_CKE_0	4A	AH14			
101	5CSx_IO	CLK3n/B4A_RX_B55n	4A	AA15			
102	5CSx_IO	B4A_TX_B52p/B_CKE_1	4A	AG14			
103	PWR	GND	-	-			
104	5CSx_IO	B4A_TX_B52n/DQ5B/B_DQ_11	4A	AH13			
105	5CSx_IO	B4A_RX_B54p/DQ5B/B_DQ_13	4A	AD17			
106	5CSx_IO	B4A_TX_B49p/DQ5B/B_DQ_10	4A	AH12			
107	5CSx_IO	B4A_RX_B54n/DQ5B/B_DQ_12	4A	AE17			
108	PWR	GND	-	-			
109	5CSx_IO	B4A_RX_B51p/DQS5B/B_DQS_1	4A	W14			
110	5CSx_IO	B4A_TX_B48p/DQ4B/B_DM_0	4A	AG11			
111	5CSx_IO	B4A_RX_B51n/DQSn5B/B_DQS#_1	4A	V13			
112	5CSx_IO	B4A_TX_B48n/DQ4B/B_DQ_7	4A	AH11			
113	5CSx_IO	B4A_RX_B50p/DQ5B/B_DQ_9	4A	AF17			
114	5CSx_IO	B4A_TX_B45p/DQ4B/B_DQ_6	4A	AG10			
115	5CSx_IO	B4A_RX_B50n/DQ5B/B_DQ_8	4A	AG16			
116	5CSx_IO	B4A_TX_B45n/DQ4B/B_ODT_1	4A	AH9			
117	5CSx_IO	CLK2p/B4A_RX_B47p	4A	Y13			
118	5CSx_IO	B4A_TX_B44p/B_ODT_0	4A	AG9			
119	5CSx_IO	CLK2n/B4A_RX_B47n	4A	AA13			
120	5CSx_IO	B4A_TX_B44n/DQ4B/B_DQ_3	4A	AH8			
121	5CSx_IO	B4A_RX_B46p/DQ4B/B_DQ_5	4A	AF15			
122	5CSx_IO	B4A_TX_B41p/DQ4B/B_DQ_2	4A	AG8			
123	5CSx_IO	B4A_RX_B46n/DQ4B/B_DQ_4	4A	AE15			
124	5CSx_IO	RZQ_0/B4A_TX_B41n	4A	AH7			
125	PWR	GND	-	-			
126	-	Key <sup>3</sup>	-	-			
127	-	Key <sup>3</sup>	-	-			
128	-	Key <sup>3</sup>	-	-			
129	-	Key <sup>3</sup>	-	-			
130	-	Key <sup>3</sup>	-	-			
131	-	Key <sup>3</sup>	-	-			
132	-	Key <sup>3</sup>	-	-			
133	5CSx_IO	B4A_RX_B43p/DQS4B/B_DQS_0	4A	U14			
134	PWR_VIO	+VIO_3B	-	-			
135	5CSx_IO	B4A_RX_B43n/DQSn4B/B_DQS#_0	4A	U13			
136	PWR	GND	-	-			
137	5CSx_IO	B4A_RX_B42p/DQ4B/B_DQ_1	4A	AG13			
138	5CSx_IO	B3B_TX_B29p/DQ2B/B_A_10	3B	AE8			
139	5CSx_IO	B4A_RX_B42n/DQ4B/B_DQ_0	4A	AF13			
140	5CSx_IO	B3B_TX_B29n/DQ2B/B_A_11	3B	AF9			
141	5CSx_IO	B3B_RX_B38p/DQ3B/B_A_4	3B	AE12			
142	5CSx_IO	B3B_TX_B28p/B_A_12	3B	AE7			
143	5CSx_IO	B3B_RX_B38n/DQ3B/B_A_5	3B	AD12			
144	5CSx_IO	B3B_TX_B28n/DQ2B/B_A_13	3B	AF8			



Module Pin Number	Class	SCH NET Name	Bank Number	Cyclone V 5CSXFC6 U672	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin
145	5CSx_IO	B3B_RX_B30p/DQ2B/B_A_8	3B	AD11			
146	5CSx_IO	B3B_TX_B32p/DQ2B/B_CAS#	3B	AF5			
147	5CSx_IO	B3B_RX_B30n/DQ2B/B_A_9	3B	AE11			
148	5CSx_IO	B3B_TX_B32n/DQ2B/B_RAS#	3B	AF6			
149	5CSx_IO	B3B_RX_B34p/DQ3B/B_BA_1	3B	AF11			
150	5CSx_IO	B3B_TX_B33p/DQ3B/B_BA_0	3B	AF7			
151	5CSx_IO	B3B_RX_B34n/DQ3B/B_BA_2	3B	AF10			
152	5CSx_IO	B3B_TX_B33n/GND	3B	AG6			
153	PWR	GND	-	-			
154	5CSx_IO	B3B_TX_B40p/DQ3B/B_A_0	3B	AH6			
155	5CSx_IO	B3B_RX_B35p/DQ3B/B_CK	3B	T13			
156	5CSx_IO	B3B_TX_B40n/DQ3B/B_A_1	3B	AH5			
157	5CSx_IO	B3B_RX_B35n/DQ3B/B_CK#	3B	T12			
158	PWR	GND	-	-			
159	5CSx_IO	B3B_RX_B27p/DQ3B/B_CS#_0	3B	T11			
160	5CSx_IO	CLKOUT0,CLKOUTp,FPLL_BL_FB/ B3B_TX_B37p/DQ3B/B_A_2	3B	AG5			
161	5CSx_IO	B3B_RX_B27n/DQ3B/B_CS#_1	3B	U11			
162	5CSx_IO	CLKOUT1,CLKOUTn/B3B_TX_B37n/DQ3B/B_A_3	3B	AH4			
163	5CSx_IO	CLK1p/B3B_RX_B39p	3B	V12			
164	5CSx_IO	B3B_TX_B25p/DQ2B/B_WE#	3B	AE4			
165	5CSx_IO	CLK1n/B3B_RX_B39n	3B	W12			
166	5CSx_IO	B3B_TX_B25n/GND	3B	AF4			
167	5CSx_IO	CLK0p,FPLL_BL_FBp/B3B_RX_B31p	3B	V11			
168	5CSx_IO	B3B_TX_B36p/B_A_6	3B	AH3			
169	5CSx_IO	CLK0n,FPLL_BL_FBn/B3B_RX_B31n	3B	W11			
170	5CSx_IO	B3B_TX_B36n/DQ3B/B_A_7	3B	AH2			
171	5CSx_IO	B3B_RX_B26p/DQ2B/B_A_14	3B	AD10			
172	5CSx_IO	CLK6p,FPLL_TL_FBp/B8A_RX_T9p	8A	E11			
173	5CSx_IO	B3B_RX_B26n/DQ2B/B_A_15	3B	AE9			
174	5CSx_IO	CLK6n,FPLL_TL_FBn/B8A_RX_T9n	8A	D11			
175	PWR	GND	-	-			
176	PWR_VIO	+VIO_8A	-	-			
177	5CSx_IO	CLK7p/B8A_RX_T1p	8A	D12			
178	5CSx_IO	CLKOUT0,CLKOUTp,FPLL_TL_FB/B8A_TX_T4p	8A	E8			
179	5CSx_IO	CLK7n/B8A_RX_T1n	8A	C12			
180	5CSx_IO	CLKOUT1,CLKOUTn/B8A_TX_T4n	8A	D8			
181	PWR_VIO	VIO_3A5A5B/NC with FPGA DDR Memory	-	-			
182	PWR	GND	-	-			
183	5CSx_EIO	B5A_RX_R2_P/NC with FPGA DDR Memory	5A/NC	AA20			
184	5CSx_EIO	B3A_TX_B8_P/NC with FPGA DDR Memory	3A/NC	AC4			
185	5CSx_EIO	B5A_RX_R2_N/NC with FPGA DDR Memory	5A/NC	Y19			
186	5CSx_EIO	B3A_TX_B8_N/NC with FPGA DDR Memory	3A/NC	AD4			
187	5CSx_EIO	B5A_RX_R4_P/NC with FPGA DDR Memory	5A/NC	Y17			
188	5CSx_EIO	B3A_TX_B6_P/NC with FPGA DDR Memory	3A/NC	AD5			
189	5CSx_EIO	B5A_RX_R4_N/NC with FPGA DDR Memory	5A/NC	Y18			
190	5CSx_EIO	B3A_TX_B6_N/NC with FPGA DDR Memory	3A/NC	AE6			
191	5CSx_EIO	B3A_RX_B7_P/NC with FPGA DDR Memory	3A/NC	Y11			
192	5CSx_EIO	B3A_TX_B4_P/NC with FPGA DDR Memory	3A/NC	AA4			



Module Pin Number	Class	SCH NET Name	Bank Number	Cyclone V 5CSXFC6 U672	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin
193	5CSx_EIO	B3A_RX_B7_N/NC with FPGA DDR Memory	3A/NC	AA11			
194	5CSx_EIO	B3A_TX_B4_N/NC with FPGA DDR Memory	3A/NC	AB4			
195	5CSx_EIO	B3A_RX_B5_P/NC with FPGA DDR Memory	3A/NC	U10			
196	5CSx_EIO	B3A_TX_B2_P/NC with FPGA DDR Memory	3A/NC	Y5			
197	5CSx_EIO	B3A_RX_B5_N/NC with FPGA DDR Memory	3A/NC	V10			
198	5CSx_EIO	B3A_TX_B2_N/NC with FPGA DDR Memory	3A/NC	Y4			
199	5CSx_EIO	B3A_RX_B3_P/NC with FPGA DDR Memory	3A/NC	U9			
200	PWR	GND	-	-			
201	5CSx_EIO	B3A_RX_B3_N/NC with FPGA DDR Memory	3A/NC	T8			
202	5CSX_GXB	GXB_RX_0_P	GXB_L0	AF2			
203	5CSx_EIO	B3A_RX_B1_P/NC with FPGA DDR Memory	3A/NC	W8			
204	5CSX_GXB	GXB_RX_0_N	GXB_L0	AF1			
205	5CSx_EIO	B3A_RX_B1_N/NC with FPGA DDR Memory	3A/NC	Y8			
206	PWR	GND	-	-			
207	PWR	GND	-	-			
208	5CSX_GXB	GXB_RX_1_P	GXB_L0	AB2			
209	5CSX_GXB	GXB_TX_0_P	GXB_L0	AD2			
210	5CSX_GXB	GXB_RX_1_N	GXB_L0	AB1			
211	5CSX_GXB	GXB_TX_0_N	GXB_L0	AD1			
212	PWR	GND	-	-			
213	PWR	GND	-	-			
214	5CSX_GXB	GXB_RX_2_P	GXB_L0	V2			
215	5CSX_GXB	GXB_TX_1_P	GXB_L0	Y1			
216	5CSX_GXB	GXB_RX_2_N	GXB_L0	Y2			
217	5CSX_GXB	GXB_TX_1_N	GXB_L0	V1			
218	PWR	GND	-	-			
219	PWR	GND	-	-			
220	5CSX_GXB	GXB_REFCLK0_P	GXB_L0	V5			
221	5CSX_GXB	GXB_TX_2_P	GXB_L0	T2			
222	5CSX_GXB	GXB_REFCLK0_N	GXB_L0	V4			
223	5CSX_GXB	GXB_TX_2_N	GXB_L0	T1			
224	PWR	GND	-	-			
225	PWR	GND	-	-			
226	5CSX_GXB	GXB_RX_3_P	GXB_L1	P2			
227	5CSX_GXB	GXB_REFCLK1_P	GXB_L1	P8			
228	5CSX_GXB	GXB_RX_3_N	GXB_L1	P1			
229	5CSX_GXB	GXB_REFCLK1_N	GXB_L1	N8			
230	PWR	GND	-	-			
231	PWR	GND	-	-			
232	5CSX_GXB	GXB_RX_4_P	GXB_L1	K2			
233	5CSX_GXB	GXB_TX_3_P	GXB_L1	M2			
234	5CSX_GXB	GXB_RX_4_N	GXB_L1	K1			
235	5CSX_GXB	GXB_TX_3_N	GXB_L1	M1			
236	PWR	GND	-	-			
237	PWR	GND	-	-			
238	5CSX_GXB	GXB_RX_5_P	GXB_L1	F2			
239	5CSX_GXB	GXB_TX_4_P	GXB_L1	H2			
240	5CSX_GXB	GXB_RX_5_N	GXB_L1	F1			
241	5CSX_GXB	GXB_TX_4_N	GXB_L1	H1			

Module Pin Number	Class	SCH NET Name	Bank Number	Cyclone V 5CSXFC6 U672	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin
242	5CSx_D	USB1_FAULT_N	-	-			
243	PWR	GND	-	-			
244	5CSx_HPS	SDMMC_CLK_IN/USB0_CLK/HPS_GPIO44	7C	B12	SDMMC_CLK_IN	USB0_CLK	
245	5CSX_GXB	GXB_TX_5_P	GXB_L1	D2			
246	5CSx_D	USB1_PS_ON	-	-			
247	5CSX_GXB	GXB_TX_5_N	GXB_L1	D1			
248	5CSx_HPS	SDMMC_D1/USB0_D3/HPS_GPIO39	7C	B6	SDMMC_D1	USB0_D3	
249	5CSx_D	QSPI_SS0,BOOTSEL1/HPS_GPIO33	7B	A6	QSPI_SS0,BOOTSEL1		
250	5CSx_HPS	SDMMC_D0/USB0_D2/HPS_GPIO38	7C	C13	SDMMC_D0	USB0_D2	
251	5CSx_HPS	RGMI11_RX_CLK/NAND_DQ5/HPS_GPIO24	7B	J12	NAND_DQ5	RGMI11_RX_CLK	USB1_D
252	5CSx_HPS	SDMMC_PWREN/USB0_D1/HPS_GPIO37	7C	A5	SDMMC_PWREN	USB0_D1	
253	5CSx_HPS	HPS_GPIO28,BOOTSEL2/NAND_WE	7B	D15	NAND_WE	QSPI_SS1	
254	5CSx_HPS	SDMMC_CLK/USB0_STP/HPS_GPIO45	7C	B8	SDMMC_CLK	USB0_STP	
255	5CSx_HPS	RGMI11_RX_CTL/NAND_DQ3/HPS_GPIO22	7B	J13	NAND_DQ3	RGMI11_RX_CTL	USB1_D
256	5CSx_D	RTC_PSW/IRQ2_N	-	-			
257	5CSx_HPS	RGMI11_RXD0/NAND_DQ0/HPS_GPIO19	7B	A14	NAND_DQ0	RGMI11_RXD0	
258	5CSx_HPS	SDMMC_CMD/USB0_D0/HPS_GPIO36	7C	D14	SDMMC_CMD	USB0_D0	
259	5CSx_HPS	RGMI11_RXD1/NAND_DQ6/HPS_GPIO25	7B	A11	NAND_DQ6	RGMI11_RXD1	USB1_D
260	5CSx_HPS	SDMMC_D3/USB0_NXT/HPS_GPIO47	7C	B9	SDMMC_D3	USB0_NXT	
261	5CSx_HPS	RGMI11_RXD2/NAND_DQ7/HPS_GPIO26	7B	C15	NAND_DQ7	RGMI11_RXD2	
262	5CSx_HPS	SDMMC_D2/USB0_DIR/HPS_GPIO46	7C	B11	SDMMC_D2	USB0_DIR	
263	5CSx_HPS	RGMI11_RXD3/NAND_WP/HPS_GPIO27	7B	A9	NAND_WP	RGMI11_RXD3	QSPI_S
264	5CSx_HPS	SDMMC_D4/USB0_D4/HPS_GPIO40	7C	H13	SDMMC_D4	USB0_D4	
265	5CSx_HPS	RGMI11_MDC/NAND_DQ2/I2C3_SCL/HPS_GPIO21	7B	A13	NAND_DQ2	RGMI11_MDC	I2C3_SC
266	5CSx_HPS	SDMMC_D5/USB0_D5/HPS_GPIO41	7C	A4	SDMMC_D5	USB0_D5	
267	5CSx_HPS	RGMI11_MDIO/NAND_DQ1/I2C3_SDA/HPS_GPIO20	7B	E16	NAND_DQ1	RGMI11_MDIO	I2C3_SD
268	5CSx_HPS	SDMMC_D6/USB0_D6/HPS_GPIO42	7C	H12	SDMMC_D6	USB0_D6	
269	5CSx_HPS	RGMI11_TX_CTL/NAND_DQ4/HPS_GPIO23	7B	A12	NAND_DQ4	RGMI11_TX_CTL	USB1_D
270	5CSx_HPS	SDMMC_D7/USB0_D7/HPS_GPIO43	7C	B4	SDMMC_D7	USB0_D7	
271	5CSx_HPS	RGMI11_TX_CLK/NAND_ALE/HPS_GPIO14	7B	J15	NAND_ALE	RGMI11_TX_CLK	QSPI_S
272	5CSx_D	USB1_ID	-	-			
273	PWR-Output	+1.8VOUT	-	-			
274	5CSx_D	USB1_D_N	-	-			
275	5CSx_HPS	RGMI11_TXD3/NAND_RB/HPS_GPIO18	7B	D17	NAND_RB	RGMI11_TXD3	USB1_D
276	5CSx_D	USB1_D_P	-	-			
277	5CSx_HPS	RGMI11_TXD2/NAND_RE/HPS_GPIO17	7B	A15	NAND_RE	RGMI11_TXD2	USB1_D
278	5CSx_D	+USB1_VBUS	-	-			
279	5CSx_HPS	RGMI11_TXD1/NAND_CLE/HPS_GPIO16	7B	J14	NAND_CLE	RGMI11_TXD1	USB1_D
280	PWR	GND	-	-			
281	5CSx_HPS	RGMI11_TXD0/NAND_CE/HPS_GPIO15	7B	A16	NAND_CE	RGMI11_TXD0	USB1_D
E1	-	Reserved (Future Use) - 10-Pin Equivalent	-	-			
E2	-	Reserved (Future Use) - 10-Pin Equivalent	-	-			
E3	PWR	GND - 10-Pin Equivalent	-	-			
E4	PWR	GND - 10-Pin Equivalent	-	-			
<b>On-Module HPS Interfaces Below (No External Access)</b>							
I2C	5CSx_D	I2C0_SDA	7A	C19	I2C0_SDA	UART1_RX	SPIM1_C
I2C	5CSx_D	I2C0_SCL	7A	B16	I2C0_SCL	UART1_TX	SPIM1_C
QSPI	5CSx_D	QSPI_I00/USB1_CLK/HPS_GPIO29	7B	A8	QSPI_I00		USB1_C

Module Pin Number	Class	SCH NET Name	Bank Number	Cyclone V 5CSXFC6 U672	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin
QSPI	5CSx_D	QSPI_IO1/USB1_STP/HPS_GPIO30	7B	H16	QSPI_IO1		USB1_S
QSPI	5CSx_D	QSPI_IO2/USB1_DIR/HPS_GPIO31	7B	A7	QSPI_IO2		USB1_D
QSPI	5CSx_D	QSPI_IO3/USB1_NXT/HPS_GPIO32	7B	J16	QSPI_IO3		USB1_N
QSPI	5CSx_D	QSPI_CLK/HPS_GPIO34	7B	C14	QSPI_CLK		
QSPI	5CSx_D	QSPI_SS1/HPS_GPIO35	7B	B14	QSPI_SS1		
QSPI	5CSx_D	HPS_GPIO0	7D	E4	RGMIIO_TX_CLK		
USB1	5CSx_D	HPS_GPIO9	7D	C6	RGMIIO_TX_CTL		
USB1	5CSx_D	USB1_D0	7D	C10	RGMIIO_TXD0	USB1_D0	
USB1	5CSx_D	USB1_D1	7D	F5	RGMIIO_TXD1	USB1_D1	
USB1	5CSx_D	USB1_D2	7D	C9	RGMIIO_TXD2	USB1_D2	
USB1	5CSx_D	USB1_D3	7D	C4	RGMIIO_TXD3	USB1_D3	
USB1	5CSx_D	USB1_D4	7D	C8	RGMIIO_RXD0	USB1_D4	
USB1	5CSx_D	USB1_D5	7D	D4	RGMIIO_MDIO	USB1_D5	I2C2_SD
USB1	5CSx_D	USB1_D6	7D	C7	RGMIIO_MDC	USB1_D6	I2C2_SC
USB1	5CSx_D	USB1_D7	7D	F4	RGMIIO_RX_CTL	USB1_D7	
USB1	5CSx_D	USB1_CLK	7D	G4	RGMIIO_RX_CLK	USB1_CLK	
USB1	5CSx_D	USB1_STP	7D	C5	RGMIIO_RXD1	USB1_STP	
USB1	5CSx_D	USB1_DIR	7D	E5	RGMIIO_RXD2	USB1_DIR	
USB1	5CSx_D	USB1_NXT	7D	D5	RGMIIO_RXD3	USB1_NXT	

**Notes:**

- 1) For more information about pin definitions and pin connection guidelines please refer to the Cyclone V Device Connection Guidelines ([PCG-01014](#))
- 2) The Keys are shown in the numbering but no actual pins exist. The connector is 314-pins counted as follows: 7 for the "keys" plus 40 for the E1, E2, E3 and E4 pin-groups.

## ELECTRICAL CHARACTERISTICS

**Table 9: Electrical Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Voltage supply, volt input.		4.8	5.0	5.15	Volts
I <sub>5.0</sub>	Quiescent Current draw[1]	5CSX-H6-42A 5.0 volt input, 800 MHz Dual Core, 1GB DDR3, no FPGA fabric, Linux idle		420		mA
I <sub>5.0</sub>	Quiescent Current draw[1]	5CSX-H6-42A 5.0 volt input, 800 MHz Dual Core, 1GB DDR3, FPGA fabric programmed with Dev Kit example, Linux idle		540		mA
I <sub>5.0</sub>	Quiescent Current draw[1]	5CSE-L2-3Y8 5.0 volt input, 600 MHz Single Core, 512MB DDR3, no FPGA fabric, Linux idle		354		mA
I <sub>5.0</sub>	Quiescent Current draw[1]	5CSE-L2-3Y8 5.0 volt input, 600 MHz Single Core, 512MB DDR3, FPGA fabric programmed with Dev Kit example, Linux idle		368		mA
I <sub>1.8V-Out</sub>	Output current capability 1.8V supply from MitySOM	Only recommended to support Bank 7B IO signals			500	mA
V <sub>1.8V-Out</sub>	1.8V supply from MitySOM	Only recommended to support Bank 7B IO signals	1.62	1.8	1.98	Volts
I <sub>3VBAT</sub>	RTC Battery Backup Current draw	VBAT = 3.0V, volatile key storage not enabled		600	1100	nA
I <sub>3VBAT</sub>	RTC Battery Backup Current draw	VBAT = 3.0V, Theoretical maximum			4700	nA
<p>1. Power utilization of the MitySOM-5CSX is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external DDR3 RAM utilization.</p>						

## ORDERING INFORMATION

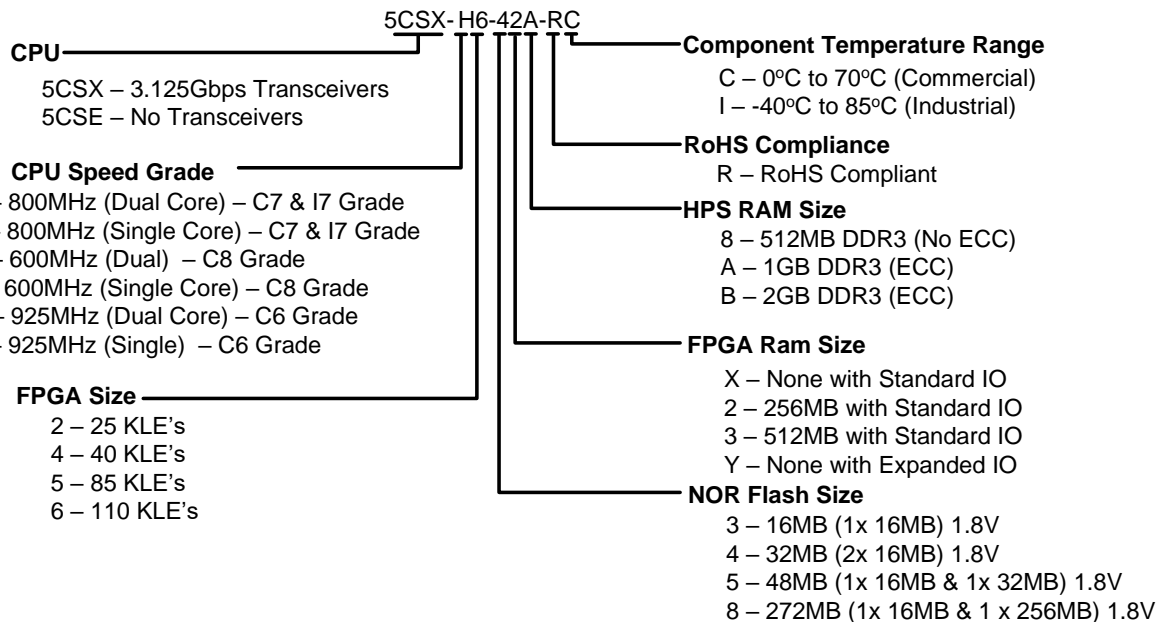
The following table lists the standard module configurations. For shipping status, availability, and lead time of these configurations please contact your Critical Link representative or visit one of our authorized distributors.

**Table 10: Standard Model Numbers**

Model	Cores	CPU MHz	Speed Grade	FPGA KLE	NOR	FPGA I/O	FPGA RAM	HPS RAM	Component Temperature Ratings
5CSE-L2-3Y8-RC	Single	600	8	25	16MB	133	N/A	512MB	0°C to 70° C
5CSE-H4-3YA-RC	Dual	800	7	40	16MB	133	N/A	1GB	0°C to 70° C
5CSE-H4-3YA-RI	Dual	800	7	40	16MB	133	N/A	1GB	-40°C to 85° C
5CSE-H4-8YA-RI	Dual	800	7	40	272MB	133	N/A	1GB	-40°C to 85° C
5CSX-H5-4YA-RC	Dual	800	7	85	32MB	133	N/A	1GB	0°C to 70° C
5CSX-H5-4YA-RI	Dual	800	7	85	32MB	133	N/A	1GB	-40°C to 85° C
5CSX-H6-42A-RC	Dual	800	7	110	32MB	107	256MB	1GB	0°C to 70° C
5CSX-H6-42A-RI	Dual	800	7	110	32MB	107	256MB	1GB	-40°C to 85° C
5CSX-H6-4YA-RC	Dual	800	7	110	32MB	133	N/A	1GB	0°C to 70° C
5CSX-H6-4YA-RI	Dual	800	7	110	32MB	133	N/A	1GB	-40°C to 85° C
5CSX-H6-53B-RC	Dual	800	7	110	48MB	107	512MB	2GB	0°C to 70° C

## MitySOM-5CSx Module Family Model Number Guide

If a module suitable for your specific application is not found in Table 10 please reference the following MitySOM-5CSx model number decoder for configuring a custom module. Please contact your Critical Link representative to determine pricing, lead-time and availability of a custom module.



## MECHANICAL INTERFACE

A mechanical outline of the MitySOM-5CSx is illustrated in Figure 2, below.

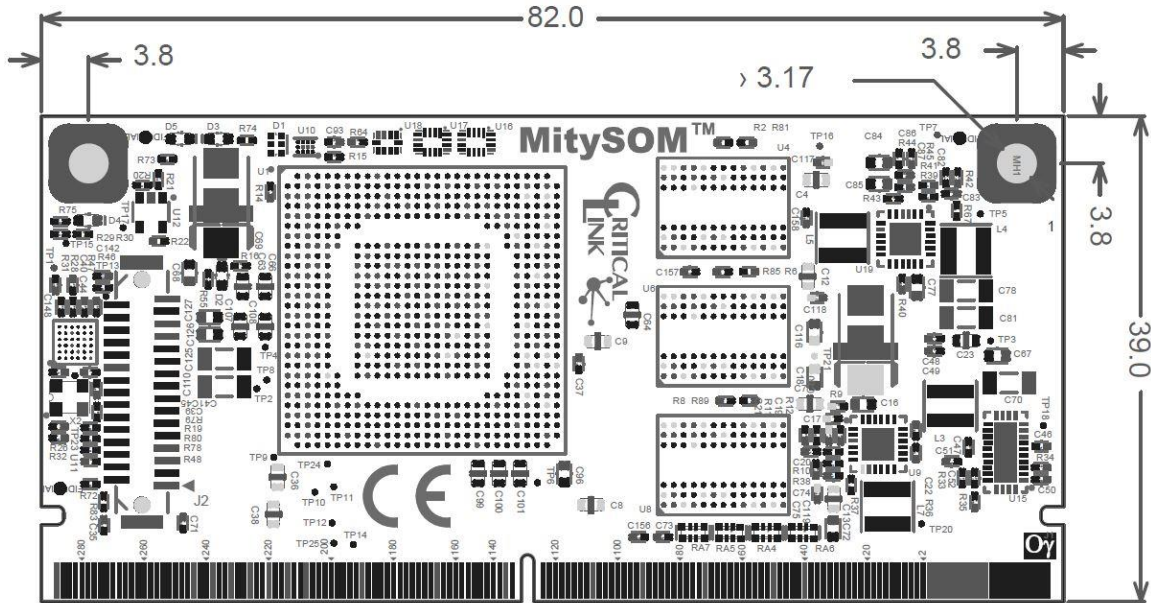


Figure 2 MitySOM-5CSx Mechanical Outline

## REVISION HISTORY

Revision	Date	Change Description
ENGINEERING	May 31, 2013	Preliminary specification
ENGINEERING	September 12, 2013	Initial release
ENGINEERING	March 5, 2014	Update MitySOM product name
ENGINEERING	March 31, 2014	Update memory data
ENGINEERING	November 19, 2014	Modifications for MitySOM-5CSE
ENGINEERING	September 10, 2015	Update tables 1, 3 and 7 and add HPS DDR memory speed. Added module part number decoder to ordering information section.
ENGINEERING	October 12, 2018	Update Altera/Intel documentation links, add additional Table 8 information and add Table 3 for JTAG debug header.
1A	April 25, 2019	General notes enhancements including add Table 3 J2 Hirose Connector, add Model Number Guide to Table 10.

**FOOTNOTES**

[1] [https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/cyclone-v/cv\\_5400a.pdf](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/cyclone-v/cv_5400a.pdf)

[2] [https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/cyclone-v/cv\\_5v4.pdf](https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/cyclone-v/cv_5v4.pdf)

[3] [https://www.intel.com/content/www/us/en/programmable/products/boards\\_and\\_kits/download-cables.html](https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/download-cables.html)

[4] <https://www.intel.com/content/www/us/en/programmable/support/support-resources/operation-and-testing/power/pow-powerplay.html>

[5] <https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/dp/cyclone-v/pcg-01014.pdf>



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