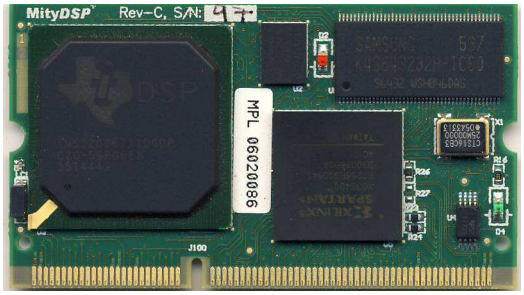
FEATURES

- TI TMS320C6711 Digital Signal Processor
  - 200 MHz
  - Hardware Floating Point Unit
  - 64 KB L2 cache
  - 2 Integrated McBSPs
  - JTAG Emulation/Debug
- On-Board Xilinx FPGA
  - XC3S400
  - 300 MHz Clock Logic
  - 288 KBits Block RAM
  - 3,584 Slices
  - JTAG Interface/Debug
- 8 MB CPU SDRAM
- 2 MB NOR FLASH
- Standard SO-DIMM Interface
  - 100 FPGA User I/O Pins
  - 2 McBSP Interfaces
  - DSP Emulator Interface
  - FPGA JTAG Interface
  - 3.3, 2.5, 1.23 V Power Interface

APPLICATIONS

- Embedded Instrumentation
- Rapid Development / Deployment
- Embedded Digital Signal Processing
- Industrial Instrumentation
- Medical Instrumentation
- Embedded Control Processing



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DESCRIPTION

The MityDSP is a highly configurable, very small form-factor processor card that features a Texas Instruments TMS320C6711 200 MHz Digital Signal Processor (DSP) tightly integrated with a Xilinx XC3S400 Spartan Field Programmable Gate Array (FPGA), FLASH and SDRAM memory subsystems. Both the DSP and the FGPA are capable of loading/executing programs and logic images developed by end users. The MityDSP provides a complete digital processing infrastructure necessary for embedded applications development.

Users of the MityDSP are encouraged to develop applications and FPGA firmware using the MityDSP hardware and software development kit provided by Critical Link LLC. The development kit includes API libraries compatible with the TI Code Composer Studio compiler as well as FPGA netlist components compatible with the Xilinx ISE FPGA synthesis tool. The libraries provide the necessary functions needed to configure the MityDSP, program standalone MityDSP embedded applications, and interface with the various hardware components on the board. In addition, the libraries include several interface "cores" – FPGA and DSP software modules designed to interface with various data converter modules (ADCs, DACs, LCD interfaces, etc) – as well as bootloading and FLASH programming utilities.

Figure 1 provides a top level block diagram of the MityDSP processor card. As shown in the figure, the primary interface to the MityDSP is through a standard SO-DIMM card edge interface. The interface provides power, DSP emulator, FPGA JTAG, synchronous serial connectivity, and up to 100 pins of configurable FPGA I/O for application defined

interfacing. Details of the SO-DIMM connector interface are included in the SO-DIMM Interface Description, below.

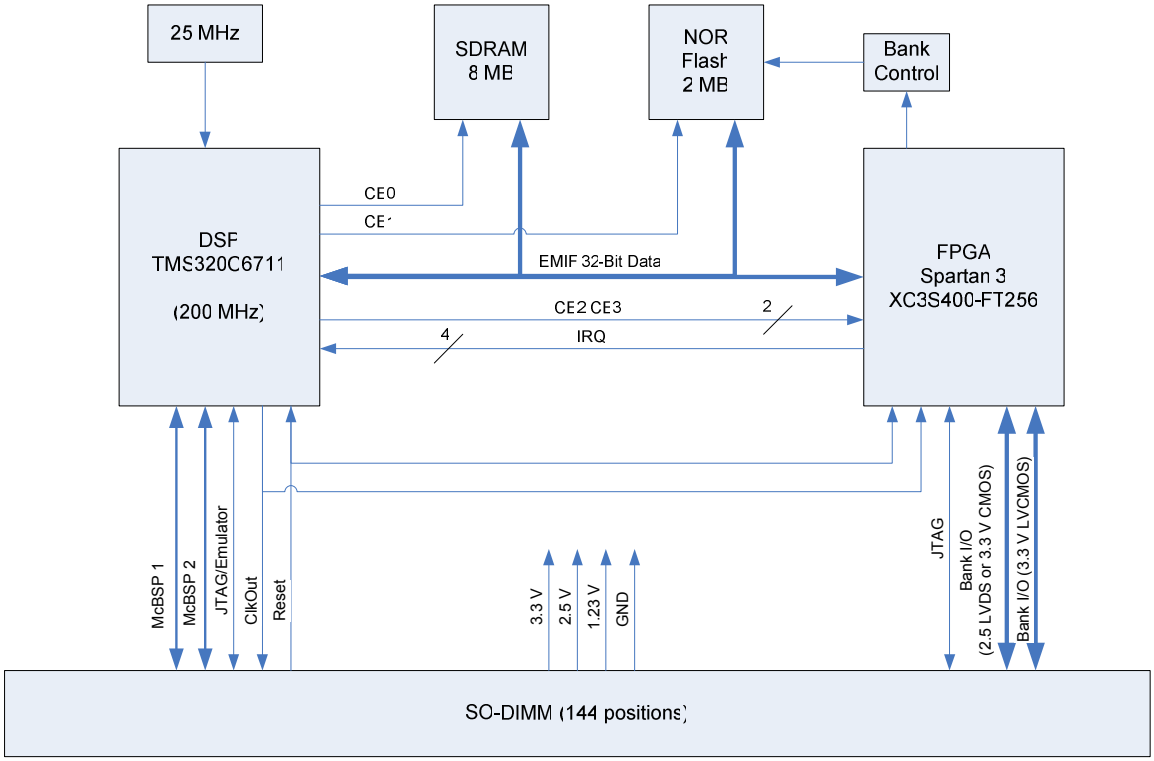

Figure 1 MityDSP Block Diagram

FPGA Bank I/O

The MityDSP provides 100 lines of FPGA I/O directly to the SO-DIMM card edge interface. The 100 lines of FPGA I/O are distributed across TBD banks of the FPGA. These I/O lines and their associated logic are completely configurable within the FPGA, although typically a minimum of 2 lines are reserved for providing interface circuitry for field FLASH upgrades.

With the Xilinx Spartan series of FPGA, a bank may be configured to operate on a different electrical interface standard based on input voltage and termination configurations. Of the 100 pins, 80 of the pins have been configured to use 3.3 Volt CMOS level logic. The remaining 20 pins, located on bank 7 of the FPGA, have been routed as differential pairs and may be configured as single ended 3.3 Volt or 2.5 Volt CMOS level logic, or may be configured as 2.5 Volt LVDS pairs. The configuration option is accomplished via resistor population on the board. Default configuration is for 3.3 Volt CMOS level logic. For pre-configured 2.5 Volt logic, please contact Critical Link sales representatives.

The FPGA Bank I/O provides optional pull-up and pull-down resistors for single ended configuration. For LDVS pairs, termination resisters have been added to support enabling of 100 Ohm DCI termination. Refer to the Xilinx Spartan 3 users guide for more information.

Integrated DSP Serial Communications Modules

The C6711 processor includes two multichannel buffered serial ports (McBSPs) which have been routed directly to the SO-DIMM interface. Both Critical Link (as part of the MityDSP development kit) and TI provide several McBSP interface libraries for integration with various data acquisition modules.

EMIF Interface / System Memory

The C6711 DSP and the Spartan FPGA are connected using the DSP External Memory Interface (EMIF). The EMIF interface includes 4 chip select spaces. The EMIF interface supports multiple data width transfers and bus wait state configurations based on chip select space. 8, 16, and 32 bit data word sizes may be used. Two of the four chip select lines (CE2, CE3) are reserved for the FPGA interface. The MityDSP also includes 4 lines between the FPGA and the C6711 for the purposes of generating interrupt signals.

In addition to the FPGA, 2 MB of on-board NOR FLASH memory and 8 MB of SDRAM are connected to the DSP using the EMIF bus. The FLASH memory is 8 bits wide and is connected to third chip select line of the EMIF (CE1). The FLASH memory is typically used to store the following types of data:

- secondary bootloader DSP software
- FPGA bootloader images
- application DSP software
- application DSP images
- application data (non-volatile storage)

The C6711 DSP EMIF interface is capable of addressing 1 MB of data on the EMIF interface. In order to provide access to the remaining 1 MB of FLASH memory, the upper address line of the FLASH is controlled by Bank Control logic. Upon reset the Bank Control Logic defaults to bank zero for bootloading support. Following bootloading, the bank control logic is controlled by the FPGA. Refer to the MityDSP User's Guide for more information on bank control logic.

The SDRAM memory is 32 bits wide and is connected to the fourth chip select line of the EMIF (CE0). The SDRAM provides an application user with program and data storage space beyond the 64 KB of internal SRAM available in the C6711 processor. The SDRAM / EMIF may be clocked at rates up to 100 MHz, supporting burst transfer data rates of 400 MB per second.

The TI C6711 processor includes 64 KB of internal SRAM memory. The SRAM may be configured as programmable RAM or as level 2 (L2) cache. The C6711 processor also

provides 2 KB of level 1 (L1) data and instruction caching. Full DMA transfer between internal memory and SDRAM is supported in the architecture.

Debug Interface

Both the JTAG interface signals for the FPGA and the JTAG and emulator signals for the C6711 processor have been brought out to the SO-DIMM card edge interface to support in-circuit debugging. The JTAG chains are separate on the interface. With an appropriate break-out cable, the interface will support the use of standard Xilinx Platform JTAG cable programming and the Spectrum Digital processor emulator (or equivalent). Details of the pin-outs for the debug header are included in the Debug Interface Description, below.

Growth Options

The MityDSP has been designed to support several upgrade options listed in the table below. For ordering information and details regarding these options, please contact a Critical Link sales representative.

Option / Part	Description
MityDSP – Industrial Temp Grade	Industrial temperature range (-40 to 70 C), TI TMS320C6711 CPU speed grade approved for 150 MHz operation.
MityDSP – XM	FPGA Upgraded to XS3C1000 SDRAM Upgraded to 32 MBytes FLASH Upgraded to 16 MBytes
MityDSP – XM Industrial Temp Grade	MityDSP-XM, industrial temperature range (-40 to 70 C), TI TMS320C6711 CPU speed grade approved for 150 MHz operation.

Example Application

The figure below illustrates an example application utilizing the MityDSP processor card. The application requires modulating a laser drive with an excitation signal, capturing the results from a photo-detector and applying a lock-in detector circuit in order to detect signals of interest. In addition, several low speed thermal and pressure sensors are monitored and used to control system cooling and mass flow control devices.

The system provides standard RS-232 interfaces for integrating with off-the-shelf flow control and temperature control devices. The system also requires a USB interface to support direct PC communications and also requires an Ethernet interface to support remote access.

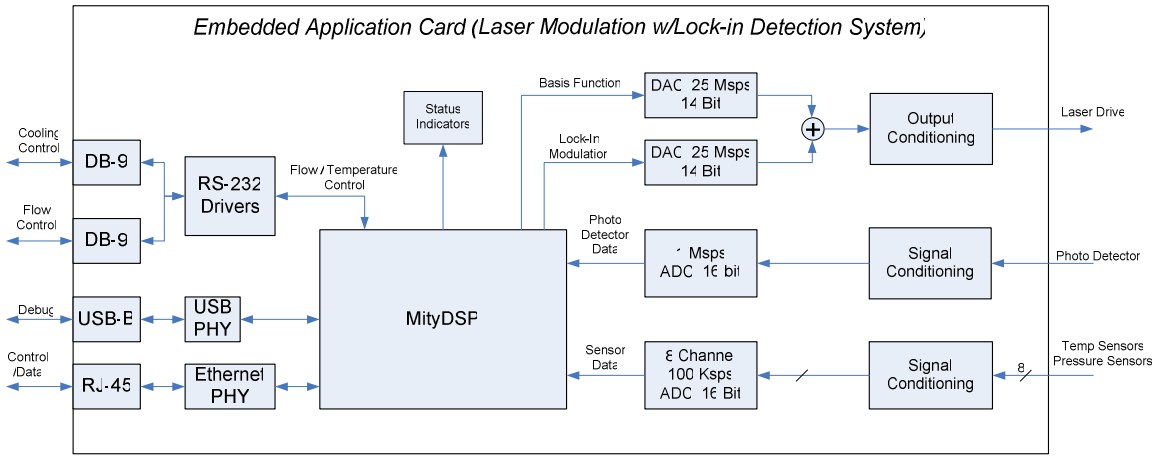

Figure 2 Typical MityDSP Application

In this application, the developer need only focus on the interface circuitry – signal conditioning, ADC selection, communications I/O – as the processing platform design is complete within the MityDSP. The engineer is able to interface directly to the selected DACs and ADCs by connecting them to the Bank I/O on the FPGA and utilizing the MityDSP hardware and software development kit APIs. Waveform generation, synchronization, and Lock-In processing can be implemented directly in the FPGA or divided between the FPGA and the DSP according to design requirements.

The same design approach is accomplished for the USB, network, and RS-232 communications links. The MityDSP developer's kit provides standard UART interfaces, a 10/100 EMAC, and includes a port of the LwIP TCP/IP layer stack for the MityDSP C6711.

This approach minimizes the design time required (in application software, FPGA firmware, and PCB design) for system infrastructure and allows focusing on the application specific requirements.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vcc	3.4 V
Storage Temperature Range	-65 to 80C
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range	0 to 55C
Humidity	0 to 95% Non-condensing
Vibration, Z-Axis	TBS
Vibration, X/Y-Axis	TBS

SO-DIMM Interface Description

The primary interface connector for the MityDSP is the SO-DIMM card edge interface.

Table 1 SO-DIMM Pin-Out

Pin	I/O	Signal	Pin	I/O	Signal
A1	-	+3.3 V	B1	-	+3.3 V
A2	-	GND	B2	-	GND
A3	I	DSP_TMS	B3	I	MRESET#
A4	O	DSP_TDO	B4	I	DSP_TRST
A5	I	DSP_TDI	B5	I	DSP_EMU1
A6	I	DSP_TCK	B6	I	DSP_EMU0
A7	I	CLKS0	B7	I	CLKS1
A8	I/O	CLKR0	B8	I/O	CLKR1
A9	I/O	CLKX0	B9	I/O	CLKX1
A10	I	DR0	B10	I	DR1
A11	O	DX0	B11	O	DX1
A12	I/O	FSR0	B12	I/O	FSR1
A13	I/O	FSX0	B13	I/O	FSX1
A14	-	GND	B14	I	GND
A15	-	+1.23 V	B15	-	+1.23 V
A16	O	RESET#	B16	-	CLKOUT2
A17	O	RESET	B17	-	CLKOUT3
A18	-	GND	B18	-	GND
A19	I	FPGA_TCK	B19	O	FPGA_TDO
A20	I	FPGA_TDI	B20	I	FPGA_TMS
A21	I/O	IO_L13	B21	I/O	IO_K14
A22	I/O	IO_H16	B22	I/O	IO_L12
A23	I/O	IO_K13	B23	I/O	IO_J14
A24	I/O	IO_H15	B24	I/O	IO_G16
A25	I/O	IO_J13	B25	I/O	IO_H14
A26	I/O	IO_G15	B26	I/O	IO_K12

Pin	I/O	Signal	Pin	I/O	Signal
A27	I/O	IO_E16	B27	I/O	IO_F15
A28	I/O	IO_G14	B28	I/O	IO_H13
A29	I/O	IO_D16	B29	I/O	IO_E15
A30	I/O	IO_F14	B30	I/O	IO_C16
A31	I/O	IO_G13	B31	I/O	IO_D15
A32	I/O	IO_B16	B32	I/O	IO_E14
A33	I/O	IO_C15	B33	I/O	IO_F13
A34	I/O	IO_D14	B34	I/O	IO_G12
A35	I/O	IO_F12	B35	I/O	IO_E13
A36	I/O	IO_B14	B36	I/O	IO_A14
A37	I/O	IO_B13	B37	I/O	IO_D12
A38	I/O	IO_A13	B38	I/O	IO_C12
A39	I/O	IO_E11	B39	I/O	IO_B12
A40	I/O	IO_A12	B40	I/O	IO_D11
A41	I/O	IO_C11	B41	I/O	IO_B11
A42	I/O	IO_D9	B42	I/O	IO_E10
A43	I/O	IO_C9	B43	I/O	IO_D10
A44	I/O	IO_B8	B44	I/O	IO_A10
A45	I/O	IO_A8	B45	I/O	IO_B10
A46	I/O	IO_C10	B46	I/O	IO_A9
A47	I/O	IO_D8	B47	I/O	IO_C8
A48	I/O	IO_P7	B48	I/O	IO_B7
A49	I/O	IO_A7	B49	I/O	IO_C7
A50	I/O	IO_D7	B50	I/O	IO_E7
A51	I/O	IO_M7	B51	I/O	IO_P6
A52	I/O	IO_B6	B52	I/O	IO_C6
A53	I/O	IO_D6	B53	I/O	IO_A5
A54	I/O	IO_E6	B54	I/O	IO_B5
A55	I/O	IO_C5	B55	I/O	IO_A4
A56	I/O	IO_D5	B56	I/O	IO_B4
A57	I/O	IO_A3	B57	I/O	IO_N7
A58	I/O	IO_J4	B58	I/O	IO_M14
A59	I/O	IO_K5	B59	I/O	IO_M10
A60	I/O	GND	B60	-	GND
A61	I/O	IO_L2P_E4	B61	I/O	IO_L4P_F5
A62	I/O	IO_L2N_F4	B62	I/O	IO_L4N_G5
A63	I/O	IO_L3P_F3	B63	I/O	IO_L8P_D3
A64	I/O	IO_L3N_F2	B64	I/O	IO_L8N_E3
A65	I/O	IO_L5P_G4	B65	I/O	IO_L7P_C3
A66	I/O	IO_L5N_G3	B66	I/O	IO_L7N_C2
A67	I/O	IO_L6P_H4	B67	I/O	IO_L0P_D2
A68	I/O	IO_L6N_H3	B68	I/O	IO_L0N_D1
A69	I/O	IO_L9P_G1	B69	I/O	IO_L1P_E2
A70	I/O	IO_L9N_H1	B70	I/O	IO_L1N_E1
A71	-	GND	B71	-	GND
A72	-	+2.5 V	B72	-	+2.5 V

The signal group description for the above pins is included in Table 2

Table 2 Signal Group Description

Signal / Group	I/O	Description
3.3 V	N/A	3.3 volt input power referenced to GND.
2.5 V	N/A	2.5 volt input power referenced to GND.
1.23 V	N/A	1.23 volt input power referenced to GND.
MRESET#	I	Manual Reset. When pulled to GND for a minimum of 1 usec, resets the DSP processor.
DSP_TMS, DSP_TDO, DSP_TDI, DSP_TCK, DSP_EMU1, DSP_EMU2, DSP_TRST	IO	These pins are direct connects to the JTAG emulator port on the TMS6711 DSP processor. For further information regarding the electrical standards of this connection, please refer to the TMS6711 Data Sheets and JTAG Users Guide from Texas Instruments.
FPGA_TMS, FPGA_TDI, FPGA_TDO, FPGA_TCK	IO	These pins are direct connects to the JTAG programming port on the Xilinx XC3S400 FPGA device. For further information regarding the electrical standards of this connection, please refer to the Xilinx Spartan JTAG programmers guide and datasheets.
CLKR0,CLKX0,DR0, DX0, FSR0	IO	These pins are direct connects to the corresponding McBSP port 0 pins on the TMS645x DSP processor. For further interface information, please refer to the TMS645x McBSP Users Guide and Data Sheets.
CLKR1,CLKX1,DR1, DX1, FSR1	IO	These pins are direct connects to the corresponding McBSP port 1 pins on the TMS645x DSP processor. For further interface information, please refer to the TMS645x McBSP Users Guide and Data Sheets.
RESET#, RESET	O	Reset output signals (active low and active high pair) from the TMS6711 DSP. These signals may be used to initiate reset circuitry on I/O MityDSP carrier cards. These signals are held low a minimum of TBD ns.
GND	N/A	System Digital Ground.
IO_XX	IO	FPGA General Purpose I/O pin. FPGA I/O pins have been routed to the MityDSP connector on FPGA pins XX. These pins all provide 3.3 V bank logic and are available for application use.
IO_LXP_XX, IO_LYN_XX	IO	FPGA I/O pins. These pins are routed to FPGA pins XX. For stock MityDSP/XM parts, these pins are tied to 3.3 V logic. However, the MityDSP-XM provides an option to configure these pins to use 2.5 V logic and be run as LVDS

Signal / Group	I/O	Description
		pairs according to the P/N (positive/negative) numbering in the netnames.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V33	Voltage supply, 3.3 volt input.		3.2	3.3	3.4	Volts
I33	Quiescent Current draw, 3.3 volt input			300	TBS	mA
I33-max	Max current draw, positive 3.3 volt input.			350	TBS	ma
V25	Voltage supply, 2.5 volt input.		2.45	2.5	2.55	Volts
I25	Quiescent Current draw, 2.5 volt input			200	TBS	mA
I25-max	Max current draw, positive 2.5 volt input.			TBS	TBS	mA
V12	Voltage supply, 1.23 volt input.		1.2	1.23	1.25	Volts
I12	Quiescent Current draw, 1.23 volt input			200	TBS	mA
I12-max	Max current draw, positive 1.23 volt input.			TBS	TBS	mA
CLKOUT	Output Clock Frequency, B16 & B17		25	25	25	MHz
FCPU	CPU internal clock Frequency (PLL output)		25	100	200	MHz
FEMIF	EMIF bus frequency	Must be ½ CPU	12.5	50	100	MHz
	1. Power utilization of the MityDSP is heavily dependant on end-user application. Major factors include: CPU PLL configuration, FPGA utilization, and external SDRAM utilization.					

MECHANICAL INTERFACE

A mechanical outline of the MityDSP is illustrated in Figure 3, below.

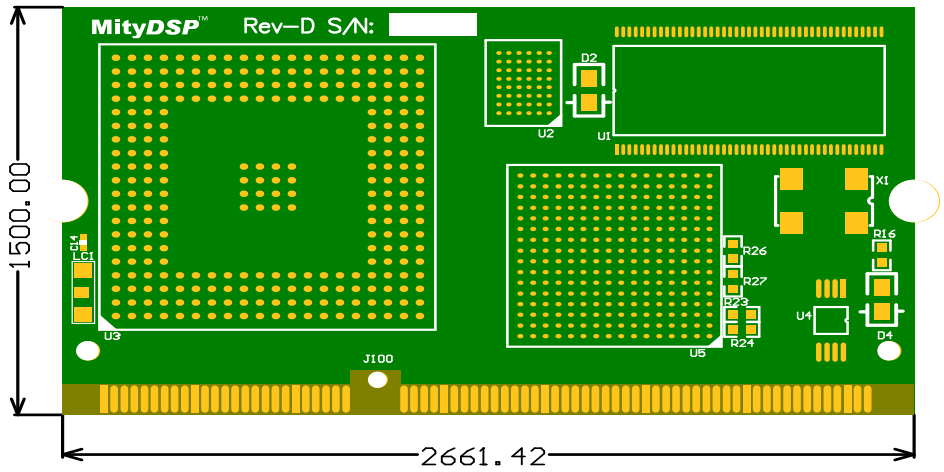

Figure 3 MityDSP Mechanical Outline

REVISION HISTORY

Date	Change Description
21-APR-2007	Initial Delivery
28-AUG-2007	Added Signal Group/Description Table

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