FEATURES

- High Performance MityDSP-L138F CPU
  - TI OMAP-L138
  - Xilinx Spartan 6 FPGA
- Vision Sensor Boards Supported
  - 0.3MP Monochrome
  - 0.3MP Color
  - 1.0MP Monochrome
  - 5.0MP Monochrome
  - 5.0MP Color
- Video Capture
- Image Analysis
- Linux and HMI (Qt)

Expansion

- UART Header (RS232 or RS485)
- WQVGA LCD Interface
- 4 Status LED's
- 4-Pin GPIO Header

APPLICATIONS

- Machine Vision
- Quality Control
- Semiconductor Inspection
- Image Processing (DSP and FPGA)

Digital Interfaces

- DVI Video Output
- 10/100 Mbit Ethernet Interface
- Audio Output
- USB Host and OTG
- CAN Bus Interface
- SD/MMC Card Socket

Additional Hardware

- AC to DC 12V Adapter
- Tripod for Camera
- Pre-Loaded SD card
- Camera Lens
- Ethernet and Serial Cables

Overview

The Vision Development Kit (VDK) by Critical Link is a complete hardware and software framework designed to accelerate the development of vision applications. The framework offers both a Xilinx Spartan 6 FPGA and a TI OMAP-L138 dual core processor, and is based on Critical Link's production-ready MityDSP-L138F System on Module (SoM).

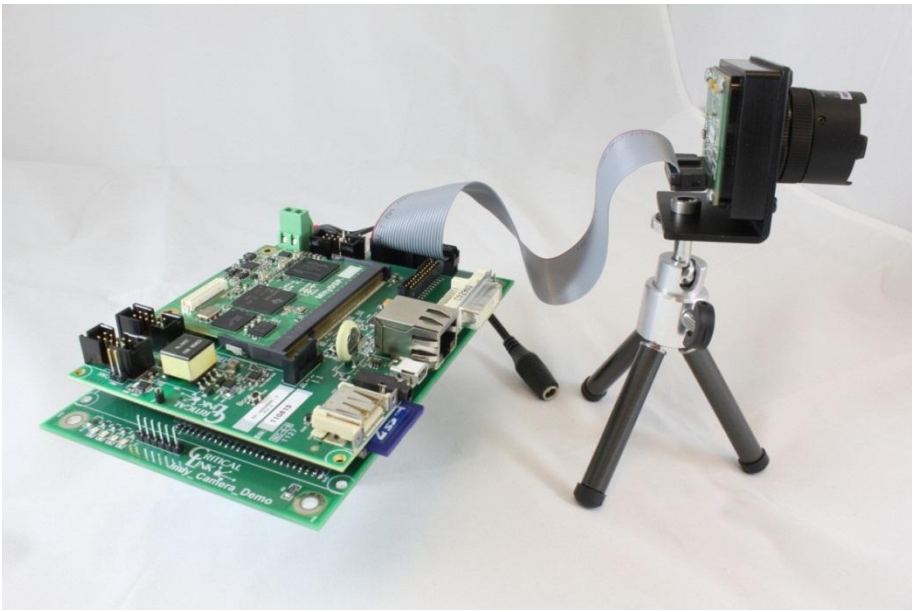

Figure 1 - Vision Development Kit

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The system is designed to route raw video data from the CCD sensor board into the MityDSP-L138F. The FPGA captures the input data and performs optional user defined algorithm(s) on the video data, then routes the data to the DSP core of the OMAP-L138 processor via the UPP interface.

The DSP can then performs additional processing and notifies the ARM core that the final processed video data (or results if no final video data is required) is available via a DSPLINK shared memory interface. The ARM accepts the data and updates the local frame buffer with the needed results using a Qt drawing framework. Figure 2 shows a system block diagram for the Xilinx FPGA and DSP and ARM cores (TI OMAP-L138).

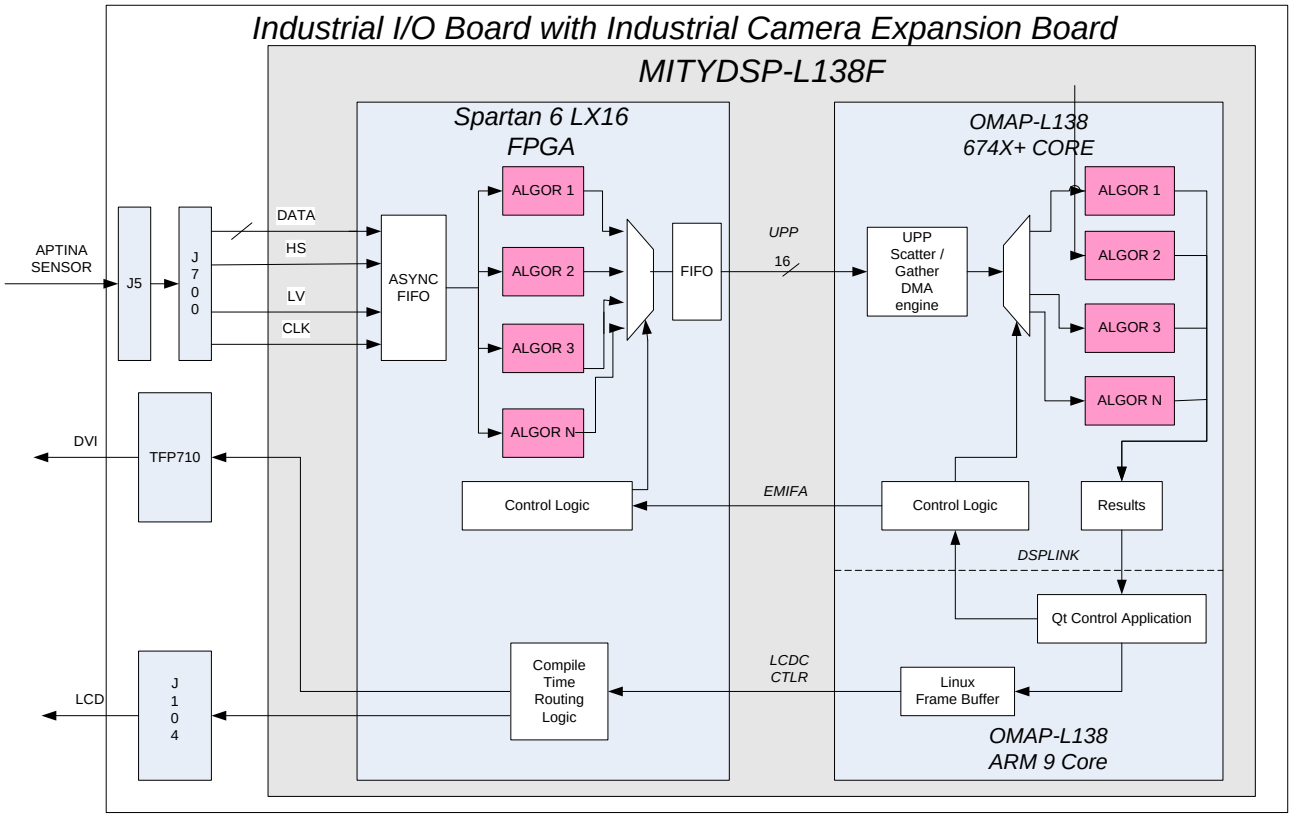

Figure 2 – System Block Diagram for FPGA, DSP, and ARM

This document covers the following topics:

- Major system components: Sensor, FPGA, DSP, and ARM
- Hardware Design Information
- Key interfaces
- Development tools
- Getting started
- Examples
- Included Components and Ordering information

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Figure 3 shows the key subcomponents and interfaces for the VDK.

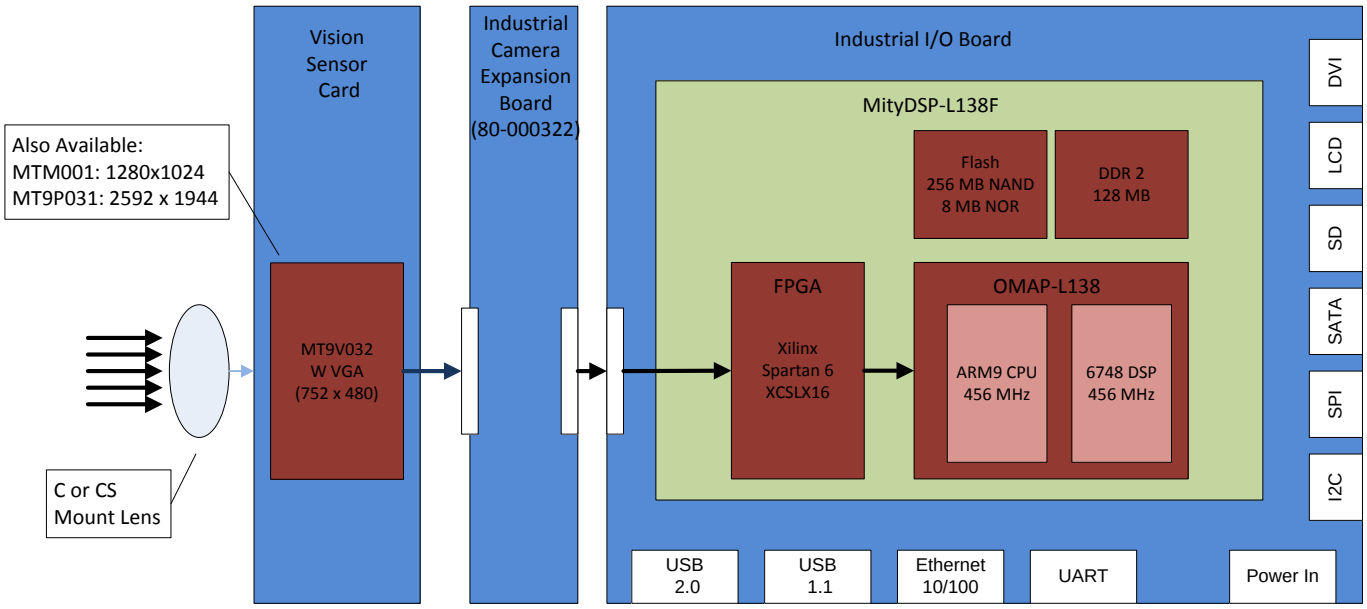

Figure 3 - System Block Diagram for FPGA / DSP / ARM

Major System Components

Sensor

The development kit comes standard with Aptina's monochrome Wide VGA sensor (MT9V032). This sensor supports a resolution of 752 x 480 pixels and comes with a mount that accepts either a C or CS mount lens. A T0412 FICS-3 4mm F1.2 Lens is included as the standard lends. In addition to the Wide VGA sensor, both the MTM001 (1280x1024 pixels) and MT9P031 (2592x1944) are also available. The MT9V032 and MT9P031 sensors are available in either monochrome or color format and the MTM001 is monochrome only -- please see 'Ordering Information' section for more details. Finally, custom sensor options are also available --please contact Critical Link for additional details.

The sensor card connects directly to the Industrial Camera Expansion (80-000322) board through a 26-pin cable (included). This is an expansion board which is mounted beneath a Critical Link Industrial IO Development Kit through its three 50-pin expansion headers. Please see Table 1 - Vision Development Kit HW Design File Locations section in this document for datasheet information on both of these boards.

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FPGA

A Xilinx Spartan 6 XCSLX16 FPGA is the first part of the processing chain. It receives sensor data and performs any time-critical functions best suited for the FPGA (vs. software). The FPGA is architected to receive sensor data and make it available for the algorithm processing blocks (see Figure 2). Once FPGA processing is completed, the pixel data is transmitted to the OMAP-L138 over the UPP port.

Examples of functions which may be performed in the FPGA include:

- Color Space Conversion
- Edge detection
- Convolution
- Custom processing blocks

The VDK contains instructions on adding your own custom algorithms to our provided base FPGA design. This information is provided in the "VDK Algorithm Addition.pdf" document which is included on the VDK DVD.

DSP

Texas Instrument's 'C674x core (part of the OMAP-L138) provides the DSP processing function. The VDK framework in the OMAP receives the pixel data from the UPP port and makes it available to one or more processing elements (see Figure 2). A number of processing elements can be combined to make up the final desired processing. Once processing is completed, pixel data are presented to DSPLink for transport to the ARM processor.

TI 'C64x image processing library -- provided in source form -- includes numerous processing functions which are well suited for image processing. Table 2 shows a summary of the available functions. The Vision Development contains instructions on adding your own additional algorithms to our provided DSP reference design. This information is provided in the "VDK Algorithm Addition.pdf" document which is included on the VDK DVD.

Summary of TI's 'C64x Image Processing Functions	
Boundary and Perimeter Detection	Median Filtering
Dilation and Erosion	Pixel Expansion
Edge Detection	Forward and Reverse DCT
Thresholding	Motion Estimation
Color Space Conversion	MPEG-2 Variable Length Encoding
Convolution	Quantization
Correlation	Wavelet Processing
Error Diffusion	Background Subtraction

Additional information on Texas Instruments TMS320C64x Image Processing library:
http://focus.ti.com/docs/toolsw/folders/print/sprc094.html

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ARM

The 456 MHz ARM9 runs Linux (Open Embedded Angstrom distribution) and is responsible for all embedded computing type tasks, such as managing a GUI, communication stacks, and file system. A robust GUI is available via Qt, and both Ethernet and USB communication stacks are available in addition to all standard Linux facilities and tools.

The VDK contains instructions on modifying the provided QT GUI reference design. This information is provided in the "VDK Algorithm Addition.pdf" document which is included on the VDK DVD.

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As shown in Figure 3 the Vision Development kit is comprised of 4 different printed circuit boards (PCB's). Each of these boards: MityDSP-L138F, Sensor, Industrial IO Board and Industrial Camera Expansion (80-000322) Board have their own datasheets. The Industrial IO and Industrial Camera Expansion Boards also have schematic, BOM and gerber PDF's available. Copies of all of these files are available at the following locations:

File Description	File Type	File Location
MityDSP-L138F	Datasheet	http://www.mitydsp.com/products-services/cpu-engines/mitydsp-l138F/
Sensor	Datasheet(s)	Contact Us
Industrial IO	Datasheet	L138-1808-1810 Development Kit DVD and http://www.mitydsp.com/products-services/base-boards/mitydsp-l138f-dev-kit/
Industrial IO	Schematic	L138-1808-1810 Development Kit DVD or Contact Us
Industrial IO	Bill of Materials	L138-1808-1810 Development Kit DVD or Contact Us
Industrial IO	Gerbers	L138-1808-1810 Development Kit DVD or Contact Us
Industrial Camera Expansion Board (80-000322)	Datasheet	Vision Development Kit DVD or http://www.mitydsp.com/products-services/base-boards/vision-dev-kit/
Industrial Camera Expansion Board (80-000322)	Schematic	Vision Development Kit DVD or Contact Us
Industrial Camera Expansion Board (80-000322)	Bill of Materials	Vision Development Kit DVD or Contact Us
Industrial Camera Expansion Board (80-000322)	Gerbers	Vision Development Kit DVD or Contact Us

Table 1 - Vision Development Kit HW Design File Locations

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Key Interfaces

One of the primary benefits of using Critical Link's Vision Development Kit is that the transport of pixel data from sensor through the FPGA, DSP and ARM processors has been developed and optimized. This 'infrastructure' is essential to deploying a complete system, but can take many months of effort to develop and perfect. All the key interfaces are provided with the framework and are summarized in Table 2 below.

From	To	Hardware Interface	Data Rate
Sensor	FPGA	Direct Sensor Interface	Up to 200 M Pixel / sec
FPGA	DSP	UPP Port	Up to 75 MHz (@ 16 bits)
DSP	ARM	DSPLink (1)	Shared memory interface
ARM	Host	USB, Ethernet (10,100)	Various data rates

Table 2 - Vision DK Interface Summary

Note 1: DSPLink is a framework provided by TI for DSP / ARM communication. This framework includes facilities for transporting data between ARM and DSP, as well as code download and DSP reset. Critical Link has enhanced DSPLink by providing wrapper functions that allow both ARM and DSP applications easy access to data movement.

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Development Tools

This VDK leverages existing development tools from Xilinx and TI, and as such, should fit seamlessly within the standard development environment. The development tools are available at the following web link and are summarized below:

http://support.criticallink.com/redmine/projects/indio/wiki/Vision_Framework_Kit

Further information concerning many MityDSP-L138 topics can be found at:

http://support.criticallink.com/redmine/projects/arm9-platforms/wiki

Component	Development Tools	Version	Tool Location
FPGA	Xilinx ISE Webpack Version 13 or Higher	13 or Higher	http://support.criticallink.com/redmine/projects/arm9-platforms/wiki/FPGA_Development_Tools
	JTAG Programming Cable		http://support.criticallink.com/redmine/projects/arm9-platforms/wiki/FPGA_Development_Tools
DSP	TI Code Composer (CCS)	5.2 or Higher	http://processors.wiki.ti.com/index.php/Download_CCS
	Spectrum Digital JTAG Emulator	XDS510 Preferred	http://support.criticallink.com/redmine/projects/arm9-platforms/wiki/DSP_Development_Tools
ARM	Eclipse IDE	Provided with CCS	http://support.criticallink.com/redmine/projects/arm9-platforms/wiki
	GCC tool chain	Nov 2010	http://support.criticallink.com/redmine/projects/arm9-platforms/wiki/GCC_Toolchain

Table 3 - Summary of Development Tools

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Getting Started

Starting a project started using the Vision Development Kit from Critical Link is straightforward:

1. Identify application and generate vision algorithm
2. Select a test / verification vehicle, which may be a Matlab or a general C / C++ programming environment.
3. Develop, debug, and verify algorithms on selected platform. Once you have validated the algorithm(s), you are ready to port them to the target hardware (Vision Development kit)
4. Set up development environment for the MityDSP-L138F Vision Framework
    - "VDK Environment Setup.pdf" included on VDK DVD
        i. Base L138-1808-1810 Linux Virtual Machine Development Environment
        ii. Update with supplemental Vision Development Kit specific files
5. To facilitate quick addition of a new algorithm a step-by-step document has been created to cover adding algorithms to either the FPGA or DSP and having them be accessed by the ARM Qt GUI application. Please follow the "Vision DK Algorithm Addition.pdf" document included on your Vision Development Kit DVD.
    - Port algorithm to Vision DK
        i. Convert to C / C++ (if using Matlab and the DSP)
        ii. Use Vision DK algorithm block calling convention: Pointer to data-in, size, and pointer to data_out.
        iii. Add algorithm to the ARM GUI
6. Verify algorithm on target hardware.

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Examples

The development kit is provided with the following examples which are meant to illustrate basic functionality:

Mode	Description
Raw Mode	Camera data is aligned to 16-bit integers and copied to frame buffer as 5-6-5 output
Gray Scale (FPGA)	Camera data treated as monochrome data and is converted to gray scale color using 5-6-5LCD color mapping (effective 32 levels of colors). Conversion done in FPGA
Gray Scale (DSP)	Camera data treated as monochrome data and is converted to gray scale color using 5-6-5LCD color mapping (effective 32 levels of colors). Gray scale conversion done in DSP
Bayer Color Conversion (DSP)	Camera data is treated as color information formatted in standard Bayer pattern. The Bayer pattern is converted to standard 5-6-5 LCD color for display on LCD
Sobel 3x3 Edge Detection	Camera data is treated as monochrome and 3x3 edge detection algorithm is run on the DSP with result converted to gray scale (5-6-5) 32 levels color map display

Table 4 - Vision DK Examples

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Included Components

The following table lists the components that are included with a Vision Development Kit. See Table 6 for specific development kit ordering information.

Table 5: Included Items

Description	Qty. Included
Vision Development Kit Board Set	Qty. 1
MityDSP-L138F Module	Qty. 1
Selected Camera Sensor with Lens, Tripod and Cable	Qty. 1
Null Modem Serial cable M/F and 10-pin adapter	Qty. 1
12V 1.2A AC to DC Supply	Qty. 1
Ethernet cable – 7 foot	Qty. 1
DVD with L138-1808-1810 Development Environment	Qty. 1
DVD with Vision Development Kit Supplemental Files	Qty. 1
VDK Development Kit Schematic Files	
VDK Development Kit Gerber Drawings	
VDK Development Kit Bill Of Materials	

ORDERING INFORMATION

The following table lists the orderable module configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 6: Orderable Model Numbers

Model	Sensor	Color/Monochrome	Resolution	SoM	FPGA
80-000492	MT9V032	Monochrome	WVGA (752x480 pixels)	L138-FG-225-RC	6SLX16
80-000493	MT9V032	Color	WVGA (752x480 pixels)	L138-FG-225-RC	6SLX16
80-000494	MT9M001	Monochrome	XGA (1280x1024 pixels)	L138-FG-225-RC	6SLX16
80-000495	MT9P031	Monochrome	5 M Pixel (2592x1944 pixels)	L138-FG-225-RC	6SLX16
80-000496	MT9P031	Color	5 M Pixel (2592x1944 pixels)	L138-FG-225-RC	6SLX16

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REVISION HISTORY

Date	Change Description
29-Nov-2011	Initial Release
13-JUN-2012	Updates for production release

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