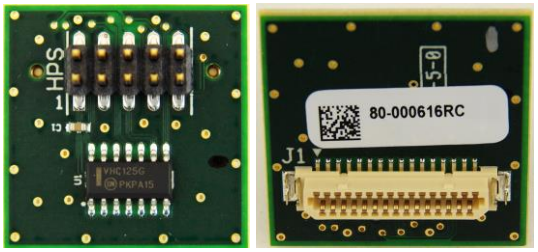
FEATURES

- MitySOM-5CSx Family Debug Adapter
- HPS (ARM) and FPGA JTAG debug interfaces
- Compatible Critical Link System on Modules
  - MitySOM-5CSE
  - MitySOM-5CSX



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DESCRIPTION

The MitySOM-5CSx Debug Adapter board for the MitySOM-5CSx Family of System on Modules from Critical Link allows for access to both the HPS (ARM) and FPGA JTAG chain debug interfaces. Each compatible System on Module includes a 31-pin Hirose connector which this adapter board connects to. Note that this adapter does not support TRACE capabilities. Please contact your Critical Link representative for information about a TRACE capable adapter.

Critical Link recommends that a USB-Blaster, USB-Blaster II or EthernetBlaster II Download Cable be used from Altera for debug, configuration and programming of the MitySOM-5CSx.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range	-40°C to 80°C

OPERATING CONDITIONS

Ambient Temperature Range Commercial	0°C to 70°C
Humidity	0 to 95% Non-condensing

DEBUG INTERFACE

A Hirose 31 pin connector (DF9-31P-1V(32)) is provided on each compatible module to allow for the connection of this adapter board for both HPS (ARM processor(s)) and FPGA debug. Below is the pin-out for the Hirose connector and the debug connector on the adapter board.

Debug Interface Connector Description (J1)

Table 1 J1 Hirose Connector

Pin	I/O	Signal	Pin	I/O	Signal
1	-	GND	2	I/O	HPS_RST_N
3	-	GND	4	-	NC
5	-	GND	6	I	JTAG_HPS_TCK
7	-	GND	8	-	NC
9	-	GND	10	O	JTAG_HPS_TDO
11	-	GND	12	-	VCC (3.3V)
13	-	GND	14	I	JTAG_HPS_TDI
15	-	GND	16	I	JTAG_HPS_TRST
17	-	GND	18	I	JTAG_HPS_TMS
19	-	GND	20	-	GND
21	-	GND	22	-	NC
23	-	GND	24	I	JTAG_FPGA_TMS
25	-	GND	26	I	JTAG_FPGA_TCK
27	-	GND	28	O	JTAG_FPGA_TDO
29	-	GND	30	I	JTAG_FPGA_TDI
31	-	GND			

HPS JTAG Interface Description (HPS)

Connection for the MitySOM-5CSx JTAG interface of a compatible System on Module from Critical Link. The connector used is a male 10-pin 0.100 inch header compatible with Altera's USB Blaster, USB Blaster II or EthernetBlaster II download cables.

Table 2 Processor JTAG Connector

Pin	I/O	Signal	Pin	I/O	Signal
1	O	JTAG_HPS_TCK	2	-	GND
3	I	JTAG_HPS_TDO	4	-	VCC (3.3V)
5	O	JTAG_HPS_TMS	6	I/O	HPS_RST_N
7	-	NC	8	O	JTAG_HPS_TRST
9	O	JTAG_FPGA_TDI	10	-	GND

ORDERING INFORMATION

The following table lists the standard debug adapter ordering information. For shipping status, availability, and lead time please contact your Critical Link representative.

Table 3: Standard Debug Adapter Part Number

Part Number	Description
80-000616	MitySOM-5CSx JTAG Debug Adapter

MECHANICAL INTERFACE

The mechanical outline of the Debug Adapter is illustrated in Figure 1, as shown below.

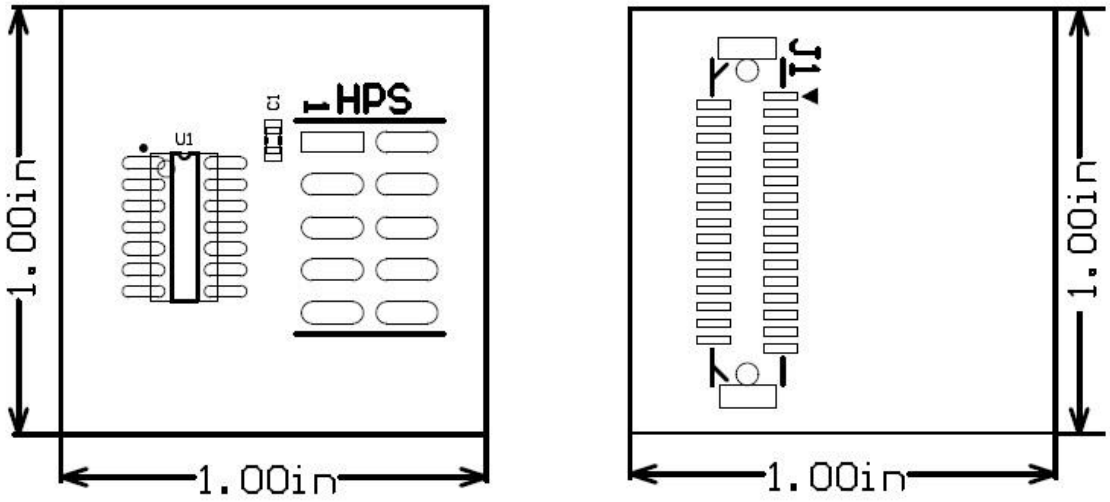

Figure 1 MitySOM-5CSx Debug Adapter Mechanical Outline

REVISION HISTORY

Date	Change Description
18-JAN-2016	Initial revision

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