FEATURES

- Supported Critical Link Modules
  - MitySOM-1810 and 1810F
  - MityDSP-L138 and L138F
  - MitySOM-1808 and 1808F
  - MityDSP-6748F

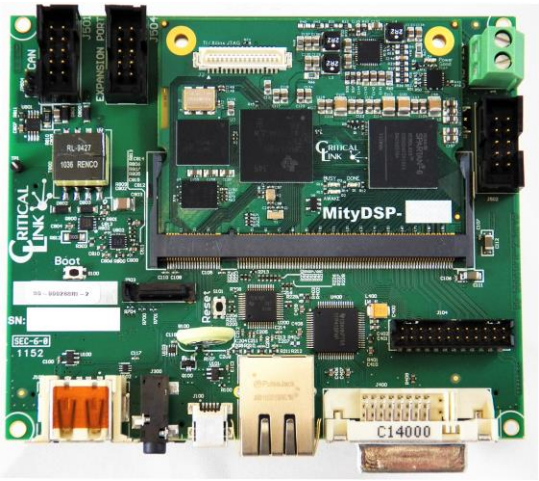
- Software Included:
  - Real-Time Linux Kernel
  - uBoot
  - User Boot Loader

Digital Interfaces:

- RS-232 Serial Interface
- USB Host Interface
- USB OTG Interface
- 10/100 MBit Ethernet Interface
- Electrically Isolated CAN Bus Interface
- UART Expansion for PROFIBUS/RS-485 or RS232 Interface
- DVI Video Interface
- SD/MMC Card Socket
- Audio Output
- SATA

Expansion:

- 3 50-pin IO Expansion Slots
- Integrated +3V/+5V/±12V Power Supply



MityDSP-L138F Installed

APPLICATIONS:

- PROFIBUS Development
- Process Automation
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Rapid Prototyping

DESCRIPTION

The Industrial IO Development Kit provides all the hardware and software support for system designers and developers to evaluate the AM1810, AM1808 or OMAPL138 Microprocessors. Included is your choice of a Critical Link MitySOM-1810, MitySOM-1808, MityDSP-6748F or MityDSP-L138 series System on Modules.

In addition, the Industrial IO Development Kit includes on board RS-232, 10/100 MBit Ethernet, Universal Serial Bus (USB) Host and USB-On The-Go (OTG) communication interfaces and an Electrically Isolated CAN interface. The single UART expansion port allows for the connection of either the PROFIBUS(module dependent)/RS-485 expansion board (optional) with 2500V galvanic isolation barrier or a simple RS232 serial port expansion kit (optional). Integrated Digital Video Interface (DVI) controller for external display connection with DDC support. Interface to QVGA\WQVGA display via 5 pair LVDS link with additional SPI interface for resistive touch controller (requires an FPGA based module to be installed), Multi Media Card (MMC) interface, 3 I/O Expansion connectors for custom add-on card and integrated power supply with +3V/+5V/±12V outputs from single 12VDC input.

A block diagram of the Industrial IO Development Kit is illustrated in Figure 1. All available processor GPIO ports and FPGA I/O lines (if FPGA module is installed) are either used directly by the Industrial IO Development Kit or are routed to the 3 50-pin Expansion IO connectors. Control of the on-board interface hardware and connected Expansion IO cards require proper configuration of the MitySOM / MityDSP ARM, DSP, and FPGA. While not required, it is strongly recommended that the MitySOM software and firmware development kit and supplied API be used to manage these interfaces.

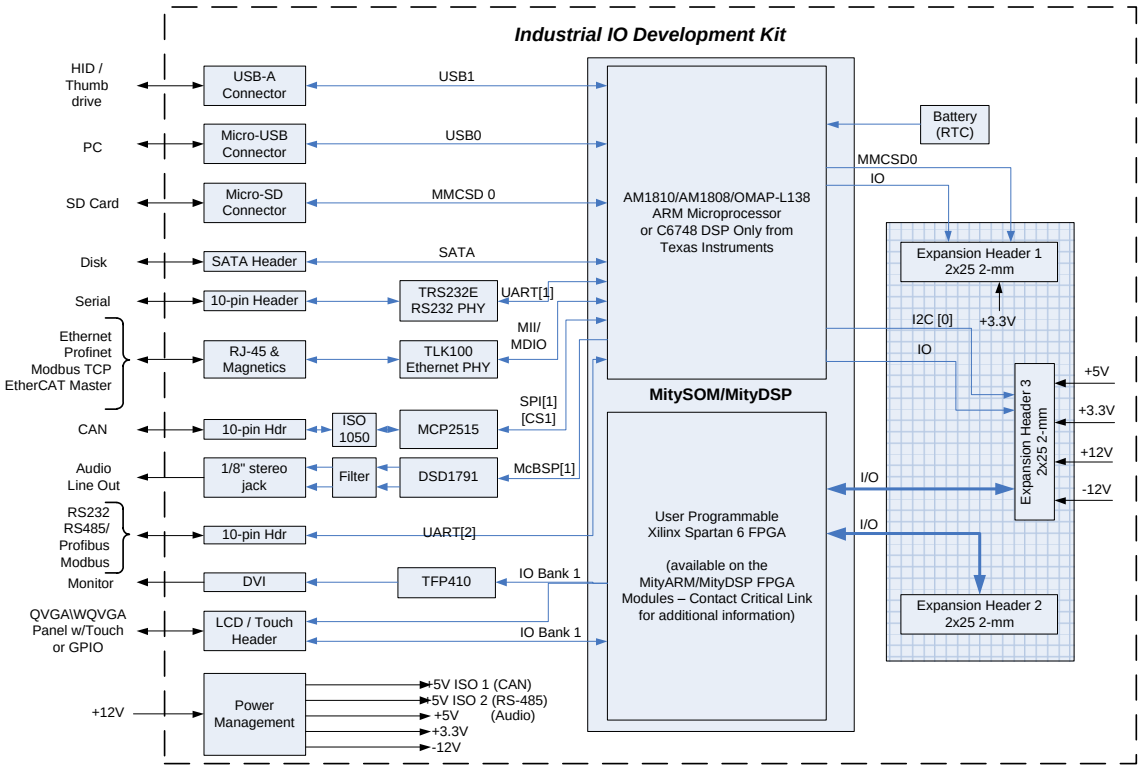


Figure 1: Industrial IO Development Kit Block Diagram

RS-232 Interface Description

The on-board RS-232 level driver provides standard serial interface at data rates up to 115,200 baud. The serial interface is routed to the primary MitySOM / MityDSP serial bootloading port in order to allow remote code download and FLASH upgrades on an attached MitySOM / MityDSP from this connector.

USB Interface Description

The on-board USB interface utilizes dedicated HOST and OTG controllers inside OMAP processor. Linux drivers are available.

Ethernet Interface Description

The on-board Ethernet interface features a network PHY capable of running at 10/100Mbit including link auto-negotiation and MII/MDIO capability. An industry standard RJ-45 connector is provided for external connection. This Ethernet interface may be used to perform remote code download and FLASH upgrades on an attached MitySOM or MityDSP module.

QVGA/WQVGA LVDS Interface Description

The Industrial IO Development Kit provides a flat-ribbon cable low profile interface for five Low Voltage Differential Signaling (LVDS) pairs. The interface design is intended to support high speed off board interconnects. In addition to custom user interfacing, the pairs may be used to interface to a Quarter VGA LCD screen using the MitySOM / MityDSP hardware and software development kit LCD interface libraries and an appropriate daughterboard interface. Off-the-shelf display solutions for WQVGA interfaces are provided by Critical Link.

The interface can also be customized to support 17 IO lines at +3.3V CMOS/LVTTL signaling levels based on FPGA configuration. This interface is available only with an FPGA based MitySOM or MityDSP module installed.

DVI Interface Description

The Industrial IO Development Kit provides a standard DVI interface for external monitor connection. Based on CPU utilization, recommended resolution should be limited to VGA (640x480) with 5-6-5 color pallet.

CAN Interface Description

The on-board CAN provides a CAN V2.0B compliant interface. This interface is managed by a Microchip MCP2515 CAN controller connected to MitySOM / MityDSP via the SPI1 interface. The galvanic isolation is provided by a dedicated TI ISO1050 transceiver. The ISO1050 is powered by an isolated power supply with 1000V* isolation from the primary supply.

Jumper JP504 can provide dedicated bus termination of 120Ohm. To enable termination, place shorting jumper across JP504.

The Electrical interface is provided via J501, 10-pin shrouded header.

Linux Driver and API examples are available to support CAN functionality.

UART Expansion Interface Description (80-000268RI-2 Assemblies)
The on-board dedicated UART port provides standard serial interface at data rates up to 115,200 baud. The serial interface is routed to the UART2 serial port of MitySOM / MityDSP. This expansion port can accept an optional PROFIBUS/RS485 Expansion Board or an RS232 Expansion Board. Please contact your Critical Link representative.

See the compatibility chart below to determine which modules can support the PROFIBUS protocol.

Module Type	PROFIBUS Support	RS485 Support
MitySOM-1810	Yes	Yes
MitySOM-1810F	Yes	Yes
MityDSP-L138	Yes	Yes
MityDSP-L138F	Yes	Yes
MitySOM-1808	No	Yes
MitySOM-1808F	No	Yes
MityDSP-6748F	No	Yes

The port also provides a +5.0V@100mA power via isolated power supply with 1000V* isolation from the primary supply as well as +3.3V@300mA from the main non-isolated power supply with a common ground. A single enable GPIO is also routed to this port in addition to the TX and RX UART signals.

The Electrical interface is provided via J504, 10-pin shrouded header

When the PROFIBUS/RS485 Expansion Board is used it provides galvanic isolation by a dedicated TI ISO1176 transceiver. The ISO1176 is powered by an isolated power supply with 2500Vrms* isolation from the primary supply. Jumpers on the PROFIBUS/RS485 Expansion Board can provide dedicated bus termination.

Please see the PROFIBUS/RS485 Expansion Board documentation found here: http://www.mitydsp.com/products-services/base-boards/interface-modules/expansion-profibus-rs485/

When the RS232 Expansion Board is used the transceiver on it is powered from the +3.3V supply of the Development Kit. It does not provide any isolation.

Please see the RS232 Expansion Board documentation found here: http://www.mitydsp.com/products-services/base-boards/interface-modules/expansion-rs232/

Note: On older Industrial IO Development Kit base boards, 80-000268RI-1 assemblies, the PROFIBUS/RS485 hardware was installed directly on the base board. The expansion board was not necessary and therefore not included. Please contact Critical Link for details or a previous datasheet if necessary.

Real Time Clock Battery

The Industrial IO Development Kit includes a battery used to provide power to the installed modules real time clock. This battery has been sized to allow for approximately 6 months of unpowered time with a module installed until the battery will be depleted.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage	13.2 V
Storage Temperature Range	0 to 80C

OPERATING CONDITIONS

Ambient Temperature Range	0 to 70C
Humidity	0 to 95% Non-condensing

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Power Dissipation					
V_S	Supply Voltage.		12±5%		V
I_S	Supply Current		0.45[1]		A
Real Time Clock (RTC) Battery					
I_{draw}	Current draw on battery with Module Installed		10		uA
$T_{duration}$	Battery life with Module Installed and no input power supplied		6		Months
Notes:	1. Power Supply load is dependent on Development Kit configuration and utilization.				

Notes: 1. Expansion card is not attached, 100% DSP/FPGA utilization, RS-232 and Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTION

Input Power

The Industrial IO Development Kit power interface, J600, requires a single +12Volt power supply.

Table 1: Input Power Interface Pin Description

Signal	J600 Position
+12V	1
GND	2

QVGA/WQVGA LVDS /Auxiliary Interface Description

The Auxiliary / LVDS interface connector provides up to 5 pairs of LVDS signals connected to the Spartan 6 device on a connected MitySOM / MityDSP (modules with FPGA only). The interface uses a standard 2mm 24 position male header. Table 3 defines the LVDS connector pinout when an FPGA enabled module is installed, Table 2 defines the pinout for Auxiliary interfaces from the module when a non-FPGA module is installed. In this case the signals are routed directly from the AM1810 or OMAP-L138 to this connector.

A cable using AMP® TBD connector (or equivalent) should be used. Use of the LVDS pairs as outputs will require addition of termination resistors (100 Ohm) on externally designed circuit assemblies. Use of the LVDS pairs as inputs will require population of 0603 sized termination resistors on the Industrial IO Development Kit on the provided solder pads. Refer to the detailed schematic and assembly drawing for further information.

Critical Link offers a line of off the shelf display solutions including a WQVGA 4.3" LCD Display with touchscreen that includes the necessary driver board, display and cable for quick development. Information is available about this solution on our website at: http://www.mitydsp.com/products-services/base-boards/interface-modules/expansion-wqvga/

Table 2: J104 Aux / LVDS Interface Pin Description – MitySOM/MityDSP without FPGA

Pin	Signal	Type	Standard	Notes
1	+5 V	Power	-	500 mA Max.
2	+5 V	Power	-	500 mA Max.
3	GND	Power	-	
4	GND	Power	-	
5	VP_CLKOUT3	I/O	3.3V LVCMOS	Software configurable OMAP IO
6	LCD_MCLK	I/O	3.3V LVCMOS	Software configurable OMAP IO
7	RESET_OUT	I/O	3.3V LVCMOS	Software configurable OMAP IO
8	VP_CLKIN3	I/O	3.3V LVCMOS	Software configurable OMAP IO
9	EMA_CS4	I/O	3.3V LVCMOS	Software configurable OMAP IO
10	EMA_CS5	I/O	3.3V LVCMOS	Software configurable OMAP IO
11	EMA_RAS	I/O	3.3V LVCMOS	Software configurable OMAP IO
12	EMA_CS2	I/O	3.3V LVCMOS	Software configurable OMAP IO
13	GND	Power	-	
14	GND	Power	-	
15	EMA_WE	I/O	3.3V LVCMOS	Software configurable OMAP IO
16	EMA_CAS	I/O	3.3V LVCMOS	Software configurable OMAP IO
17	GND	Power	-	
18	EMA_D11	I/O	3.3V LVCMOS	Software configurable OMAP IO
19	EMA_D12	I/O	3.3V LVCMOS	Software configurable OMAP IO
20	EMA_D13	I/O	3.3V LVCMOS	Software configurable OMAP IO
21	EMA_D14	I/O	3.3V LVCMOS	Software configurable OMAP IO
22	EMA_A12	I/O	3.3V LVCMOS	Software configurable OMAP IO
23	EMA_D15	I/O	3.3V LVCMOS	Software configurable OMAP IO
24	EMA_A13	I/O	3.3V LVCMOS	Software configurable OMAP IO

Note that these signals are pin-muxed in the CPU and may be available for a variety of functions.

Table 3: J104 Aux / LVDS Interface Pin Description – MitySOM/MityDSP with FPGA Installed

Pin	Signal	Type	Standard	Notes
1	+5 V	-	-	500 mA Max.
2	+5 V	-	-	500 mA Max.
3	GND	-	-	
4	GND	-	-	
5	DISP_A0_P	I/O	LVDS	Display/LVDS Data channel 0
6	DISP_A0_N	I/O	LVDS	Display/LVDS Data channel 0
7	DISP_A1_P	I/O	LVDS	Display/LVDS Data channel 1
8	DISP_A1_N	I/O	LVDS	Display/LVDS Data channel 1
9	DISP_A2_P	I/O	LVDS	Display/LVDS Data channel 2
10	DISP_A2_N	I/O	LVDS	Display/LVDS Data channel 2
11	DISP_A3_P	I/O	LVDS	Display/LVDS Data channel 3
12	DISP_A3_N	I/O	LVDS	Display/LVDS Data channel 3
13	GND	-	-	
14	GND	-	-	
15	DISP_CLKIN_P	I/O	LVDS	Display/LVDS Clock (or Data)
16	DISP_CLKIN_N	I/O	LVDS	Display/LVDS Clock (or Data)
17	GND	-	-	
18	SPARE IO	I/O	CMOS	Display Aux. I/O
19	DISP_I2	I	CMOS	Display Touch-screen Input 2
20	DISP_I1	I	CMOS	Display Touch-screen Input 1
21	DISP_I0	I	CMOS	Display Touch-screen Input 0
22	DISP_O2	O	CMOS	Display Touch-screen Output 2
23	DISP_O1	O	CMOS	Display Touch-screen Output 1
24	DISP_O0	O	CMOS	Display Touch-screen Output 0

Alternatively all IO can be configured as 3.3V CMOS and LVTTL IO

Expansion IO Interface

The Industrial IO Development Kit provides three expansion IO connectors. Each connector includes one 50 position dual row receptacle. Mating connectors for these receptacles is a 2x25 2mm male header.

Table 4 provides the signals descriptions for each pin when any type of supported MitySOM/MityDSP module is installed in the Industrial IO Development Kit.

Table 5 and Table 7 provide signal descriptions for each pin when a MitySOM/MityDSP without an FPGA is installed.

Table 6 and Table 8 provide signals description for each pin when a MitySOM/MityDSP with an FPGA installed. The modules with FPGA's include an on-board, user programmable Spartan-6 FPGA which provides the electrical standards for the various nets.

Table 4: J700 Connector Pin Assignments – MitySOM/MityDSP (with or without FPGA)

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	GND	Power		
4	GND	Power		
5	+3.3V	Power		250mA Max (Per pin)
6	+3.3V	Power		250mA Max (Per pin)
7	+3.3V	Power		250mA Max (Per pin)
8	+3.3V	Power		250mA Max (Per pin)
9	RESERVED			
10	RESERVED			
11	RESERVED			
12	RESERVED			
13	RESERVED			
14	RESERVED			
15	RESERVED			
16	RESERVED			
17	RESERVED			
18	RESERVED			
19	OMAP_GP0_5	I/O	3.3V LVCMOS	Software configurable GPIO
20	OMAP_GP0_15	I/O	3.3V LVCMOS	Software configurable GPIO
21	OMAP_GP0_13	I/O	3.3V LVCMOS	Software configurable GPIO
22	OMAP_GP0_6	I/O	3.3V LVCMOS	Software configurable GPIO
23	MMCSD0_CLK[1]		3.3V LVCMOS	MMC Interface Clock
24	MMCSD0_CMD[1]		3.3V LVCMOS	MMC Interface Command\ata
25	MMCSD0_DAT0[1]		3.3V LVCMOS	MMC Interface Data Bit 0
26	MMCSD0_DAT3[1]		3.3V LVCMOS	MMC Interface Data Bit 3
27	MMCSD0_DAT1[1]		3.3V LVCMOS	MMC Interface Data Bit 1
28	MMCSD0_DAT2[1]		3.3V LVCMOS	MMC Interface Data Bit
29	RESERVED			
30	RESERVED			
31	RESERVED			
32	RESERVED			
33	RESERVED			
34	RESERVED			
35	RESERVED			
36	RESERVED			
37	RESERVED			
38	RESERVED			
39	RESERVED			
40	RESERVED			
41	RESERVED			
42	RESERVED			
43	RESERVED			
44	GND	Power		
45	RESERVED			
46	GND	Power		
47	GND	Power		
48	GND	Power		
49	GND	Power		
50	GND	Power		

Note 1 - The MMCSD0 signals require the installation of 33 Ohm 0402 resistors for R700, R701, R702, R703, R704, and R705. Without the resistors, the corresponding pins on J700 are no-connects. Contact Critical Link for additional information.

Note that these signals are pin-muxed in the CPU and may be available for a variety of functions.

Table 5: J701 Connector Pin Assignments – MitySOM/MityDSP without FPGA

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	VP_CLKIN1		3.3V LVCMOS	Software configurable OMAP IO
4	UPP_CH1_START		3.3V LVCMOS	Software configurable OMAP IO
5	UPP_CH1_D14 / RMII_TXD0		3.3V LVCMOS	Software configurable OMAP IO
6	UPP_CH1_D15 / RMII_TXD1		3.3V LVCMOS	Software configurable OMAP IO
7	UPP_CH1_D12 / RMII_RXD1		3.3V LVCMOS	Software configurable OMAP IO
8	UPP_CH1_D13 / RMII_TXEN		3.3V LVCMOS	Software configurable OMAP IO
9	UPP_CH1_D10 / RMII_RXER		3.3V LVCMOS	Software configurable OMAP IO
10	UPP_CH1_D11 / RMII_RXD0		3.3V LVCMOS	Software configurable OMAP IO
11	UPP_CH1_D8 / RMII_CRS_DV		3.3V LVCMOS	Software configurable OMAP IO
12	UPP_CH1_D9 / RMII_REF_CLK		3.3V LVCMOS	Software configurable OMAP IO
13	UPP_CH1_D6		3.3V LVCMOS	Software configurable OMAP IO
14	UPP_CH1_D7		3.3V LVCMOS	Software configurable OMAP IO
15	GND	Power		
16	GND	Power		
17	OMAP_GP0_5	I/O	3.3V LVCMOS	Software configurable OMAP IO
18	OMAP_GP0_15	I/O	3.3V LVCMOS	Software configurable OMAP IO
19	OMAP_GP0_6	I/O	3.3V LVCMOS	Software configurable OMAP IO
20	OMAP_GP0_13	I/O	3.3V LVCMOS	Software configurable OMAP IO
21	OMAP_GP0_1	I/O	3.3V LVCMOS	Software configurable OMAP IO
22	OMAP_GP0_4	I/O	3.3V LVCMOS	Software configurable OMAP IO
23	OMAP_GP0_3	I/O	3.3V LVCMOS	Software configurable OMAP IO
24	OMAP_GP0_2	I/O	3.3V LVCMOS	Software configurable OMAP IO
25	OMAP_GP0_0	I/O	3.3V LVCMOS	Software configurable OMAP IO
26	RESERVED			
27	I2C0_SDA[3]	I/O	3.3V LVCMOS	Software configurable OMAP IO
28	I2C0_SCL[3]	I/O	3.3V LVCMOS	Software configurable OMAP IO
29	GND	Power		
30	GND	Power		
31	GND	Power		
32	GND	Power		
33	-12V[4]	Power		250mA Max (Per pin)
34	-12V[4]	Power		250mA Max (Per pin)
35	-12V[4]	Power		250mA Max (Per pin)
36	-12V[4]	Power		250mA Max (Per pin)
37	+3.3V[4]	Power		250mA Max (Per pin)
38	+3.3V[4]	Power		250mA Max (Per pin)
39	+3.3V[4]	Power		250mA Max (Per pin)
40	+3.3V[4]	Power		250mA Max (Per pin)
41	+5V[4]	Power		250mA Max (Per pin)
42	+5V[4]	Power		250mA Max (Per pin)
43	+5V[4]	Power		250mA Max (Per pin)
44	+5V[4]	Power		250mA Max (Per pin)
45	+12V[4]	Power		250mA Max (Per pin)
46	+12V[4]	Power		250mA Max (Per pin)
47	+12V[4]	Power		250mA Max (Per pin)
48	+12V[4]	Power		250mA Max (Per pin)
49	GND	Power		
50	GND	Power		

Note that these signals are pin-muxed in the CPU and may be available for a variety of functions.

Table 6: J701 Connector Pin Assignments – MitySOM/MityDSP with FPGA Installed

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	FPGA_IO_48_N[1,2]			Hardware Configurable FPGA IO
4	FPGA_IO_48_P[1,2]			Hardware Configurable FPGA IO
5	FPGA_IO_46_N[1,2]			Hardware Configurable FPGA IO
6	FPGA_IO_46_P[1,2]			Hardware Configurable FPGA IO
7	FPGA_IO_44_N[1,2]			Hardware Configurable FPGA IO
8	FPGA_IO_44_P[1,2]			Hardware Configurable FPGA IO
9	FPGA_IO_42_N[1,2]			Hardware Configurable FPGA IO
10	FPGA_IO_42_P[1,2]			Hardware Configurable FPGA IO
11	FPGA_IO_40_N[1,2]			Hardware Configurable FPGA IO
12	FPGA_IO_40_P[1,2]			Hardware Configurable FPGA IO
13	FPGA_IO_38_N[1,2]			Hardware Configurable FPGA IO
14	FPGA_IO_38_P[1,2]			Hardware Configurable FPGA IO
15	GND	Power		
16	GND	Power		
17	OMAP_GP0_5	I/O	3.3V LVCMOS	Software configurable GPIO
18	OMAP_GP0_15	I/O	3.3V LVCMOS	Software configurable GPIO
19	OMAP_GP0_6	I/O	3.3V LVCMOS	Software configurable GPIO
20	OMAP_GP0_13	I/O	3.3V LVCMOS	Software configurable GPIO
21	OMAP_GP0_1	I/O	3.3V LVCMOS	Software configurable GPIO
22	OMAP_GP0_4	I/O	3.3V LVCMOS	Software configurable GPIO
23	OMAP_GP0_3	I/O	3.3V LVCMOS	Software configurable GPIO
24	OMAP_GP0_2	I/O	3.3V LVCMOS	Software configurable GPIO
25	OMAP_GP0_0	I/O	3.3V LVCMOS	Software configurable GPIO
26	RESERVED			
27	I2C0_SDA[3]	I/O	3.3V LVCMOS	Software configurable GPIO
28	I2C0_SCL[3]	I/O	3.3V LVCMOS	Software configurable GPIO
29	GND	Power		
30	GND	Power		
31	GND	Power		
32	GND	Power		
33	-12V[4]	Power		250mA Max (Per pin)
34	-12V[4]	Power		250mA Max (Per pin)
35	-12V[4]	Power		250mA Max (Per pin)
36	-12V[4]	Power		250mA Max (Per pin)
37	+3.3V[4]	Power		250mA Max (Per pin)
38	+3.3V[4]	Power		250mA Max (Per pin)
39	+3.3V[4]	Power		250mA Max (Per pin)
40	+3.3V[4]	Power		250mA Max (Per pin)
41	+5V[4]	Power		250mA Max (Per pin)
42	+5V[4]	Power		250mA Max (Per pin)
43	+5V[4]	Power		250mA Max (Per pin)
44	+5V[4]	Power		250mA Max (Per pin)
45	+12V[4]	Power		250mA Max (Per pin)
46	+12V[4]	Power		250mA Max (Per pin)
47	+12V[4]	Power		250mA Max (Per pin)
48	+12V[4]	Power		250mA Max (Per pin)
49	GND	Power		
50	GND	Power		

Notes:
[1] 3.3V CMOS or 3.3V LVTTL Standard signal levels.
[2] <signal_name>_N/_P can be configured as a differential pair or single-ended FPGA I/O
[3] The I2C bus controlled by MitySOM / MityDSP hardware. Slave address 0x90 reserved for Power Management Controller IC. User should not attempt to write any data to this address as it will result in module damage.
[4] Maximum current per power bus should be limited to 1.0Amp, it is advised to have input fuses on expansion board.

Table 7: J702 Connector Pin Assignments – MitySOM/MityDSP without FPGA

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	UPP_CH1_D5	I/O	3.3V LVCMOS	Software configurable OMAP IO
4	UPP_CH1_ENABLE	I/O	3.3V LVCMOS	Software configurable OMAP IO
5	UPP_CH1_D3	I/O	3.3V LVCMOS	Software configurable OMAP IO
6	UPP_CH1_D4	I/O	3.3V LVCMOS	Software configurable OMAP IO
7	UPP_CH1_WAIT	I/O	3.3V LVCMOS	Software configurable OMAP IO
8	UPP_CH1_D2	I/O	3.3V LVCMOS	Software configurable OMAP IO
9	UPP_CH1_D0	I/O	3.3V LVCMOS	Software configurable OMAP IO
10	UPP_CH1_D1	I/O	3.3V LVCMOS	Software configurable OMAP IO
11	UPP_CH0_ENABLE	I/O	3.3V LVCMOS	Software configurable OMAP IO
12	UPP_CH1_CLK	I/O	3.3V LVCMOS	Software configurable OMAP IO
13	VP_CLKIN2	I/O	3.3V LVCMOS	Software configurable OMAP IO
14	VP_CLKOUT2	I/O	3.3V LVCMOS	Software configurable OMAP IO
15	UPP_CH0_START	I/O	3.3V LVCMOS	Software configurable OMAP IO
16	UPP_CH0_WAIT	I/O	3.3V LVCMOS	Software configurable OMAP IO
17	VP_CLKIN0	I/O	3.3V LVCMOS	Software configurable OMAP IO
18	UPP_CH0_CLK	I/O	3.3V LVCMOS	Software configurable OMAP IO
19	EMA_OE	I/O	3.3V LVCMOS	Software configurable OMAP IO
20	EMA_CS0	I/O	3.3V LVCMOS	Software configurable OMAP IO
21	EMA_BA1	I/O	3.3V LVCMOS	Software configurable OMAP IO
22	EMA_BA0	I/O	3.3V LVCMOS	Software configurable OMAP IO
23	EMA_A1	I/O	3.3V LVCMOS	Software configurable OMAP IO
24	EMA_A0	I/O	3.3V LVCMOS	Software configurable OMAP IO
25	EMA_A3	I/O	3.3V LVCMOS	Software configurable OMAP IO
26	EMA_A2	I/O	3.3V LVCMOS	Software configurable OMAP IO
27	EMA_A5	I/O	3.3V LVCMOS	Software configurable OMAP IO
28	EMA_A4	I/O	3.3V LVCMOS	Software configurable OMAP IO
29	EMA_A11	I/O	3.3V LVCMOS	Software configurable OMAP IO
30	EMA_A10	I/O	3.3V LVCMOS	Software configurable OMAP IO
31	EMA_A9	I/O	3.3V LVCMOS	Software configurable OMAP IO
32	EMA_A8	I/O	3.3V LVCMOS	Software configurable OMAP IO
33	EMA_A7	I/O	3.3V LVCMOS	Software configurable OMAP IO
34	EMA_A6	I/O	3.3V LVCMOS	Software configurable OMAP IO
35	EMA_D8	I/O	3.3V LVCMOS	Software configurable OMAP IO
36	EMA_D9	I/O	3.3V LVCMOS	Software configurable OMAP IO
37	Reserved	I/O	3.3V LVCMOS	Software configurable OMAP IO
38	Reserved	I/O	3.3V LVCMOS	Software configurable OMAP IO
39	EMA_CLK	I/O	3.3V LVCMOS	Software configurable OMAP IO
40	EMA_SDCKE	I/O	3.3V LVCMOS	Software configurable OMAP IO
41	EMA_WEN_DQM1	I/O	3.3V LVCMOS	Software configurable OMAP IO
42	EMA_WEN_DQM0	I/O	3.3V LVCMOS	Software configurable OMAP IO
43	EMA_D0	I/O	3.3V LVCMOS	Software configurable OMAP IO
44	EMA_D1	I/O	3.3V LVCMOS	Software configurable OMAP IO
45	EMA_D2	I/O	3.3V LVCMOS	Software configurable OMAP IO
46	EMA_D3	I/O	3.3V LVCMOS	Software configurable OMAP IO
47	EMA_D4	I/O	3.3V LVCMOS	Software configurable OMAP IO
48	EMA_D5	I/O	3.3V LVCMOS	Software configurable OMAP IO
49	GND	Power		
50	GND	Power		

Table 8: J702 Connector Pin Assignments – MitySOM/MityDSP with FPGA Installed

Pin	Signal	Type	Standard	Notes
1	GND	Power		
2	GND	Power		
3	FPGA_IO_36_N[1]	I/O	LVDS, 3.3V LVCMOS/LVTTL	
4	FPGA_IO_36_P[1]	I/O	LVDS, 3.3V LVCMOS/LVTTL	
5	FPGA_IO_34_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
6	FPGA_IO_34_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
7	FPGA_IO_32_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
8	FPGA_IO_32_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
9	FPGA_IO_30_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
10	FPGA_IO_30_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
11	FPGA_IO_28_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
12	FPGA_IO_28_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
13	FPGA_IO_26_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
14	FPGA_IO_26_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
15	FPGA_IO_24_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
16	FPGA_IO_24_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
17	FPGA_IO_22_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
18	FPGA_IO_22_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
19	FPGA_IO_47_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
20	FPGA_IO_47_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
21	FPGA_IO_45_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
22	FPGA_IO_45_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
23	FPGA_IO_43_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
24	FPGA_IO_43_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
25	FPGA_IO_41_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
26	FPGA_IO_41_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
27	FPGA_IO_39_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
28	FPGA_IO_39_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
29	FPGA_IO_33_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
30	FPGA_IO_33_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
31	FPGA_IO_35_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
32	FPGA_IO_35_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
33	FPGA_IO_37_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
34	FPGA_IO_37_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
35	FPGA_IO_23_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
36	FPGA_IO_23_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
37	RESERVED			
38	RESERVED			
39	FPGA_IO_11_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
40	FPGA_IO_11_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
41	FPGA_IO_13_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
42	FPGA_IO_13_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
43	FPGA_IO_15_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
44	FPGA_IO_15_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
45	FPGA_IO_17_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
46	FPGA_IO_17_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
47	FPGA_IO_19_N	I/O	LVDS, 3.3V LVCMOS/LVTTL	
48	FPGA_IO_19_P	I/O	LVDS, 3.3V LVCMOS/LVTTL	
49	GND	Power		
50	GND	Power		

Notes:
[1] <signal_name>_N/_P can be configured as a differential pair or single-ended FPGA IO.

Signal Naming Description

Table 9: Daughter Card Signal Description

Signal	Type	Standard	Notes
FPGA_IO_##_N/P	I/O	LVDS/3.3V CMOS/ 3.3V LVTTL	Direct Interface to MitySOM / MityDSP Spartan6 FPGA.
OMAP_GP0_##	I/O	3.3V CMOS	Direct Interface to MitySOM / MityDSP processor
DO_##	O	3.3V CMOS	Digital Output. Update Rate of 20 nsec. DO_CLK provides sampling clock – outputs should be sampled on rising edge.
DI_##	I	3.3V CMOS	Digital Input. Sampling interval < 2 µs.

CAN Interface

Table 10: J501 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	RESERVED			
2	CANL	I/O		CAN Bus Signal L
3	GND	Power		CAN Bus Isolated Ground
4	RESERVED			
5	RESERVED			
6	RESERVED			
7	CANH	I/O		CAN Bus Signal H
8	RESERVED			
9	+5V	Power		Isolated +5V Output, 20mA Max
10	RESERVED			

Notes: please see Figure 2 for physical pin-out of connector

UART Expansion Interface (80-000268RI-2 Assemblies)

Table 11: J504 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	RS485_TX_ENB	I/O		Software configurable OMAP IO
2	RS485_RX	I/O		Software configurable OMAP IO (UART2_RX/I2C_SCL/GPIO)
3	+3.3V	I/O		+3.3V 300mA Max
4	RESERVED			
5	GND_ISO485	Power		Isolated RS485 GND
6	RS485_TX	IO		Software configurable OMAP IO (UART2_TX/I2C1_SDA/GPIO)
7	GND	Power		System GND
8	RESERVED			
9	RESERVED			
10	+5V_RS485	Power		Isolated +5V Output, 100mA Max

Notes: please see Figure 2 for physical pin-out of connector

Note: On older Industrial IO Development Kit base boards, 80-000268RI-1 assemblies, the PROFIBUS/RS485 hardware was installed directly on the base board. The expansion board was not necessary and therefore not included. Please contact Critical Link for details or a previous datasheet if necessary.

RS-232 Interface

Table 12: J502 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	RESERVED			
2	RS232_RX	I		RS232-level Input Signal
3	RS232_TX	O		RS232-level Output Signal
4	RESERVED			
5	GND	Power		RS-232 Ground
6	RESERVED			
7	RESERVED			
8	RESERVED			
9	RESERVED			
10	RESERVED			

Notes: please see Figure 2 for physical pin-out of connector

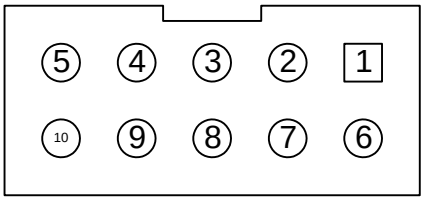


Figure 2: J501, J502, J504 Pin-out (Top View)

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

Board mounting is compatible to ETX standard.

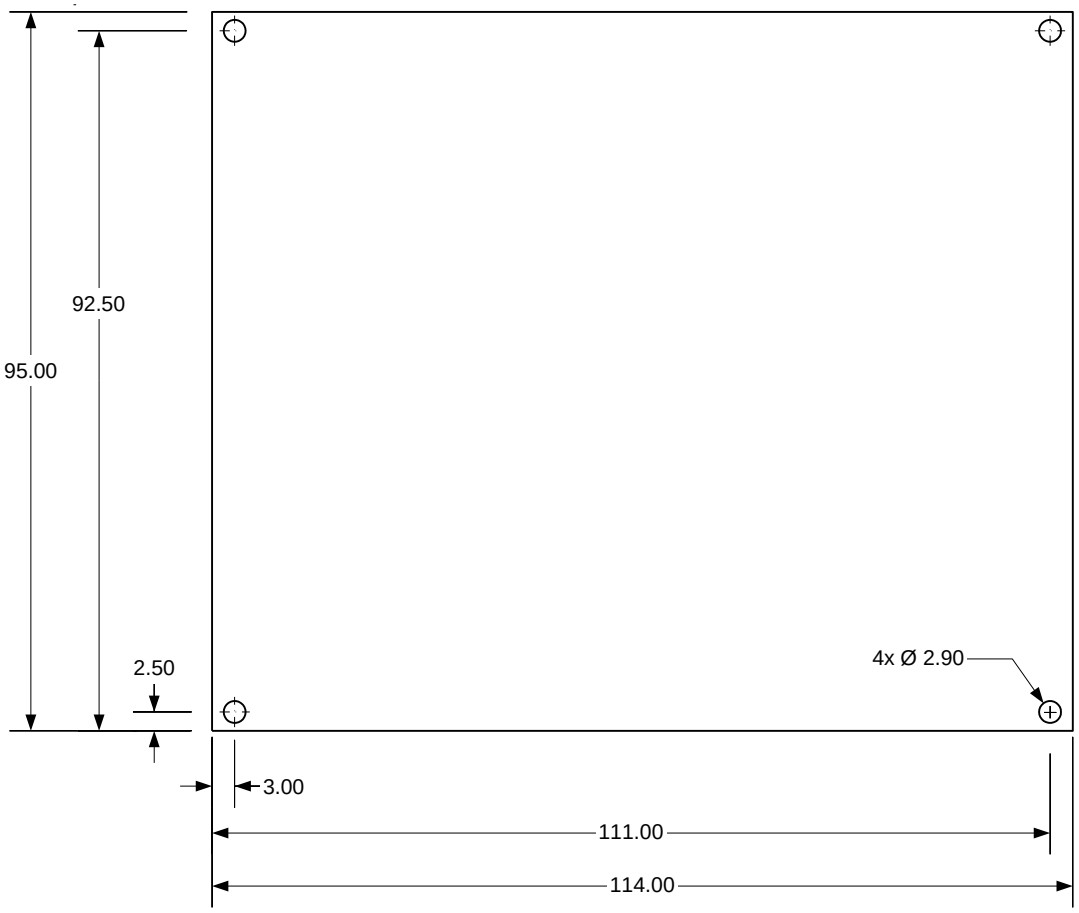


Figure 3: Industrial IO Development Kit Outline and Mounting Holes Locations (Top View, mm)

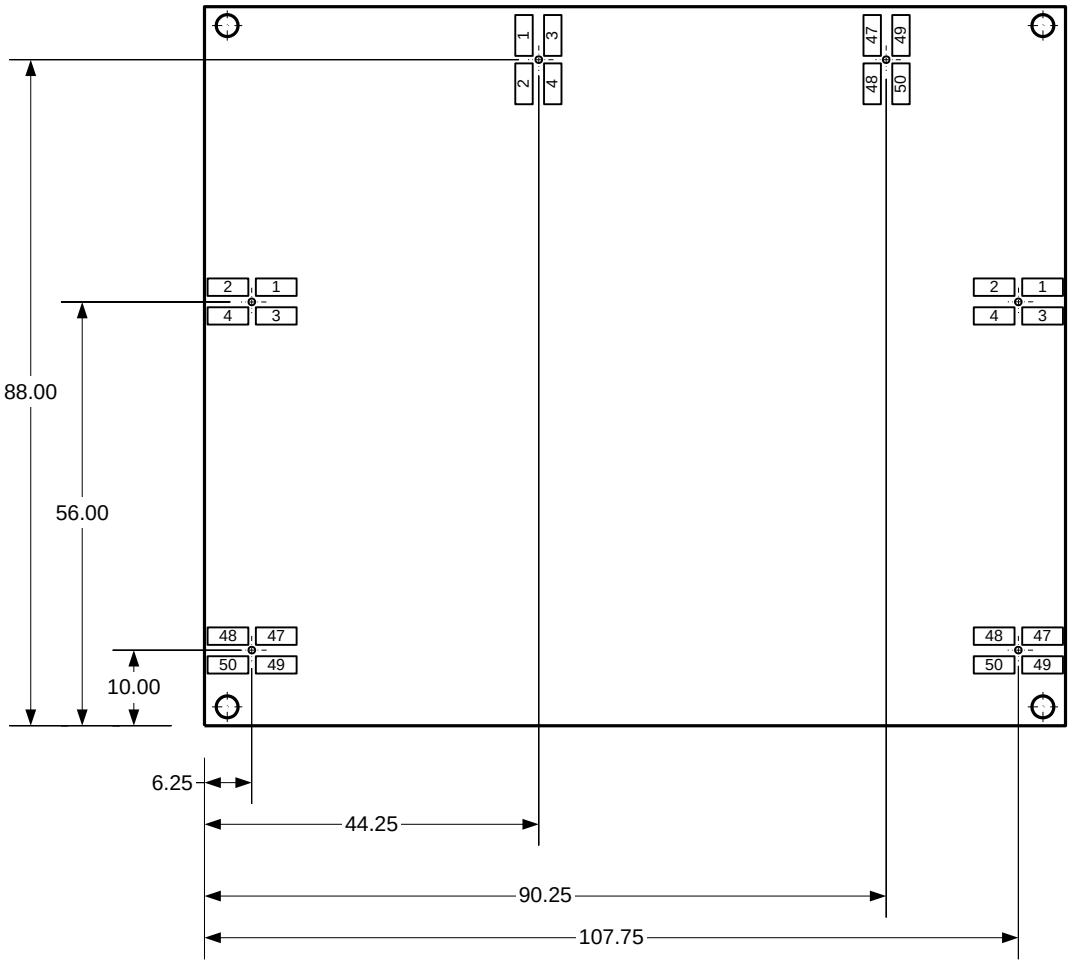


Figure 4: Mounting holes for expansion I/O connectors based on Molex 79109-1224 connector (Top View, mm)

ORDERING INFORMATION

Development Kits

The following table lists the standard Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 13: Standard Model Numbers

Development Kit Model	Module Included	PROFIBUS Support	LVDS/LCD Support
80-000365	L138-FI-225-RC	Yes	Yes
80-000382	L138-FI-236-RL	Yes	Yes
80-000395	L138-FG-225-RC	Yes	Yes
80-000413	L138-DG-225-RI	Yes	Yes
80-000454	L138-DI-225-RI	Yes	Yes
80-000334	L138-FX-225-RC	Yes	No
80-000315	1808-FG-225-RC	No	Yes
80-000317	1808-FX-225-RC	No	No
80-000320	1810-DG-225-RC	Yes	Yes
80-000348	1810-DX-225-RC	Yes	No
*Contact Critical Link	6748-FG-225-RC	No	Yes

Expansions Kits

The following table lists the available expansion kits for the above development kits. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 14: Expansion Kit Model Numbers

Expansion Kit Model	Type	Interface Port	Notes
80-000541	RS232 Expansion Board	J504	Any module
80-000540	PROFIBUS/RS485 Expansion Board	J504	See above table. All modules support RS485.
80-000536	WQVGA LCD w/Driver Board	J104	Any module WITH an FPGA

REVISION HISTORY

Date	Change Description
22-NOV-2010	Initial revision. 80-000268-RI-1 assemblies.
27-AUG-2012	General updates and changes for 80-000268-RI-2 assemblies.
27-SEP-2012	Updated J700 info regarding MMC signals and removed SPI_CS0 (pin 29) as it is reserved for SPI NOR FLASH. Addressed pin naming issues for J700, J701 and J702.
27-MAR-2013	Updated 5V Isolated current output to 100mA from 150mA
5-MAR-2014	Update MitySOM product name. Corrected J702 pin 26.

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