

CR10N60F A9K

General Description:

CR10N60F A9K, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

Features:

- **Fast Switching**
- **Low ON Resistance**
- **Low Gate Charge**
- **Low Reverse transfer capacitances**
- **100% Single Pulse avalanche energy Test**

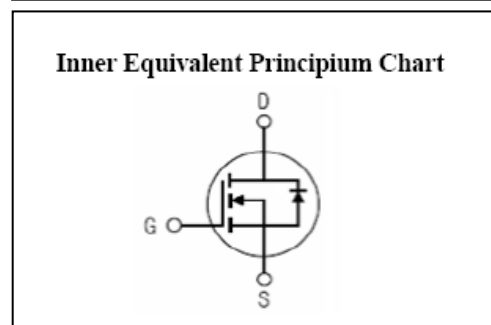
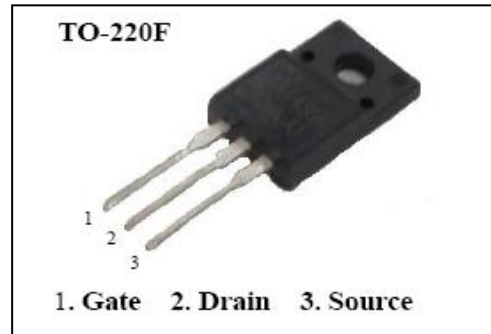
Applications:

Power switch circuit of adaptor and charger.

Absolute (Tc= 25°C unless otherwise specified):

Symbol	Parameter	Rating	Units
V _{DSS}	Drain-to-Source Voltage	600	V
I _D	Continuous Drain Current	10	A
	Continuous Drain Current T _C = 100 °C	6.3	A
I _{DM} ^{a1}	Pulsed Drain Current	40	A
V _{GS}	Gate-to-Source Voltage	± 30	V
E _{AS} ^{a2}	Single Pulse Avalanche Energy	580	mJ
dv/dt ^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P _D	Power Dissipation	40	W
	Derating Factor above 25 °C	0.32	W/°C
T _J , T _{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	°C
T _L	Maximum Temperature for Soldering	300	°C

V _{DSS}	600	V
I _D	10	A
P _D (T _C =25°C)	40	W
R _{DS(ON)Typ}	0.68	Ω



Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Unit s
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	600	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	$I_D=250\mu A, \text{Reference } 25^\circ\text{C}$	--	0.67	--	$V/^\circ\text{C}$
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=600V, V_{GS}=0V, T_J=25^\circ\text{C}$	--	--	1	μA
		$V_{DS}=480V, V_{GS}=0V, T_J=125^\circ\text{C}$	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+30V$	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-30V$	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V, I_D=5A$	--	0.68	0.9	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	--	4.0	V
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=15V, I_D=5A$	--	9.5	--	S
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$	--	1530	--	pF
C_{oss}	Output Capacitance		--	116	--	
C_{rss}	Reverse Transfer Capacitance		--	4.9	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D = 10A, V_{DD} = 300V, R_G = 10\Omega$	--	26	--	ns
t_r	Rise Time		--	23	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	49	--	
t_f	Fall Time		--	27	--	
Q_g	Total Gate Charge	$I_D = 10A, V_{DD} = 480V, V_{GS} = 10V$	--	31	--	nC
Q_{gs}	Gate to Source Charge		--	7	--	
Q_{gd}	Gate to Drain ("Miller") Charge		--	12	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	10	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	40	A
V_{SD}	Diode Forward Voltage	$I_S=10A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=10A, T_j = 25^\circ C$ $dI_F/dt=100A/us,$ $V_{GS}=0V$	--	1010	--	ns
Q_{rr}	Reverse Recovery Charge		--	5150	--	nC
I_{RRM}	Reverse Recovery Current		--	13.5	--	A
Pulse width $t_p \leq 300 \mu s, \delta \leq 2\%$						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	3.13	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	62.5	$^\circ C/W$

^{a1}: Repetitive rating; pulse width limited by maximum junction temperature

^{a2}: $L=10mH, I_D=10A, \text{Start } T_j=25^\circ C$

^{a3}: $I_{SD}=10A, di/dt \leq 100A/us, V_{DD} \leq BV_{DS}, \text{Start } T_j=25^\circ C$

Test Circuit and Waveform

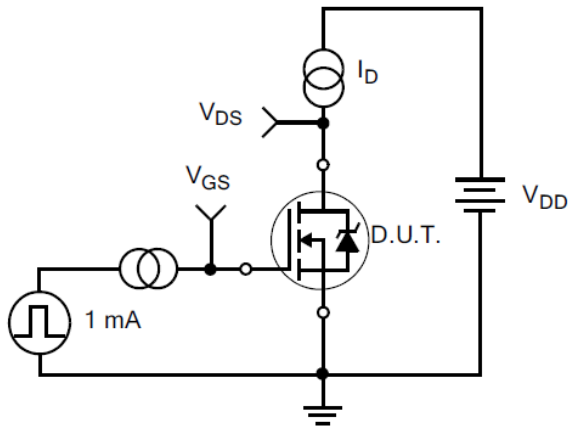


Figure 14. Gate Charge Test Circuit

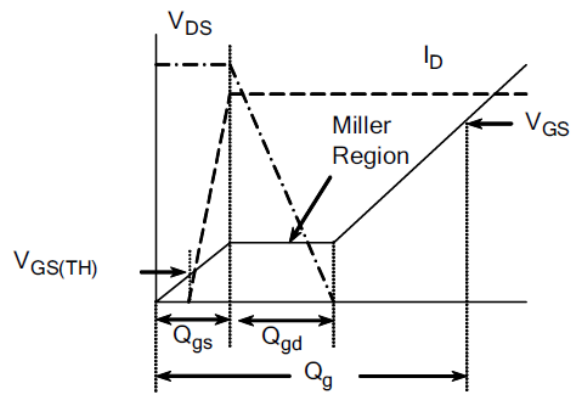


Figure 15. Gate Charge Waveforms

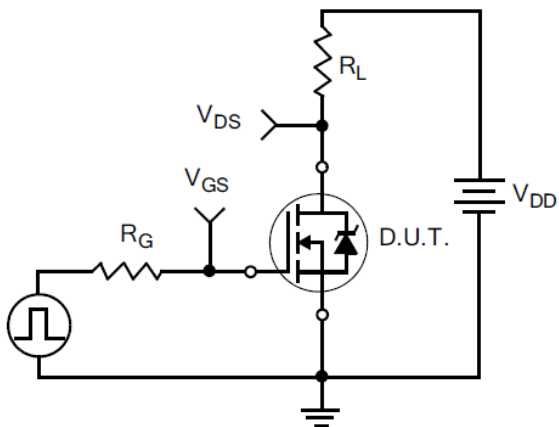


Figure 16. Resistive Switching Test Circuit

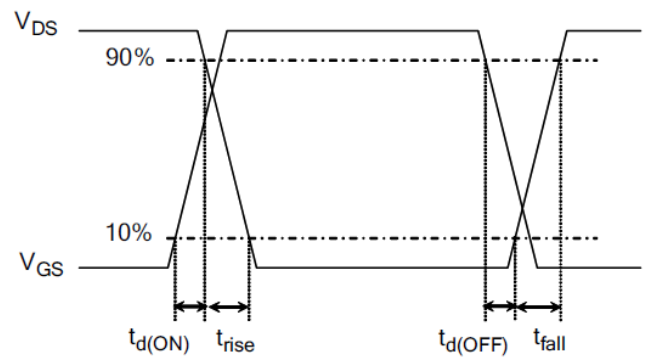


Figure 17. Resistive Switching Waveforms

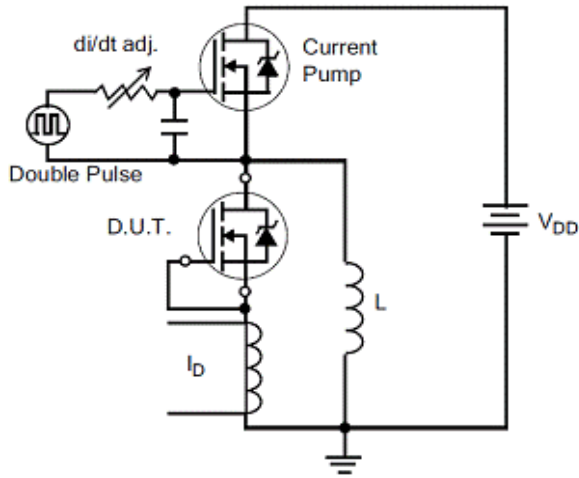


Figure 18. Diode Reverse Recovery Test Circuit

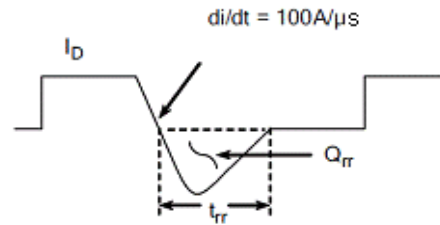


Figure 19. Diode Reverse Recovery Waveform

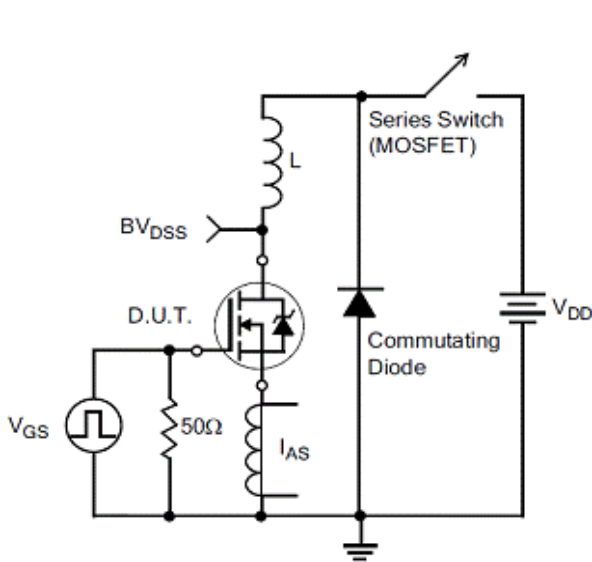


Figure20.Unclamped Inductive Switching Test Circuit

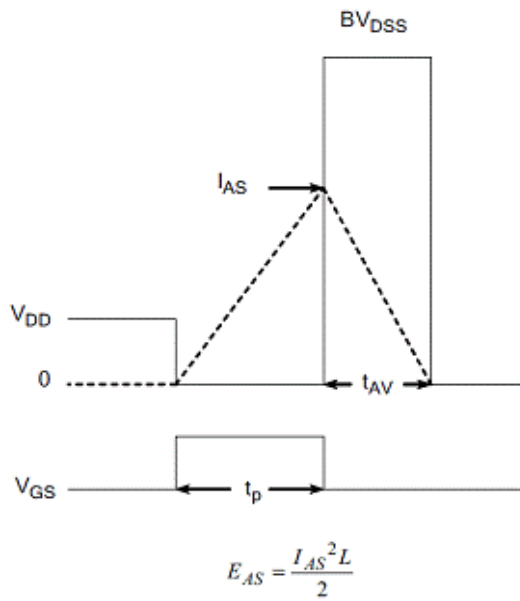
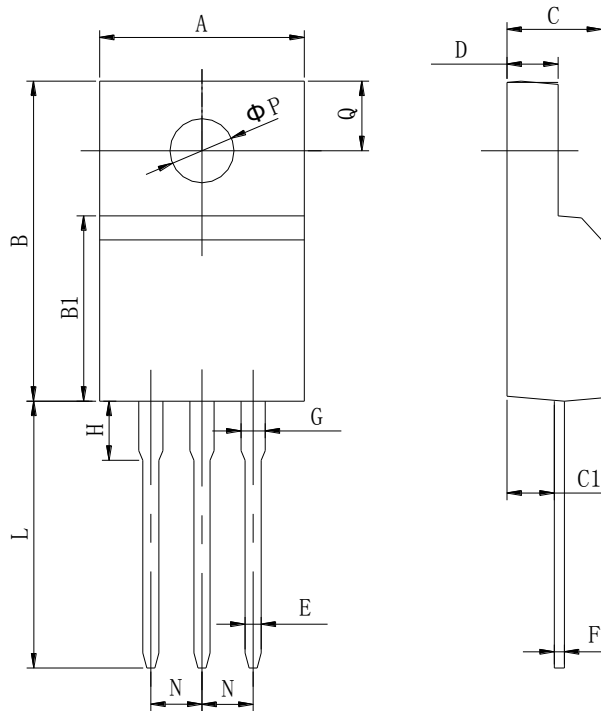


Figure21.Unclamped Inductive Switching Waveform

Package Information


Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
L*	12.0	14.0
N	2.34	2.74
Q	3.15	3.55
ϕP	2.90	3.30

*adjustable

TO-220F Package

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