

Features

- Uses CRM(CQ) advanced SkyMOS1 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

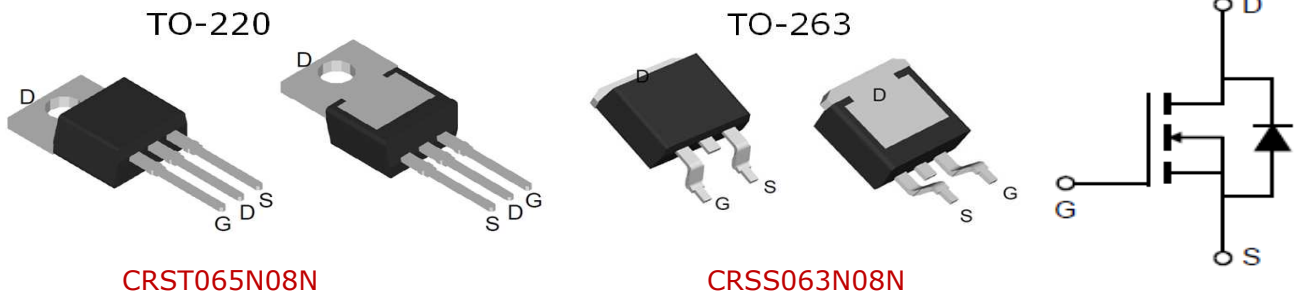
Applications

- Motor control and drive
- Battery management
- UPS (Uninterruptible Power Supplies)

Product Summary

V_{DS}	85V
$R_{DS(on)}$	5.6mΩ
I_D	80A

100% Avalanche Tested



CRST065N08N

CRSS063N08N

Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRST065N08N	-	TO-220	Tube	N/A	N/A	50pcs
CRSS063N08N	-	TO-263	Tube	N/A	N/A	50pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	85	V
Continuous drain current	I_D	$T_C = 25^\circ\text{C}$ (Silicon limit)	121
		$T_C = 25^\circ\text{C}$ (Package limit)	80
		$T_C = 100^\circ\text{C}$ (Silicon limit)	77
Pulsed drain current ($T_C = 25^\circ\text{C}$, t_p limited by T_{jmax})	$I_{D\ pulse}$	320	A
Avalanche energy, single pulse ($L=0.5\text{mH}$, $R_g=25\Omega$)	$E_{AS(\text{Note 1})}$	110	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation ($T_C = 25^\circ\text{C}$)	P_{tot}	164	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$

※. Notes: 1.EAS is tested at starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $I_{AS} = 21\text{A}$, $V_{GS} = 10\text{V}$.
 $I_{AS(\text{max})}=42\text{A}$; $E_{AS(\text{max})}=441\text{mJ}$ under above Conditions;

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	0.76	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	65	

Electrical Characteristic (at $T_j = 25\text{ }^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	85	97	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	0.05	1	μA	$V_{DS}=80V, V_{GS}=0V$ $T_j=25^\circ C$ $T_j=125^\circ C$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.6	6.5	mΩ	$V_{GS}=10V, I_D=50A$ TO-220
		-	5.4	6.3		TO-263
Transconductance	g_{fs}	-	70	-	S	$V_{DS}=5V, I_D=40A$

Dynamic Characteristic

Input Capacitance	C_{iss}	-	2860	-	pF	$V_{GS}=0V, V_{DS}=42.5V,$ $f=1MHz$
Output Capacitance	C_{oss}	-	790	-		
Reverse Transfer Capacitance	C_{rss}	-	19	-		
Gate Total Charge	Q_G	-	47	-	nC	$V_{GS}=10V, V_{DS}=40V,$ $I_D=50A, f=1MHz$
Gate-Source charge	Q_{gs}	-	13	-		
Gate-Drain charge	Q_{gd}	-	11	-		
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	$V_{ds}=42.5V$ $I_d=10A$ $R_g=3.5\Omega$ $V_{gs}=10V;$ (Note 2,3)
Rise time	t_r	-	31	-		
Turn-off delay time	$t_{d(off)}$	-	36	-		
Fall time	t_f	-	19	-		
Gate resistance	R_G	-	3.3	-	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.9	1.4	V	$V_{GS}=0V, I_{SD}=50A$
Body Diode Reverse Recovery Time	t_{rr}	-	56	-	ns	$I_S=30A, V_{GS}=0V,$ $dI_F/dt=100A/us;$
Body Diode Reverse Recovery Charge	Q_{rr}	-	54	-	nC	

※. Notes

2.Pulse Test : Pulse Width $\leq 300us$, duty cycle $\leq 2\%$.

3.Essentially independent of operating temperature.

Typical Performance Characteristics

Fig 1: Output Characteristics

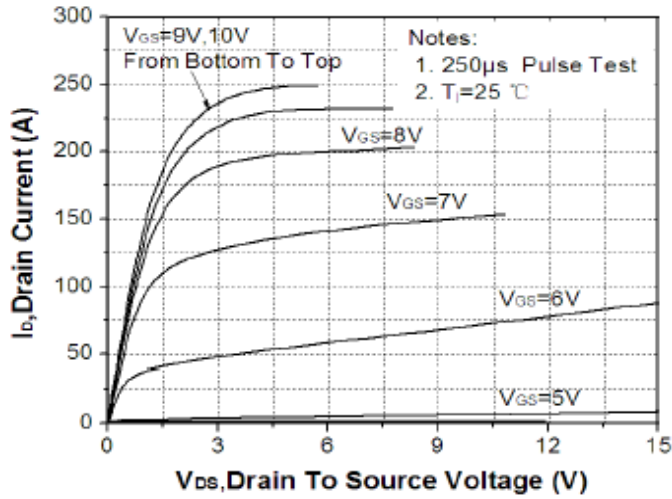


Fig 2: Transfer Characteristics

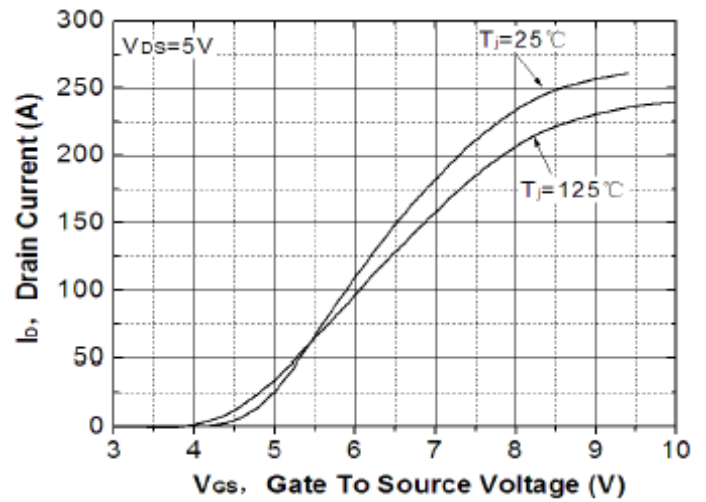


Fig 3: R_{ds(on)} vs Drain Current and Gate Voltage

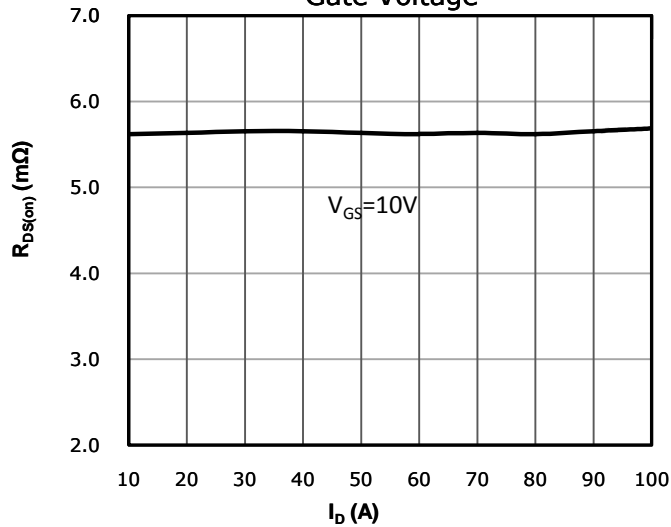


Fig 4: R_{ds(on)} vs Gate Voltage

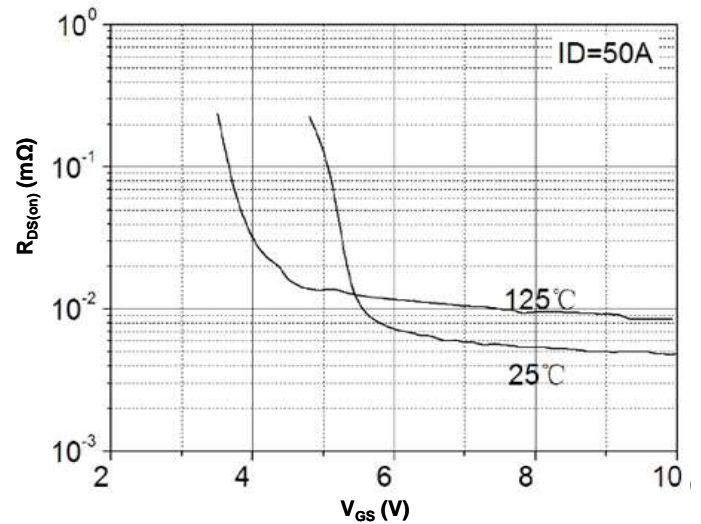


Fig 5: R_{ds(on)} vs. Temperature

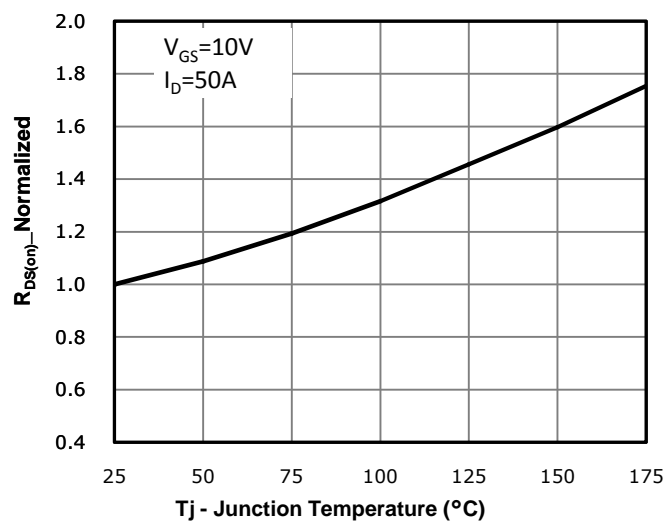


Fig 6: Capacitance Characteristics

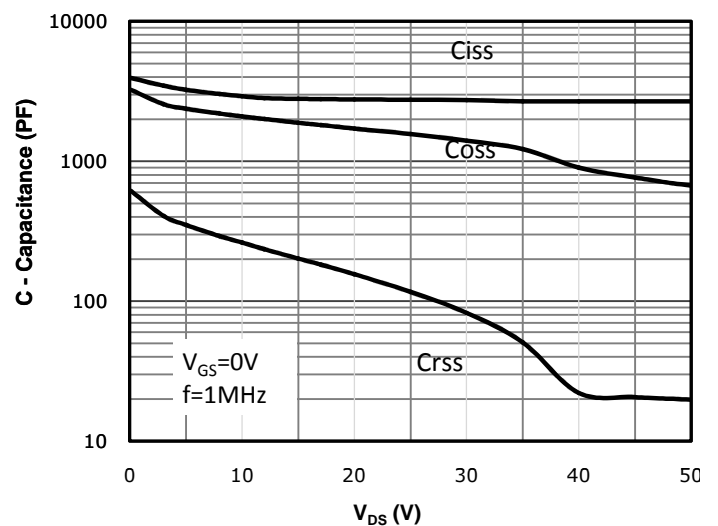


Fig 7: Gate Charge Characteristics

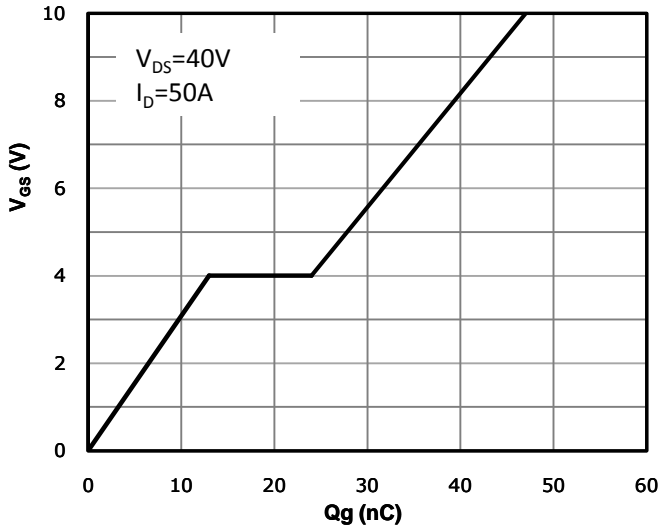


Fig 8: Body-diode Forward Characteristics

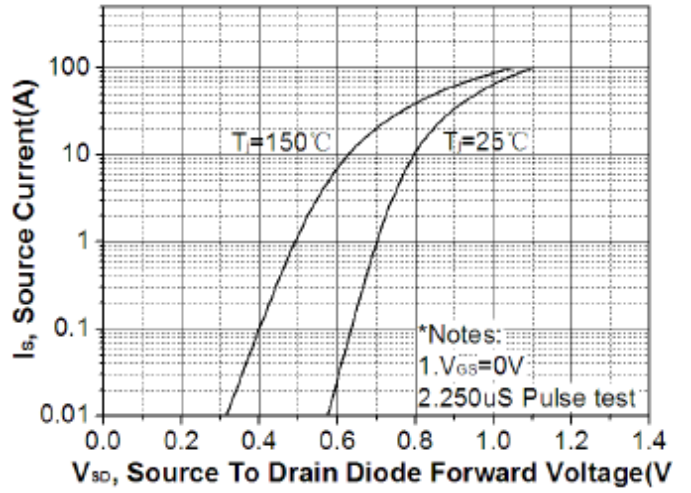


Fig 9: Power Dissipation

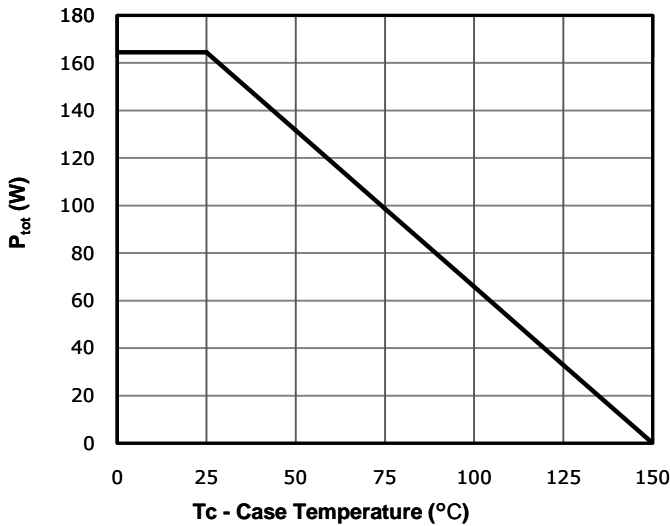


Fig 10: Drain Current Derating

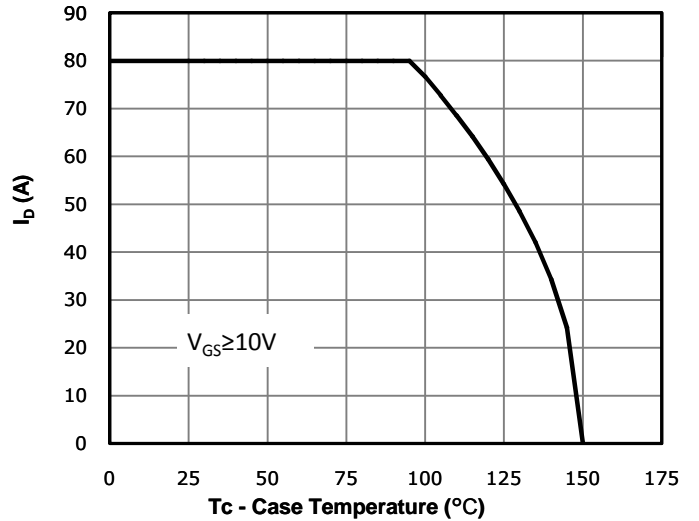


Fig 11: Safe Operating Area

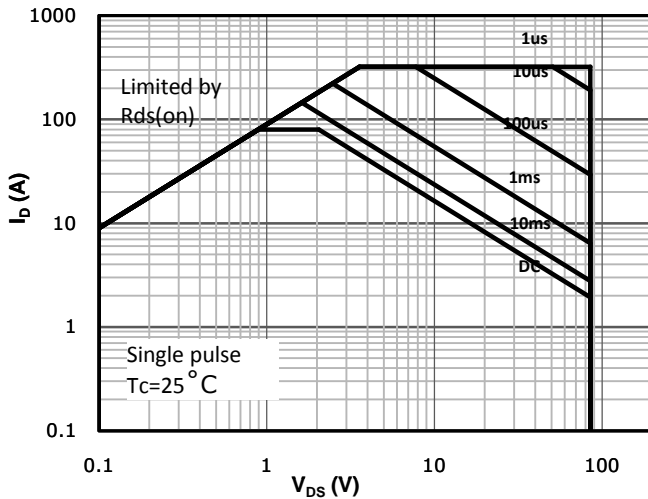
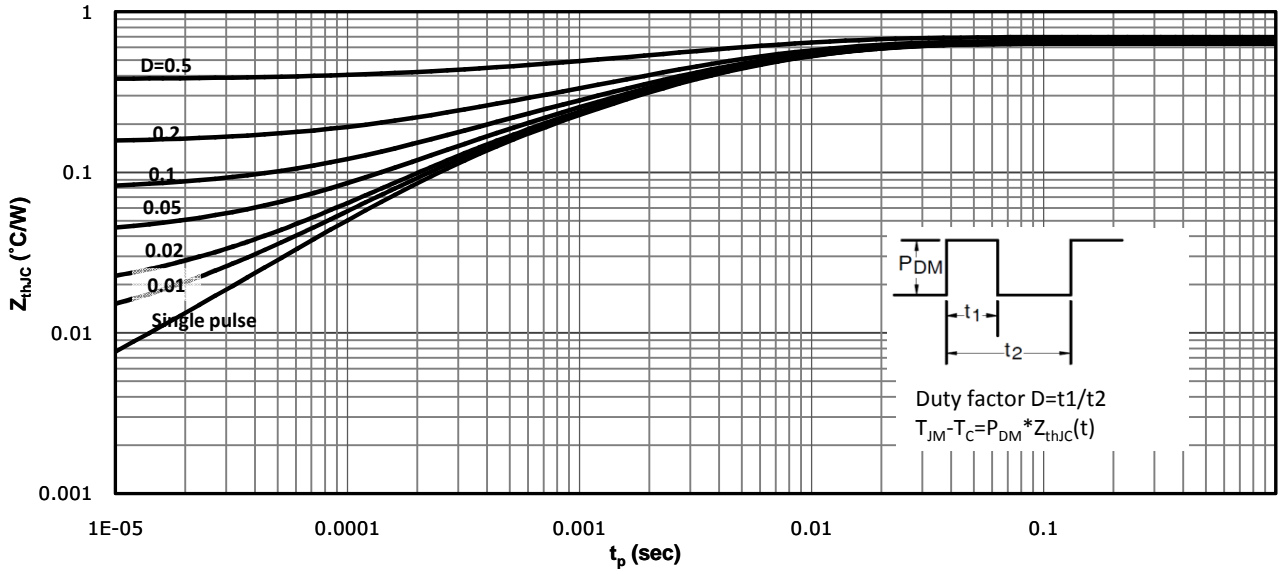
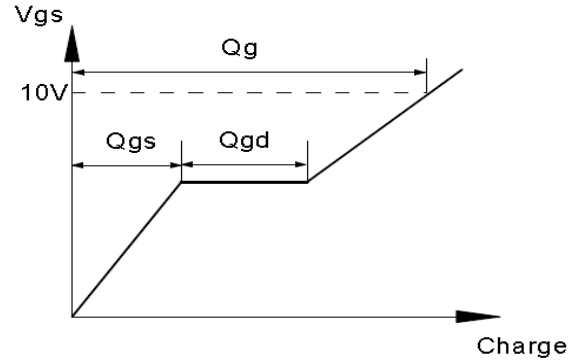
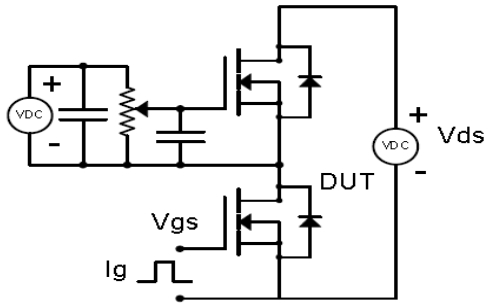


Fig 12: Max. Transient Thermal Impedance

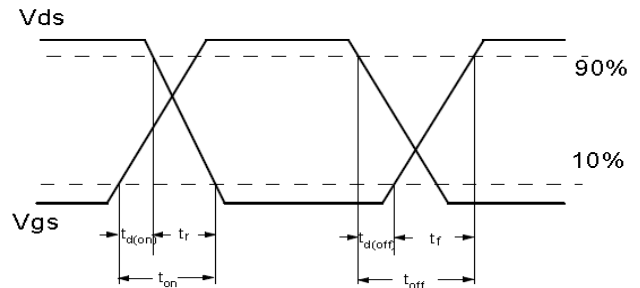
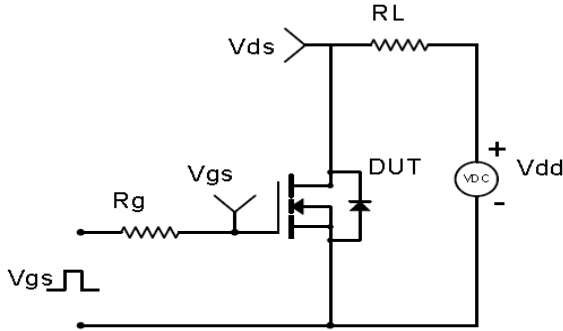


Test Circuit & Waveform

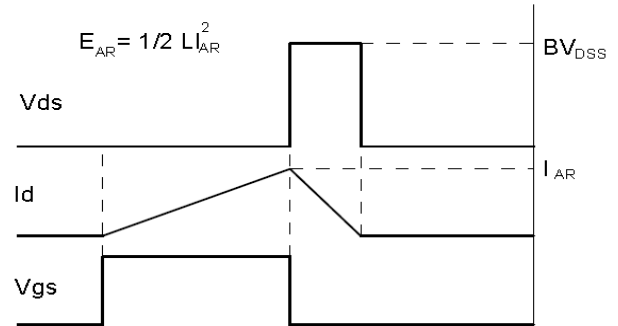
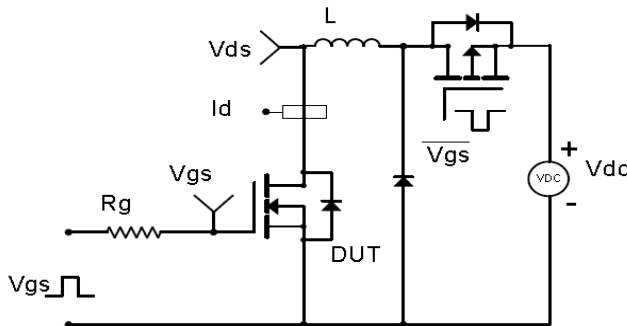
Gate Charge Test Circuit & Waveform



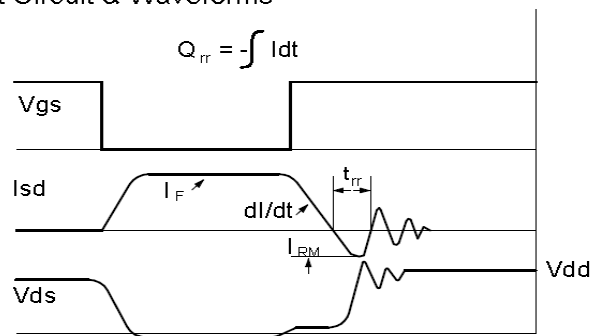
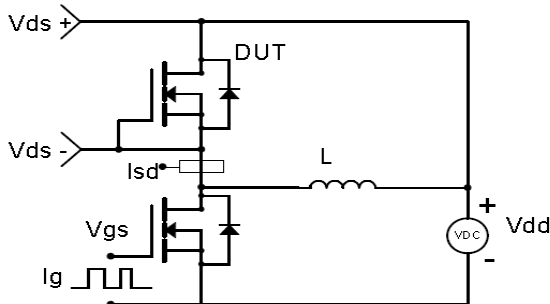
Resistive Switching Test Circuit & Waveforms



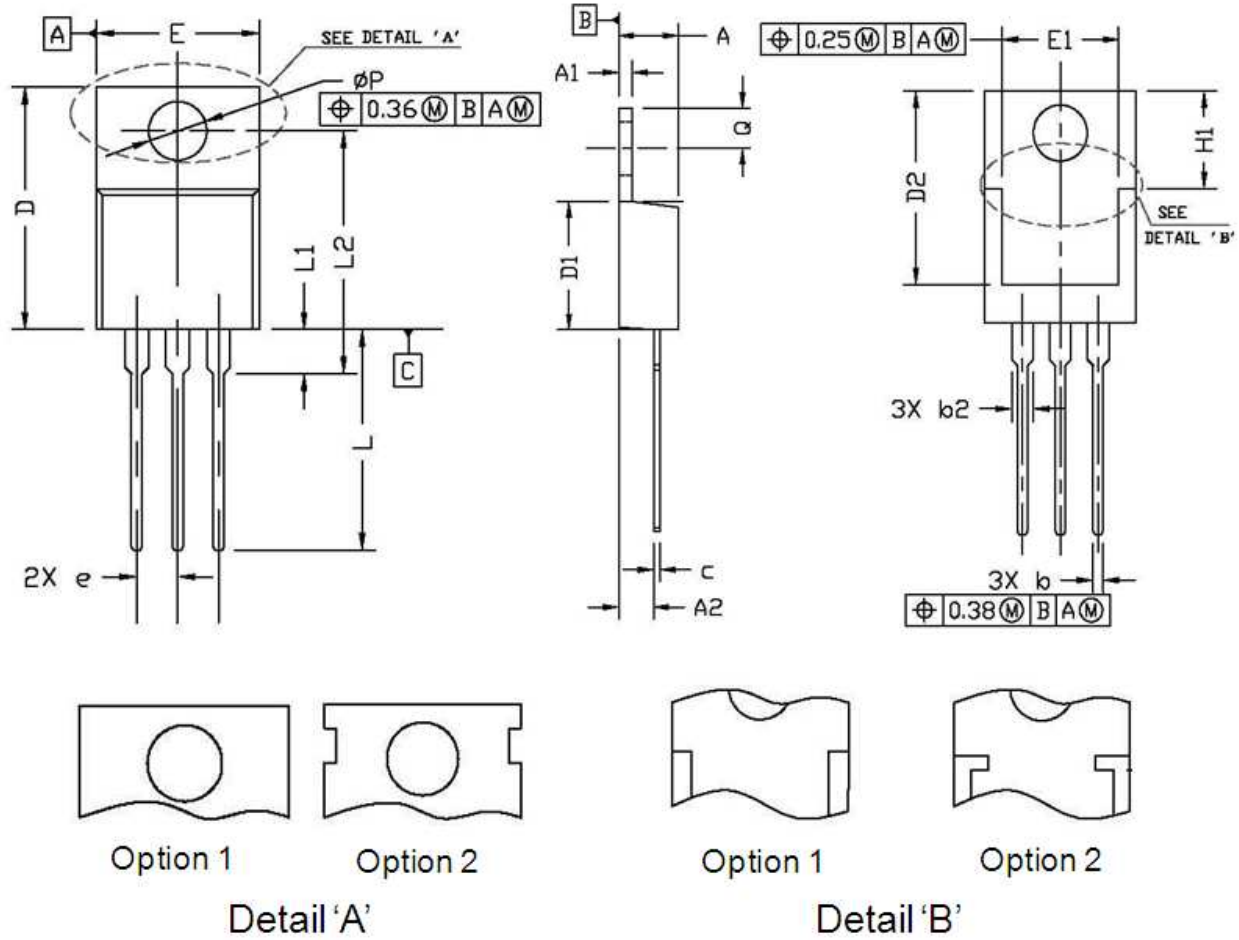
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

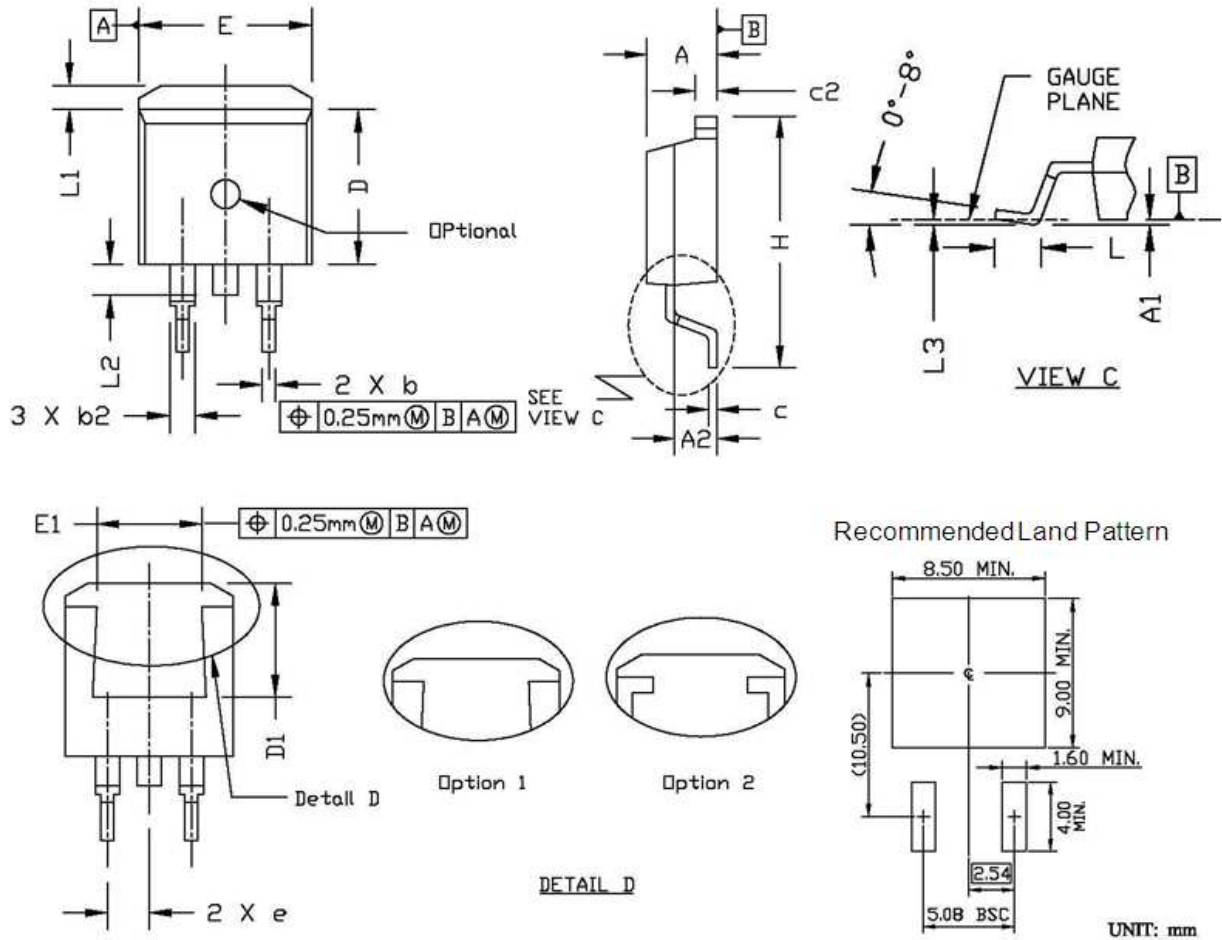


Package Outline: TO-220-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.30	4.80	0.169	0.189
A1	1.20	1.45	0.047	0.057
A2	2.20	2.90	0.087	0.114
b	0.69	0.95	0.027	0.037
b2	1.00	1.60	0.039	0.063
c	0.33	0.65	0.013	0.026
D	14.70	16.20	0.579	0.638
D1	8.59	9.65	0.338	0.380
D2	11.75	13.60	0.463	0.535
e	2.54 BSC.		0.100 BSC.	
E	9.60	10.60	0.378	0.417
E1	7.00	8.46	0.276	0.333
H1	6.20	7.00	0.244	0.276
L	12.60	14.80	0.496	0.583
L1	2.70	3.80	0.106	0.150
L2	12.13	16.50	0.478	0.650
Q	2.40	3.10	0.094	0.122
P	3.50	3.90	0.138	0.154

Package Outline: TO-263



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.30	4.86	0.169	0.191
A1	0.00	0.25	0.000	0.010
A2	2.34	2.79	0.092	0.110
b	0.68	0.94	0.027	0.037
b2	1.15	1.35	0.045	0.053
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.38	9.45	0.330	0.372
D1	6.90	8.17	0.272	0.322
e	2.54 BSC.		0.100 BSC.	
E	9.78	10.50	0.385	0.413
E1	6.50	8.60	0.256	0.339
H	14.61	15.88	0.575	0.625
L	2.24	3.00	0.088	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
L3	0.00	0.25	0.000	0.010

Revision History

Revision	Date	Major changes
1.0	2018-02-09	Release of formal version.
2.0	2019-05-28	Supplement package outline info.

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qualified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

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