

CC6420

Low Noise, High Efficiency, 5V/12V 450mA Single Coil Sine Wave Current Motor Driver

FEATURES

- ◆ Built-in high sensitive hall sensor
- ◆ High efficiency, Zero Current Switch (ZCS) and Zero magnet Switch (ZBS)
- ◆ Low noise, using SVPWM technology to realize sine wave control of the motor, reducing electromagnetic noise
- ◆ PWM speed control with minimal speed setting
- ◆ Strong driving capability, $R_{\text{DS(on)}} = 1.5\Omega$, High output current, up to 450mA
- ◆ Wide operating voltage, 3.5V to 18V
- ◆ Rotation Detect (RD) and Frequency Generator (FG) are optional
- ◆ Protection: Reverse voltage, Thermal Protection, LRP (Lock Rotation Protection), Current Limit Protection
- ◆ AGC control
- ◆ Intelligent soft start, reduce the motor starting current, reduce the impact on the power supply
- ◆ The rotational speed curve is configurable
- ◆ ESD (HBM) 6kV

APPLICATION

- ◆ Single Coil Brushless DC Motor
- ◆ Single Coil Brushless DC Fan

GENERAL DESCRIPTION

CC6420 is a one-chip solution for single-coil brushless DC motor/fan with PWM speed control.

The chip is designed and manufactured using an innovative advanced high-voltage BiCMOS process that is optimized for Hall sensors and motor drives. It integrates a driver power tube, a voltage regulator module, a high-precision Hall sensor, a chopper offset cancellation module, a Hall signal linear amplification and modulation module, and a digital logic control module.

In terms of motor control, it has a soft-start function, which can eliminate the spike current when the motor starts. The chip comes with a sine wave modulation driver module and a built-in automatic gain modulation module. After stabilizing the gain, the motor enters the sine wave modulation state, which can improve the running efficiency of the fan and reduce the noise.

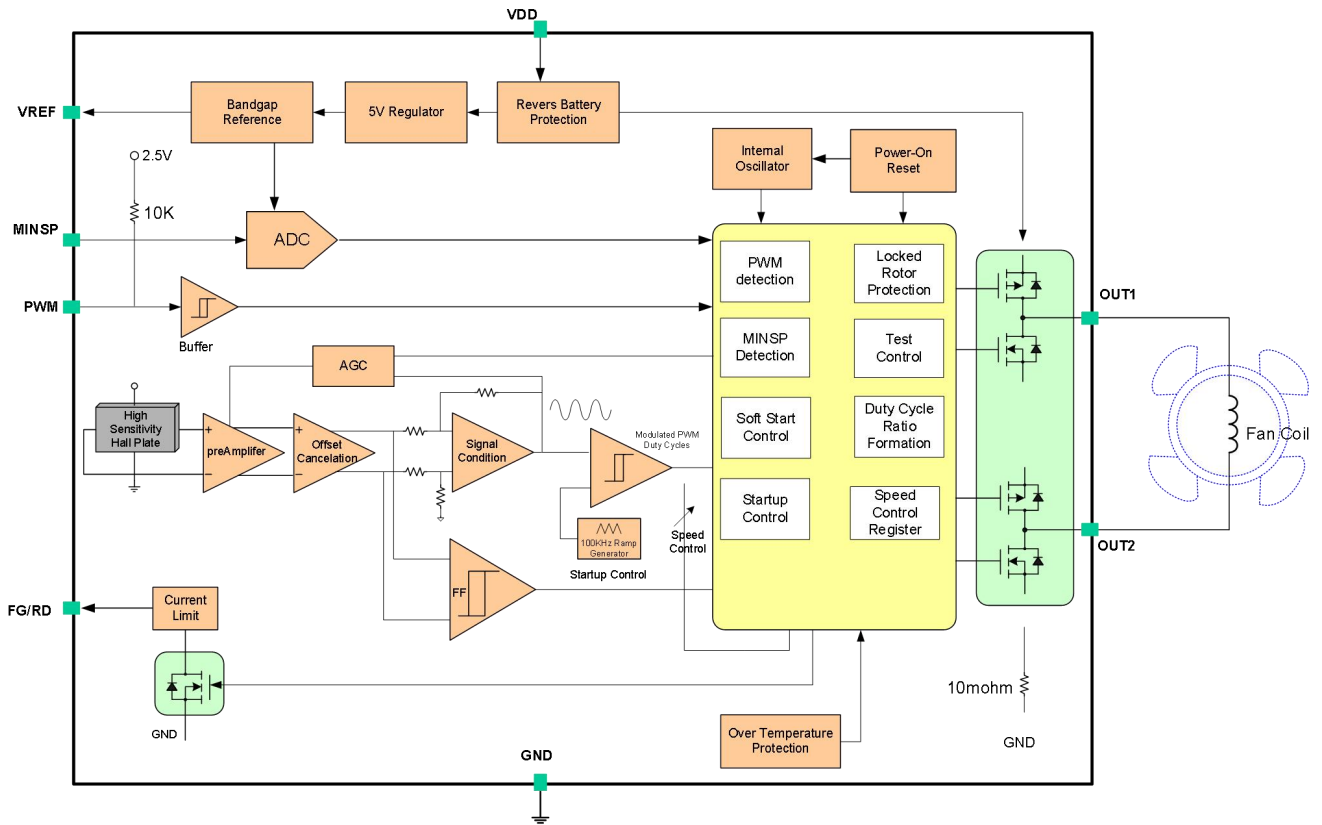
In terms of speed control, the motor supports PWM modulation, minimum speed configuration, speed profile configuration and direction of rotation control to meet different speed profile requirements.

Support FG/RD function, external pull-up resistor feedback fan operation status and speed information.

The chip has built-in overheating protection and blocking protection to prevent the motor from burning out under accidental conditions such as blocking or short-circuiting.

CC6420 is available in two packages, which are SOP8 and DFN8-3x3. Comply with RoHS requirements.

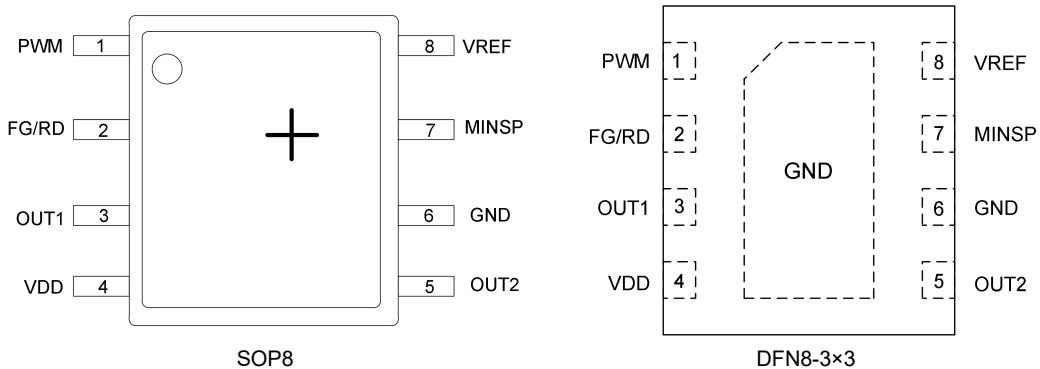
FUNCTION BLOCK DIAGRAM



ORDER INFORMATION

Part No.	Package code	Package Information
CC6420SO-FG	SOP8	tape reel, 2500 pcs/reel
CC6420SO-RD	SOP8	tape reel, 2500 pcs/reel
CC6420SPB-FG	SOP8	tape reel, 2500 pcs/reel
CC6420DN-FG	DFN8 3×3	tape reel, 3000 pcs/reel
CC6420DN-RD	DFN8 3×3	tape reel, 3000 pcs/reel

PIN DEFINITION



Name	Pin No.		Function
	SOP8	DFN8	
PWM	1	1	PWM speed control
FG/RD	2	2	Frequency generation/ Rotation Detect
OUT1	3	3	H bridge output 1
VDD	4	4	VDD
OUT2	5	5	H bridge output 2
GND	6	6	GND
MINSP	7	7	Minimal speed setting
VREF	8	8	Reference voltage
		Base	GND

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	V _{DD}	21	V
Reverse Voltage	V _{DDREV}	-28	V
Output Current (Peak)	I _{OUTP}	1000	mA
Output Current (Continuous)	I _{OUTC}	450	mA
FG/RD output voltage	V _{FG/RD}	18	V
FG/RD output current	I _{FG/RD}	30	mA
FG/RD reverse output current	I _{FG/RD}	-30	mA
PWM input voltage	V _{PWM}	7	V
Reverse PWM input voltage	V _{PWM}	-0.3	V
MINSP input voltage	V _{MINSP}	7	V
Reverse MINSP input voltage	V _{MINSP}	-0.3	V
Operating Temperature Range	T _A	-40~125	°C
thermal resistance	R _{thja} (SOP8)	150	°C/W
	R _{thja} (DFN8 3×3)	60	
Junction Temperature	T _J	150	°C
Storage Temperature	T _S	-55~150	°C
Magnetic Flux Density	B	Unlimited	mT
ESD Protection	HBM	6	kV

Note: Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum rated conditions for extended periods may degrade device reliability.

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V _{DD}	3.5	18	V
Operating Ambient Temperature	T _A	-40	125	°C
Continuous Output Current	I _{OUTC}	-	400	mA

ELECTRICAL PARAMETERS ($V_{DD}=4.5V$ to $18V$ @ $25^{\circ}C$, unless specified otherwise)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	3.5	-	20	V
Supply current	I_{DD}	$V_{DD}=12V$	-	6	8	mA
Reverse current	I_{DDREV}	$V_{DD}=-20V$	-	-	1	mA
PWM input low voltage	V_{IL}		-	-	0.4	V
PWM input high voltage	V_{IH}		2.1	-	5.5	V
PWM input frequency	F_{IN}		0.1	-	100	kHz
PWM internal pull-up resistor	R_{IN}		-	10	-	k Ω
H bridge on resistance	R_{DSON}	$T=25^{\circ}C, V_{DD}=12V, I_{OUT}=450mA$	-	2.0	-	Ω
H bridge on resistance	R_{DSON}	$T=25^{\circ}C, V_{DD}=4.5V, I_{OUT}=300mA$	-	2.0	-	Ω
Soft start duty cycle range	DCout_ss		25	-	100	%
Soft start time	T_{SOFT}		-	3	-	s
FG/RD output saturation voltage	V_{OL}	$B > B_{OP}, I_{OUT}=5mA$	-	0.2	0.5	V
FG/RD output current limit	I_{CL}	$B > B_{OP}$	-	30	-	mA
FG/RD output leakage current	I_{OFF}	$V_{OUT}=16V, V_{DD}=12V, B < B_{RP}$	-	0.1	2	μA
Reference output voltage	V_{REF}		2.45	2.5	2.55	V
Reference output current capability	I_{REF}		-	-	5	mA
Locked rotor protection ON time	T_{ON}		-	1.5	-	s
Locked rotor protection OFF time	T_{OFF}		-	4.0	-	s
Over temperature protection	T_{SD}	$V_{IN}=18V$	-	160	-	$^{\circ}C$
Over temperature protection hysteresis	ΔT_{SD}		-	30	-	$^{\circ}C$

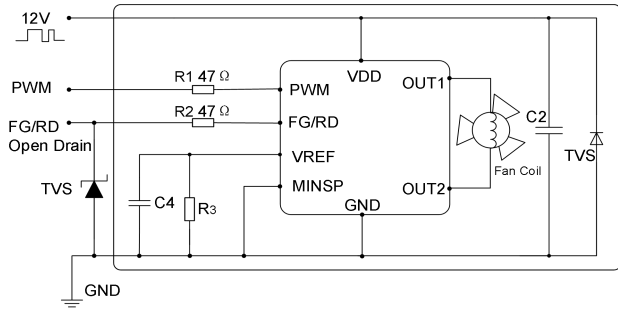
MAGNETIC SPECIFICATIONS

Parameter		Symbol	Min.	Typ.	Max.	Unit
Start up	operating point	B_{OP}	5	20	40	Gauss
	Release point	B_{RP}	-40	-20	-5	Gauss
	hysteresis	B_{HYS}	10	40	80	Gauss
Sine wave current mode	operating point	B_{OP}	-	5	-	Gauss
	Release point	B_{RP}	-	-5	-	Gauss
	hysteresis	B_{HYS}	-	10	-	Gauss

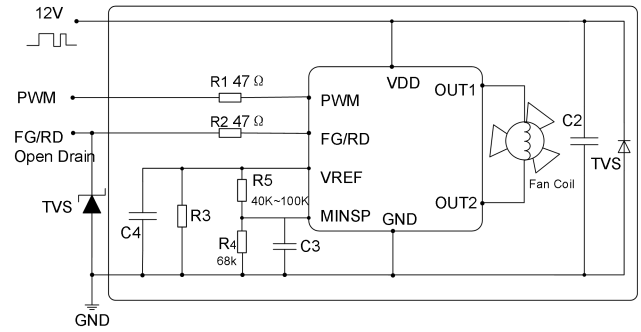
DRIVER OUTPUT VS. MAGNETIC POLE

Parameter	Test Condition	OUT1	OUT2	FG
North pole	$B < B_{RP}$	High	Low	High
South pole	$B > B_{OP}$	Low	High	Low

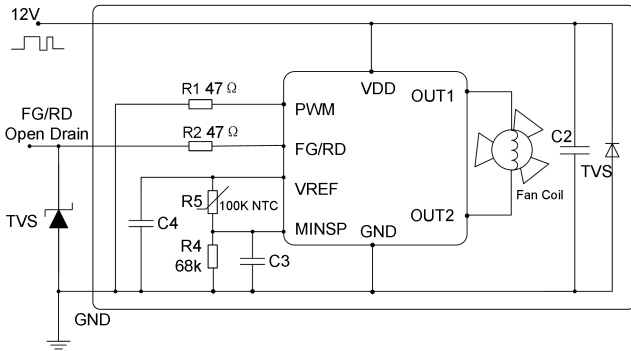
TYPICAL APPLICATION CIRCUIT



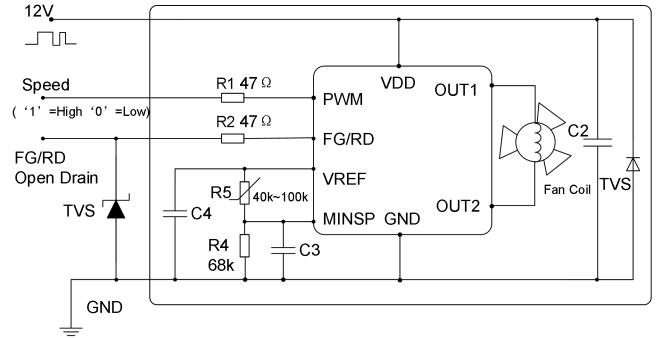
4-wire PWM Cooling Fan (no minimal speed setting)



4-wire PWM Cooling Fan (with minimal speed setting)



Temperature Controlled Cooling Fan



2-Speed Cooling Fan

APPLICATION INFORMATION

PWM Pin

The resistance R1 should not be too large or too small, R1 will help to filter out the spike burr on PWM signal. If the resistance is too small, the effect is not good, the resistance should not be too large. When the fan external wire is too long, RC filtering will be formed with the distributed capacitance. When the PWM frequency is high, the duty cycle and amplitude of the signal will be distorted, resulting in the fan speed inconsistent with the preset duty cycle. In case of this situation, please use oscilloscope to monitor the waveform on PWM pin. The waveform should be clean without signal distortion.

The PWM input features a built-in pull-up resistor of 10Kohm, and the external input signal can be open drain signal or digital signal (VIL range is 0-0.4V, VIH range is 2.1-5.5V). When the peak value of the input signal exceeds 5.5V, the method of resistance voltage attenuation must be used to control the signal amplitude within 5.5V.

FG/RD Pin

The 2 Pin of CC6420 can be selected as FG / RD signal according to the demand, which is open leakage output. Its limit withstand voltage is 21V, and the limit output current is 30mA. The 2 Pin cannot directly drive the circuit with external voltage higher than 21V or control the power circuit with current greater than 30mA. Since the FG/RD pin is directly output to external, it is recommended that the pin be connected with a certain resistance before output. When the external abnormality occurs, it will protect the chip and reduce the damage events.

When external voltage signal is needed, appropriate resistance can be connected between VDD and FG / RD.

Special application scenario: Fan needs minimum rotational speed, and it should be able to shut down completely, and FG/RD signal is output to external.

Add PMOS or PNP triode on VDD to control VDD turn off. Do not use NPN / NMOS to turn off GND ground wire of fan.

There is a circuit inside the chip. When GND circuit is turned off, the current loop will be formed from VDD -> FG / RD.

VDD & GND Pin

VDD and GND are the power pins of the chip. When the H-bridge

is disconnected, the reverse voltage on the coil inductance will also be fed into the pin.

Do not connect any components in GND circuit in series, such as 0 Ω resistor, magnetic bead, etc.

Benefit from the characteristics of SVPWM sine wave, the chip will achieve Zero Current Switch (ZCS) and Zero magnet Switch (ZBS), and the burst voltage will be relatively small. In each SVPWM modulation, when H-bridge disconnects, the current on the coil inductor cannot change suddenly, a certain surge voltage will still be generated. Please add appropriate capacitance to the VDD Pin and GND Pin according to the total coil current. Generally speaking, the greater the current, the greater the capacitance value. The 2.2-4.7uF ceramic capacitor can absorb the surge voltage.

When the Fan has the following bad conditions, it is necessary to consider whether the chip power supply is subject to high-frequency interference:

1. When the working voltage is relatively low, the chip enters the square wave working state (the output pin keeps the high-level, the output is not the PWM wave).
2. One FG signal is lost for every 15 signals (which may cause the detected value of the rotational speed is lower than the actual rotational speed of the fan in the application of the terminal customer).
3. There are a lot of burr on the edge of FG signal output (Resulting the detected value of rotational speed is higher than the actual rotational speed in the application of terminal customers).

In general, a small capacitance high frequency decoupling capacitor is directly connected to the VDD Pin and GND Pin to filter out the high frequency interference in the power supply, which can effectively solve the above undesirable phenomenon. The capacitor is usually 0.1 uF ceramic capacitor. In PCB layout and wiring, the high-frequency decoupling capacitor should be placed as close to the chip as possible, and using the shortest and thickest copper foil connects the capacitor to the VDD Pin and GND Pin.

In most cases, CC6420 chip has good anti-interference ability, even if there is no high-frequency decoupling capacitor, it also can normal working. Whether the capacitor is paralleled needs to

APPLICATION INFORMATION

be determined by the prototype measurement.

According to experience, when the working voltage of the chip is lower than 6V, the chip is vulnerable to medium and high frequency interference of the power supply, which may lead to the above adverse conditions. Therefore, it is recommended that the capacitor position should be reserved in PCB design to facilitate the subsequent debugging of fan.

OUT1 & OUT2 Pin

The OUT1 Pin and OUT2 Pin are connected to both ends of the coil L1 & L2, the control coil will generate the correct magnetic field, and the fan can rotate continuously.

In application, the loop area of OUT1, L1 – L2 and OUT2 should be smaller, so that the electromagnetic radiation released by the fan will be reduced.

In addition, one end of the coil, such as L1 and OUT1 connected in series with a magnetic bead, can also absorb the external electromagnetic radiation energy.

VREF Pin

VREF pin is the internal reference and external output pin, and the reference voltage is the basis of signal processing in analog circuit. If VREF is pulled down to 1V, the whole chip will work abnormally.

Note: VREF must add a capacitance to the ground, >1uF, to enhance the stability of the system loop.

Sensing point (Layout) Position

CC6420 is based on the principle of linear Hall. The chip needs to sample the current magnetic stripe strength in real time, adjust AGC gain, and output SVPWM signal corresponding to duty cycle. Therefore, the chip has the following two requirements for the position of the sensing point on the PCB (Figure 1):

1. The sensing point should be located on the straight line from the axis to the big end of the silicon steel sheet.
2. The sensing point should be placed on the projection plane of magnetic stripe as far as possible. If it is limited by structure, it should be close to the projection plane of magnetic stripe.

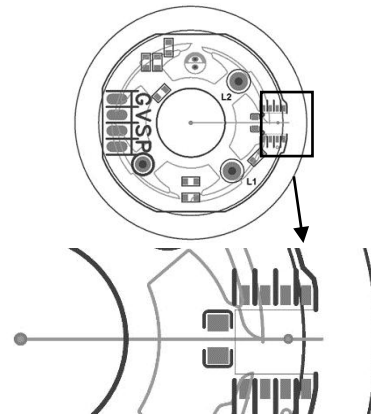


Figure 1

Sensing distance

The gap between the chip and the magnetic stripe should not be too large, and the intensity of the magnetic stripe should not be too small. Otherwise, when the internal automatic gain adjustment circuit is adjusted to the maximum gain, the maximum duty cycle of OUT1 & OUT2 cannot reach 100%. At this time, the gap between the chip and the magnetic stripe should be reduced, or the magnetic stripe with greater magnetic field strength should be replaced.

EMI

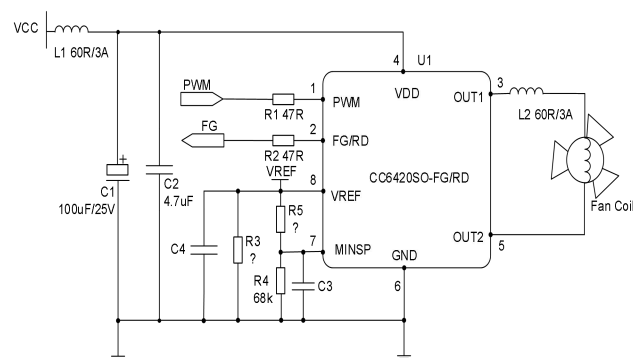


Figure 2

Note: increasing the L1 & L2 of magnetic beads is beneficial to meet the EMI radiation requirements. In order to avoid saturation of the magnetic bead current, the higher the rated current is, the better. It is recommended to 3-5 times the working current.

APPLICATION INFORMATION

Setting of speed control curve

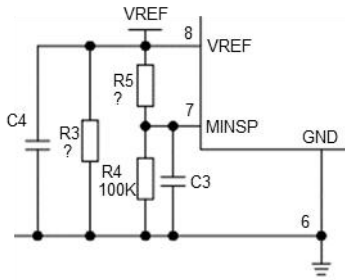


Figure 3

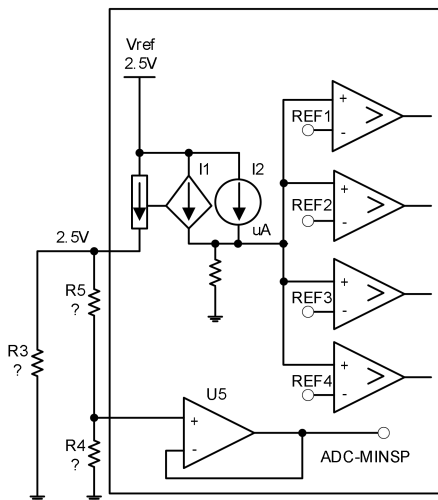


Figure 4

Fig. 3 and Fig. 4 show the block diagram of CC6420 VREF and MINSP to adjust the rotational speed curve.

1. Use only the lowest rotational speed scenario

In the scenario of only using the lowest rotational speed, R3 is suspended without welding, and the sum of resistance (R5 + R4) must be greater than 100kΩ. It is recommended to fix R4 at 100kΩ, unless R5 can be modified as appropriate when the standard resistance value cannot be selected.

CC6420 can be configured with external resistors R5 and R4. The chip determines the minimum rotational speed of the fan by sampling the voltage on the 7-pin (MINSP). The lower the voltage on the 7-pin, the smaller the minimum speed; vice versa.

When R5 is open circuit, the voltage on MINSP is 0V, and there is no function of minimum rotational speed; when R5 is short circuited, the voltage on MINSP is 2.5V, and the fan will always operate at full speed and is not controlled by

PWM signal.

The minimum rotational speed configuration accuracy is 32level, that is, the setting resolution of the minimum rotational speed is about 0%, 3%, 6% Scenarios where only the speed slope is used.

2. Use only speed slope scenarios

By setting the load resistance R3 on the VREF Pin, the output current of the reference can be changed. The current mirror source of the internal 1:1 will generate a voltage on the base resistance. This voltage will be compared with the four internal reference voltages REF1 ~ 4, and will output 4 digital signals of the slope of the speed. (Table 1)

Table 1

$R_{VREF}(k\Omega)$	$I_{REF}(\mu A)$	PWM DCin while RPM=0
$\infty \sim 14.7 k\Omega$	0~170	0%
14.7 kΩ~6.46 kΩ	170~387	10%
6.46 kΩ~3.04 kΩ	387~820	20%
3.04 kΩ~0.82 kΩ	820~3000	30%

By setting different load resistance, the rotational speed of low PWM input can be lower, which can meet the requirements of different rotational speed curves.

3. Scenarios where the minimum rotational speed and rotational speed slope are used simultaneously

The rotational speed curve in Figure 5 is an example. For a specific rotational speed curve, the requirements are as follows:

- 1) The maximum speed is 3000rpm,
- 2) When the duty cycle is 60%, the speed is required to be below 2000 rpm,
- 3) When the duty cycle is 40%, the speed is required to reach 1000 rpm.

At this time, in order to meet the requirements of condition II, we must select [curve d], set the PWM duty cycle at starting speed to 30%, and select R3 = 2.2k. However, when the duty cycle is 40%, the rotational speed is lower than 1000 rpm, and the minimum rotational speed needs to be set to 33%. R4 is fixed at 100k and R5 is about 200k.

APPLICATION INFORMATION

Note: the minimum rotational speed is only positively related to the voltage of 7-pin MINSP, not in proportion. It is often necessary to readjust the resistance value of R5 according to the actual rotational speed.

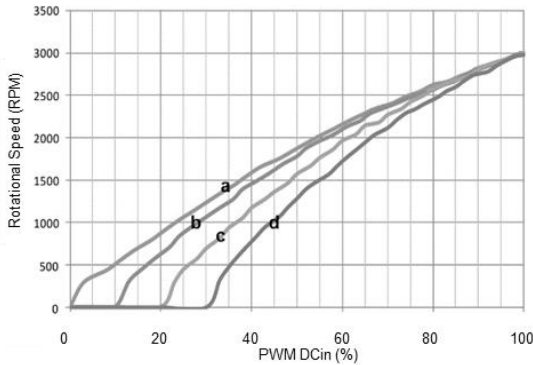


Figure 5

Analog-regulating speed

CC6420 can not only recognize digital speed regulation through PWM Pin, but also analog speed regulation through voltage on MINSP Pin. The effective voltage range is 0-2.5V. (Figure 6)

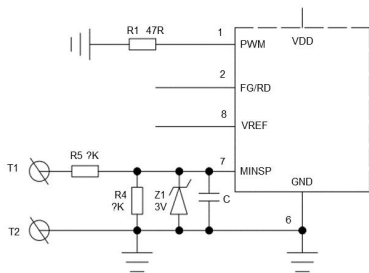


Figure 6

When PWM is forced to the ground, the fan speed is only controlled by the voltage on the 7-pin (MINSP).

When using the MINSP function, it is recommended to increase the capacitance. When the MINSP function is not used, grounding is recommended. When the speed regulating voltage range is 0 ~ 2.5V, R4 is suspended. When the voltage range of the speed regulation exceeds 2.5V, the voltage must be attenuated to the maximum voltage range that the 7-pin can bear through R5 and R4, and some design redundancy should be reserved. When the starting voltage is not 0V in the speed regulating voltage range, such as 1-5V, a suitable diode or

voltage stabilizing diode is connected in series between T1 and R5 to reduce the voltage. Then, the ratio of R5 to R4 is set, and the maximum value of partial voltage is set at 2.5V.

Start-up & Restart of Locked-rotor Characteristics

CC6420 has intelligent soft start function. Soft start can eliminate the peak current during motor starting and improve the system reliability. In the start-up state, the duty cycle of the output signal increases from 25% to 50% by 5% every 100ms. the maximum starting time is 3 s. in this stage, it is not controlled by external PWM and MINSP voltage.

During the start-up state, CC6420 detects the magnetic field strength of the environment and makes adaptive gain adjustment. When the start-up cycle is over, the rotation speed detection circuit will detect whether the fan reaches the specified speed; if the threshold is reached, it will enter the sine wave working state after the adaptive adjustment is completed. If the speed is not reached, restart again until the speed reaches the threshold to ensure the reliable start of the fan.

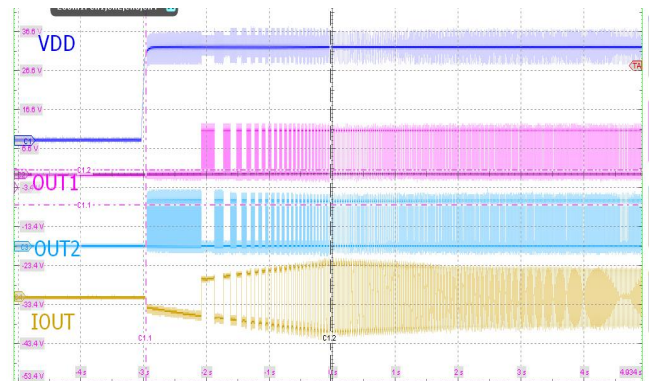


Figure 7 Output voltage & coil current wave at startup

POWER DISSIPATION & MAXIMUM OUTPUT CURRENT

The maximum heat dissipation power of the package body is determined by the following equation:

$$P_{D(MAX)} = (T_J - T_A) / R_{thja}$$

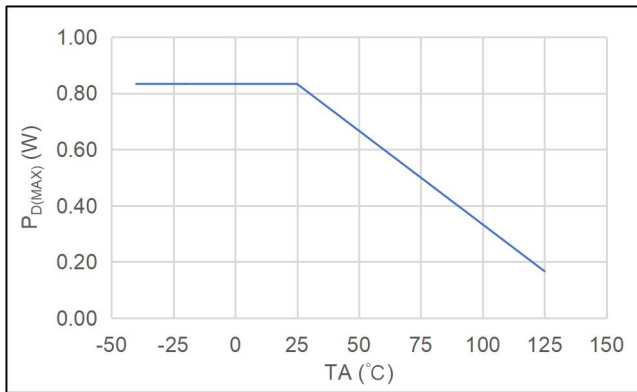
While normal operation, the power dissipated in CC6420:

$$P = I_{CONT}^2 \times R_{DSON} + V_{DD} \times I_{DD}$$

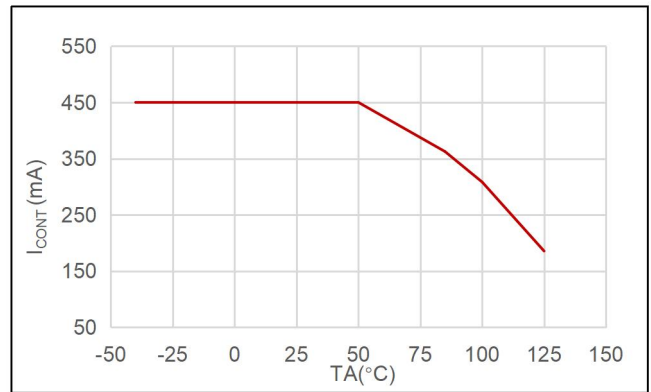
The maximum output current I_{MAX} :

$$I_{MAX} = \sqrt{(P_{D(MAX)} - V_{DD} \times I_{DD}) / R_{DSON}}$$

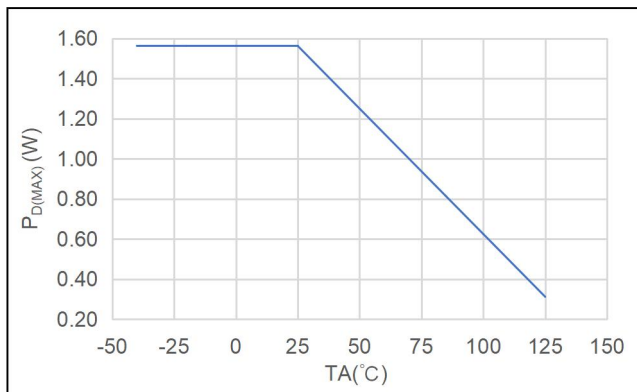
The PD curve and the output current curve:



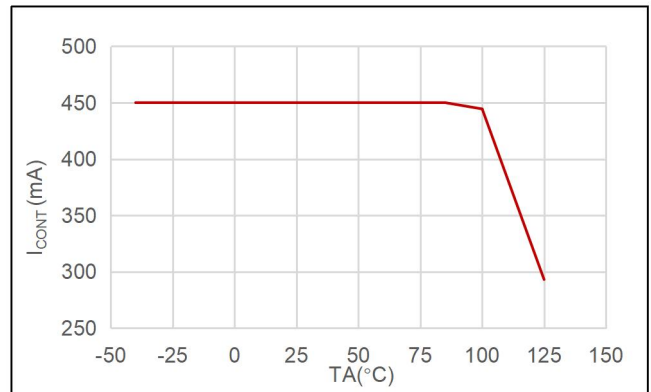
PD(MAX) vs. Temp. (SOP8)



ICONT(MAX) vs. Temp. (SOP8)

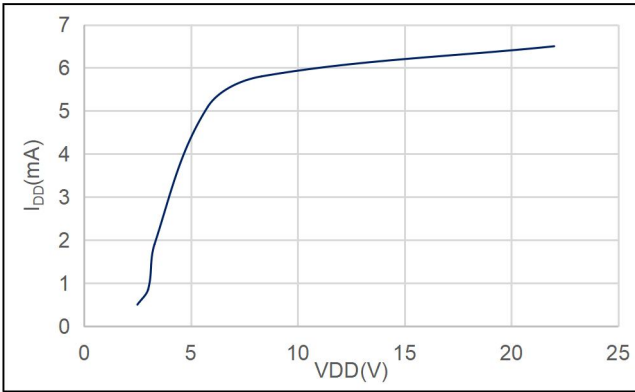


PD(MAX) vs. Temp. (DFN8)

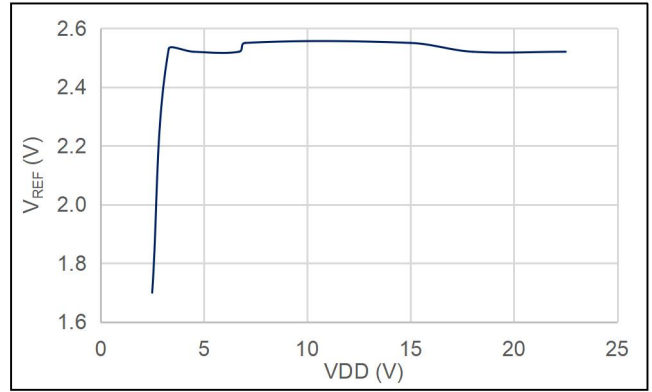


ICONT(MAX) vs. Temp. (DFN8)

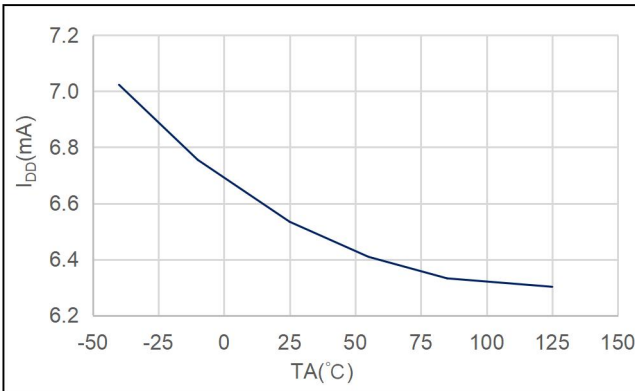
Curve & Waveform (VDD=12V @TA= 25°C, unless specified otherwise)



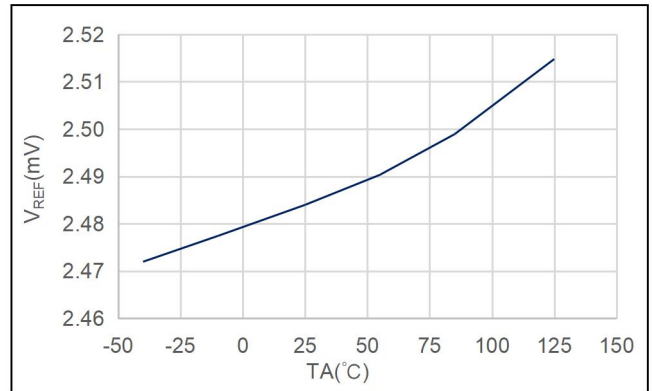
I_{DD} vs. V_{DD}



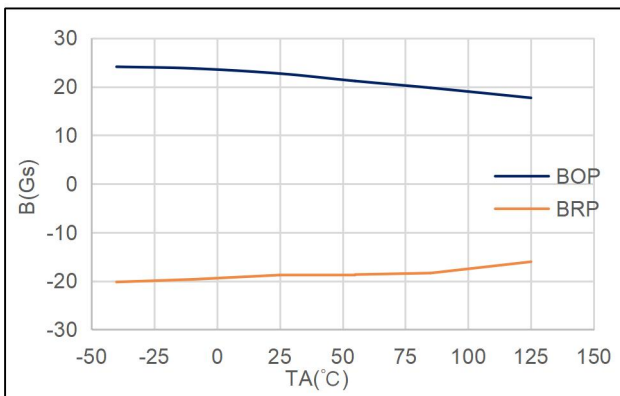
V_{REF} vs. V_{DD}



I_{DD} vs. TA

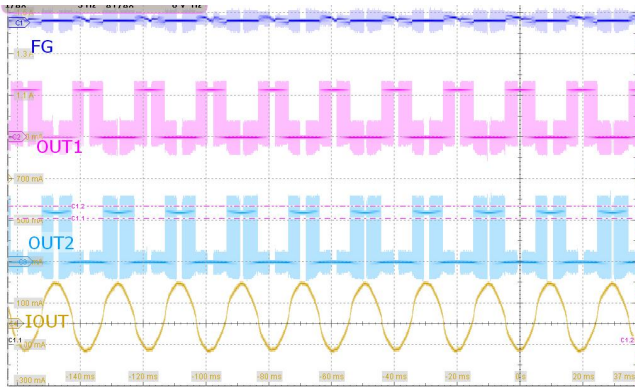


V_{REF} vs. TA

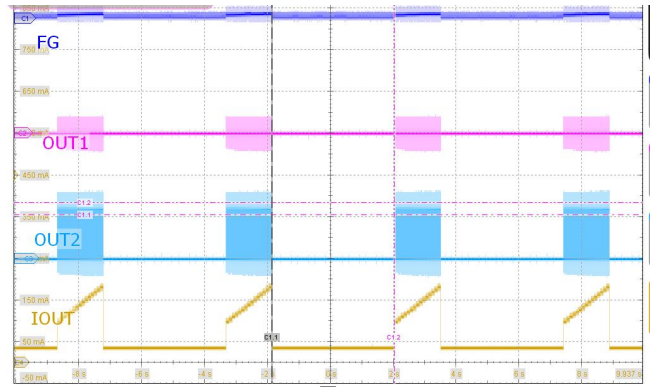


B_{OP} & B_{RP} vs. TA

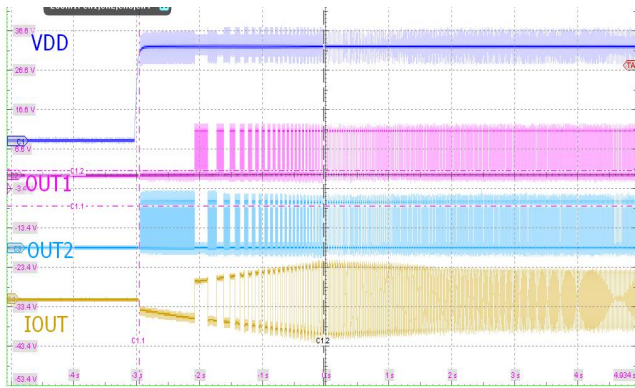
CURVE & WAVEFORM(VDD=12V @TA= 25°C, unless otherwise specified)



Steady-state waveform



Stall waveform

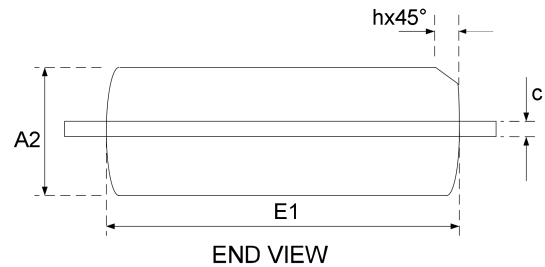
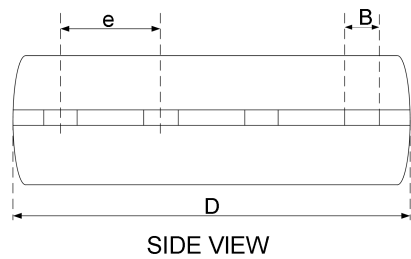
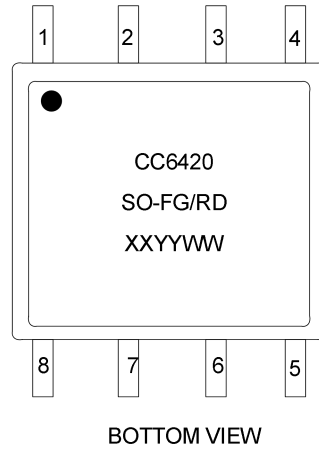
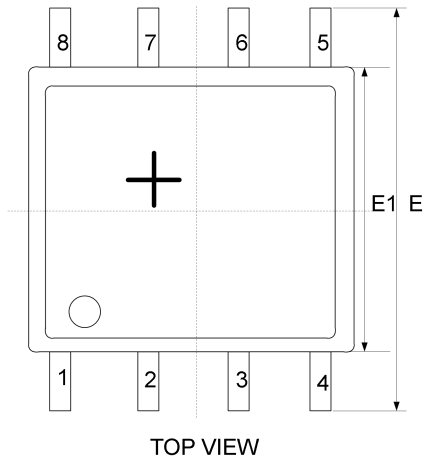


Power-on waveform

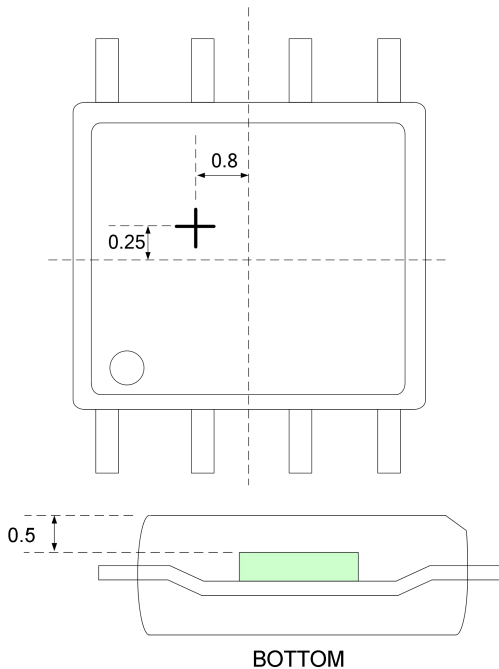
PACKAGE INFORMATION

1) SOP8

1.1) straight pin



HALL PLATE POSITION



Symbol	Dimension (millimeter)		
	Min.	Typ.	Max.
A2	1.4	-	1.6
B	0.35	0.4	0.49
c	0.20	0.25	0.30
D	4.8	4.93	5.0
E1	3.80	3.94	4.00
e	1.27BSC		
E	5.84	6.00	6.20
h	0.25	0.33	0.41

Note:

1. All dimensions are millimeters

Marking:

1'st line: CC6420 – product name

2'nd line: SO-FG/RD -- Type

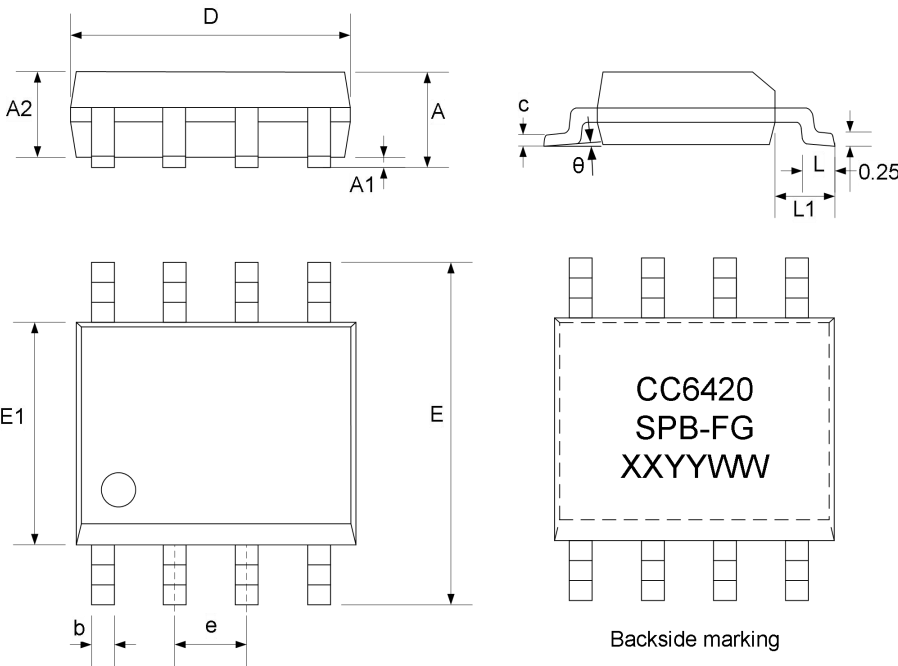
3'rd line: XXYYWW

XX – code

YY – last 2 digits of year

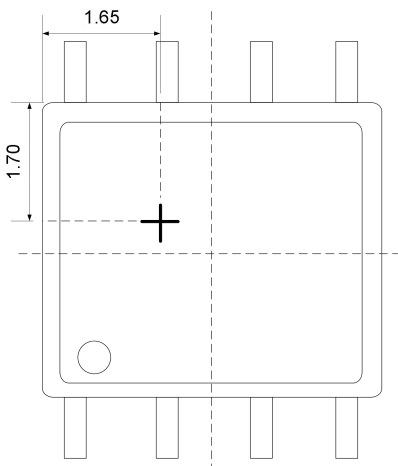
WW – Production batch number

1.2) bent pin



Symbol	Size(mm)		
	Min.	Typ.	Max.
A	1.50	-	1.70
A1	0.10	-	0.25
A2	1.30	1.40	1.50
b	0.33	0.40	0.47
c	0.20	-	0.25
D	4.70	4.90	5.10
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.55	0.60	0.75
L1	1.05(BSC)		
θ	0°	4°	8°

HALL PLATE POSITION



Note:

1. All dimensions are millimeters

Marking:

1'st line: CC6420 – product name

2'nd line: SPB-FG-- Type

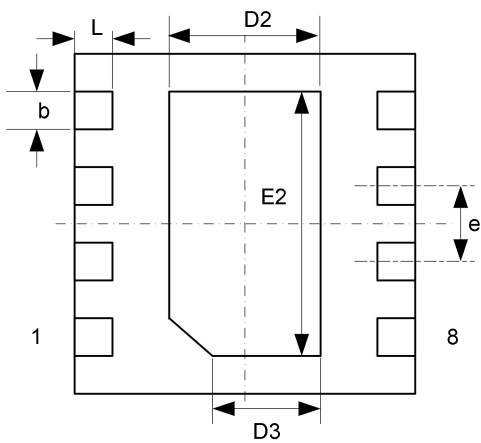
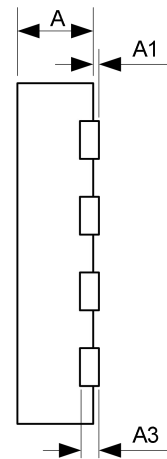
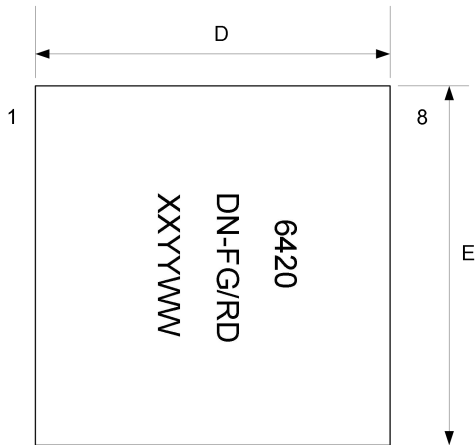
3'rd line: XXYYWW

XX – code

YY – last 2 digits of year

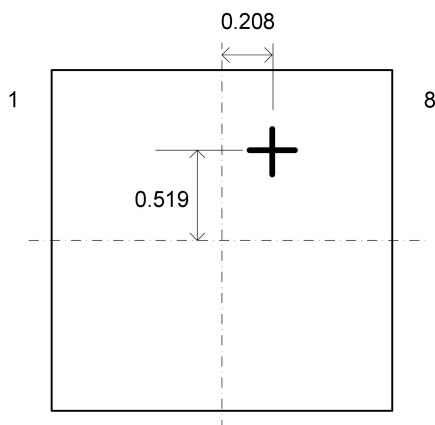
WW – Production batch number

2) DFN8 3x3



Symbol	Dimension(millimeter)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	-	-	0.05
A3	0.203 REF		
b	0.23	0.28	0.33
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
D3	-	1.15	-
E2	2.20	2.30	2.40
e	0.65 TYP		
L	0.25	0.30	0.35

HALL PLATE POSITION



Note:

1. All dimensions are millimeters.

Marking:

1'st line: CC6420 – product name

2'nd line: SO-FG/RD -- Type

3'rd line: XXYYWW

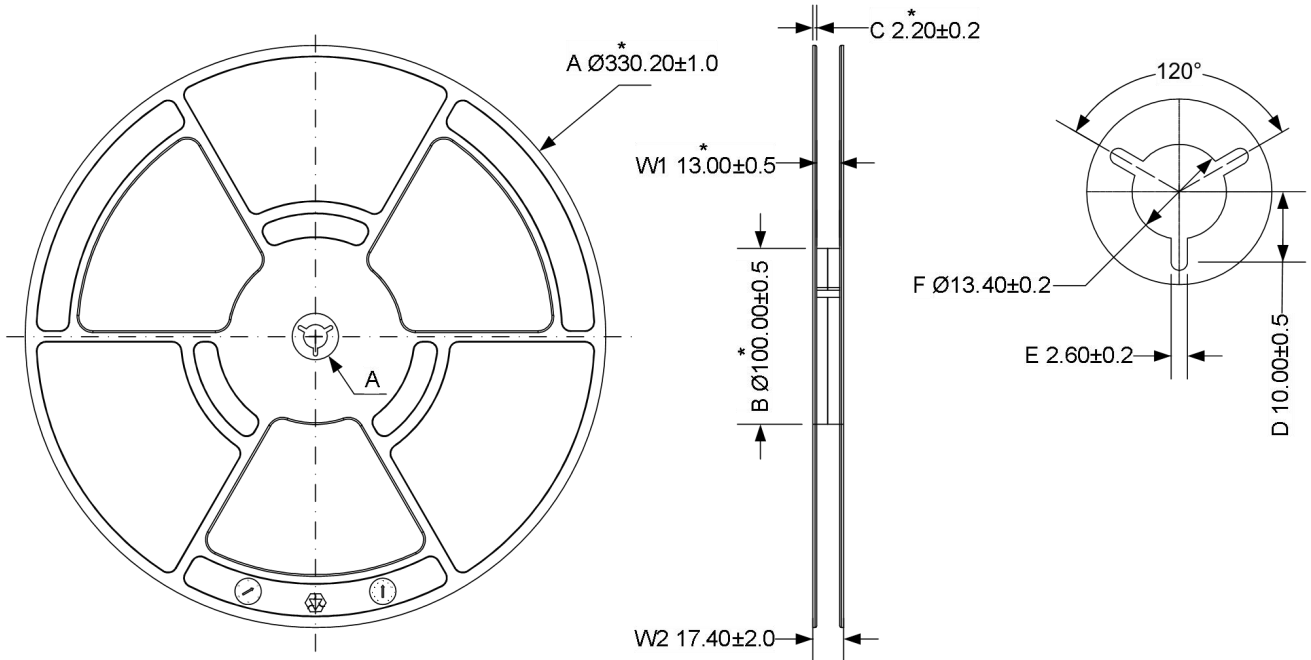
XX – code

YY – last 2 digits of year

WW – Production batch number

PACKAGING INFORMATION

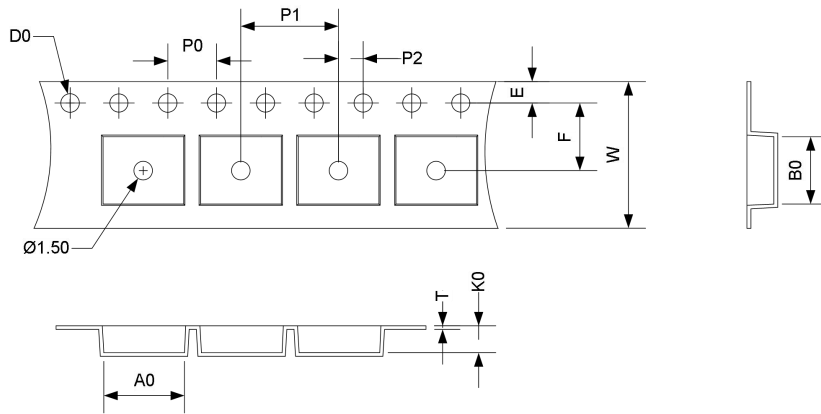
SOP8 package — Reel size



NOTE:

- (1) *Marked as a key size.
- (2) All dimensions are millimeters

SOP8 package — Carrier tape size



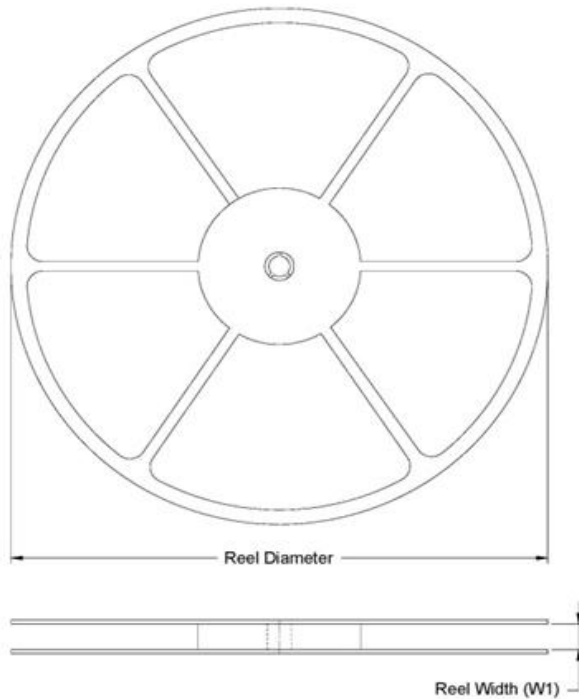
Symbol	*W	*A0	*B0	*K0	P0	P1
Size	12±0.30	6.50±0.1	5.40±0.1	2.05±0.1	4.0±0.1	8.00±0.1
Symbol	P2	F	S	E	D0	T
Size	2.0±0.1	5.5±0.1	0.0±0.1	1.75±0.1	1.5 ^{+0.1} _{-0.0}	0.3±0.05

Note: 1. *Marked as key dimensions, all dimensions are in mm;

2. The cumulative error of any 10 ratchet holes shall not exceed ±0.2mm;

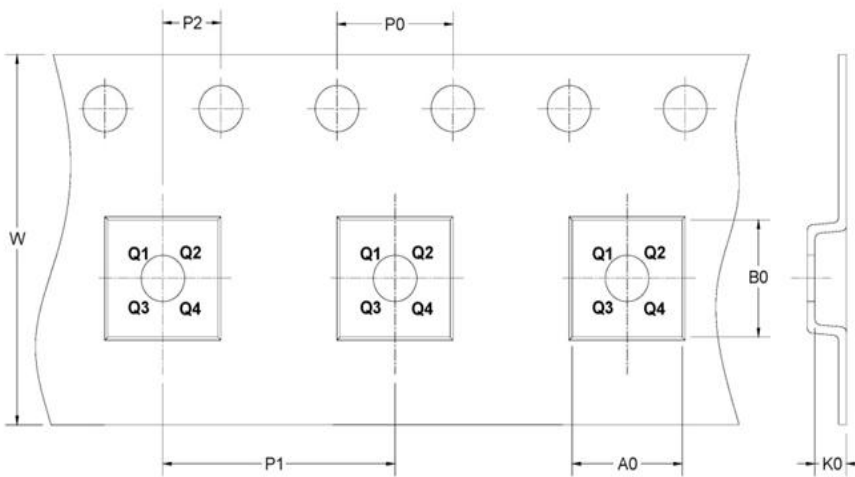
3. The non-parallelism of 250mm distance in the length direction of the carrier belt must not exceed 1mm.

DFN8 3×3 package — Reel size



Reel Width W1	Reel Diameter
12mm	178mm

DFN8 3×3 package — Carrier tape size



Note: PIN1 position in Q1

➔ DIRECTION OF FEED

Symbol	A0	B0	K0	P0	P1	P2	W
Size (mm)	3.23	3.23	1.05	4.00	4.00	2.00	12

REVISION HISTORY

Revision Date	Description of Revision	Revision
2024.04	<ol style="list-style-type: none">1. Simplify the GENERAL DESCRIPTION of the home page;2. Supplemental SOP8 Bent Pin Package Size Information;3. Supplemental reel and carrier tape size information for SOP8 packages and DFN8 3x3 packages.	rev3.2

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