Model 645H

Very Low Jitter HCSL Clock

Part Dimensions:
5.0 × 3.2 × 1.4mm • 58.1mg

Features

- High Speed Current Steering Logic [HCSL] Output
- Ceramic Surface Mount Package
- Low Phase Jitter Performance, 500fs Typical
- Fundamental or 3rd Overtone Crystal Design
- Frequency Range 13.5MHz – 160MHz *
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418

Applications

- PCI Express [PCIe]
- Data Storage Systems
- Ethernet Line Cards
- Serial ATA Express [SATAe]
- Intel Chipsets
- Network Servers
- Switches and Routers
- Set-Top Boxes/DVRs

Standard Frequencies

- 25MHz	**- 100MHz**	- 155.52MHz
- 27MHz	- 106.25MHz	- 156.25MHz
- 50MHz	- 125MHz	

* Check with factory for availability of frequencies not listed.

Description

CTS Model 645H is a low cost, high performance clock oscillator supporting HCSL output. Employing the latest IC technology, M645H has excellent stability and low phase jitter performance.

Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
645	H	XXX or XXXX	3	I	3	T

Code	Output
H	HCSL - Pin 1 Enable

Code	Stability
5	±25ppm
4	±30ppm
3	±50ppm
2	±100ppm

Code	Voltage
2	+2.5Vdc
3	+3.3Vdc

Code	Frequency
Product Frequency Code [1]	

Code	Temp. Range
C	-20°C to +70°C
I	-40°C to +85°C
G	-40°C to +105°C [2]

Code	Packing
T	1k pcs./reel

Notes:

1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.

2] Check factory for availability. Stability codes 2 and 3 only.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.3	-	4.0	V
Supply Voltage	V_{CC}	±5%	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current	I_{CC}	Maximum Load Maximum Current Value @ +3.3V	-	-	60	mA
Operating Temperature	T_A	-	-20 -40 -40	 +25 	+70 +85 +105	℃
Storage Temperature	T_{STG}	-	-50	-	+125	℃

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f_O	-		13.5 - 160		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	-		25, 30, 50 or 100		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC}	-5	±3	5	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		HCSL		-
Output Load	R_L	Terminated to ground	-	50	-	Ohms
Output Voltage Levels	V_{OH} V_{OL}	HCSL Load	-580 -150	- -	850 150	mV
Output Duty Cycle	SYM	Differential Output, @ V_{CC} - 1.3V	45	-	55	%
Differential Output Voltage	V_{OD}	R_L = 50 Ohms to ground	0.4	-	-	Vp-p
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 50 Ohms to ground	-	0.50	0.70	ns

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	T_S	Application of V_{CC}	-	5	10	ms
Enable Function [Standby]						
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	0.7V_{CC}	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.3V_{CC}	V
Disable Current	I_{IL}	Pin 1 Logic '0', Output Disabled	-	15	-	µA
Enable Time	T_{PLZ}	Pin 1 Logic '1', Output Enabled	-	-	2	ms
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	500	-	fs

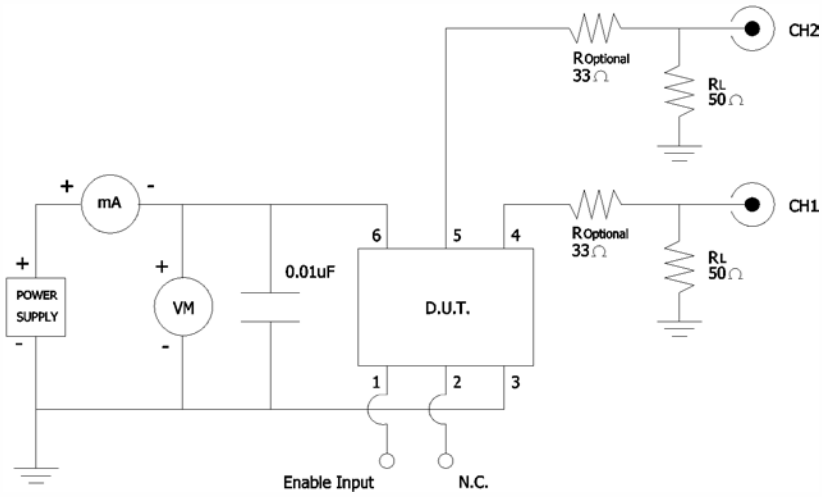
Electrical Specifications

Enable Truth Table

Pin 1	Pin 4 & Pin 5
Logic '1'	Output Enabled
Open	Output Enabled
Logic '0'	Output Disabled, High Impedance

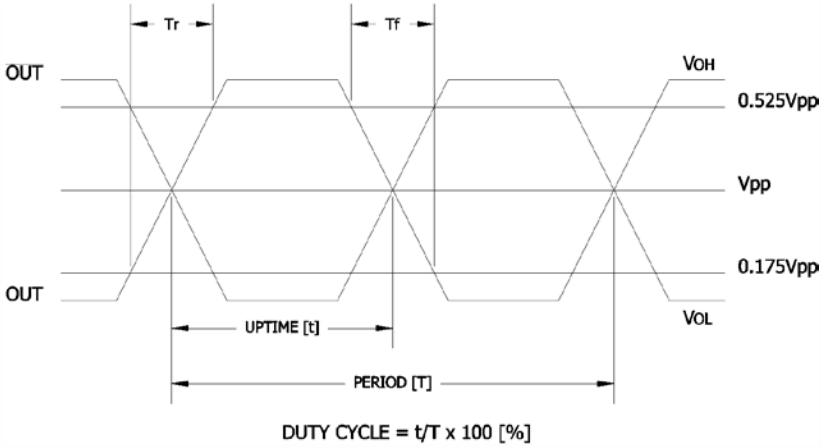
Test Circuit

HCSL



Output Waveform

HCSL

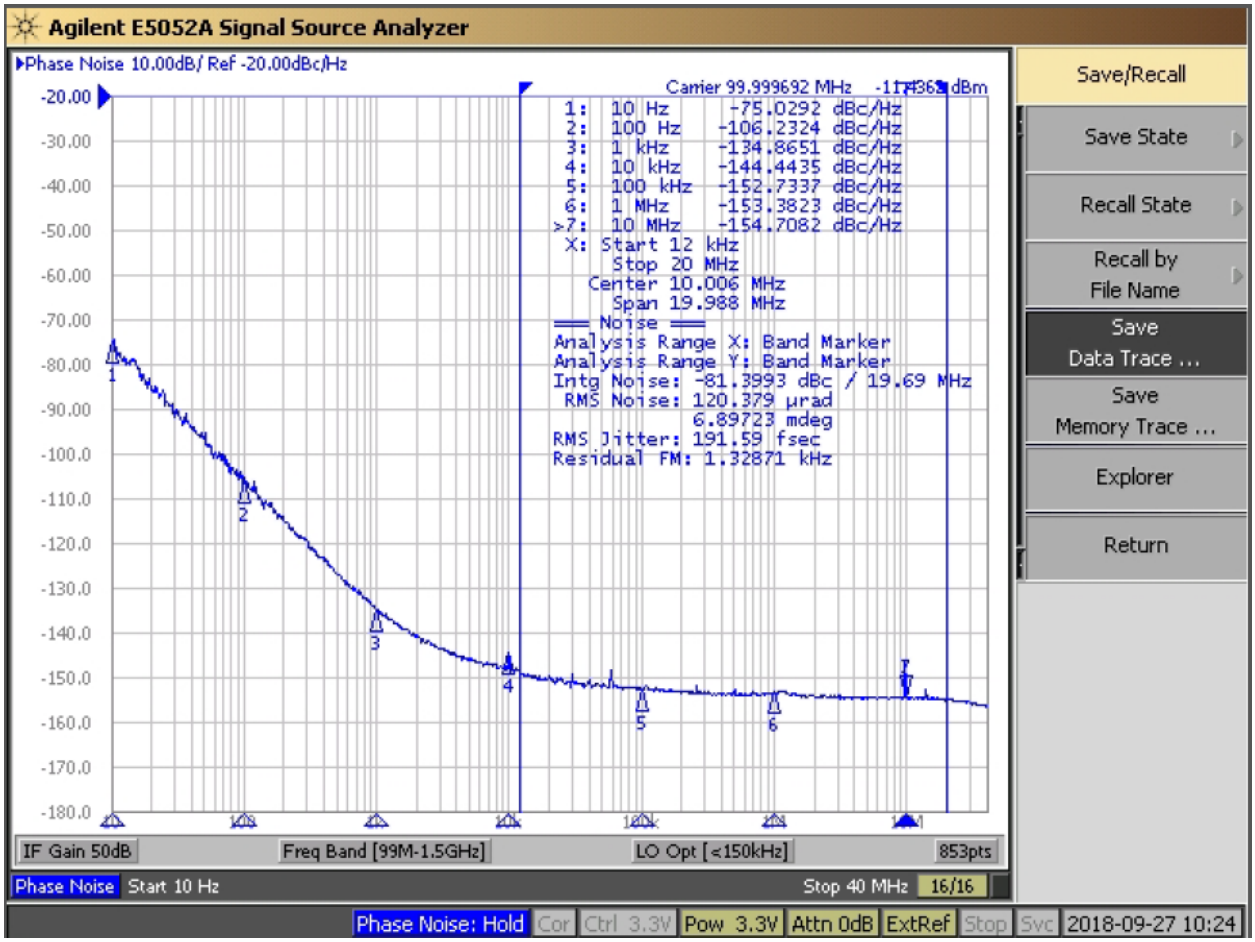


Electrical Specifications

Performance Data

Phase Noise [typical]

100.00MHz, HCSL, V_{CC} = 3.3V, T_A = +25°C



Electrical Specifications

Performance Data

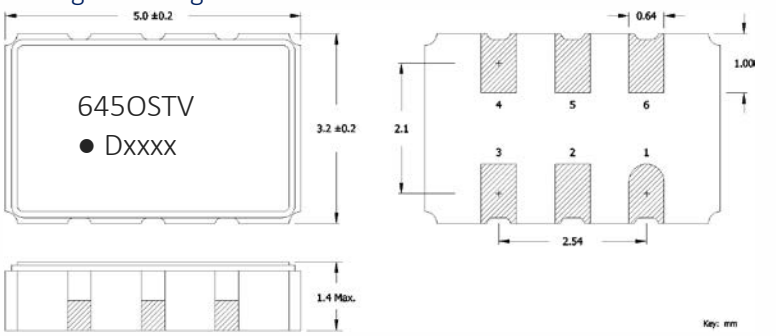
Phase Noise Tabulated

Typical, 100.00MHz, HCSL, V_{CC} = 3.3V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
HCSL @ 100.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-75.9328	
		@ 100Hz	-106.9929	
		@ 1kHz	-135.1951	dBc/Hz
	-	@ 10kHz	-144.2209	
		@ 100kHz	-152.8159	
		@ 1MHz	-153.5793	
		@ 10MHz	-154.8219	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	188.2315	fs

Mechanical Specifications

Package Drawing

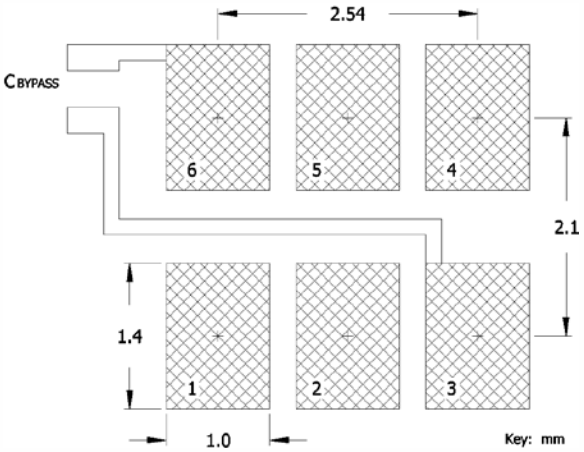


Marking Information

1. O – Output Type; H = HCSL.
2. ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
3. V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
4. D – Date Code. See Table I for codes.
5. xxxx – Frequency Code.
   3-digits, frequencies below 100MHz
   4-digits, frequencies 100MHz or greater

[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

Pin Assignments

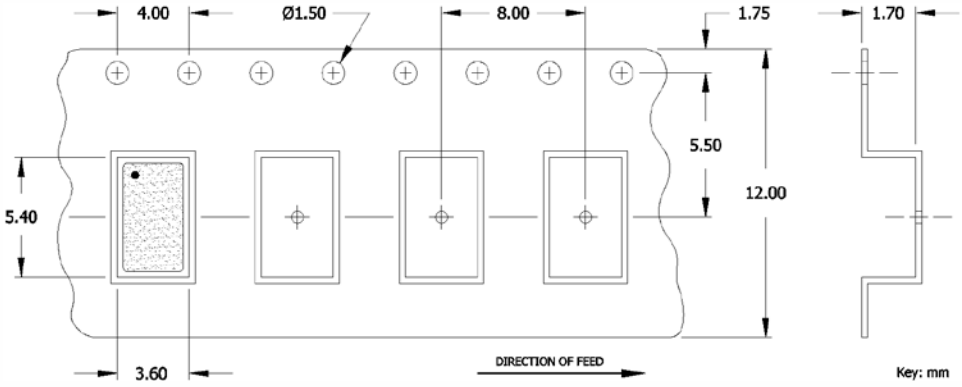
Pin	Symbol	Function
1	EOH	Enable
2	N.C.	No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	$\overline{\text{Output}}$	Complimentary RF Output
6	V_{CC}	Supply Voltage

Table I - Date Code

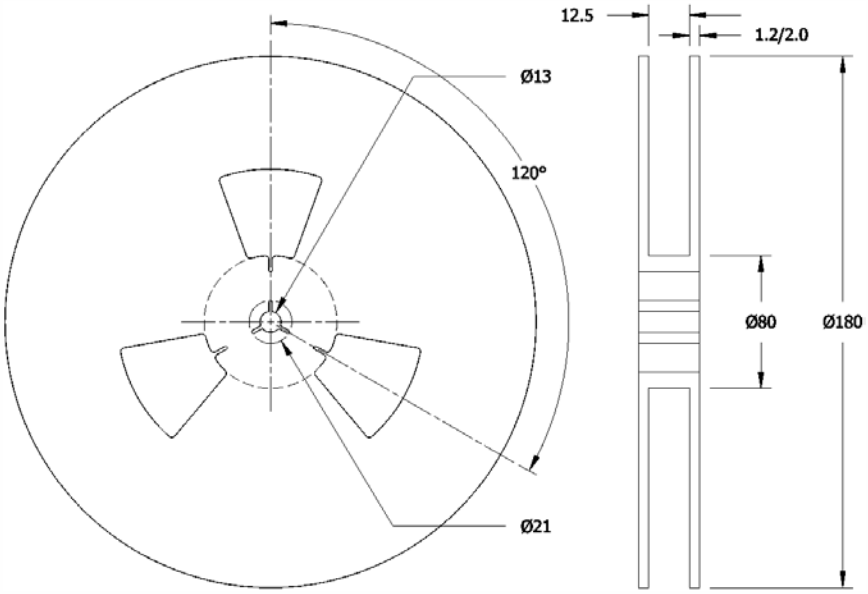
YEAR \ MONTH	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001 2005 2009 2013 2017	A	B	C	D	E	F	G	H	J	K	L	M
2002 2006 2010 2014 2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003 2007 2011 2015 2019	a	b	c	d	e	f	g	h	j	k	l	m
2004 2008 2012 2016 2020	n	p	q	r	s	t	u	v	w	x	y	z

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.

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