CUI INC®

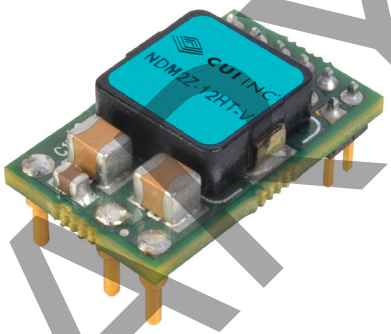
MODEL: NDM2Z-12H | **DESCRIPTION:** AUTO COMPENSATED, DIGITAL DC-DC POL CONVERTER

GENERAL CHARACTERISTICS

- 4.5~14 V input range
- 0.6~5.0 V programmable output
- voltage tracking
- voltage margining
- *Snapshot*™ parametric capture
- voltage/current/temperature monitoring
- synchronization and phase spreading
- remote differential voltage sense
- programmable soft start and soft stop
- fault management

FEATURES

- compact package
  horizontal:
  21.0 x 12.7 x 7.2 mm
  (0.827 x 0.500 x 0.284 in)
- 12 A output
- high efficiency
- auto compensation
- SMBus interface
- PMBus™ Compatible
- Ericsson footprint compatible



novum advanced power

PMBus Power Management. Defined.

RoHS

MODEL

MODEL	input voltage (Vdc)	output voltage (Vdc)	output current max (A)	output wattage max (W)
NDM2Z-12H	4.5~14	0.6~5.0	12	60

PART NUMBER KEY

NDM2Z-12H X - X X - XXX

- Base Number
- Pin Style: S = surface-mount, T = through-hole
- Pin Configuration: A = standard configuration
- Package Option: A = loose parts, B = tape and reel, C = tray
- Firmware Configuration: 000~ZZZ

Example part number: **NDM2Z-12HT-AA-002**

horizontal module
through-hole pins
standard pin configuration
loose parts package option
firmware configuration 002

CONTENTS

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

parameter	conditions/description	min	typ	max	units
V_{in}	input voltage			15	V
digital pin voltage	CTRL, DDC, SA0, SALRT, SDA, SCL, SYNC, VSET, PG	-0.3		6.5	V
analog pin voltage	+S, -S, VTRK	-0.3		6.5	V
ground voltage differential	(GND - PREF)	-0.3		0.3	V
operating temperature	T_{P1}	-40		120	°C
storage temperature		-55		125	°C

RECOMMENDED OPERATING CONDITIONS

$-30°C < T_{P1} < +95°C$, $4.5\ V < V_{in} < 14\ V$, typical measurements made at V_{in} = 12 V, V_{out} = 1.0 V, $I_{out} = I_{max}$, T_{P1} = 25°C, $=C_{in}$ = 470 µF/10 mΩ, C_{out} = 470 µF/8 mΩ

INPUT / OUTPUT

parameter	conditions/description	min	typ	max	units
V_{in}	input supply voltage	4.5		14	V
I_{out}	output current	0		12	A
V_{out}	adjustable via resistor or PMBus™ commands	0.6		5.0	V
V_{out} margin	adjustable via PMBus commands	0		110	%
voltage accuracy	over line, load and temperature measured at +S and -S	-1		1	%
line regulation	$4.5\ V \le V_{in} \le 14\ V$ V_{out} = 0.6 V V_{out} = 1.0 V V_{out} = 1.8 V V_{out} = 3.3 V		 2.4 2.2 1.7 2.8		mV
load regulation	$0\ A \le I_{out} \le I_{max}$ V_{out} = 0.6 V V_{out} = 1.0 V V_{out} = 1.8 V V_{out} = 3.3 V		 0.4 0.6 0.6 2.6		mV
voltage set-point resolution	when V_{out} set via PMBus commands	-0.025		0.025	% FS
voltage ripple and noise	V_{out} = 0.6 V V_{out} = 1.0 V V_{out} = 1.8 V V_{out} = 3.3 V		12 18 21 21		mVp-p
ramp-up time	adjustable via PMBus	0		200	ms
on time delay	adjustable via PMBus	5		500,000	ms
load transient voltage deviation	I_{out}: 25%→75%→25% of I_{max}, dI/dt=2 A/µs V_{out} = 0.6 V V_{out} = 1.0 V V_{out} = 1.8 V V_{out} = 3.3 V		 56 77 102 160		mV
load transient recovery time[1]	I_{out}: 25%→75%→25% of I_{max}, dI/dt=2 A/µs V_{out} = 0.6 V V_{out} = 1.0 V V_{out} = 1.8 V V_{out} = 3.3 V		 TBD 20 0 0		µs

Notes: 1. settling to within 3% of V_{out}

PRELIMINARY

POWER / EFFICIENCY

parameter	conditions/description		min	typ	max	units
output power	V_{out} = 5.0 V + 10% margin		0		66	W
efficiency	I_{out} = 50% of max	V_{out} = 0.6 V		85.3		%
		V_{out} = 1.0 V		89.8		
		V_{out} = 1.8 V		92.7		
		V_{out} = 3.3 V		94.2		
	I_{out} = max	V_{out} = 0.6 V		81.1		%
		V_{out} = 1.0 V		86.6		
		V_{out} = 1.8 V		90.9		
		V_{out} = 3.3 V		93.3		
idle power	V_{out} = 0.6 V			0.45		W
	V_{out} = 1.0 V			0.58		
	V_{out} = 1.8 V			0.94		
	V_{out} = 3.3 V			1.78		
	CTRL deasserted			0.13		
switching frequency				320		kHz

FAULT PROTECTION

parameter	conditions/description	min	typ	max	units
output over voltage protection	(OVP) adjustable via PMBus commands			5.6	V
output over current protection	(OCP) adjustable via PMBus commands			TBD	A
input under voltage protection	adjustable via PMBus commands		4.5		V
input over voltage protection	adjustable via PMBus commands		14		V
over temperature protection	(OTP) measured on the module		125		°C
thermal protection hysteresis	difference between temperature fault and warning		15		°C

POWER CONNECTIONS

symbol	pin	IO type	description
VIN	1A	Power	Input voltage
GND	2A	Ground	Power ground
VOUT	3A	Power	Output voltage

COMMUNICATION CONNECTIONS

symbol	pin	IO type	description
VTRK/PG	4A	Analog/Digital	Voltage tracking input or power good output
PREF	4B	Ground	Pin-strap ground
+S	5A	Analog	Output voltage positive sense input
-S	5B	Analog	Output voltage negative sense input
SA0	6A	Digital	SMBus address pinstrap
DDC	6B	Digital	Digital-DC Communications bus (equivalent to Ericsson Power GCB)
SCL	7A	Digital	SBMBus clock
SDA	7B	Digital	SMBus data
VSET	8A	Digital	Output voltage pin-strap
SYNC	8B	Digital	Synchronization I/O
SALRT	9A	Digital	SMBus alert
CTRL	9B	Digital	Remote control or enable pin

PRELIMINARY

LOGIC INPUT/OUTPUT CHARACTERISTICS

parameter	conditions/description	min	typ	max	units
input high voltage (V_{IH})	CTRL, DDC, SA0, SCL, SDA, SYNC, VSET	2			V
input low voltage (V_{IL})	CTRL, DDC, SA0, SCL, SDA, SYNC, VSET			0.8	V
output high voltage (V_{OH})	DDC, SALRT, SDA, SYNC, PG	2.25			V
output low voltage (V_{OL})	DDC, SALRT, SDA, SYNC, PG			0.4	V

OUTPUT DECOUPLING CAPACITOR RECOMMENDATION

parameter	conditions/description	min	typ	max	units
C_{OUT}	total output capacitance located on host board	300		15,000	µF

DDC CONFIGURATION REQUIREMENTS

A pull-up resistor is required on the DDC in order to guarantee the rise time as follows:
Rise $Time_{DDC}$ = R_{DDC} * C_{DDC} < 1 µs

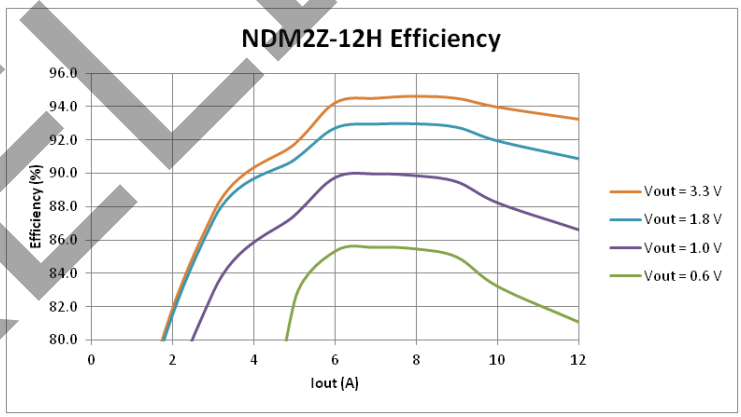
R_{DDC} is the DDC pull-up resistor and C_{DDC} is the DDC capacitive loading. The pull-up resistor should be tied to an external 3.3V or 5V supply. The designer needs to ensure that the resistor pull-up voltage is present during module power-up. Each module connected to the DDC presents ~10 pF, each inch of FR4 PCB trace introduces ~2 pF of capacitive loading.

SMBUS CONFIGURATION REQUIREMENTS

The complete specifications for the SMBus can be found on the following web pages: www.pmbus.info , smbus.org

TYPICAL CHARACTERISTICS

Conditions [applies to all graphs unless stated otherwise]: T_{P1} = 25°C, V_{in} = 12 V, C_{in} = 470 µF/10 mΩ, C_{out} = 470 µF/8 mΩ, I_{out} = Imax



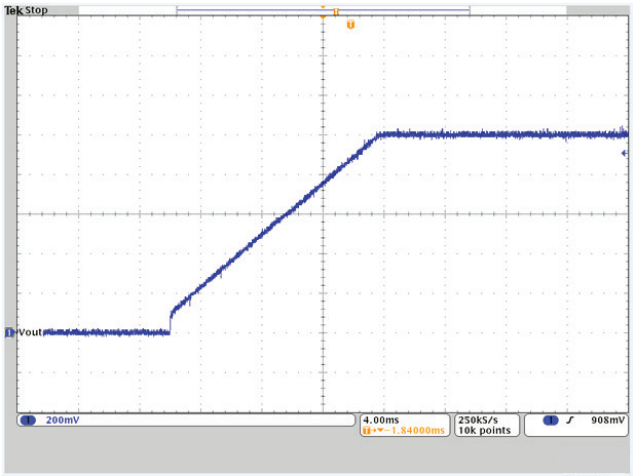
PRELIMINARY

TYPICAL CHARACTERISTICS (CONTINUED)

Conditions (applies to all graphs unless stated otherwise): T_{P1} = 25°C, V_{in} = 12 V, C_{in} = 470 µF/10 mΩ, C_{out} = 470 µF/8 mΩ, I_{out} = Imax

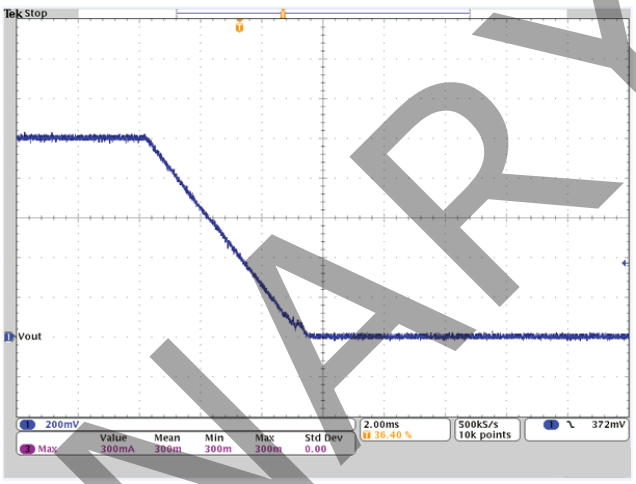
Start-up

(V_{out} = 1.0 V)



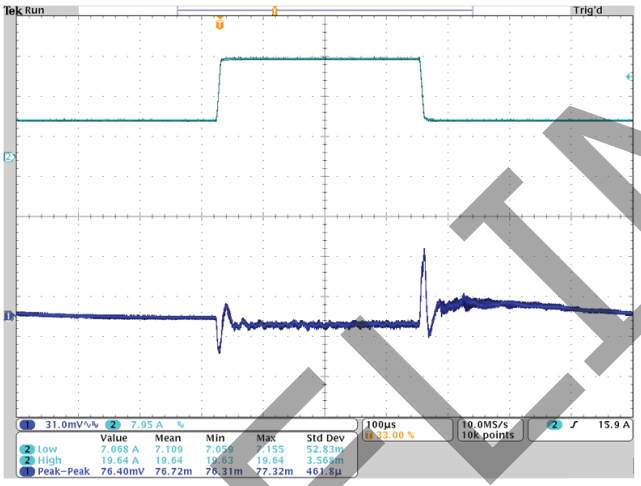
Shut-down

(V_{out} = 1.0 V)



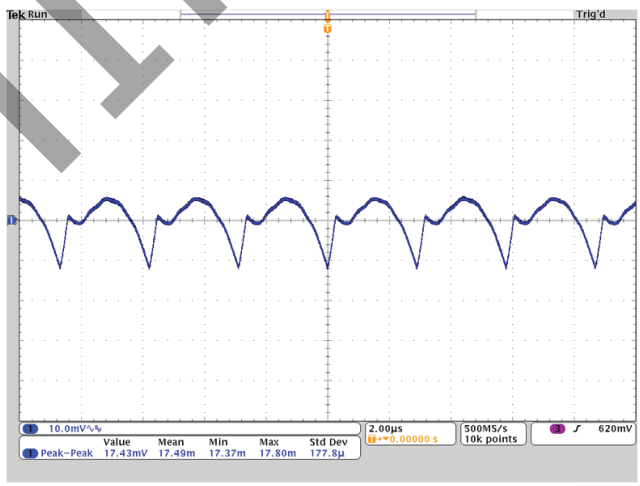
Output Load Transient Response

(V_{out} = 1.0 V, I_{out} = 3.0 ➞ 9.0 ➞ 3.0 A, 2 A/µs)



Output Ripple and Noise

(V_{out} = 1.0 V)

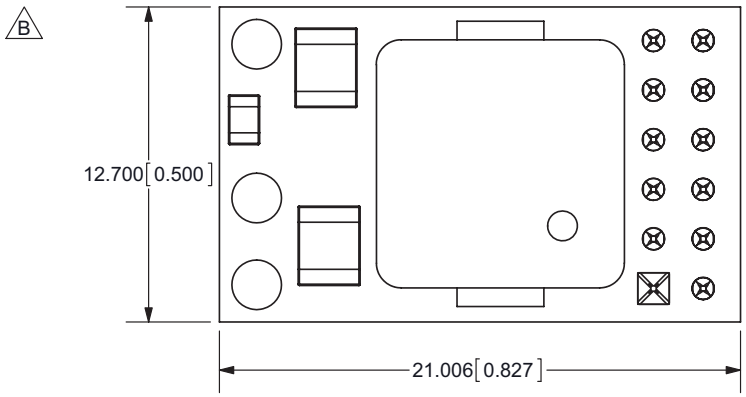


PRELIMINARY

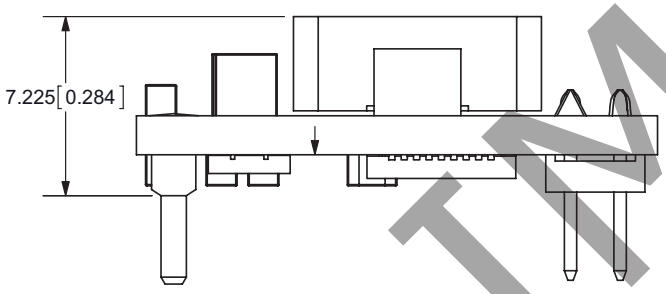
MECHANICAL DRAWING

THROUGH-HOLE

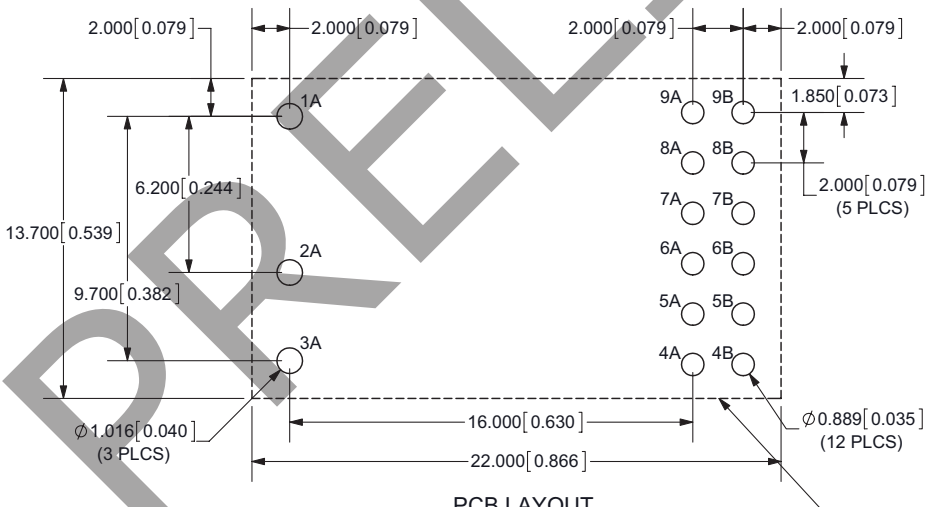
units: mm [inches]
tolerance unless specified:
X.X ±0.50 [0.02]
X.XX ±0.25 [0.01]
(not applied on footprint or typical values)



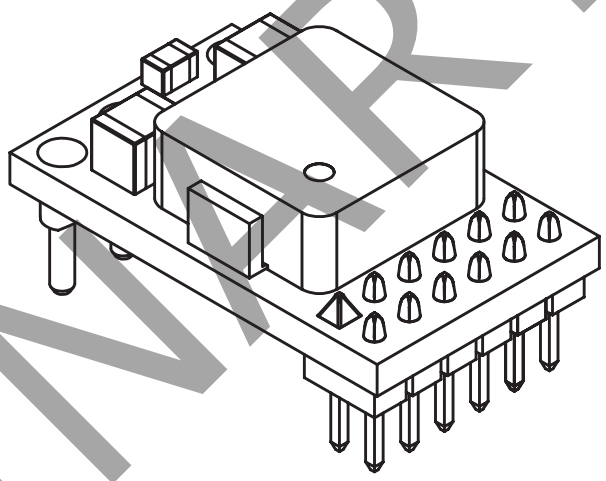
TOP VIEW



FRONT VIEW



PCB LAYOUT
TOP VIEW
Recommended keep out area for user components



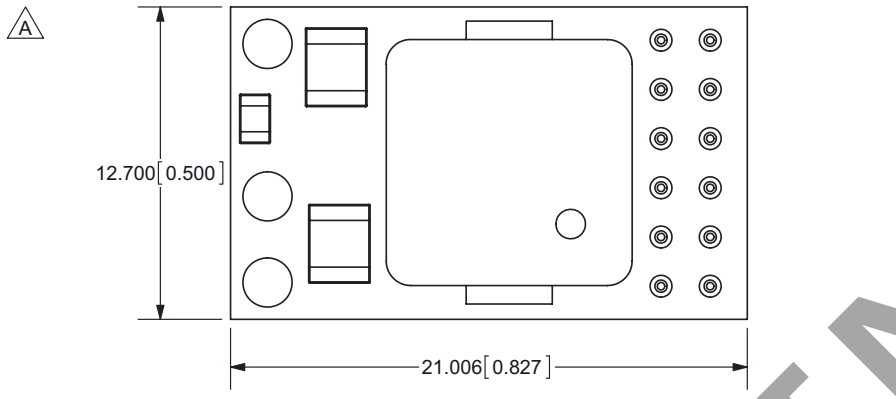
PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A	VIN	Copper Alloy	Au 0.25 µm over Ni 2.5 µm
2A	GND		
3A	VOUT		
4A	VTRK/PG		Au 0.76 µm
4B	PREF		
5A	+S		
5B	-S		
6A	SA0		
6B	DDC		
7A	SCL		
7B	SDA		
8A	VSET		
8B	SYNC		
9A	SALRT		
9B	CTRL		

PRELIMINARY

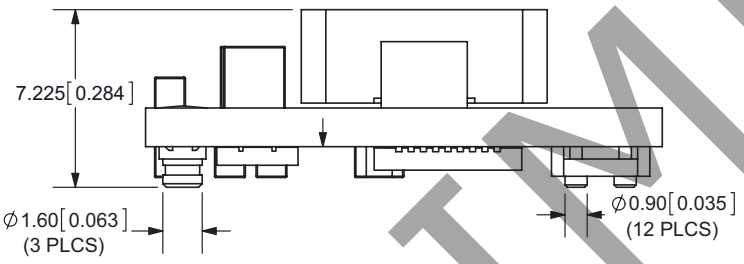
MECHANICAL DRAWING (CONTINUED)

SURFACE MOUNT

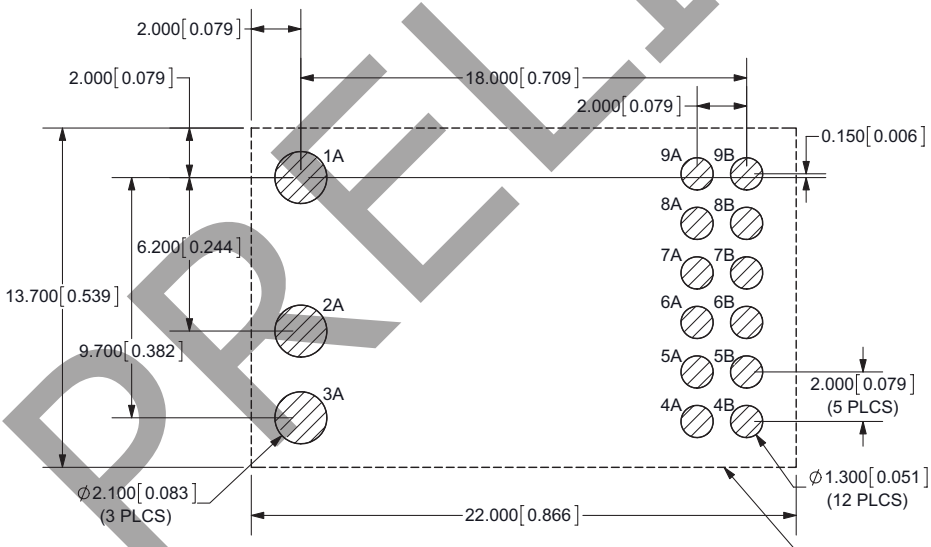
units: mm [inches]
tolerance unless specified:
X.X ±0.50 [0.02]
X.XX ±0.25 [0.01]
(not applied on footprint or typical values)



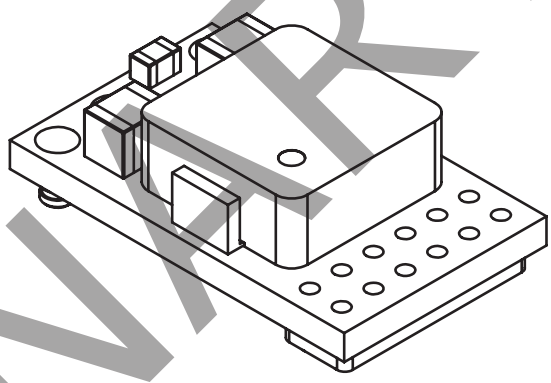
TOP VIEW



FRONT VIEW



PCB LAYOUT
TOP VIEW
Recommended keep out area for user components



PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A	VIN	Copper Alloy	Au 0.1 µm over Ni 1~3 µm
2A	GND		
3A	VOUT		
4A	VTRK/PG		Au 0.1 µm over Ni 2 µm
4B	PREF		
5A	+S		
5B	-S		
6A	SA0		
6B	DDC		
7A	SCL		
7B	SDA		
8A	VSET		
8B	SYNC		
9A	SALRT		
9B	CTRL		

PRELIMINARY

OPERATING INFORMATION

The NDM2Z-12 modules are available in different configurations; not all pins and functions are supported by each configuration. This document describes all pins and functions.
The Novum Z Products PMBus Commands application note defines the available PMBus™ commands.

REQUIRED CONFIGURATIONS

NDM2Z-12 Module Pins

Each NDM2Z-12 module should have a resistor placed between VSET and PREF to set the output voltage of the module. The maximum output voltage which can be configured by PMBus commands can never exceed 110% of the voltage set by the VSET pin. The SMBus address of each module is set by either pin-strap configuration or resistor value associated with the SA0 pin. More information regarding setting the SMBus address for a module can be found in the section titled "SMBus".

PCB Layout

Good performance of any point of load voltage regulator module can only be achieved with careful PCB layout considerations. Ground planes or very wide traces should be used for power and ground routing. Input capacitors should be placed close to the input voltage pins of the module and output capacitors should be placed close to the load. The module should also be placed as close as possible to the load.

INPUT AND OUTPUT CAPACITORS

Input Capacitors

Input capacitors are recommended to be used with the NDM2Z-12 module in order to minimize input voltage ripple. A 330 µF POSCAP or electrolytic and 3x 22 µF ceramic capacitors should be placed as close as possible to the input pins of the module. Additional input capacitors may be used if less input voltage ripple is desired.

Output Capacitors

Output capacitors are recommended to be used with the NDM2Z-12 module in order to improve transient response and minimize output voltage ripple. A 330 µF POSCAP or electrolytic and 3x 22 µF ceramic capacitors should be placed as close as possible to the load. Additional output capacitors may be used to further improve the output voltage characteristics.

POWER CONVERSION AND MANAGEMENT

Power Conversion Overview

The NDM2Z-12 module has several features to enable high power conversion efficiency. Non-linear loop response (NLR) improves the response time and reduces the output deviation as a result of load transients. The incorporation of DFM enhances the performance of CUI modules over that available from conventional analog POL offerings.

Power Management Overview

The NDM2Z-12 module incorporates a wide range of power management features. All power management functions can be configured via the SMBus interface. The NDM2Z-12 can monitor and report many characteristics of the module including input voltage, output voltage, output current and internal temperature. Additionally, the NDM2Z-12 includes circuit protection features that protect the module and load from damage due to system faults. Monitoring parameters can also be configured to provide alerts for specific conditions. The ability of CUI modules to digitally control, configure and monitor OS features provides significant benefits over traditional analog POL products.

CONFIGURING THE MODULE

Pin Settings

Pin SA0 is used to set the SMBus address of the NDM2Z-12 module. Details of this feature are discussed in the section titled "SMBus". Pin SYNC is used to synchronize the switching clock of the module to an external clock source. More information regarding synchronization can be found in the section titled "SWITCHING FREQUENCY AND SYNCHRONIZATION".
Pin VSET is used to configure the output voltage of the module. The voltage established by the VSET pin limits the maximum output voltage that can be configured by SMBus commands.
The SA0, SYNC and VSET pin configurations are read by the module when power is applied or whenever a SMBus RESTORE command is issued.
The CTRL pin is active high and can be used to enable the module. Internal connections on the module will drive the CTRL pin high if it is left floating.
Pins +S and -S are used for remote voltage sensing of the output voltage.

PRELIMINARY

Unused Pins

Table 1 describes the required or allowed connections for unused pins on the NDM2Z-12 module.

Table 1: Unused Pins

VSET	Tie to PREF with 133 kΩ resistor, see VOUT_COMMAND PMBus command
VTRK/PG, SA0, SYNC, CTRL, +S, -S	Float
DDC, SCL, SDA, SALRT	Pulled high with resistor, see "RECOMMENDED OPERATIN CONDITIONS"

Configuration of Parameters Using the SMBus

The NDM2Z-12 module is supplied with default settings. All module settings (except for module SMBus address, configured by pin SA0) can be re-configured via the SMBus interface. The output voltage can not be set to greater than 110% of the voltage set by the VSET pin.

START-UP PROCEDURE

Start-up Sequence

The NDM2Z-12 module follows an internal start-up procedure after power is applied to pin VIN. Table 2 describes the start-up sequence. If the module is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting CTRL (or applying input voltage to the module if CTRL is not used). Once this process is completed, the module is ready to accept assertion of CTRL and commands via the SMBus interface.

Table 2: NDM2Z-12 Start-up sequence

STEP	STEP NAME	DESCRIPTION	TIME DURATION
1	Power applied or RESTORE_FACTORY	Input voltage is applied to NDM2Z-12 module pin VIN or RESTORE_FACTORY PMBus command issued	Depends on input supply ramp time
2	Factory configuration settings	Module loads factory configuration settings. This step is also performed after using PMBus commands to restore the factory configuration file.	Approximately 10 ms (module will ignore a CTRL signal and PMBus commands during this period)
3	SA0, SYNC and VSET pin settings	Module loads values configured by the SA0, SYNC and VSET pins.	
4	Default configuration settings	Module loads default configuration settings. This data over-rides pin setting data, except for maximum limit for VOUT_COMMAND. This step also performed after using PMBus commands to restore the default configuration file.	
5	User configuration settings	Module loads user configuration settings. This data over-rides pin setting and default configuration data, except for maximum limit for VOUT_COMMAND. This step also performed after using PMBus commands to restore the user configuration file.	
6	Module ready	The module is ready to accept a CTRL signal.	---
7	Pre-ramp delay	The module requires approximately 5 ms following a CTRL signal and prior to ramping its output. Additional pre-ramp delay may be configured using PMBus commands.	Approximately 5 ms

Soft-start Delay Ramp Times

Once CTRL is asserted the NDM2Z-12 module requires a pre-ramp delay time before the output voltage may be allowed to start the ramp-up process. After the delay period has expired, the output will begin to ramp towards the target voltage according to the pre-configured soft-start ramp time that has been set. It is recommended to set the soft-start ramp time to a value greater than 500 µs in order to prevent fault conditions due to excessive inrush current. Soft start delay and ramp times may be set using PMBus commands.

Output Pre-Bias

An output pre-bias condition exists when a non-zero voltage is present on the NDM2Z-12 module output before the module output voltage is enabled. If a pre-bias voltage exists, the output voltage of the module is set to match the existing pre-bias voltage. The output voltage is then ramped to the final regulation value in the specified ramp time. The pre-bias voltage can be higher or lower than the final output voltage. Higher pre-bias output voltages will cause energy to be pumped into the input voltage rail powering the module. This condition could cause the module to report an error condition if the input voltage exceeds the input over voltage lock out threshold. The module will report an error condition if the pre-bias output voltage exceeds the output over voltage protection threshold.

PRELIMINARY

Power Good

The PG pin on the NDM2Z-12 module will assert if the output of the module is within tolerance of the target voltage and no fault conditions exist. A PG delay period is defined as the time from when all conditions within the module for asserting PG are met to when PG is actually asserted. By default, PG delay is set equal to the soft-start ramp time setting. The tolerance, polarity and delay of PG may be configured via PMBus commands.

Soft-stop Delay and Ramp Times

After CTRL is de-asserted the NDM2Z-12 module utilizes a pre-ramp delay time before the output starts the ramp-down process. After the delay period has expired, the output will begin to ramp towards ground according to the pre-configured soft-stop ramp time that has been set. It is recommended to set the soft-start ramp down to a value greater than 500 µs in order to prevent voltage spikes in the module input supply rail due the energy stored in the output capacitors. There will be a delay after the output voltage has reached ground potential and then the output of the module will be set to high impedance. Once the output of the module is high impedance the output voltage may float to a non-zero value if another source or leakage path is connected to the output. The soft-stop delay and ramp times may be configured via PMBus commands.
PMBus commands can be used to set the output of the NDM2Z-12 module to high impedance as soon as the output voltage drops below a selectable threshold.

OUTPUT VOLTAGE SETTING

Pin-Strap and Resistor Setting Methods

Using the pin-strap method, the voltage on the VOUT pin of the NDM2Z-12 module can be set to one of three default voltages as shown in Table 3. Table 4 lists the available output voltage settings with a resistor connected between VSET and PREF.

Table 3: Pin-strap VOUT voltage settings

VSET	VOUT (V)
LOW (< 0.8 V)	0.6
OPEN (N/C)	1.2
HIGH (> 2.0 V)	2.5

Table 4: Resistor VOUT voltage settings

RESISTOR (kΩ)	VOUT (V)	RESISTOR (kΩ)	VOUT (V)
10.0	0.60	46.4	1.50
11.0	0.65	51.1	1.60
12.1	0.70	56.2	1.70
13.3	0.75	61.9	1.80
14.7	0.80	68.1	1.90
16.2	0.85	75.0	2.00
17.8	0.90	82.5	2.10
19.6	0.95	90.9	2.20
21.5	1.00	100.0	2.30
23.7	1.05	110.0	2.50
26.1	1.10	121.0	3.00
28.7	1.15	133.0	3.30
31.6	1.20	147.0	4.00
34.8	1.25	162.0	5.00
38.3	1.30	178.0	5.50
42.2	1.40		

SMBus Setting Method

The voltage present at the VOUT pin of the NDM2Z-12 module can be reconfigured using PMBus commands. A voltage level reconfigured by a PMBus command overrides the voltage set by the VSET pin, but cannot be set to greater than 110% of the voltage set by the VSET pin.

Voltage Tracking

The NDM2Z-12 module includes a feature that allows the output ramp voltage to track the ramp of a reference voltage which is applied to the VTRK/PG pin. The voltage ramp tracking capability can be configured so that member modules track at either 50% or 100% of the reference voltage ramp rate. In addition, a member module can be configured so that the termination voltage either tracks or ignores perturbations on the reference voltage once it has stabilized. Tracking at 50% and tracking final voltage perturbations is intended for DDR memory applications. All other applications which required voltage tracking should use 100% tracking and ignore final voltage perturbations. The reference voltage for tracking must have a target voltage which is equal to or greater than the target voltage of the member modules. The turn-on delay of the reference voltage must be at least 10 ms greater than that set for the member modules. In voltage tracking mode, the turn-off delay of the member modules establishes the time duration which the member modules will track the reference voltage after CTRL is de-asserted. The turn-off delay of the member modules must be at least 5 ms greater than the sum of the turn-off delay and fall time of the reference voltage.

PRELIMINARY

Current sharing modules which are also configured to track a voltage must have all of the VTRK/PG pins tied together. All of the CTRL pins of the member modules must also be connected together and driven by a common source. The rise and fall times of the member modules should be set between 5 ms and 10 ms to ensure current sharing while ramping. PMBus commands can be used to configure the voltage tracking features.

Voltage Margining

The NDM2Z-12 module offers a means to vary the output voltage higher or lower relative to the nominal voltage setting. The rate of change of the output voltage during voltage margining is also configurable. The margin feature can be reconfigured through PMBus commands.

SWITCHING FREQUENCY AND SYNCHRONIZATION

Switching Frequency

The switching frequency of the NDM2Z-12 module can be reconfigured by PMBus commands or controlled by an external clock source connected to the SYNC pin. If the module is operated at a switching frequency of other than the factory default setting, the compensation may need to be adjusted and the ripple, noise, transient response and efficiency may be affected.

SYNC Auto Detect

The NDM2Z-12 module will automatically check for a clock signal on the SYNC pin after CTRL is asserted (or applying input voltage to the module if CTRL is not used). If a clock signal is present, the module will synchronize to the rising edge of the external clock. The external clock signal must be stable and conform to the "RECOMMENDED OPERATING CONDITIONS" parameters when CTRL is asserted (or applying input voltage to the module if CTRL is not used). In the event of a loss of the external clock signal, the output voltage of the module may show transient overshoot or undershoot and the module will automatically configure to switch at a frequency close to the previous incoming frequency. If no incoming clock signal is present when CTRL is asserted (or applying input voltage to the module if CTRL is not used), the module will switch at the frequency set by the configuration file.

CONTROL LOOP

Adaptive Loop Compensation

The NDM2Z-12 module employs automatic adaptive loop compensation to increase the performance and stability of the module over a wide range of conditions. The default setting configures the module to re-compensate the control loop every time the output voltage ramps to the regulated level. PMBus commands can be used to configure when the module re-compensates the loop.
The user also has the option to manually configure the loop compensation.

Non-Linear Response (NLR) Settings

The NDM2Z-12 module incorporates a non-linear response (NLR) loop that decreases the response time and the output voltage deviation in the event of a sudden output load current step. This implementation results in a higher equivalent loop bandwidth than what would be possible using a traditional linear loop. PMBus commands can be used to configure the NLR response of the module.

Adaptive Diode Emulation

Please contact CUI technical support regarding the implementation of adaptive diode emulation.

Adaptive Frequency Control

The NDM2Z-12 module includes adaptive frequency control to improve conversion efficiency. Adaptive frequency control is not available for current sharing groups and is not allowed when the module is placed in auto-detect mode and a clock source is present on the SYNC pin.
Adaptive frequency control is only available while the module is operating within adaptive diode emulation mode. Adaptive frequency control can be enabled and disabled with PMBus commands.

MULTI-MODULE CONFIGURATION

Output Sequencing

Multiple device sequencing of NDM2Z-12 modules may be achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain. The CTRL pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. CTRL must be driven low to initiate a sequenced turnoff of the group.

PRELIMINARY

Fault Spreading

NDM2Z-12 modules can be configured to broadcast a fault event over the GCB (Group Communication Bus) to the other modules in the group. When a nondestructive fault occurs and the module is configured to shut down on a fault, the module will shut down and broadcast the fault event over the GCB. The other modules on the GCB will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so. PMBus commands can be used to configure the transmission and reception of faults.

Phase Spreading

When multiple NDM2Z-12 modules share a common DC input supply, it may be desirable to adjust the clock phase offset of each module. In order to enable phase spreading, all modules must be synchronized to the same switching clock. For modules driven by a common synchronizing clock the phase offset of each module is controlled by the module addresses; phase offset = device address x 45°.
For example:

- A module address of 0x00 or 0x20 would configure 0° of phase offset
- A module address of 0x01 or 0x21 would configure 45° of phase offset
- A module address of 0x02 or 0x22 would configure 90° of phase offset

The phase offset of each module may also be set via the PMBus.

POWER FAULT MANAGEMENT

Input Under and Over Voltage Lockout

Input under voltage lockout (UVLO) and input over voltage lockout (OVLO) indicate faults for the NDM2Z-12 module when the input voltage falls outside of preset thresholds. The default response due to an input voltage fault is an immediate shutdown of the module. The module will continuously check for the presence of the fault condition. Once the fault condition is no longer present, the module will be re-enabled. PMBus commands can be used to configure the thresholds and response of the module to the fault condition.

Output Under and Over Voltage Protection

The NDM2Z-12 module employs an output voltage protection circuit that can be used to protect load circuitry from being subjected to voltages outside of prescribed limits. A hardware comparator is used to compare the voltage seen at the +S pin to voltage thresholds. If the +S pin voltage is outside of these thresholds the PG pin will de-assert and the module will indicate a fault condition. The default response to an output voltage fault is to immediately shut down. The module will continuously check for the presence of the fault condition, when the fault condition no longer exists the module will be re-enabled. PMBus commands can be used to set the voltage thresholds and configure the response of the module to the fault condition. When operating from an external clock the only allowed response to an output voltage fault is an immediate shutdown.

Output Over Current Protection

Output over current protection will protect the NDM2Z-12 module and load from damage if an overload condition is imposed on the output. The module will indicate a fault condition when the output current limit threshold is exceeded. The default response from an output current fault is an immediate shutdown of the module. The module will continuously check for the presence of the fault condition, and if the fault condition no longer exists the module will be re-enabled. PMBus commands can be used to configure the current limit threshold and the response of the module to the fault condition.

Thermal Overload Protection

The NDM2Z-12 module includes a thermal sensor that measures the temperature of the module and indicates a fault when the temperature exceeds a preset limit. The default response from a temperature fault is an immediate shutdown of the module. The module will continuously check for the fault condition and once the fault has cleared the module will be re-enabled. PMBus commands can be used to configure the thermal protection threshold and the response of the module to the fault condition. Permanent damage to the module may result if the thermal limit is set too high.

SMBUS

SMBus Communications

The NDM2Z-12 module provides a SMBus interface that enables the user to configure the module operation as well as monitor input and output parameters. The module can be used with any standard 2-wire I^2C host device, accepts most standard PMBus commands, is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. It is recommended that CTRL be pulled low while configuring the module with PMBus commands. Pull-up resistors are required on the SMBus lines as described in "RECOMMENDED OPERATING CONDITIONS".

PRELIMINARY

SMBus Addresses

When communicating with multiple SMBus devices using the SMBus interface, each device must have a unique address so the host can distinguish between the devices. The NDM2Z-12 module address can be set according to the pin-strap options listed in Table 5; address values are right-justified.

If additional module addresses are required, a resistor can be connected to pin SA0 as shown in Table 6 to provide up to 25 unique module addresses.

Table 5: Pin-strap SMBus Addressing

SA0	ADDRESS
HIGH	0x25
OPEN	0x24
LOW	0x23

Table 6: Single Resistor SMBus Addressing

R_{SA0} (kΩ)	ADDRESS	R_{SA0} (kΩ)	ADDRESS
10.0	0x64	34.8	0x71
11.0	0x65	38.3	0x72
12.1	0x66	42.2	0x73
13.3	0x67	46.4	0x74
14.7	0x68	51.1	0x75
16.2	0x69	56.2	0x76
17.8	0x6A	61.9	0x77
19.6	0x6B	68.1	0x78
21.5	0x6C	75.0	0x79
23.7	0x6D	82.5	0x7A
26.1	0x6E	90.9	0x7B
28.7	0x6F	100.0	0x7C
31.6	0x70		

Monitoring Via SMBus

A system controller can be used to monitor the NDM2Z-12 module system parameters through the SMBus. Fault conditions can be detected by monitoring the SALRT pin, which will be asserted when pre-configured fault conditions occur. Modules can also be monitored for power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Output current
- Module temperature
- Switching frequency
- Duty cycle

SINGLE WIRE COMMUNICATIONS

Digital-DC Bus

The DDC (Digital-DC Communication Bus) is used to communicate between NDMxZ modules. This dedicated bus provides the communication channel between modules for features such as sequencing, fault spreading, and current sharing. A pull-up resistor is required on the DDC as defined in "RECOMMENDED OPERATING CONDITIONS".

Snapshot™ Parameter Capture

The NDM2Z-12 module offers features that enable the user to capture parametric data during normal operation or following a fault. The Snapshot feature enables the user to read status and parameter values via a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 22 bytes will occupy the SMBus for up to 1400 µs.

The SNAPSHOT_CONTROL command enables the user to store the snapshot parameters to flash memory in response to a pending fault as well as to read the stored data from flash memory after a fault has occurred. Automatic writes to flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific response to that fault is to shut down (writing to flash memory is not allowed if the module is configured to re-try following the specific fault condition). It should also be noted that the input voltage to the module must be maintained during the time when the module is writing the data to flash memory; a process that requires between 700 µs to 1400 µs depending on whether the data is set up for a block write. Undesirable results may be observed if the input voltage to the module drops too low during this process. In the event that the module experiences a fault and power is lost, the user can extract the last SNAPSHOT parameters stored during the fault by using the SMBus to transfer data from flash memory to RAM and then using the SMBus to read data from RAM.

THERMAL CONSIDERATIONS

Mounting

Heat from the NDM2Z-12 module will be conducted through the pins to the host board. Provisions must be made for the host board to accommodate this additional heating.

Airflow

Airflow past the NDM2Z-12 module will assist in cooling the module. Factors affecting the efficiency of the cooling include the rate, direction and temperature of the airflow.

PRELIMINARY

REVISION HISTORY

rev.	date
0.9	12/12/2013
0.91	03/13/2014
0.92	11/07/2014

The revision history provided is for informational purposes only and is believed to be accurate.

PRELIMINARY

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