CUI INC
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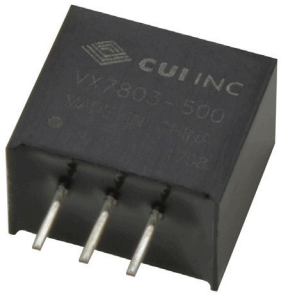
SERIES: VX78-500 | DESCRIPTION: NON-ISOLATED DC SWITCHING REGULATOR

FEATURES

- wide input
- pin-out compatible with linear regulators
- encapsulated
- UL & CSA approved
- high efficiency up to 95%
- no-load input current as low as 0.2 mA
- wide operating temp: -40°C to +85°C
- supports negative output
- short circuit protection on the output
- EN 62368-1

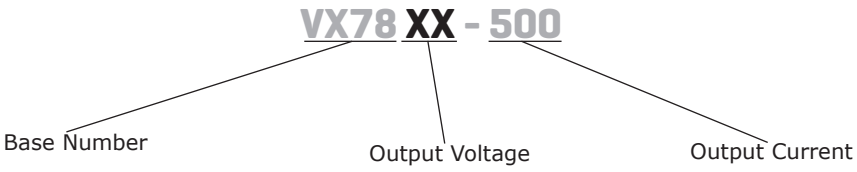


MODEL

MODEL	input voltage[1] typ (Vdc)	input voltage[1] range (Vdc)	output voltage (Vdc)	output current max (mA)	output power max (W)	ripple & noise[2] max (mVp-p)	efficiency[3] typ (%)
VX7803-500	24	4.75~36	3.3	500	1.65	75	86
VX7805-500	24	6.5~36	5	500	2.5	75	90
	12	7~31	-5	-300	1.5	75	80
VX78039-500	24	12~36	9	500	4.5	75	93
VX78012-500	24	15~36	12	500	6	75	94
	12	8~24	-12	-150	1.8	75	84
VX7815-500	24	19~36	15	500	7.5	75	95
	12	8~21	-15	-150	2.25	75	85

Notes:
1. For input voltages higher than 30 Vdc, a 22 µF / 50 V input capacitor is required.
2. Tested at nominal input, 10~100% load, 20 MHz bandwidth, with 10 µF electrolytic and 1 µF ceramic capacitor on the output. At loads below 10%, the max ripple and noise of the 3.3 & 5 Vdc outputs will be 150 mVp-p, and the other outputs will be 2% Vo.
3. Measured at min Vin, full load.
4. All specifications are measured at Ta=25°C, humidity < 75%, nominal input voltage, and rated output load unless otherwise specified.

PART NUMBER KEY



INPUT

parameter	conditions/description	min	typ	max	units
operating input voltage[1]	for positive output applications for negative output applications	4.75 7	24 12	36 31	Vdc Vdc
filter	capacitor filter				
input reverse polartiy protection	no				
no-load input current	positive outputs		0.2	1.5	mA

Note: 1. See Model section on page 1 for specific input voltage ranges.

OUTPUT

parameter	conditions/description	min	typ	max	units
maximum capacitive load[2]	for positive output applications for negative output applications			680 330	µF µF
voltage accuracy	at full load, input voltage range 3.3 Vdc output model all other models		 ±2 ±2	 ±4 ±3	 % %
line regulation	at full load, input voltage range		±0.2	±0.4	%
load regulation	at nominal input, 10~100% load		±0.4	±0.6	%
switching frequency	at nominal input voltage, full load	550		850	kHz
transient recovery time	at nominal input voltage, 25% load step change		0.2	1	ms
transient response deviation	at nominal input voltage, 25% load step change		50	250	mV
temperature coefficient	at full load			±0.03	%/°C

Note: 2. The maximum capacitive load was tested at nominal input voltage, full load.

PROTECTIONS

parameter	conditions/description	min	typ	max	units
short circuit protection	continuous, auto recovery				

SAFETY AND COMPLIANCE

parameter	conditions/description	min	typ	max	units
safety approvals	certified to 62368-1: EN certified to 60950-1: UL				
EMI/EMC	EN 55032, EN 55024				
conducted emissions	CISPR22/EN55022, class B (external circuit required, see Figure 6-b)				
radiated emissions	CISPR22/EN55022, class B (external circuit required, see Figure 6-b)				
ESD	IEC/EN61000-4-2, contact ± 4kV, class B				
radiated immunity	IEC/EN61000-4-3, 10V/m, class A				
EFT/burst	IEC/EN61000-4-4, ± 1kV, class B (external circuit required, see Figure 6-a)				
surge	IEC/EN61000-4-5, line-line ± 1kV, class B (external circuit required, see Figure 6-a)				
conducted immunity	IEC/EN61000-4-6, 3 Vr.m.s, class A				
MTBF	as per MIL-HDBK-217F, 25°C	2,000,000			hours
RoHS	2011/65/EU				

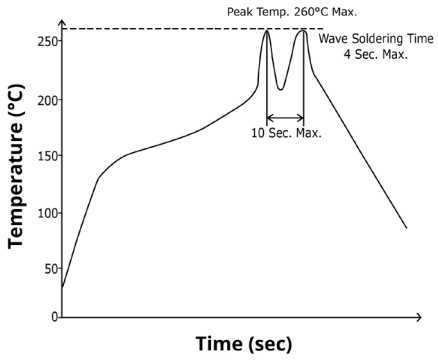
ENVIRONMENTAL

parameter	conditions/description	min	typ	max	units
operating temperature	see derating curve	-40		85	°C
storage temperature		-55		125	°C
storage humidity	non-condensing	5		95	%

SOLDERABILITY

parameter	conditions/description	min	typ	max	units
wave soldering	see wave soldering profile			260	°C

WAVE SOLDERING PROFILE



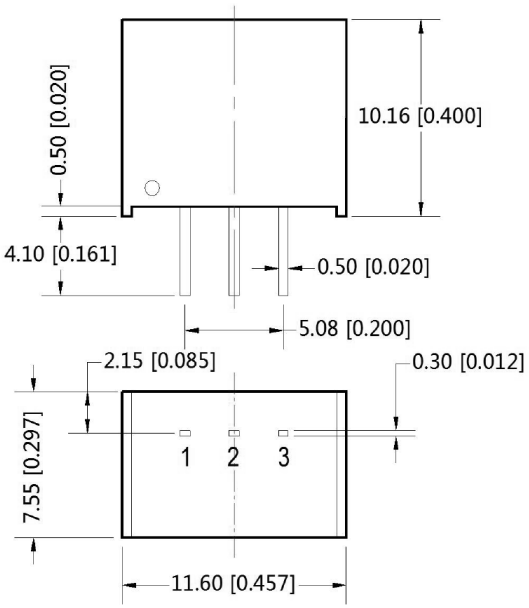
MECHANICAL

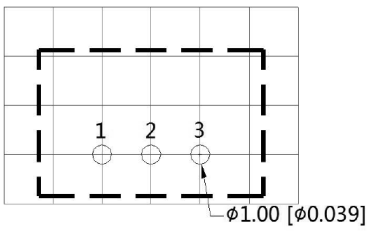
parameter	conditions/description	min	typ	max	units
dimensions	11.60 x 7.55 x 10.16 [0.457 x 0.297 x 0.400 inch]				mm
case material	black flame-retardant heat-proof plastic (UL94V-0)				
weight			1.8		g

MECHANICAL DRAWING

units: mm [inch]
tolerance: ±0.25[±0.010]
pin diameter tolerance: ±0.10[±0.004]

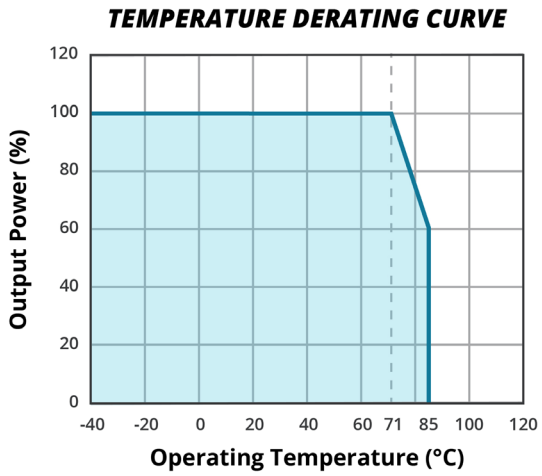
PIN CONNECTIONS		
PIN	+OUTPUT	-OUTPUT
1	+VIN	+VIN
2	GND	-VOUT
3	+VOUT	GND



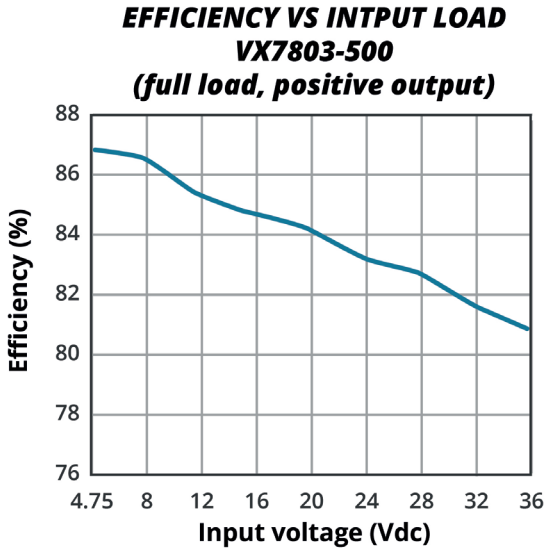


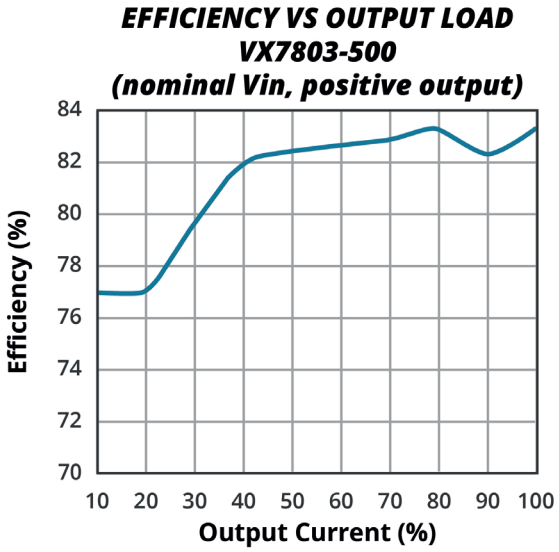
Note : Grid 2.54*2.54mm
Recommended PCB Layout
Top View

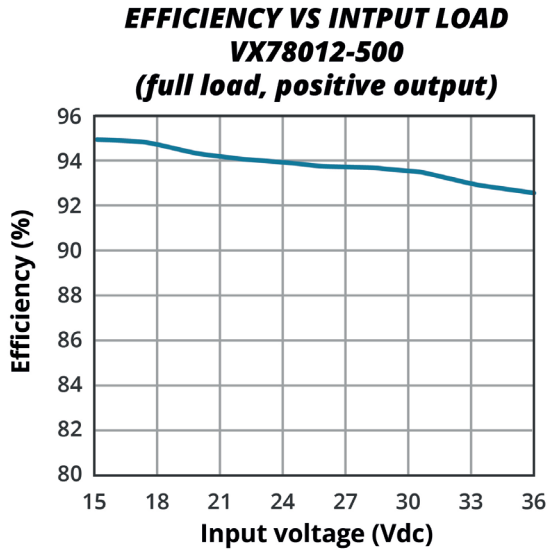
DERATING CURVE

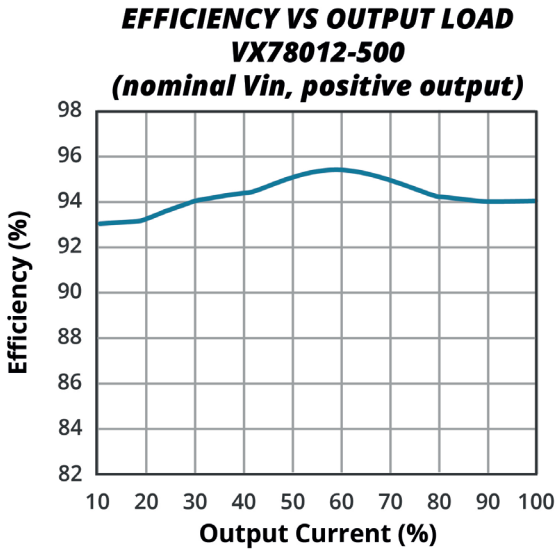


EFFICIENCY CURVES



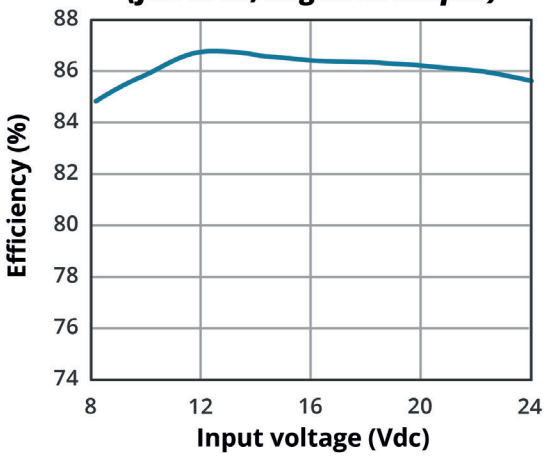




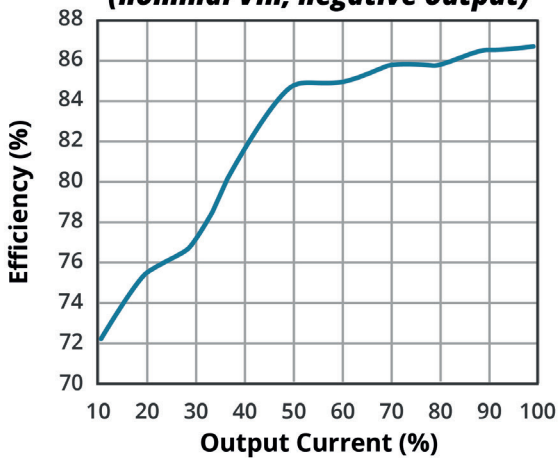


EFFICIENCY CURVES (CONTINUED)

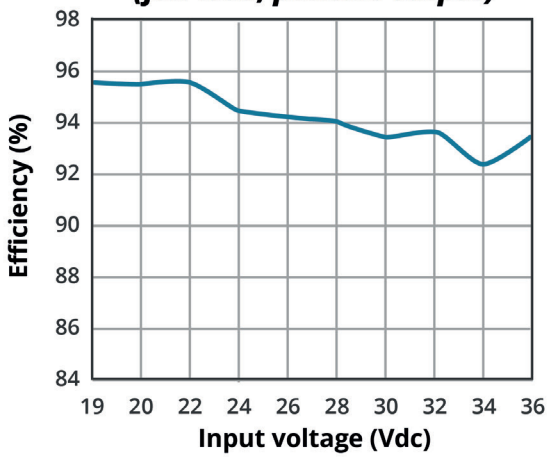
EFFICIENCY VS INTPUT LOAD
VX78012-500
(full load, negative output)



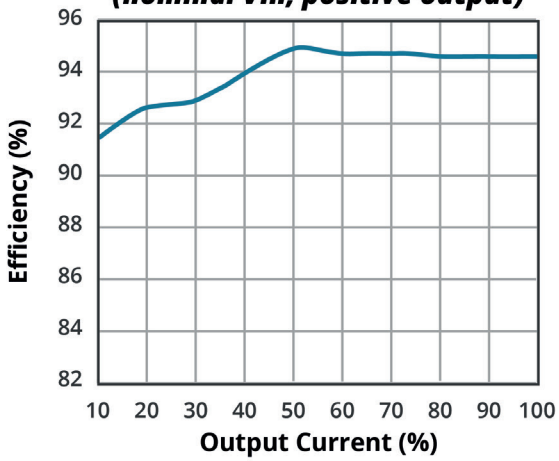
EFFICIENCY VS OUTPUT LOAD
VX78012-500
(nominal Vin, negative output)



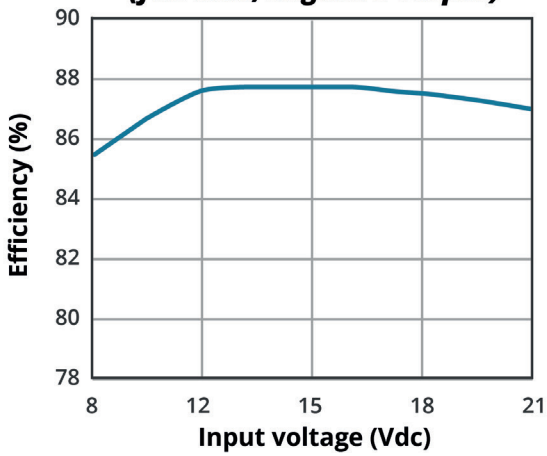
EFFICIENCY VS INTPUT LOAD
VX7815-500
(full load, positive output)



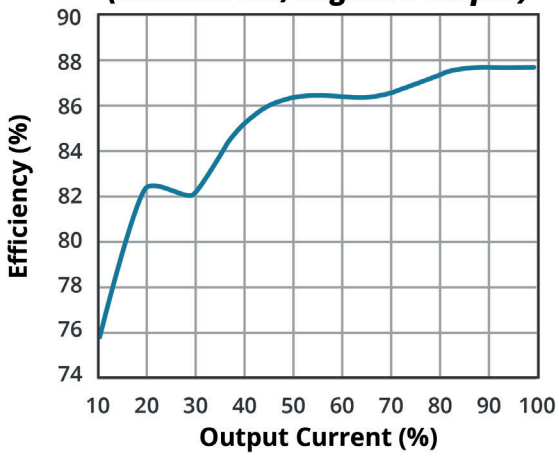
EFFICIENCY VS OUTPUT LOAD
VX7815-500
(nominal Vin, positive output)



EFFICIENCY VS INTPUT LOAD
VX7815-500
(full load, negative output)



EFFICIENCY VS OUTPUT LOAD
VX7815-500
(nominal Vin, negative output)



TYPICAL APPLICATION CIRCUIT

Figure 1
Positive Output Application Circuit

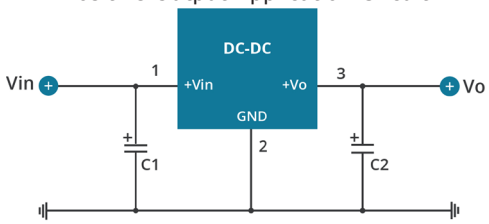


Figure 2
Negative Output Application Circuit

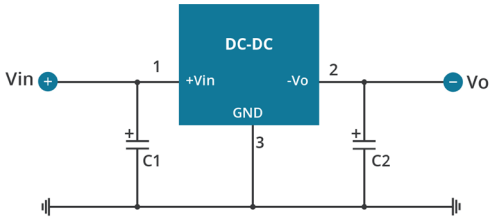


Figure 3
Positive and Negative Output Paralleling Application Circuit

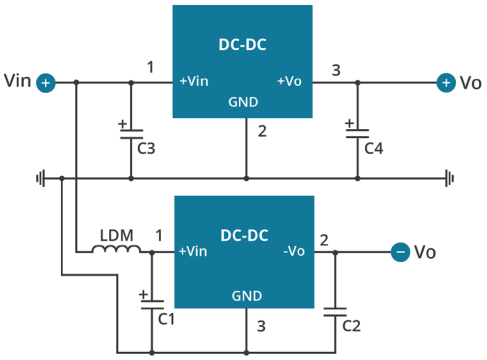


Table 1
External Capacitor Table

Model Number	C1, C3 (ceramic capacitor)	C2, C4 (ceramic capacitor)
VX7803-500	10 µF/50 V	22 µF/10 V
VX7805-500	10 µF/50 V	22 µF/10 V
VX78039-500	10 µF/50 V	22 µF/16 V
VX78012-500	10 µF/50 V	22 µF/25 V
VX7815-500	10 µF/50 V	22 µF/25 V

Figure 4
Positive Output Ripple Reduction Circuit

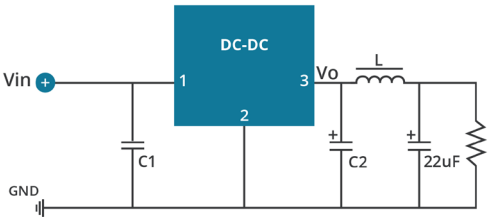
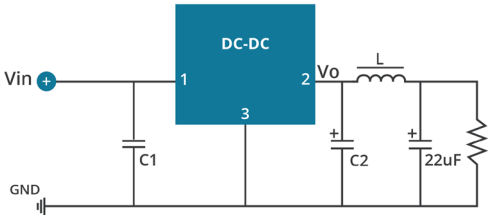


Figure 5
Negative Output Ripple Reduction Circuit



EMC RECOMMENDED CIRCUIT

Figure 6

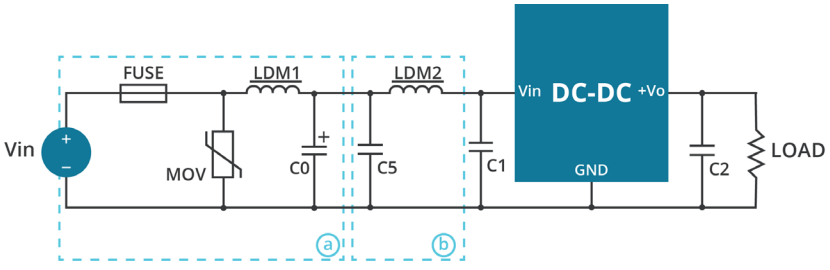


Table 2

Recommended external circuit components	
FUSE	choose according to actual input current
MOV	S20K30
LDM1	82 µH
C0	680 µF/50 V
C1, C2	see Table 1
C5	4.7 µF/50 V
LDM2	12 µH

Note:
1. C1 & C2 (C3 & C4) are required and should be connected as close to the module pins as possible.
2. To reduce the output ripple further, it is recommended to connect an "LC" filter at the output terminal with a recommended value of 10~47 µH for the L component. (See Figures 4 & 5).
3. When using application circuit in Figure 3, a 10 µH LDM component is recommended to reduce the interference.

REVISION HISTORY

rev.	description	date
1.0	initial release	05/18/2017
1.01	features and safety line updated, packaging removed	01/14/2021
1.02	derating curve and circuit figures updated	09/14/2021

The revision history provided is for informational purposes only and is believed to be accurate.

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