Universal Synchronous EPLD

Features

- 100-MHz output registered operation
- Twelve I/O macrocells, each having:
  - Registered, three-state I/O pins
  - Input and output register clock select multiplexer
  - Feed back multiplexer
  - Output enable ($\overline{OE}$) multiplexer
- Bypass on input and output registers
- All twelve macrocell state registers can be hidden
- User configurable I/O macrocells to implement JK or RS flip-flops and T or D registers
- Input multiplexer per pair of I/O macrocells allows I/O pin associated with a hidden macrocell state register to be saved for use as an input
- Four dedicated hidden registers
- Twelve dedicated registered inputs with individually programmable bypass option
- Three separate clocks—two input clocks, two output clocks
- Common (pin 14–controlled) or product term–controlled output enable for each I/O pin
- 256 product terms—32 per pair of macrocells, variable distribution
- Global, synchronous, product term–controlled, state register set and reset—inputs to product term are clocked by input clock
  - 2-ns input set-up and 9-ns output register clock to output
  - 10-ns input register clock to state register clock
- 28-pin, 300-mil DIP, LCC, PLCC
- Erasable and reprogrammable
- Programmable security bit

Functional Description

The CY7C335 is a high-performance, erasable, programmable logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance state machines.

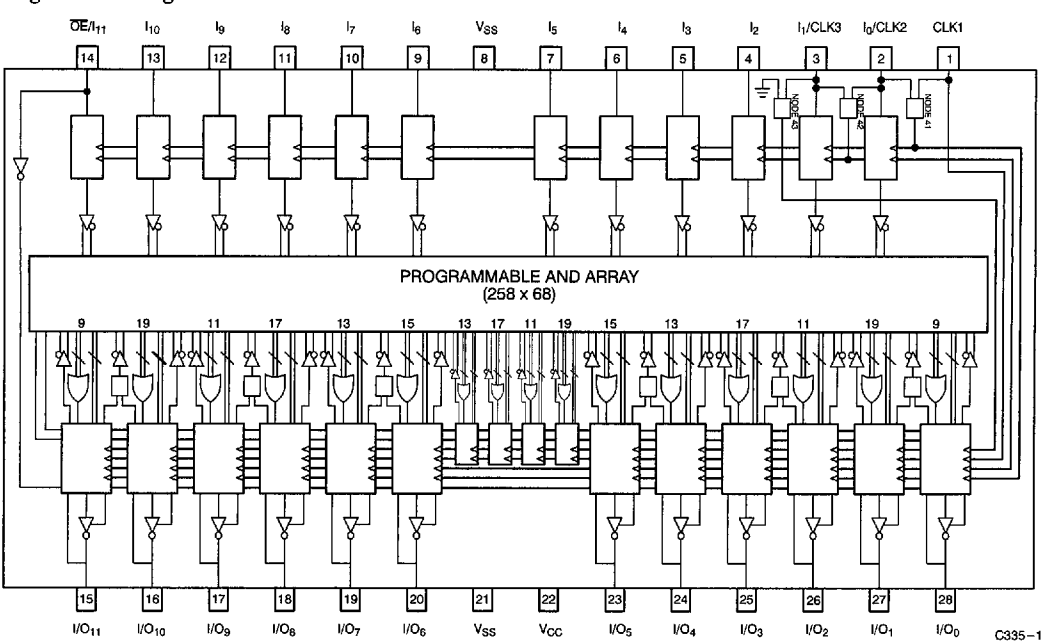
The architecture of the CY7C335, consisting of the user-configurable output macrocell, bidirectional I/O capability, input registers, and three separate clocks, enables the user to design high-performance state machines that can communicate either with each other or with microprocessors over bidirectional parallel buses of user-definable widths.

The four clocks permit independent, synchronous state machines to be synchronized to each other.

The user-configurable macrocells enable the designer to designate JK-, RS-, T-, or D-type devices so that the number of product terms required to implement the logic is minimized.

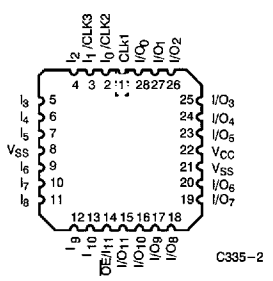
The CY7C335 is available in a wide variety of packages including 28-pin, 300-mil plastic and ceramic DIPs, PLCCs, and LCCs.

Logic Block Diagram



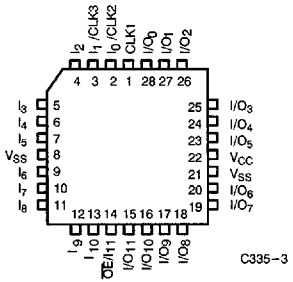
Pin Configurations

LCC
Top View



C335-2

PLCC
Top View



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Selection Guide

		CY7C335-100	CY7C335-83	CY7C335-66	CY7C335-50	CY7C335-40
Maximum Operating Frequency (MHz)	Commercial	100	83.3	66.6	50	
	Military		83.3	66.6	50	40.0
I_{CC1} (mA)	Commercial	140	140	140	140	
	Military		160	160	160	160

Architecture Configuration Bits

The architecture configuration bits are used to program the multiplexers. The function of the architecture bits is outlined in *Table 1.*

Table 1. Architecture Configuration Bits

Architecture Configuration Bit		Number of Bits	Value	Function
C0	Output Enable Select MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Output Enable Controlled by Product Term
			1—Programmed	Output Enable Controlled by Pin 14
C1	State Register Feed Back MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	State Register Output is Fed Back to Input Array
			1—Programmed	I/O Macrocell is Configured as an Input and Output of Input Path is Fed to Array
C2	I/O Macrocell Input Register Clock Select MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	ICLK1 Controls the Input Register I/O Macrocell Input Register Clock Input
			1—Programmed	ICLK2 Controls the Input Register I/O Macrocell Input Register Clock Input
C3	Input Register Bypass MUX—I/O Macrocell	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Selects Input to Feedback MUX from Input Register
			1—Programmed	Selects Input to Feedback MUX from I/O pin
C4	Output Register Bypass MUX	12 Bits, 1 Per I/O Macrocell	0—Virgin State	Selects Output from the State Register
			1—Programmed	Selects Output from the Array, Bypassing the State Register
C5	State Clock MUX	16 Bits, 1 Per I/O Macrocell and 1 Per Hidden Macrocell	0—Virgin State	State Clock 1 Controls the State Register
			1—Programmed	State Clock 2 Controls the State Register
C6	Dedicated Input Register Clock Select MUX	12 Bits, 1 Per Dedicated Input Cell	0—Virgin State	ICLK1 Controls the Input Register I/O Macrocell Dedicated Input Register Clock Input
			1—Programmed	ICLK2 Controls the Input Register I/O Macrocell Dedicated Input Register Clock Input

Table 1. Architecture Configuration Bits (continued)

Architecture Configuration Bit		Number of Bits	Value	Function
C7	Input Register Bypass MUX—Input Cell	12 Bits, 1 Per Dedicated Input Cell	0—Virgin State	Selects Input to Array from Input Register
			1—Programmed	Selects Input to Array from Input Pin
C8	ICLK2 Select MUX	1 Bit	0—Virgin State	Input Clock 2 Controlled by Pin 2
			1—Programmed	Input Clock 2 Controlled by Pin 3
C9	ICLK1 Select MUX	1 Bit	0—Virgin State	Input Clock 1 Controlled by Pin 2
			1—Programmed	Input Clock 1 Controlled by Pin 1
C10	SCLK2 Select MUX	1 Bit	0—Virgin State	State Clock 2 Grounded
			1—Programmed	State Clock 2 Controlled by Pin 3
CX (11–16)	I/O Macrocell Pair Input Select MUX	6 Bits, 1 Per I/O Macrocell Pair	0—Virgin State	Selects Data from I/O Macrocell Input Path of Macrocell A of Macrocell Pair
			1—Programmed	Selects Data from I/O Macrocell Input Path of Macrocell B of Macrocell Pair

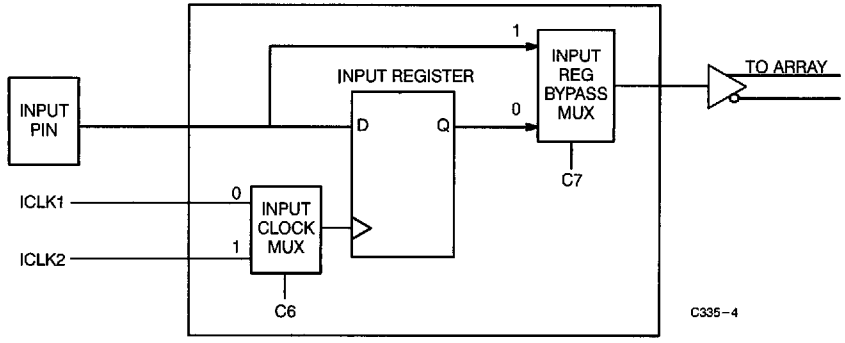


Figure 1. CY7C335 Input Macrocell

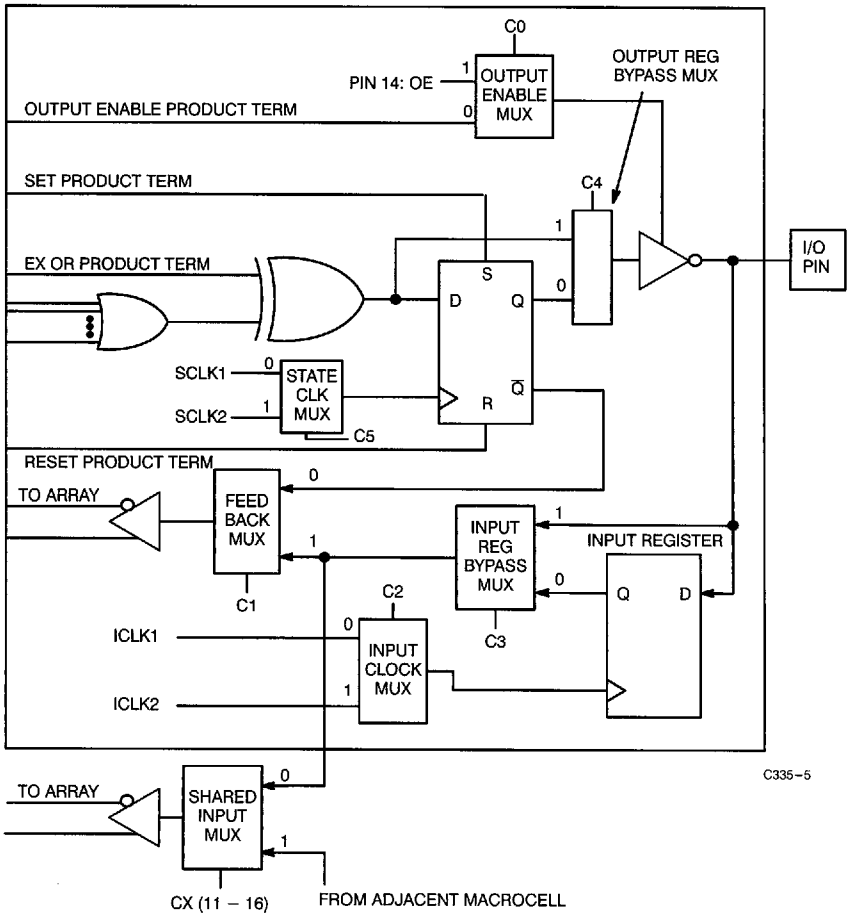


Figure 2. CY7C335 Input/Output Macrocell

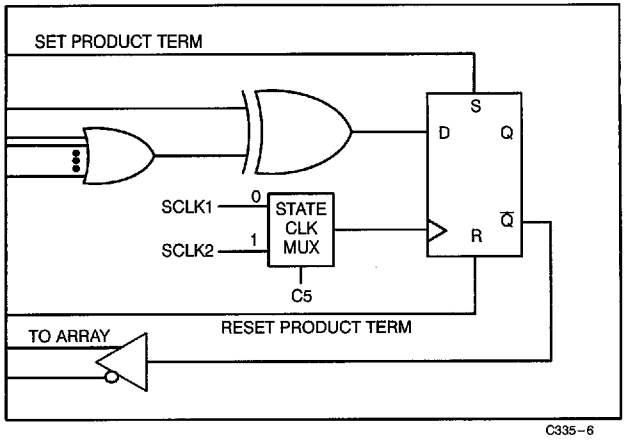


Figure 3. CY7C335 Hidden Macrocell

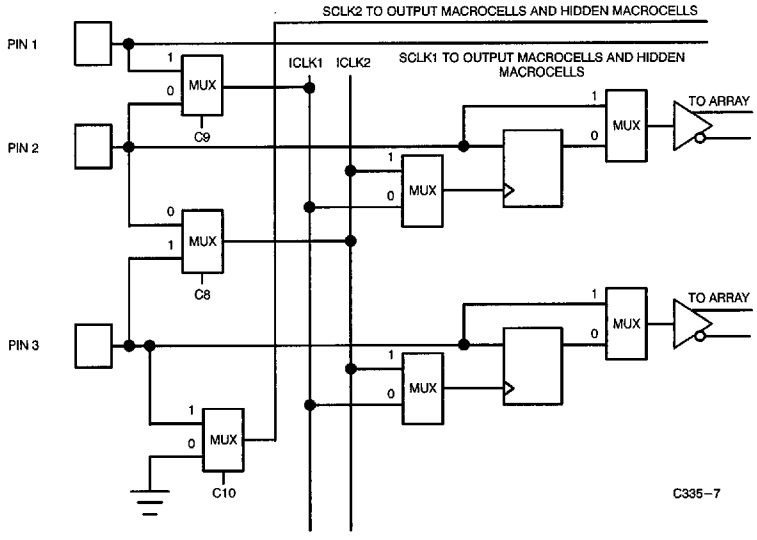


Figure 4. CY7C335 Input Clocking Scheme

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (Low) ..... 12 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil/Ind			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	Com'l		0.5	V
			I_{OL} = 8 mA	Mil/Ind			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.2		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4, 5]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		Com'l		140	mA
				Mil/Ind		160	mA
I_{CC2}	Power Supply Current at Frequency[5]	V_{CC} = Max., Outputs Disabled (in High Z State), Device Operating at f_{MAX} External (f_{MAX5})		Com'l		180	mA
				Mil/Ind		200	mA

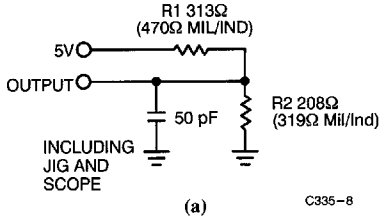
Capacitance[5]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		10	pF

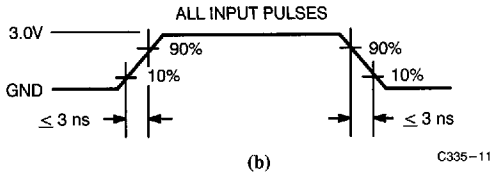
Notes:

1. t_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by ground degradation.
5. Tested initially and after any design or process changes that may affect these parameters.

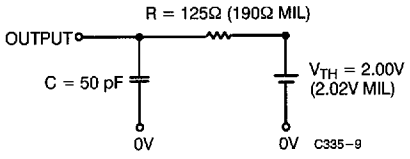
AC Test Loads and Waveforms (Commercial)



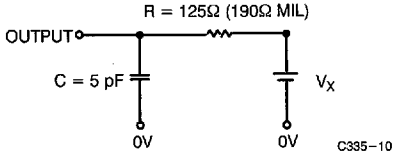
(a)



(b)



(c) Thévenin Equivalent (Load 1)



(d) Three-state Delay Load (Load 2)

Parameter	V_X	Output Waveform—Measurement Level
t_{PXZ} (−)	1.5V	V_{OH}, 0.5V, V_X C335-12
t_{PXZ} (+)	2.6V	V_{OL}, 0.5V, V_X C335-13
t_{PZX} (+)	V_{th}	V_X, 0.5V, V_{OH} C335-14
t_{PZX} (−)	V_{th}	V_X, 0.5V, V_{OL} C335-15
t_{CER} (−)	1.5V	V_{OH}, 0.5V, V_X C335-16
t_{CER} (+)	2.6V	V_{OL}, 0.5V, V_X C335-17
t_{CEA} (+)	V_{th}	V_X, 0.5V, V_{OH} C335-18
t_{CEA} (−)	V_{th}	V_X, 0.5V, V_{OL} C335-19

Figure 5. Test Waveforms

Commercial AC Characteristics

Parameter	Description	7C335-100		7C335-83		7C335-66		7C335-50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Output Propagation Delay		15		15		20		25	ns
t_{EA}	Input to Output Enable		15		15		20		25	ns
t_{ER}	Input to Output Disable		15		15		20		25	ns
Input Registered Mode Parameters										
t_{WH}	Input and Output Clock Width HIGH[5]	4		5		6		8		ns
t_{WL}	Input and Output Clock Width LOW[5]	4		5		6		8		ns
t_{IS}	Input or Feedback Set-Up Time to Input Clock	2		2		2		3		ns
t_{IH}	Input Register Hold Time from Input Clock	2		2		2		3		ns
t_{ICO}	Input Register Clock to Output Delay		18		18		20		25	ns
t_{IOH}	Output Data Stable Time from Input Clock	3		3		3		3		ns
$t_{IOH} - t_{IH}$ 33x	Output Data Stable from Input Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
t_{PZX}	Pin 14 Enable to Output Enabled		12		12		15		20	ns
t_{PXZ}	Pin 14 Disable to Output Disabled		12		12		15		20	ns
f_{MAX1}	Maximum Frequency of (2) CY7C335s in Input Registered Mode (Lowest of $1/(t_{ICO}+t_{IS})$ & $1/(t_{WL}+t_{WH})$)[5]	50		50		45.4		35.7		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lowest of $(1/(t_{ICO})$, $1/(t_{WH}+t_{WL})$, $1/(t_{IS}+t_{IH})$)[5]	55.5		55.5		50		40		MHz
t_{ICEA}	Input Clock to Output Enabled		17		17		20		25	ns
t_{ICER}	Input Clock to Output Disabled		15		15		20		25	ns
Output Registered Mode Parameters										
t_{CEA}	Output Clock to Output Enabled[5]		17		17		20		25	ns
t_{CER}	Output Clock to Output Disabled[5]		15		15		20		25	ns
t_S	Output Register Input Set-Up Time from Output Clock	8		9		12		15		ns
t_H	Output Register Input Hold Time from Output Clock	0		0		0		0		ns
t_{CO}	Output Register Clock to Output Delay		9		10		12		15	ns
t_{CO2}	Input Output Register Clock or Latch Enable to Combinatorial Output Delay (Through Logic Array)[5]		17		18		23		30	ns
t_{OH}	Output Data Stable Time from Output Clock	2		2		2		2		ns
t_{OH2}	Output Data Stable Time From Output Clock (Through Memory Array)[5]	3		3		3		3		ns
$t_{OH2}-t_{IH}$	Output Data Clock Stable Time From Output Clock Minus Input Register Hold Time[5]	0		0		0		0		ns
f_{MAX3}	Maximum Frequency with Internal Feedback in Output Registered Mode[5]	100		83.3		66.6		50		MHz
f_{MAX4}	Maximum Frequency of (2) CY7C335s in Output Registered Mode (Lowest of $1/(t_{CO}+t_S)$ & $1/(t_{WL}+t_{WH})$)[5]	58.8		50		41.6		33.3		MHz
f_{MAX5}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/(t_{CO})$, $1/(t_{WL}+t_{WH})$, $1/(t_S+t_H)$)[5]	111		100		83.3		62.5		MHz
$t_{OH} - t_{IH}$ 33x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns

Commercial AC Characteristics (continued)

Parameter	Description	7C335–100		7C335–83		7C335–66		7C335–50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Pipelined Mode Parameters										
t_{COS}	Input Clock to Output Clock	10		12		15		20		ns
f_{MAX6}	Maximum Frequency Pipelined Mode (Lowest of $1/(t_{COS})$, $1/(t_{CO})$, $1/(t_{WL} + t_{WH})$), $1/(t_{IS} + t_{IH})$[5]	100		83.3		66.6		50		MHz
f_{MAX7}	Maximum Frequency of (2) CY7C335s in Pipelined Mode (Lowest of $1/(t_{CO} + t_{IS})$ or $1/t_{COS}$)	90.9		83.3		66.6		50		MHz
Power-Up Reset Parameters										
t_{POR}	Power-Up Reset Time[5, 7]		1		1		1		1	µs

Military/Industrial AC Characteristics

Parameter	Description	7C335–83		7C335–66		7C335–50		7C335–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Combinatorial Mode Parameters										
t_{PD}	Input to Output Propagation Delay		20		20		25		30	ns
t_{EA}	Input to Output Enable		20		20		25		30	ns
t_{ER}	Input to Output Disable		20		20		25		30	ns
Input Registered Mode Parameters										
t_{WH}	Input and Output Clock Width HIGH[5]	5		6		8		10		ns
t_{WL}	Input and Output Clock Width LOW[5]	5		6		8		10		ns
t_{IS}	Input or Feedback Set-Up Time to Input Clock	3		3		3		4		ns
t_{IH}	Input Register Hold Time from Input Clock	3		3		3		4		ns
t_{ICO}	Input Register Clock to Output Delay		23		23		25		30	ns
t_{IOH}	Output Data Stable Time from Input Clock	3		3		3		3		ns
$t_{IOH} - t_{IH}$ 33x	Output Data Stable from Input Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
t_{PZX}	Pin 14 Enable to Output Enabled		15		15		20		30	ns
t_{PXZ}	Pin 14 Disable to Output Disabled		15		15		20		30	ns
f_{MAX1}	Maximum Frequency of (2) CY7C335s in Input Registered Mode (Lowest of $1/(t_{ICO} + t_{IS})$ & $1/(t_{WL} + t_{WH})$)[5]	38.4		38.4		35.7		29.4		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lowest of $(1/(t_{ICO})$, $1/(t_{WH} + t_{WL})$, $1/(t_{IS} + t_{IH}))$[5]	43.4		43.4		40		33.3		MHz
t_{ICEA}	Input Clock to Output Enabled		20		20		25		30	ns
t_{ICER}	Input Clock to Output Disabled		20		20		25		30	ns
Output Registered Mode Parameters										
t_{CEA}	Output Clock to Output Enabled [5]		20		20		25		30	ns
t_{CER}	Output Clock to Output Disabled [5]		20		20		25		30	ns
t_S	Output Register Input Set-Up Time to Output Clock	10		12		15		20		ns
t_H	Output Register Input Hold Time from Output Clock	0		0		0		0		ns
t_{CO}	Output Register Clock to Output Delay		11		12		15		20	ns
t_{CO2}	Output Register Clock or Latch Enable to Combinatorial Output Delay (Through Logic Array)[5]		22		23		30		35	ns

Notes:

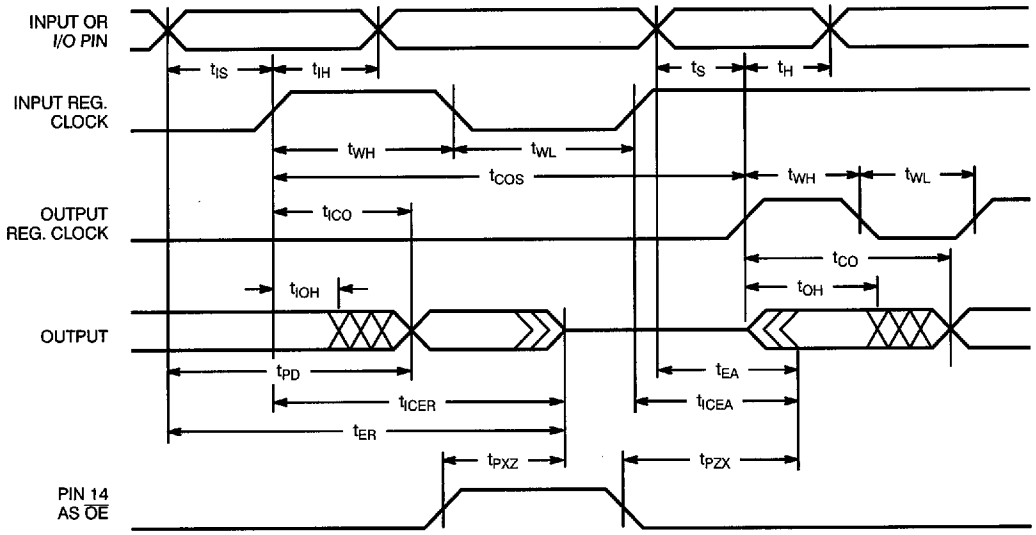
6. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C335. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.
7. This part has been designed with the capability to reset during system power-up. Following power-up, the input and output registers will be reset to a logic LOW state. The output state will depend on how the array is programmed.

Military/Industrial AC Characteristics (continued)

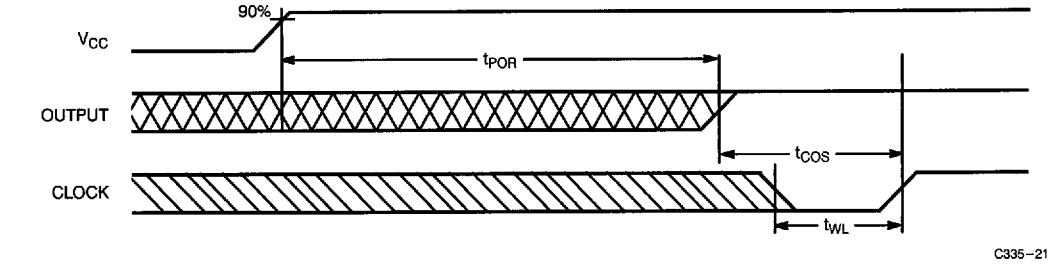
Parameter	Description	7C335–83		7C335–66		7C335–50		7C335–40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{OH}	Output Data Stable Time from Output Clock	2		2		2		2		ns
t_{OH2}	Output Data Stable Time From Output Clock (Through Memory Array)[5]	3		3		3		3		ns
$t_{OH2}-t_{IH}$	Output Data Clock Stable Time From Output Clock Minus Input Register Hold Time[5]	0		0		0		0		ns
f_{MAX3}	Maximum Frequency with Internal Feedback in Output Registered Mode[5]	83.3		66.6		50		40		MHz
f_{MAX4}	Maximum Frequency of (2) CY7C335s in Output Registered Mode (Lower of $1/(t_{CO}+t_S)$ & $1/(t_{WL}+t_{WH})$)[5]	47.6		41.6		33.3		25		MHz
f_{MAX5}	Maximum Frequency Data Path in Output Registered Mode (Lowest of $1/(t_{CO})$, $1/(t_{WL}+t_{WH})$, $1/(t_S+t_H)$)[5]	90.9		83.3		62.5		50		MHz
$t_{OH}-t_{IH}$ 33x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C330, 7C332, and 7C335[6]	0		0		0		0		ns
Pipelined Mode Parameters										
t_{COS}	Input Clock to Output Clock	12		15		20		25		ns
f_{MAX6}	Maximum Frequency Pipelined Mode (Lowest of $1/(t_{COS})$, $1/(t_{IS})$, or $1/(t_{CO})$), $1/(t_{IS}+t_{IH})$[5]	83.3		66.6		50		40		MHz
f_{MAX7}	Maximum Frequency of (2) CY7C335s in Pipelined Mode (Lowest of $1/(t_{CO}+t_{IS})$ or $1/t_{COS}$)	71.4		66.6		50		40		MHz
Power-Up Reset Parameters										
t_{POR}	Power-Up Reset Time[5, 7]		1		1		1		1	µs

2

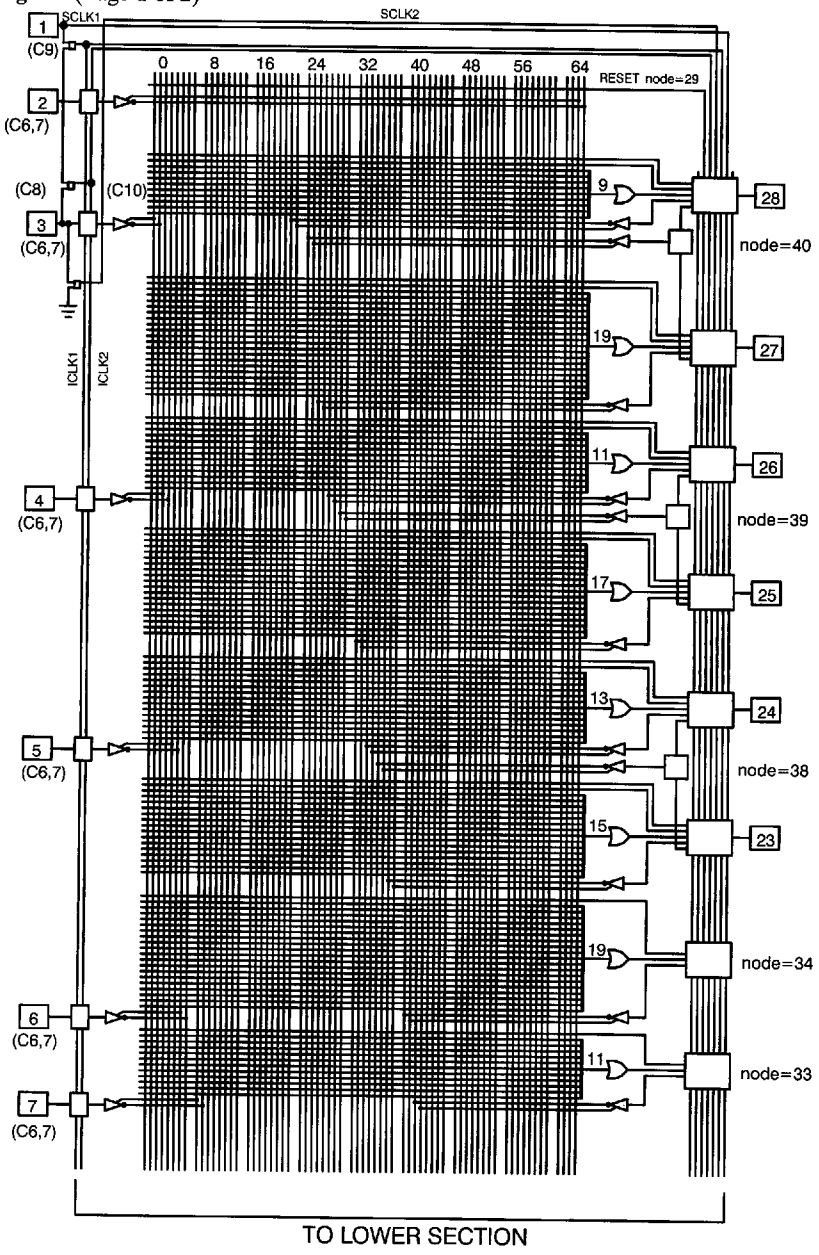
Switching Waveform



Power-Up Reset Waveform[7]



Block Diagram (Page 1 of 2)



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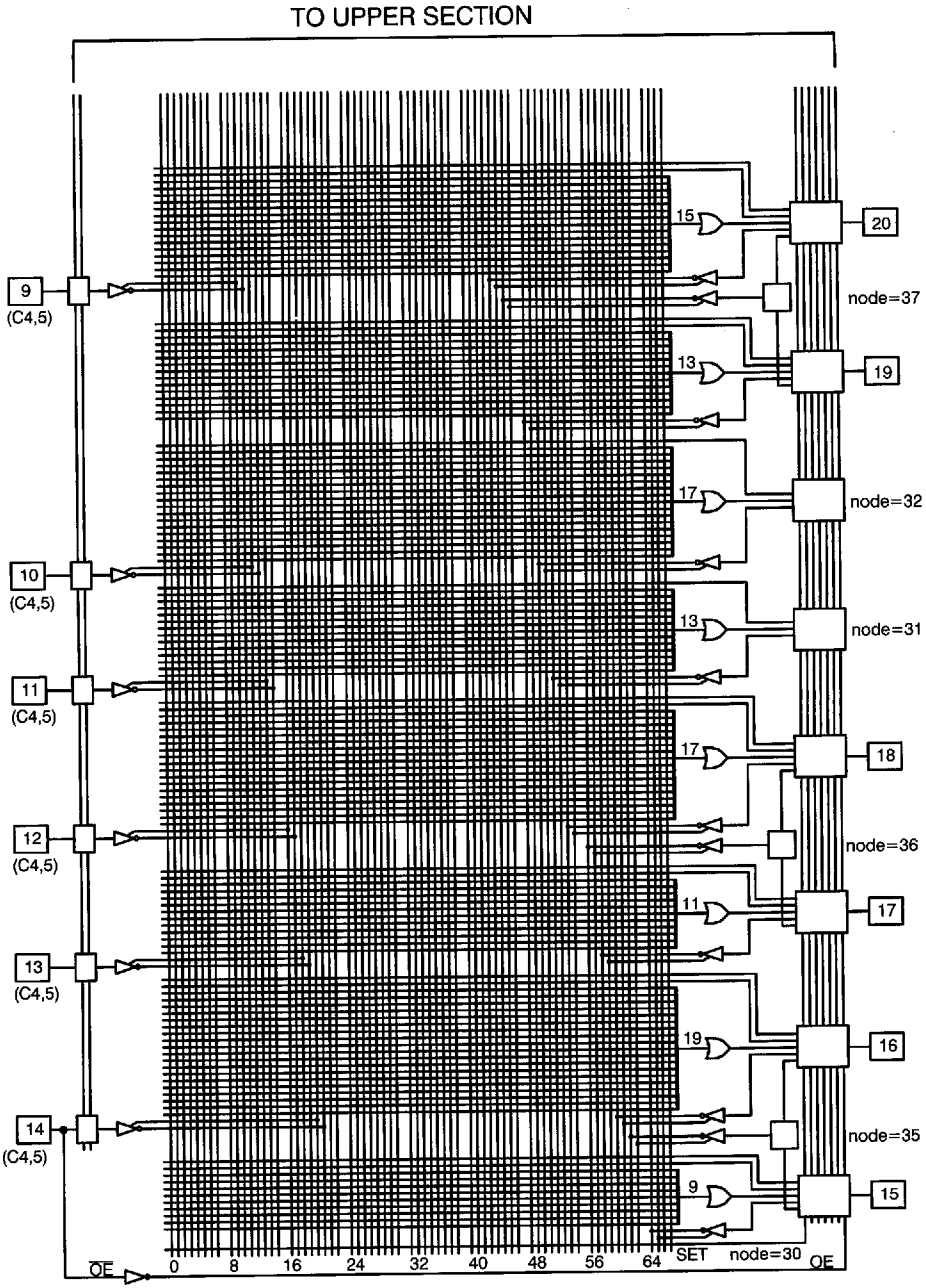
Block Diagram (Page 2 of 2)



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Ordering Information

f_{MAX} (MHz)	I_{CC1} (mA)	Ordering Code	Package Name	Package Type	Operating Range
100	140	CY7C335–100HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335–100JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335–100PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–100WC	W22	28-Lead (300-Mil) Windowed CerDIP	
83.3	160	CY7C335–83DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–83HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–83PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–83WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–83DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–83HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–83LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–83QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–83WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
83.3	140	CY7C335–83HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335–83JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335–83PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–83WC	W22	28-Lead (300-Mil) Windowed CerDIP	
66.6	160	CY7C335–66DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–66HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–66PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–66WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–66DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–66HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–66LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–66QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–66WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
66.6	140	CY7C335–66HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335–66JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335–66PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–66WC	W22	28-Lead (300-Mil) Windowed CerDIP	
50	140	CY7C335–50HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
		CY7C335–50JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C335–50PC	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–50WC	W22	28-Lead (300-Mil) Windowed CerDIP	

Ordering Information (continued)

f_{MAX} (MHz)	I_{CC1} (mA)	Ordering Code	Package Name	Package Type	Operating Range
50	160	CY7C335–50DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–50HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–50PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–50WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–50DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–50HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–50LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–50QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–50WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
40	160	CY7C335–40DI	D22	28-Lead (300-Mil) CerDIP	Industrial
		CY7C335–40HI	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–40PI	P21	28-Lead (300-Mil) Molded DIP	
		CY7C335–40WI	W22	28-Lead (300-Mil) Windowed CerDIP	
		CY7C335–40DMB	D22	28-Lead (300-Mil) CerDIP	Military
		CY7C335–40HMB	H64	28-Pin Windowed Leaded Chip Carrier	
		CY7C335–40LMB	L64	28-Square Leadless Chip Carrier	
		CY7C335–40QMB	Q64	28-Pin Windowed Leadless Chip Carrier	
		CY7C335–40WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{ICO}	9, 10, 11
t_{IS}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_H	9, 10, 11
t_{COS}	9, 10, 11

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