Am29BL162C Known Good Die

Data Sheet *(Retired Product)*

This product has been retired and is not recommended for designs. Please contact your Spansion representative for alternates. Availability of this document is retained for reference and historical purposes only.

The following document contains information on Spansion memory products.

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary.

For More Information

Please contact your local sales office for additional information about Spansion memory solutions.

Publication Number 23783 **Revision** A **Amendment** 5 **Issue Date** March 2, 2009

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SUPPLEMENT

Am29BL162C Known Good Die

16 Megabit (1 M x 16-Bit) CMOS 3.0 Volt-only, Burst-Mode, Boot Sector Flash Memory—Die Revision 1

This product has been retired and is not recommended for designs. Please contact your Spansion representative for alternates. Availability of this document is retained for reference and historical purposes only.

DISTINCTIVE CHARACTERISTICS

- **32 words sequential with wrap around (linear 32), bottom boot**
- **One 8 Kword, two 4 Kword, one 112 Kword, and seven 128 Kword sectors**
- **Single power supply operation**
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Read access times**

  22 ns burst access
  (at extended temperature range)

  80 ns initial/random access
- **Alterable burst length via BAA# pin**
- **Power dissipation (typical)**
  - — Burst Mode Read: 15 mA @ 25 MHz, 20 mA @ 33 MHz
  - — Program/Erase: 20 mA
  - — Standby mode, CMOS: 22 µA
- **5 V-tolerant data, address, and control signals**
- **Sector Protection**
  - — Implemented using in-system or via programming equipment
  - — Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
  - — Backward-compatible with AMD Am29LV and Am29F flash memories: powers up in asynchronous mode for system boot, but can immediately be placed into burst mode
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device for reading array data
- **Tested to datasheet specifications at temperature**
- **Quality and reliability levels equivalent to standard packaged components**

Publication# **23783** Rev: **A** Amendment/**5**
Issue Date: **March 2, 2009**

GENERAL DESCRIPTION

The Am29BL162C in Known Good Die (KGD) form is a 16 Mbit, 3.0 volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29BL162C Features

The Am29BL162C is organized as 1,048,576 words. It is designed to be programmed in-system with the standard system 3.0-volt V_{CC} supply. A 12.0-volt V_{PP} or 5.0 V_{CC} is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 80 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Burst Mode Features

The Am29BL162C offers a Linear Burst mode—a 32 word sequential burst with wrap around—in a bottom boot configuration only. This devices require additional control pins for **burst operations**: Load Burst Address (LBA#), Burst Address Advance (BAA#), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

AMD Flash Memory Features

Each device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. The I/O and control signals are 5V tolerant.

The Am29BL162C is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

Electrical Specifications

Refer to the Am29BL162C data sheet, publication number 22142, for full electrical specifications on the Am29BL162C in KGD form.

PRODUCT SELECTOR GUIDE

Family Part Number		**Am29BL162C**
Speed Option	Regulated Voltage Range: V_{CC} =3.0–3.6 V	**80R**
Max random/initial access time, ns (t_{ACC}, t_{IACC})		80
Max CE# access time, ns (t_{CE})		80
Max OE# and burst access time, ns (t_{OE}, t_{BACC})		22 (at 30 pF loading)

AC CHARACTERISTICS

Burst Mode Read

Parameter		Description		Speed Options and Temperature Ranges	
JEDEC	Std.			80R	Unit
	t_{IACC}	Initial Access Time LBA# Valid Clock to Output Delay (See Note)	Max	80	ns
	t_{BACC}	Burst Access Time BAA# Valid Clock to Output Delay	Max	24	ns
	t_{LBAS}	LBA# Setup Time	Min	6	ns
	t_{LBAH}	LBA# Hold Time	Min	2	ns
	t_{BAAS}	BAA# Setup Time	Min	6	ns
	t_{BAAH}	BAA# Hold Time	Min	2	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Max	4	ns
	t_{ACS}	Address Setup Time to CLK (See Note)	Min	6	ns
	t_{ACH}	Address Hold Time from CLK (See Note)	Min	2	ns
	t_{OE}	Output Enable to Output Valid	Max	24	ns
	t_{OEZ}	Output Enable to Output High Z	Max	25	ns
	t_{CEZ}	Chip Enable to Output High Z	Min	25	ns
	t_{CES}	CE# Setup Time to Clock	Min	6	ns

Note: *Initial valid data will be output after second clock rising edge of LBA# assertion.*

AC Characteristics

Erase/Program Operations

Parameter		Description		Speed Options	
JEDEC	Std			80R	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	80	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	3	sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50	µs
	t_{RB}	Recovery Time from RY/BY#	Min	0	ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Min	90	ns

Notes:

1. Not 100% tested.

AC CHARACTERISTICS

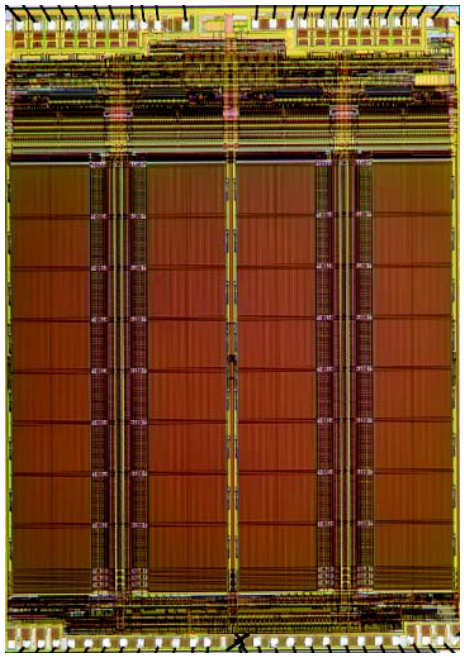
Alternate CE# Controlled Erase/Program Operations

Parameter		Description		Speed Options	
JEDEC	Std			80R	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	80	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30	ns
t_{WHWsH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	3	sec

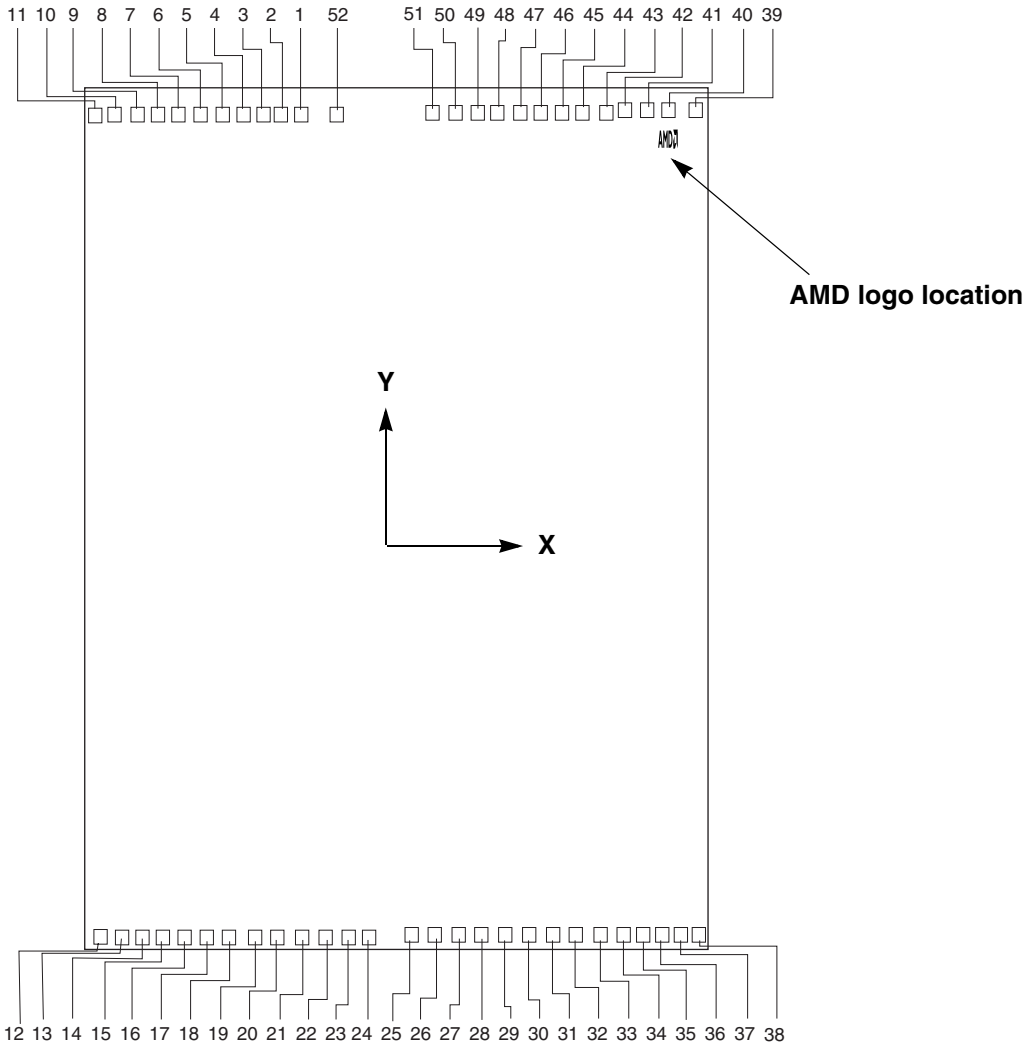
Notes:

1. Not 100% tested.

DIE PHOTOGRAPH



DIE PAD LOCATIONS



PAD DESCRIPTIONS (RELATIVE TO PAD 1)

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.00	0.00	0.00	0.00
2	V_{CC}	–8.15	0.00	–0.21	0.00
3	DQ4	–15.02	0.00	–0.38	0.00
4	DQ12	–24.66	0.00	–0.63	0.00
5	DQ5	–33.23	0.00	–0.84	0.00
6	DQ13	–42.87	0.00	–1.09	0.00
7	DQ6	–51.43	0.00	–1.31	0.00
8	DQ14	–61.08	0.00	–1.55	0.00
9	DQ7	–69.64	0.00	–1.77	0.00
10	DQ15	–79.28	0.00	–2.01	0.00
11	V_{SS}	–86.15	0.00	–2.19	0.00
12	N/C	–86.15	–282.09	–2.19	–7.16
13	A16	–77.53	–282.09	–1.97	–7.16
14	A15	–68.90	–282.09	–1.75	–7.16
15	A14	–60.28	–282.09	–1.53	–7.16
16	A13	–51.65	–282.09	–1.31	–7.16
17	A12	–41.60	–282.09	–1.06	–7.16
18	A11	–31.55	–282.09	–0.80	–7.16
19	A10	–21.50	–282.09	–0.55	–7.16
20	A9	–11.45	–282.09	–0.29	–7.16
21	A8	–1.16	–282.09	–0.03	–7.16
22	A19	8.89	–282.09	0.23	–7.16
23	V_{CC}	18.94	–282.09	0.48	–7.16
24	LBA	27.10	–282.09	0.69	–7.16
25	WE#	45.15	–282.09	1.15	–7.16
26	RESET#	55.45	–282.09	1.41	–7.16
27	RY/BY#	65.38	–282.09	1.66	–7.16
28	A18	75.43	–282.09	1.92	–7.16
29	A17	85.48	–282.09	2.17	–7.16
30	A7	95.53	–282.09	2.43	–7.16
31	A6	105.58	–282.09	2.68	–7.16
32	A5	115.63	–282.09	2.94	–7.16
33	A4	125.68	–282.09	3.19	–7.16
34	A3	135.73	–282.09	3.45	–7.16
35	A2	144.36	–282.09	3.67	–7.16
36	A1	152.98	–282.09	3.89	–7.16
37	A0	161.60	–282.09	4.10	–7.16
38	CE#	170.23	–282.09	4.32	–7.16
39	V_{SS}	170.23	0.00	4.32	0.00
40	OE#	156.98	0.00	3.99	0.00
41	DQ0	148.40	0.00	3.77	0.00
42	DQ8	138.76	0.00	3.52	0.00
43	DQ1	130.19	0.00	3.31	0.00
44	DQ9	120.55	0.00	3.06	0.00
45	DQ2	111.98	0.00	2.84	0.00
46	DQ10	102.34	0.00	2.60	0.00
47	DQ3	93.78	0.00	2.38	0.00

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
48	DQ11	84.13	0.00	2.14	0.00
49	V_{SS}	76.52	0.00	1.94	0.00
50	CLK	66.47	0.00	1.69	0.00
51	BAA	56.42	0.00	1.43	0.00
52	IND#	16.28	0.00	0.41	0.00

Note: *The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.*

PAD DESCRIPTIONS (RELATIVE TO DIE CENTER)

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	–42.04	139.03	–1.07	3.53
2	V_{CC}	–50.19	139.03	–1.27	3.53
3	DQ4	–57.06	139.03	–1.45	3.53
4	DQ12	–66.70	139.03	–1.69	3.53
5	DQ5	–75.27	139.03	–1.91	3.53
6	DQ13	–84.91	139.03	–2.16	3.53
7	DQ6	–93.47	139.03	–2.37	3.53
8	DQ14	–103.12	139.03	–2.62	3.53
9	DQ7	–111.68	139.03	–2.84	3.53
10	DQ15	–121.32	139.03	–3.08	3.53
11	V_{SS}	–128.19	139.03	–3.26	3.53
12	NC	–128.19	–143.06	–3.26	–3.63
13	A16	–119.57	–143.06	–3.04	–3.63
14	A15	–110.94	–143.06	–2.82	–3.63
15	A14	–102.32	–143.06	–2.60	–3.63
16	A13	–93.69	–143.06	–2.38	–3.63
17	A12	–83.64	–143.06	–2.12	–3.63
18	A11	–73.59	–143.06	–1.87	–3.63
19	A10	–63.54	–143.06	–1.61	–3.63
20	A9	–53.49	–143.06	–1.36	–3.63
21	A8	–43.20	–143.06	–1.10	–3.63
22	A19	–33.15	–143.06	–0.84	–3.63
23	V_{CC}	–23.10	–143.06	–0.59	–3.63
24	LBA	–14.94	–143.06	–0.38	–3.63
25	WE#	3.11	–143.06	0.08	–3.63
26	RESET#	13.41	–143.06	0.34	–3.63
27	RY/BY#	23.34	–143.06	0.59	–3.63
28	A18	33.39	–143.06	0.85	–3.63
29	A17	43.44	–143.06	1.10	–3.63
30	A7	53.49	–143.06	1.36	–3.63
31	A6	63.54	–143.06	1.61	–3.63
32	A5	73.59	–143.06	1.87	–3.63
33	A4	83.64	–143.06	2.12	–3.63
34	A3	93.69	–143.06	2.38	–3.63
35	A2	102.32	–143.06	2.60	–3.63
36	A1	110.94	–143.06	2.82	–3.63
37	A0	119.57	–143.06	3.04	–3.63
38	CE#	128.19	–143.06	3.26	–3.63
39	V_{SS}	128.19	139.03	3.26	3.53
40	OE#	114.94	139.03	2.92	3.53
41	DQ0	106.36	139.03	2.70	3.53
42	DQ8	96.72	139.03	2.46	3.53
43	DQ1	88.15	139.03	2.24	3.53
44	DQ9	78.51	139.03	1.99	3.53
45	DQ2	69.94	139.03	1.78	3.53
46	DQ10	60.30	139.03	1.53	3.53
47	DQ3	51.74	139.03	1.31	3.53

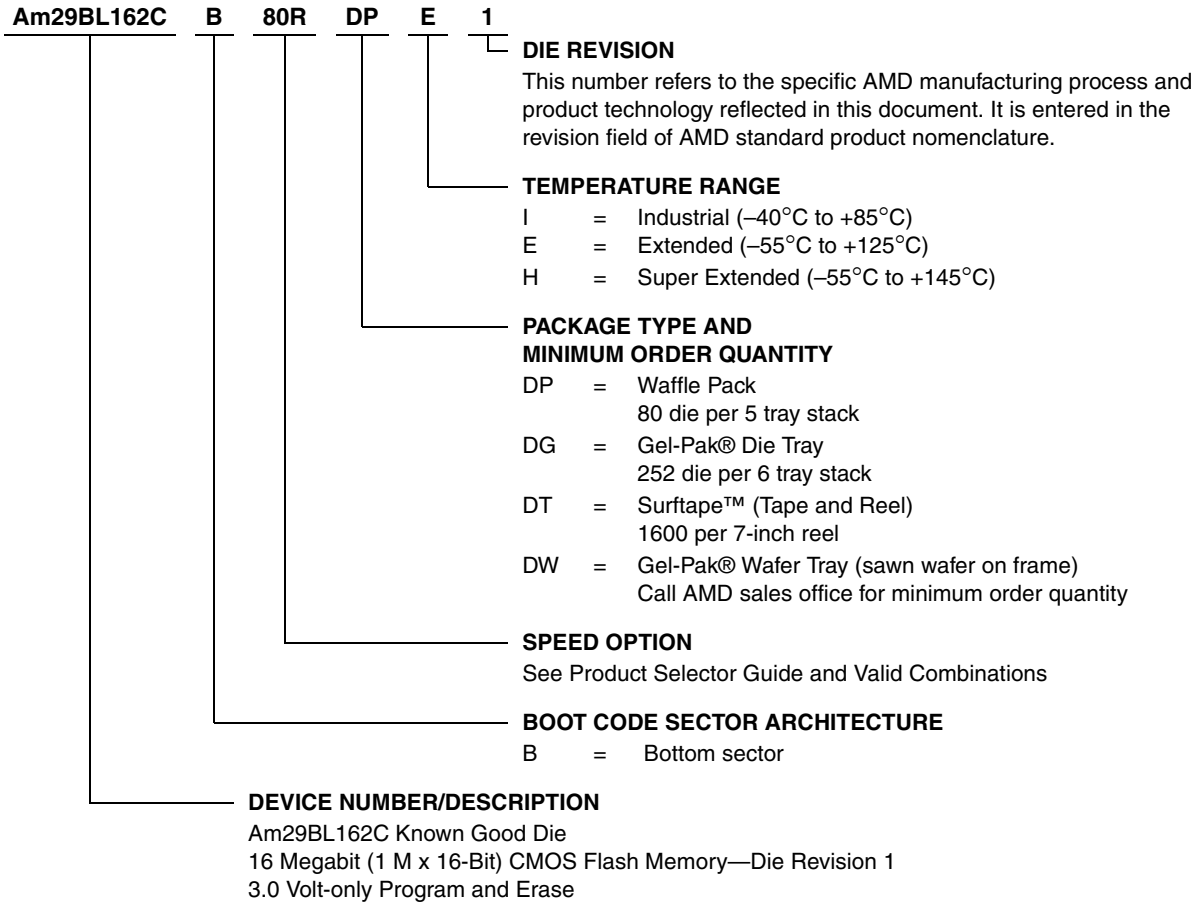
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
48	DQ11	42.10	139.03	1.07	3.53
49	V_{SS}	34.48	139.03	0.88	3.53
50	CLK	24.43	139.03	0.62	3.53
51	BAA	14.38	139.03	0.37	3.53
52	IND#	–25.76	139.03	–0.65	3.53

Note: *The coordinates above are relative to the die center and can be used to operate wire bonding equipment.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



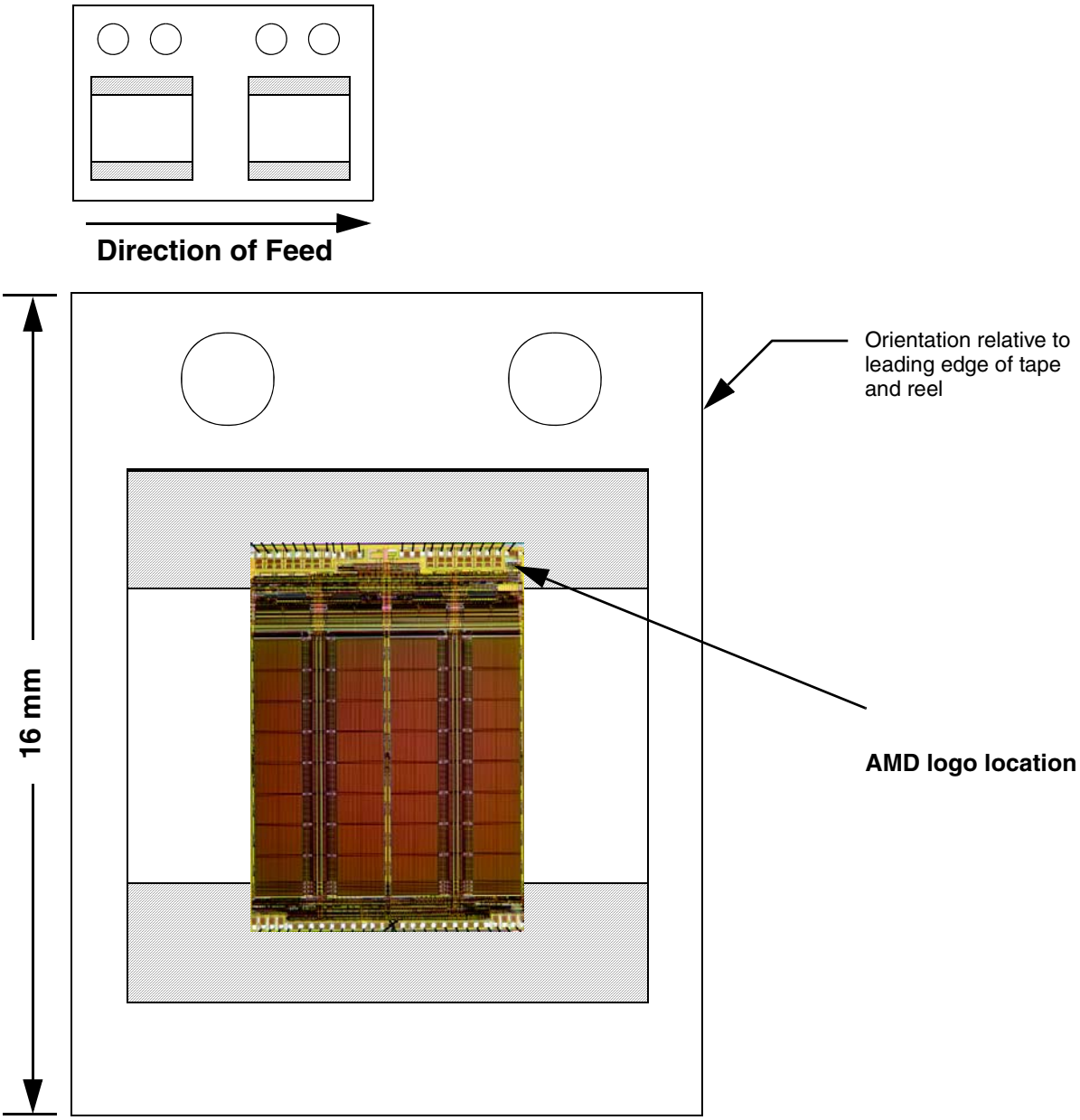
Valid Combinations	
Am29BL162CB-80R	DPI 1, DPE 1, DPH 1 DGI 1, DGE 1, DGH 1 DTI 1, DTE 1, DTH 1 DWI 1, DWE 1, DWH 1

Valid Combinations

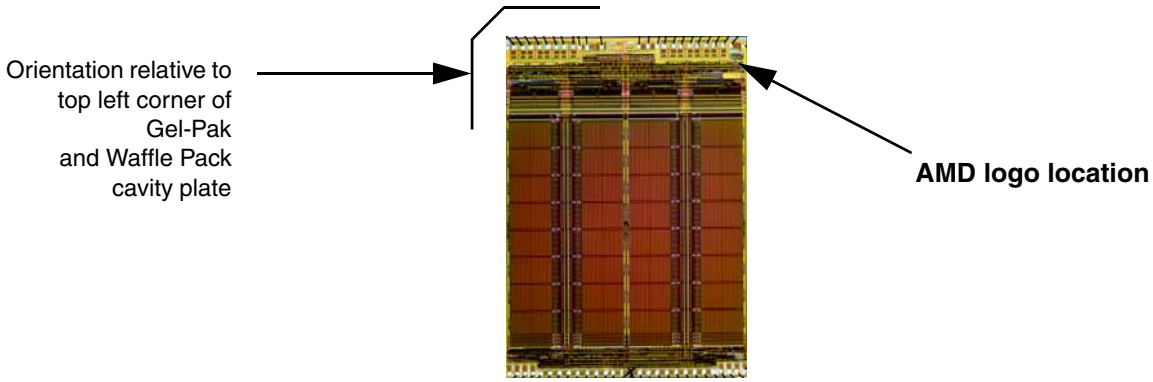
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PACKAGING INFORMATION

Surftape Packaging



Gel-Pak and Waffle Pack Packaging



PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29BL162C product qualification database. AMD implements quality assurance procedures throughout the product test flow. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in. In addition, an off-line qualification maintenance program (QMP) guarantees AMD standards are met on KGD products.

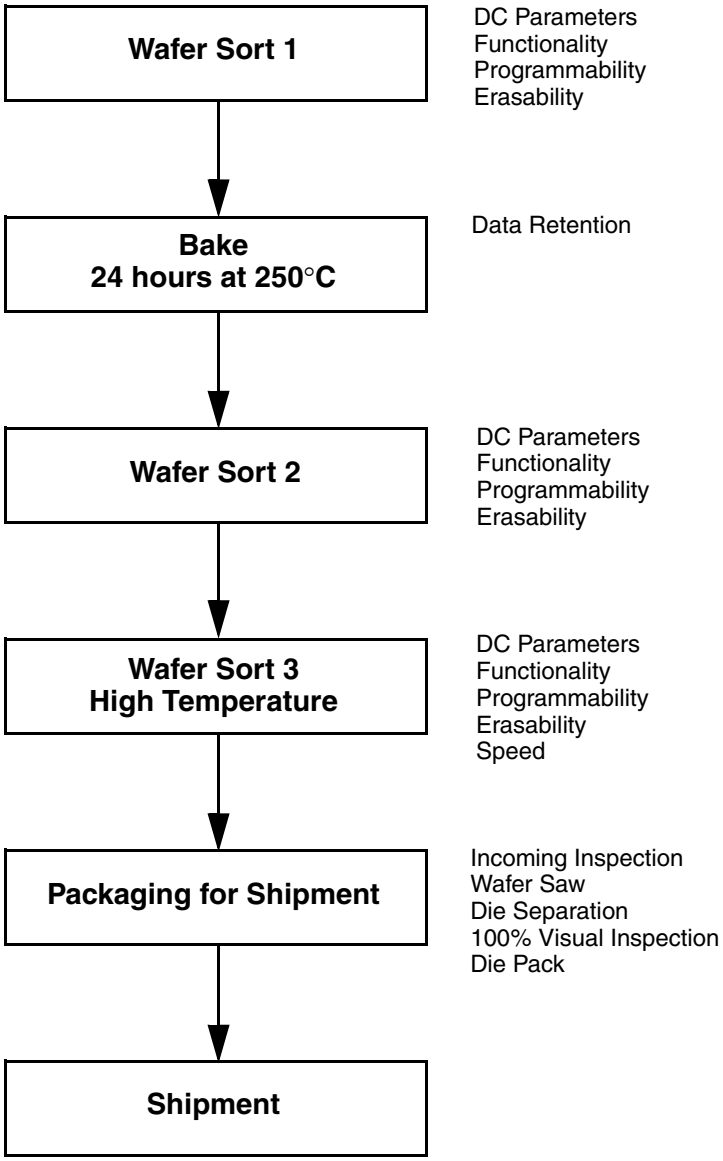


Figure 1. AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

Die dimensions . . . . . 269.7 mils x 303.94 mils
. . . . . 6.85 mm x 7.72 mm

Die Thickness. . . . . .500 µm

Bond Pad Size . . . . . .4.69 mils x 4.69mils
. . . . . 115.9 µm x 115.9 µm

Pad Area Free of Passivation . . . . . .13.99 $mils^2$
. . . . . 9,025 μm^2

Pads Per Die 51

Bond Pad Metalization . . . . . Al/Cu

Die Backside . . . . . .No metal, may be grounded (optional)

Passivation. . . . . Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . . .3.0 V to 3.6 V

Operating Temperature

Industrial . . . . . –40°C to +85°C
Extended . . . . . –55°C to +125°C
Super Extended. . . . . –55°C to +145°C

MANUFACTURING INFORMATION

Manufacturing . . . . . .FASL

Wafer Sort Test . . . . . Sunnyvale, CA, USA &
. . . . . Penang, Malaysia

Manufacturing ID (Bottom Boot) 98849ABK

Preparation for Shipment . . . . . Penang, Malaysia

Fabrication Process CS39LS

Die Revision 1

SPECIAL HANDLING INSTRUCTIONS

Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

DC PARAMETER EXCEPTIONS

The following specifications replace those given in the Am29BL162 data sheet (publication number 22142):

Parameter	Description	Test Conditions		Typ	Max	Unit
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, RESET# = V_{CC}±0.3 V		22	35	µA
I_{CC4}	V_{CC} Standby Current During Reset (Note 2)	RESET# = V_{SS} ± 0.3 V		22	35	µA
I_{CC5}	Automatic Sleep Mode (Notes 2, 3)	V_{IH} = V_{CC} ± 0.3 V; V_{IL} = V_{SS} ± 0.3 V	OE# = V_{IH}	30	50	µA
			OE# = V_{IL}	30	50	µA

Notes:

2. *Maximum I_{CC} specifications are tested with V_{CC} = V_{CC}max.*
3. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*

AC CHARACTERISTICS

Read Operations

Parameter		Description		Test Setup		Speed Options and Temperature Ranges	Unit
JEDEC	Std.					80R	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	80	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$CE\# = V_{IL}$ $OE\# = V_{IL}$	Max	80	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$OE\# = V_{IL}$	Max	80	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	24	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	24	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	25	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0	ns
			Toggle and Data# Polling		Min	10	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0	ns

Notes:

1. *Not 100% tested.*
2. *See Figure 13 and Table 10 for test specifications*

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to unpackaged die under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

AMD warrants unpackaged die of its manufacture ("Known Good Die" or "Die") against defective materials or workmanship for a period of one (1) year from date of shipment. This warranty does not extend beyond the first purchaser of said Die. Buyer assumes full responsibility to ensure compliance with the appropriate handling, assembly and processing of Known Good Die (including but not limited to proper Die preparation, Die attach, wire bonding and related assembly and test activities), and compliance with all guidelines set forth in AMD's specifications for Known Good Die, and AMD assumes no responsibility for environmental effects on Known Good Die or for any activity of Buyer or a third party that damages the Die due to improper use, abuse, negligence, improper installation, accident, loss, damage in transit, or unauthorized repair or alteration by a person or entity other than AMD ("Warranty Exclusions").

The liability of AMD under this warranty is limited, at AMD's option, solely to repair the Die, to send replacement Die, or to make an appropriate credit adjustment or refund in an amount not to exceed the original purchase price actually paid for the Die returned to AMD, provided that: (a) AMD is promptly notified by Buyer in writing during the applicable warranty period of any defect or nonconformity in the Known Good Die; (b) Buyer obtains authorization from AMD to return the defective Die; (c) the defective Die is returned to AMD by Buyer in accordance with AMD's shipping instructions set forth below; and (d) Buyer shows to AMD's satisfaction that such alleged defect or nonconformity actually exists and was not caused by any of the above-referenced Warranty Exclusions. Buyer shall ship such defective Die to AMD via AMD's carrier, collect. Risk of loss will transfer to AMD when the defective Die is provided to AMD's carrier. If Buyer fails to adhere to these warranty returns guidelines, Buyer shall assume all risk of loss and shall pay for all freight to AMD's specified location. The aforementioned provisions do not extend the original warranty period of any Known Good Die that has either been repaired or replaced by AMD.

WITHOUT LIMITING THE FOREGOING, EXCEPT TO THE EXTENT THAT AMD EXPRESSLY WARRANTS TO BUYER IN A SEPARATE AGREEMENT SIGNED BY AMD, AMD MAKES NO WARRANTY WITH RESPECT TO THE DIE'S PROCESSING OF DATE DATA, AND SHALL HAVE NO LIABILITY FOR DAMAGES OF ANY KIND, UNDER EQUITY, LAW, OR ANY OTHER THEORY, DUE TO THE FAILURE OF SUCH KNOWN GOOD DIE TO PROCESS ANY PARTICULAR DATA CONTAINING DATES, INCLUDING DATES IN AND AFTER THE YEAR 2000, WHETHER OR NOT AMD RECEIVED NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

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Buyer agrees that it will make no warranty representations to its customers which exceed those given by AMD to Buyer unless and until Buyer shall agree to indemnify AMD in writing for any claims which exceed AMD's warranty.

Known Good Die are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of the Die can reasonably be expected to result in a personal injury. Buyer's use of Known Good Die for use in life support applications is at Buyer's own risk and Buyer agrees to fully indemnify AMD for any damages resulting in such use or sale.

REVISION SUMMARY

Revision A (June 7, 2000)

Initial release.

Revision A+1 (December 19, 2000)

Corrected reference to BL162C data sheet publication number.

Ordering Information

Added quantities for Waffle Pack, Gel-Pak, and Surftape.

Revision A+2 (September 11, 2002)

Moved Pad 11 on Die Pad Locations Diagram

Added Pad 52 to Pad Description Tables (Relative to Pad 1 and Relative to Die Center)

Revision A+3 (September 13, 2002)

Changed title from Boot Sector Flash to Burst-mode, Boot Sector Flash.

Product Selector Guide

Removed Note #2.

AC Characteristics

Added Read Operations, Burst Mode Read, and Erase/Program Operations and Alternate CE# Controlled Erase/Program Operations Tables.

Revision A + 4 (April 29, 2003)

Product Test Flow

Replaced text preceding Figure 1.

Erase/Program Operations Tables.

Revision A + 4 (March 2, 2009)

Global

Added obsolescence information.

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