DATA SHEET

Am79C875

NetPHY™ 4LP Low Power Quad 10/100-TX/FX Ethernet Transceiver

DISTINCTIVE CHARACTERISTICS

- Four 10/100BASE-TX Ethernet PHY transceivers
- Supports RMII (Reduced MII) interface
- 125 meter (m) MLT-3 and Baseline Wander operation
- Low power consumption
  - 1.3 Watt (W) typical (1:1 magnetics)
  - 1.2 W typical (1.25:1 magnetics)
- Power management modes:
  - Selectable 1:1 or 1.25:1 transmit transformer
  - Unplugged - approximately 100 mW per port
  - Power Down - approximately 3 mW per port
- Single 3.3 V power supply with 5 V I/O tolerance
- Patent-pending DC restoration technique reduces baseline wander susceptibility
- Full and half-duplex operation with full-featured Auto-Negotiation function
- Next Page register support
- Automatic Polarity Detection during Auto-Negotiation and 10BASE-T signal reception
- Unique scramble seed per port reduces EMI in switch and repeater applications
- One port supports 100BASE-FX function
- Supports Inter Packet Gap as low as 40 ns for high throughput applications
- No external filters or chokes required
- Compliant with IEEE 802.3 standards for 100BASE-TX, 100BASE-FX, and 10BASE-T
- Built-in loopback and test modes
- Small 14 x 20 mm 100-pin PQR package
- Small package allows side-by-side PHY layout
  - Fits neatly behind quad magnetics
  - Saves board space over larger 208 PQFP packages
- Support for Industrial Temperature (-40°C to +85°C)

GENERAL DESCRIPTION

The NetPHY™ 4LP device is a highly integrated, low power 10BASE-T/100BASE-TX/FX Quad Ethernet transceiver. The NetPHY™ 4LP device includes integrated RMII, ENDECs, Scrambler/Descrambler, and full-featured Auto-Negotiation with support for Parallel Detection and Next Page. Port 3 can be configured as a 100BASE-FX transmitter to output an NRZI PECL level signal. Each receiver has an adaptive equalizer/DC restoration circuit for accurate clock/data recovery on the 100BASE-TX signal at different cable lengths and can perform to 125 m and beyond.

The NetPHY™ 4LP device operates on a 3.3 V supply and offers 5 V I/O tolerance for mixed signal designs. Power consumption is 1.3 W typical for the device, or 0.3 W per port using 1:1 magnetics. The NetPHY™ 4LP device can use 1.25:1 magnetics, which decreases transmit power consumption and reduces device power consumption to 1.2 W typical.

The NetPHY™ 4LP device offers an optimized pinout for network applications. RMII pins can be routed directly to the MAC and TX/RX media pins are routed directly to the magnetics. Direct routing of high speed traces is imperative for project system design and EMI noise reduction.

The NetPHY™ 4LP device's on-chip input filtering and output waveshaping eliminates the need of external hybrid filters for media connection. Integrated LED logic allows three LEDs per port to be driven directly. These features greatly simplify the design of a 100BASE-X repeater/switch board, thus requiring minimum external components.

For ease of system and chip setup and testing, the NetPHY™ 4LP device offers loopback and various advanced testing and monitoring capabilities.

The NetPHY™ 4LP device is available in the Commercial (0°C to 70°C) or Industrial (-40°C to +85°C) temperature ranges. The Industrial temperature range is well suited to environment such as enclosures with restricted air flow or outdoor equipment.

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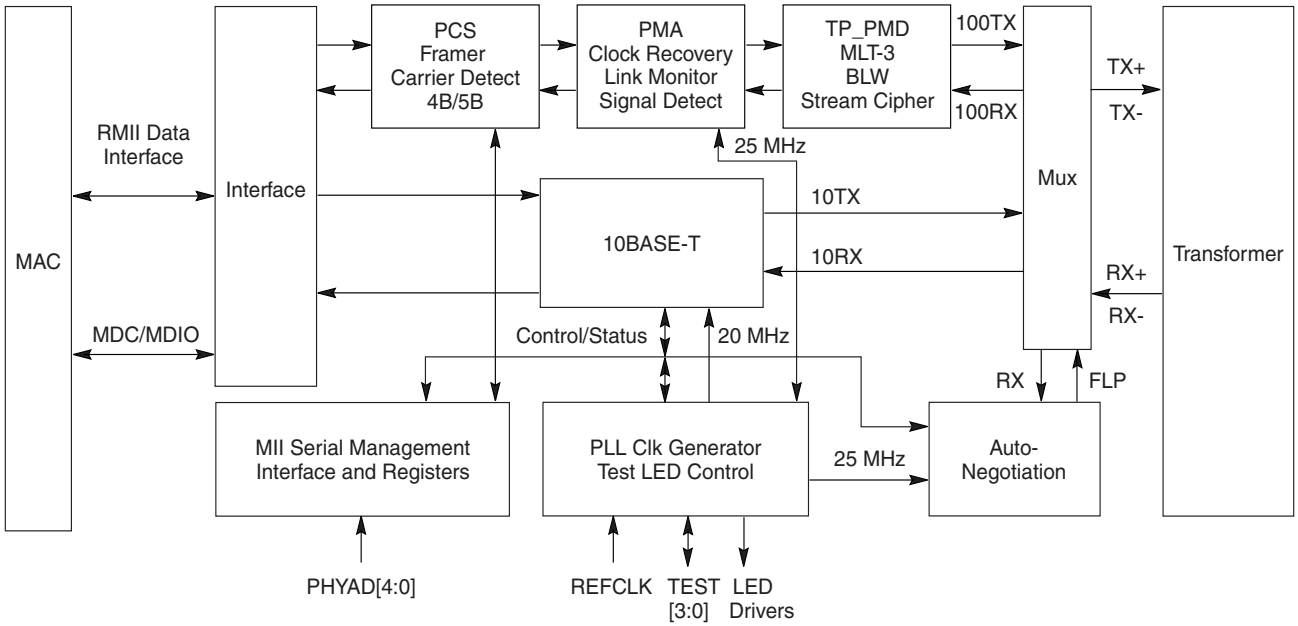
BLOCK DIAGRAM (PER PORT)



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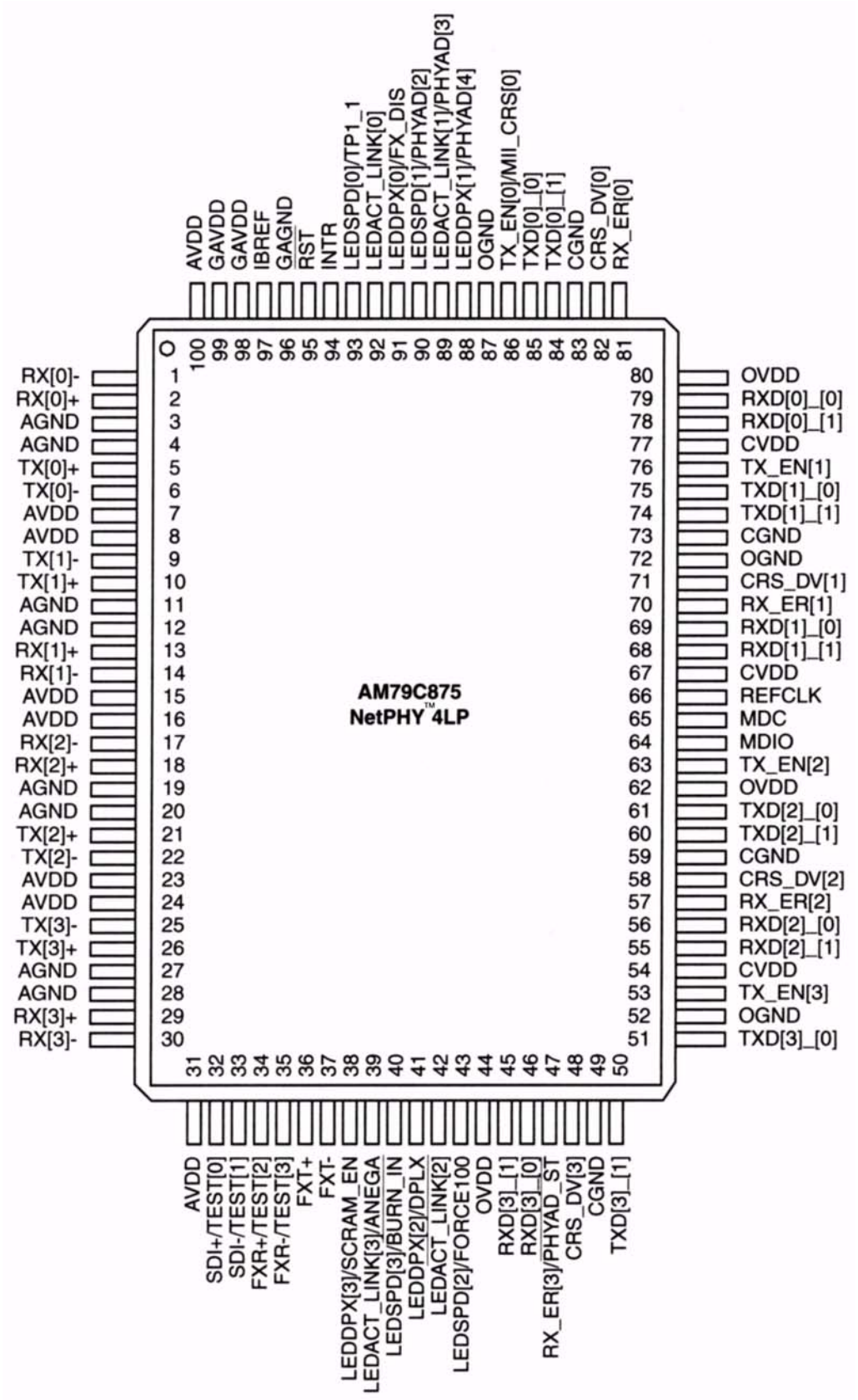
CONNECTION DIAGRAM



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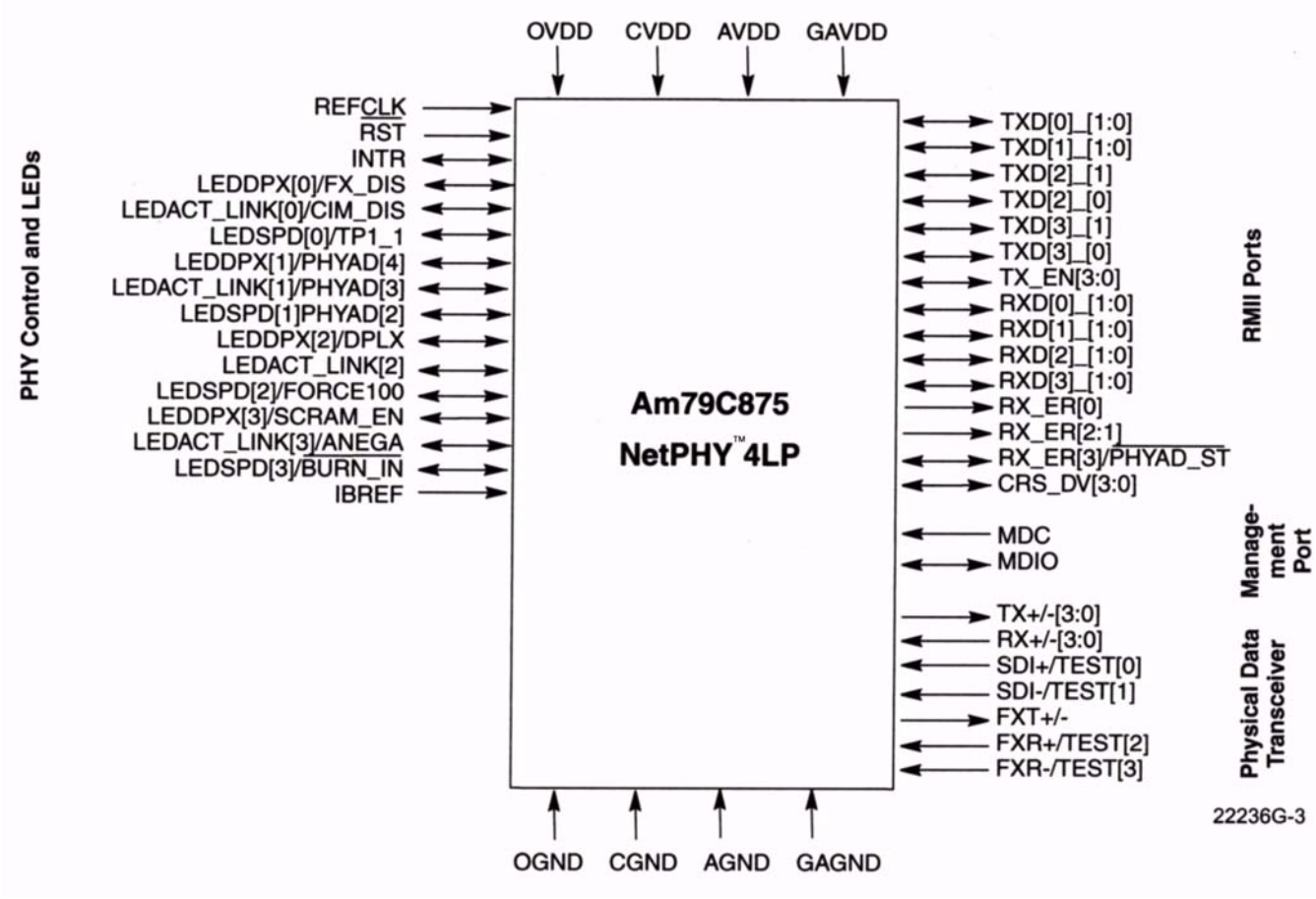
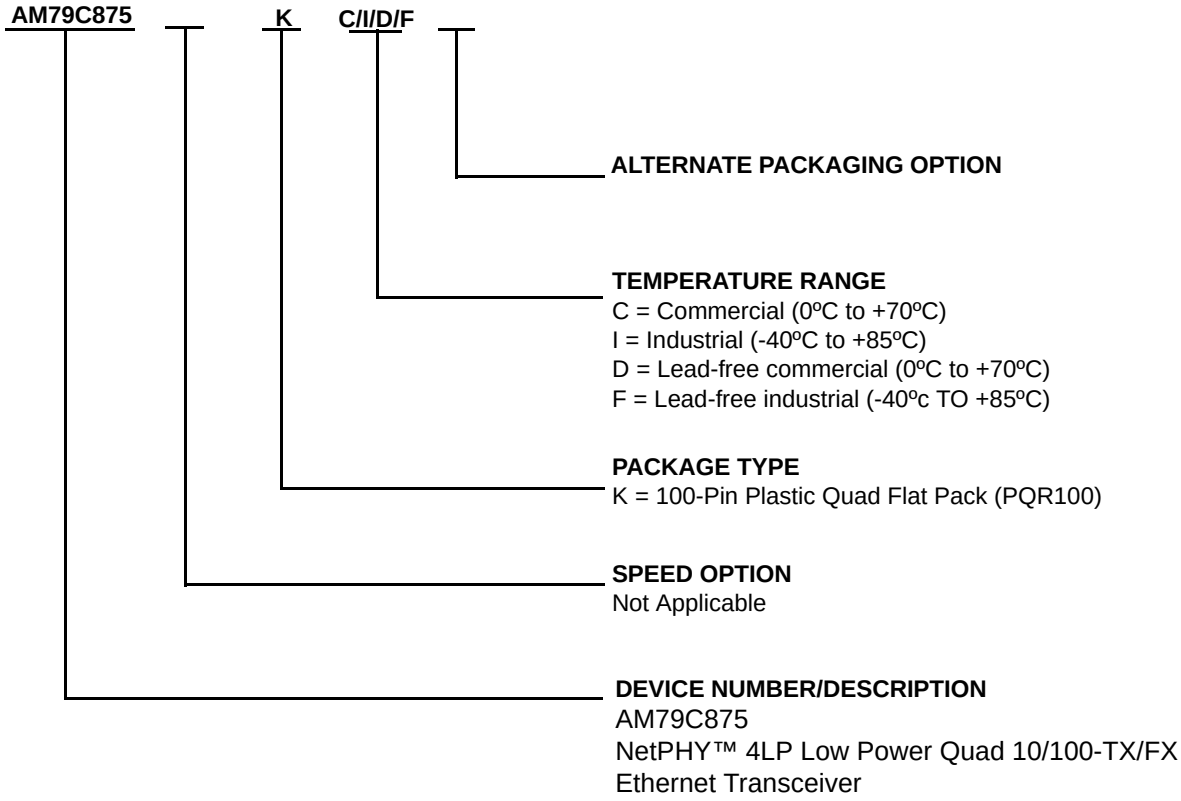
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM79C875	KC
AM79C875	KI
AM79C875	KD
AM79C875	KF

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

RELATED AMD PRODUCTS

Part No.	Description
Integrated Controllers	
Am97C973B/975B	PCnet-FAST™ III Single-Chip 10/100 Mbps PCI Ethernet Controller with Integrated PHY
Am79C976	PCnet-PRO™ 10/100 Mbps PCI Ethernet Controller
Am79C978A	PCnet-Home™ Single-Chip 1/10 Mbps PCI Home Networking Controller
Physical Layer Devices (Single-Port)	
Am79C874	NetPHY™ 1LP Low Power 10/100-TX/FX Ethernet Transceiver
Am79C901A	HomePHY™ Single-Chip 1/10 Mbps Home Networking PHY

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PIN DESIGNATIONS

Listed by Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	RX[0]-	26	TX[3]+	51	TXD[3]_[0]	76	TX_EN[1]
2	RX[0]+	27	AGND	52	OGND	77	CVDD
3	AGND	28	AGND	53	TX_EN[3]	78	RXD[0]_[1]
4	AGND	29	RX[3]+	54	CVDD	79	RXD[0]_[0]
5	TX[0]+	30	RX[3]-	55	RXD[2]_[1]	80	OVDD
6	TX[0]-	31	AVDD	56	RXD[2]_[0]	81	RX_ER[0]
7	AVDD	32	SDI+/TEST[0]	57	RX_ER[2]	82	CRS_DV[0]/
8	AVDD	33	SDI-/TEST[1]	58	CRS_DV[2]	83	CGND
9	TX[1]-	34	FXR+/TEST[2]	59	CGND	84	TXD[0]_[1]
10	TX[1]+	35	FXR-/TEST[3]	60	TXD[2]_[1]	85	TXD[0]_[0]
11	AGND	36	FXT+	61	TXD[2]_[0]	86	TX_EN[0]
12	AGND	37	FXT-	62	OVDD	87	OGND
13	RX[1]+	38	LEDDPX[3]/ SCRAM_EN	63	TX_EN[2]	88	LEDDPX[1]/ PHYAD[4]
14	RX[1]-	39	LEDACT_LINK[3]/ ANEGA	64	MDIO	89	LEDACT_LINK[1]/ PHYAD[3]
15	AVDD	40	LEDSPD[3]/ BURN_IN	65	MDC	90	LEDSPD[1]/ PHYAD[2]
16	AVDD	41	LEDDPX[2]/DPLX	66	REFCLK	91	LEDDPX[0]/FX_DIS
17	RX[2]-	42	LEDACT_LINK[2]	67	CVDD	92	LEDACT_LINK[0]
18	RX[2]+	43	LEDSPD[2]/ FORCE100	68	RXD[1]_[1]	93	LEDSPD[0]/TP1_1
19	AGND	44	OVDD	69	RXD[1]_[0]	94	INTR
20	AGND	45	RXD[3]_[1]	70	RX_ER[1]	95	$\overline{\text{RST}}$
21	TX[2]+	46	RXD[3]_[0]	71	CRS_DV[1]	96	GAGND
22	TX[2]-	47	RX_ER[3]/ PHYAD_ST	72	OGND	97	IBREF
23	AVDD	48	CRS_DV[3]	73	CGND	98	GAVDD
24	AVDD	49	CGND	74	TXD[1]_[1]	99	GAVDD
25	TX[3]-	50	TXD[3]_[1]	75	TXD[1]_[0]	100	AVDD

PIN DESCRIPTIONS

Media Connections

TX[3:0]±
Transmit Output **Output**

The TX[3:0]± pins are the differential transmit output pairs. The TX[3:0]± pins transmit 10BASE-T or MLT-3 signals depending on the state of the link of the port.

RX[3:0]±
Receive Input **Input**

The RX[3:0]± pins are the differential receive input pairs. The RX[3:0]± pins can receive 10BASE-T or MLT-3 signals depending on the state of the link of the port.

100BASE-FX Function/Test

SDI+/TEST[0]
Signal Detect Input+
(For Port 3 only) **Analog Input/Output**

This pin indicates signal quality status on the fiber-optic link in 100BASE-FX mode. When the signal quality is good, the SDI+ pin should be driven high relative to the SDI- pin. 100BASE-FX is disabled when both pins are simultaneously pulled low. SDI- can also be used for Signal Detect Common Mode Voltage input.

When in test mode, SDI+, SDI-, FXR+, and FXR- pins are used as TEST[3:0].

SDI-/TEST[1]
Signal Detect Input-
(For Port 3 only) **Analog Input/Output**

This pin indicates signal quality status on the fiber-optic link in 100BASE-FX mode. When the signal quality is good, the SDI+ pin should be driven high relative to the SDI- pin. 100BASE-FX is disabled when both pins are simultaneously pulled low. SDI- can also be used for Signal Detect Common Mode Voltage input.

When in test mode, SDI+, SDI-, FXR+, and FXR- pins are used as TEST[3:0].

FXR+/TEST[2]
Fiber Receive Input
(For Port 3 only) **Analog Input/Output**

When Port 3 is configured as FX Channel, FXR± are ECL level FX receive pins.

When in test mode, SDI±, and FXR± pins are used as TEST[3:0].

FXR-/TEST[3]
Fiber Receive Input
(For Port 3 only) **Analog Input/Output**

When Port 3 is configured as FX Channel, FXR± are ECL level FX receive pins.

When in test mode, SDI+, SDI-, FXR+, FXR- pins are used as TEST[3:0].

FXT±
Fiber Transmit Output
(For Port 3 only) **Analog Output**

When Port 3 is configured as FX Channel, FXT± are ECL level FX transmit pins.

Clock

REFCLK
Reference Clock Input Signal **Input**

The REFCLK pin is the reference clock input. The REFCLK signal must be a 50-MHz signal.

RMII Signals

TXD[3:0]_[1:0]
RMII TXD for Ports 0 to 3 **Input**

These pins are the transmit data input to the RMII of Ports 0:3.

TX_EN[3:0]
RMII Transmit Enable **Input**

These pins are the transmit enable inputs to the RMII.

RXD[3:0]_[1:0]
RMII Receive Data for Ports 0 to 3 **Output**

These pins are the receive data for Port 0:3.

RX_ER[2:0]
RMII Receive Error for Ports 0 to 2 **Output**

These pins indicate receive errors for the corresponding port. The pin goes HIGH whenever the corresponding receiver detects a symbol error.

RX_ER[3]/$\overline{\text{PHYAD\_ST}}$
RMII Receive Error for Port 3 **Input/Output**
PHY Address Shift

This pin indicates receive errors for Port 3. It goes HIGH when the corresponding receiver detects a symbol error.

At power up, this pin is used to set the PHY address by increasing it by 1. If it is HIGH at power up, the PHYAD of each port is the upper-3 bits and the port number for the lower-2 bits. If it is LOW, the PHYAD is incremented by 1. For example, if the pin is HIGH at power-up and the upper-3 bits are set to 000, the PHYAD of each port (in binary notation) is 00000, 00001, 00010, 00011 respectively. If the pin is LOW at power-up and the upper-3 bits are set to 000, the PHYAD of each port is 00001, 00010, 00011, and 00100, respectively. This allows a method of avoiding setting an address to 00000, which could cause problems with some MACs.

CRS_DV[3:0]
Carrier Sense/Data Valid
Input/Output, Pull-Down

The CRS_DV pin is asserted high when media is non-idle.

MDIO
Management Data I/O **Input/Output, Pull-Down**

This pin is a bidirectional data interface used by the MAC to access management register within the NetPHY™ 4LP device. This pin has an internal pull-down, therefore, it requires an external pull-up resistor (1.5 KΩ) as specified in IEEE-802.3 section 22.

MDC
Management Data Clock **Input, Pull-Down**

This pin is the serial management clock which is used to clock MDIO data to the MAC.

$\overline{\text{RST}}$
Reset **Input, Pull-Up**

An active low input will force the NetPHY™ 4LP device to a known reset state. Reset also can be done through the internal power-on-reset or MII Register 0, bit 15.

INTR
Interrupt **Tri-State**

This pin is true whenever the NetPHY™ 4LP device detects an event flagged as an interrupt. Events to be flagged are programmed in Register 17. Interrupts are cleared on Read. The polarity of INTR (active HIGH or active LOW) is set by Register 16, bit 14. The default is active LOW, which requires a 10 KΩ pull-up resistor.

LED Port

Note: *Consult the LED Port Configuration section for appropriate pull-up and pull-down resistors.*

LEDDPX[0]/FX_DIS
Port [0] Duplex LED **Input/Output, Pull-Up**

Low LED indicates full-duplex and high indicates half-duplex.

FX Mode: Pulled low at reset will put Port 3 in 100BASE-FX mode.

LEDACT_LINK[0]
Port [0] Transmit/Receive Activity LED
Output, Pull-Up

LED is output low for approximately 30 ms each time there is activity. LINK is an active low signal. This signal should have a 1k–4.7KΩ pull-up resistor.

LEDSPD[0]/TP1_1
Port [0] Speed LED **Input/Output, Pull-Up**

LED is output low when operating in 100BASE-X modes and high when operating in 10BASE-T modes.

TP1_1: Pulled low at reset will select transmit transformer ratio to be 1.25:1. Default is 1:1 transformer.

LEDDPX[1]/PHYAD[4]
Port [1] Duplex LED **Input/Output, Pull-Up**

LED low indicates full-duplex and high indicates half-duplex.

PHY Address[4]. This is the first address bit received in the management frame, and one of three MSBs for MII management PHY address. The two LSBs, PHYAD [1:0] are internally wired to four ports: PHYAD [11]=Port3,..., PHYAD [00] = Port0. The PHYAD will also determine the scramble seed, this will help to reduce EMI when there are multiple ports switching at the same time. To set this pin, use pull-up or pull-down resistors in the range of 1 KΩ to 4.7 KΩ.

LEDACT_LINK[1]/PHYAD[3]
Port [1] Transmit/Receive Activity LED
Input/Output, Pull-Up

LED is output low for approximately 30 ms each time there is activity. LINK is an active low signal.

PHY Address[3]. This is the second MSB and one of three MSB's for MII management PHY address. To set this pin, use pull-up or pull-down resistors in the range of 1 KΩ to 4.7 KΩ.

LEDSPD[1]/PHYAD[2]
Port [1] Speed LED **Input/Output, Pull-Up**

LED is output low when operating in 100BASE-X modes and high when operating in 10BASE-T modes.

PHY Address[2]. This is the third MSB and one of three MSB's for MII management PHY address. To set this pin, use pull-up or pull-down resistors in the range of 1 KΩ to 4.7 KΩ.

LEDDPX[2]/DPLX
Port [2] Duplex LED **Input/Output, Pull-Up**

LED low indicates full-duplex and high indicates half-duplex.

DPLX: Full Duplex Mode Enable. This pin is logically OR'ed with a full-duplex enable MII control bit to generate an internal full-duplex enable signal. When asserted high, the NetPHY™ 4LP device operates in full-duplex mode as determined through Auto-Negotiation or software setting. When asserted low, the internal control bit (Register 0, bit 8) will determine the full-duplex operating mode.

LEDACT_LINK[2]
Port [2] Transmit/Receive Activity LED
Output, Pull-Up

LED is output low for approximately 30 ms each time there is activity. LINK is an active low signal. This signal should have a 1k–4.7KΩ pull-up.

LEDSPD[2]/FORCE100
Port [2] Speed LED **Input/Output, Pull-Up**

LED is output low when operating in 100BASE-X modes and high when operating in 10BASE-T modes.

FORCE100: Force 100BASE-X Operation. When this signal is pulled high and ANEGA is low at reset, all ports will be forced to 100BASE-TX operation. When asserted low and ANEGA is low, all ports are forced to

10BASE-T operation. When ANEGA is high, FORCE100 has no effect on operation.

LEDDPX[3]/SCRAM_EN
Port [3] Duplex LED **Input/Output, Pull-Up**

LED low indicates full-duplex and high indicates half-duplex.

SCRAM_EN. Scrambler Enable. Pulled low at reset will bypass the scrambler. Default is scrambler enabled. This signal should have a 1k–4.7KΩ pull-up resistor.

LEDACT_LINK[3]/ANEGA
Port [3] Transmit/Receive Activity LED

Input/Output, Pull-Up

LED is low for approximately 30 ms each time there is activity. LINK is an active low signal.

ANEGA: Auto-Negotiation Ability. Asserted high means Auto-Negotiation enable while low means manual selection through DPLX, FORCE100. This pin also is reflected as ANEGA bit, MII Status Register 1, bit 3.

LEDSPD[3]/$\overline{\text{BURN\_IN}}$
Port [3] Speed LED **Input/Output, Pull-Up**

LED is low when operating in 100BASE-X modes and high when operating in 10BASE-T modes.

$\overline{\text{BURN\_IN}}$: Burn-In mode. Burn-in mode for reliability assurance control. This signal should have a 1k–4.7KΩ pull-up resistor.

Bias

IBREF
Reference Bias Resistor **Analog**

To be tied to an external 10-KΩ (1%) resistor which should be connected to the analog ground at the other end.

Power and Ground

OVDD
Power **Digital**

These pins are the digital +3.3 V power supply for I/O.

OGND
Ground **Digital**

These pins are the digital ground for I/O.

CVDD
Power **Digital**

These pins are the digital +3.3 V power supply for the Core logic.

CGND
Ground **Digital**

These pins are the digital ground for Core logic.

AVDD
Power **Analog**

These pins are the +3.3V power supply for analog circuit.

AGND
Ground **Analog**

These pins are the ground for analog circuit.

GAVDD
Power **Analog**

These pins are the +3.3 V power supply for common analog circuits.

GAGND
Ground **Analog**

This pin is the ground for common analog circuits.

FUNCTIONAL DESCRIPTION

Overview

The NetPHY™ 4LP transceiver is a four-port CMOS device that implements the complete physical layer for 10BASE-T and the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) functionality for 100BASE-TX. The NetPHY™ 4LP transceiver implements Auto-Negotiation allowing two devices connected across a link segment to take maximum advantage of their capabilities. Auto-Negotiation is performed as defined in the IEEE 802.3u specification.

The NetPHY™ 4LP device communicates with a switch or MAC device through the Reduced Media Independent Interface (RMII).

The NetPHY™ 4LP device consists of the following functional blocks:

- RMII Functional Blocks
- 100BASE-X Block including:
  - Transmit and Receive State Machines
  - 4B/5B Encoder and Decoder
  - Stream Cipher Scrambler and Descrambler
  - Link Monitor State Machine
  - Far End Fault Indication (FEFI) State Machine
  - MLT-3 Encoder
  - MLT-3 Decoder with adaptive equalization
- 10BASE-T Block including:
  - Manchester Encoder/Decoder
  - Jabber
  - Receive Polarity Detect
  - Waveshaping and Filtering
- Carrier Integrity Monitor
- Auto-Negotiation
- Status LEDs
- PHY Control and Management

Modes of Operation

The RMII interface provides the data path connection between the NetPHY™ 4LP transceivers and the Media Access Controller (MAC), repeater, or switch devices. The MDC and MDIO pins are responsible for communication between the NetPHY™ 4LP transceiver and the station management entity (STA).

The RMII standard reduces the pin count by halving the number of data pins, eliminating pins not used in switch applications, and using a single global clock. Each port has an independent RMII.

RMII uses seven pins per port. They are as follows:

Receive Data	RXD[X]_[1:0]
Carrier Sense	CRS_DV[X]
Receive Error	RX_ER[X]
Transmit Data	TXD[X]_[1:0]
Transmit Enable	TX_EN[X]

Note: *[X] refers to the port.*

In RMII mode, REF_CLK must be sourced by a 50-MHz clock signal.

RMII Pin Descriptions

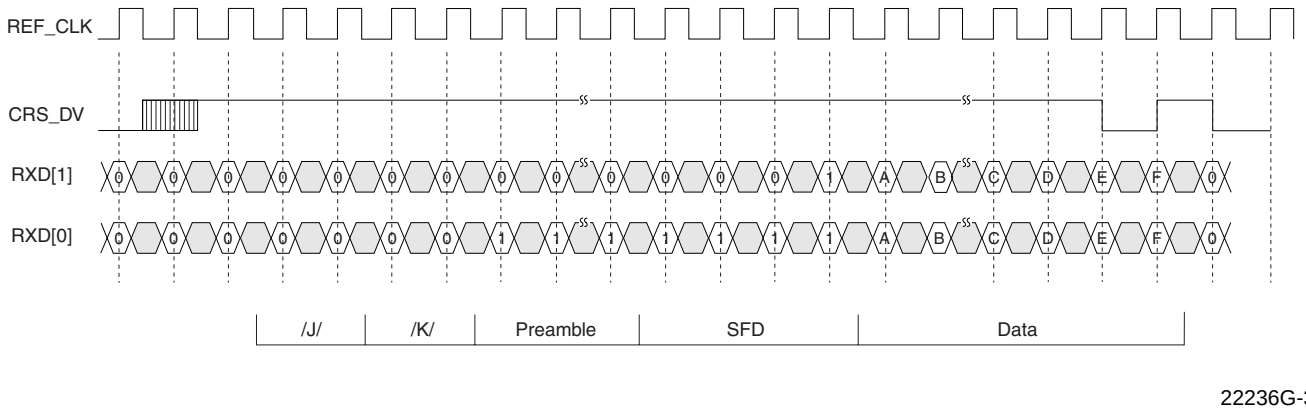
CRS_DV
Carrier Sense/Receive Data Valid

CRS_DV is asserted by the PHY when the receive medium is non-idle. Loss of carrier results in the deassertion of CRS_DV synchronous to the cycle of REF_CLK, which presents the first di-bit of a nibble onto RXD[1:0] (i.e., CRS_DV is deasserted only on nibble boundaries). If the PHY has additional bits to be presented on RXD[1:0] following the initial deassertion of CRS_DV, the PHY asserts CRS_DV on cycles of REF_CLK which present the second di-bit of each nibble. The PHY deasserts CRS_DV on cycles of REF_CLK which present the first di-bit of the nibble. As a result, starting on the byte boundaries, CRS_DV toggles at 25 MHz in 100 Mbps mode and 2.5 MHz in 10 Mbps mode when CRS ends before RX_DV (i.e., the FIFO still has bits to transfer when the carrier event ends). Therefore, the MAC can accurately recover RX_DV and CRS. Refer to Figure 1.

During a false carrier event, CRS_DV remains asserted for the duration of carrier activity. Refer to Figure 2.

The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is “00” until proper receive signal decoding takes place.

Note: *CRS_DV is asserted asynchronously in order to minimize latency of control signals through the PHY.*



Note: *CRS_DV may toggle at 25 MHz starting on a nibble boundary if bits accumulate due to the difference between CRS and RX_DV. The example waveform shows a single nibble accumulated in the FIFO.*

Figure 1. 100 Mbps Reception with No Errors

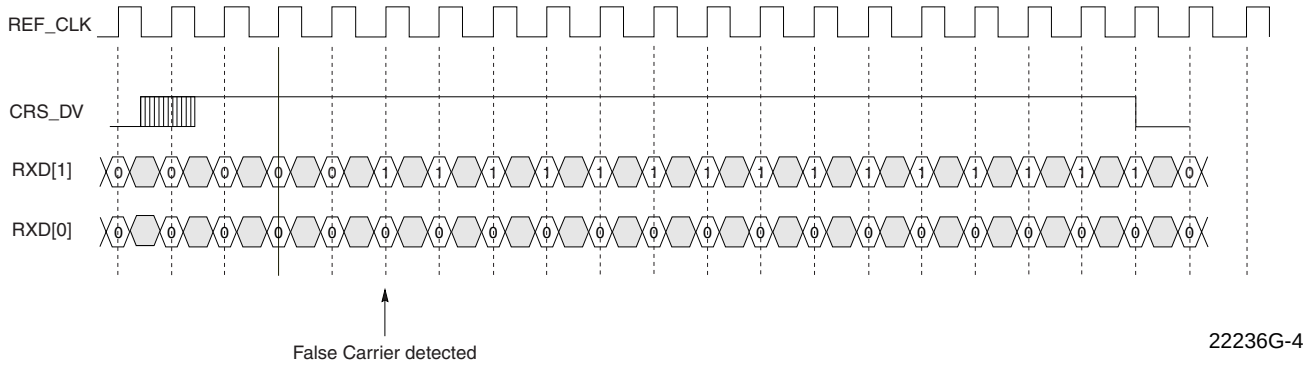


Figure 2. 100 Mbps Reception with False Carrier

RXD[1:0]
Receive Data [1:0]

RXD[1:0] transitions synchronously to REF_CLK. Upon assertion of CRS_DV, the PHY will ensure that RXD[1:0] = 00 until proper receive decoding takes place. Then for each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.

RXD[1:0] in 100 Mbps Mode

For normal reception following assertion of CRS_DV, RXD[1:0] is “00” until the receiver has determined that the receive event has a proper Start of Stream Delimiter (SSD), which is a /J/K/ pair. Thereafter, preamble will appear (RXD[1:0] = 01). Data capture by MACs occur following detection of SFD.

If False Carrier is detected (an event starting with anything other than /J/K/), then RXD[1:0] is”10” until the end of the receive event. This is a unique pattern since False Carrier can only occur at the beginning of a packet where a preamble will be decoded (i.e., RXD[1:0]=01).

RXD[1:0] in 10 Mbps Mode

Following assertion of CRS_DV, RXD[1:0] shall be “00” until the 10BASE-T PHY has recovered clock and is able to decode the receive data. Once valid receive data is available from the 10BASE-T PHY, RXD[1:0] takes on the recovered data values (i.e., starting with “01” for preamble).

At a REF_CLK frequency of 50 MHz, the value on RXD[1:0] is valid such that RXD[1:0] may be sampled every tenth cycle, regardless of the starting cycle within the group and yield the correct frame data.

TXD[1:0]
Transmit Data

TXD[1:0] transitions synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] is accepted for transmission by the PHY. TXD[1:0] is ignored by the PHY while TX_EN is deasserted.

TXD[1:0] in 100 Mbps Mode

TXD[1:0] provides valid data for each REF_CLK period while TX_EN is asserted. Refer to Figure 3.

TXD[1:0] in 10 Mbps Mode

As the REF_CLK frequency is ten times the data rate in 10 Mbps mode, the value on TXD[1:0] is valid such that TXD[1:0] may be sampled every tenth cycle, regardless of the starting cycle within the group and yield the correct frame data.

Bit Ordering

Transmission and reception of each octet is done a di-bit at a time with the order of di-bit transmission and reception as shown in Figure 4.

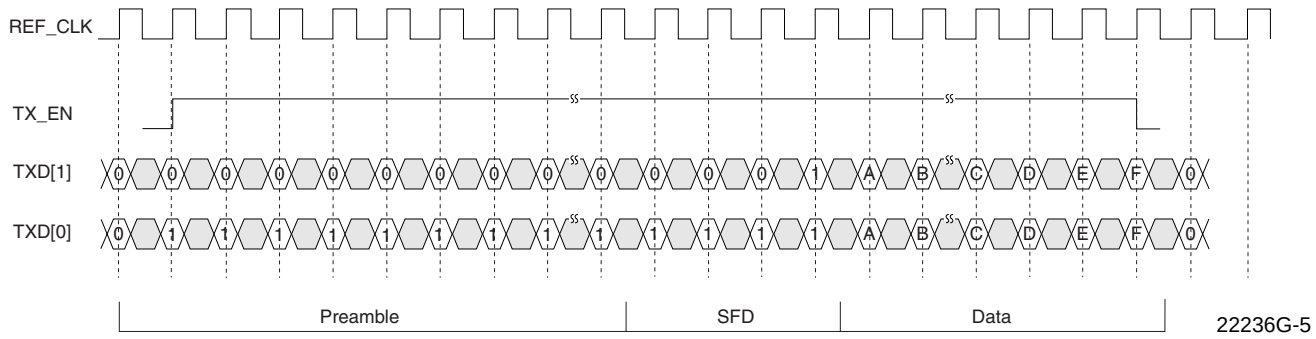


Figure 3. 100 Mbps Transmission

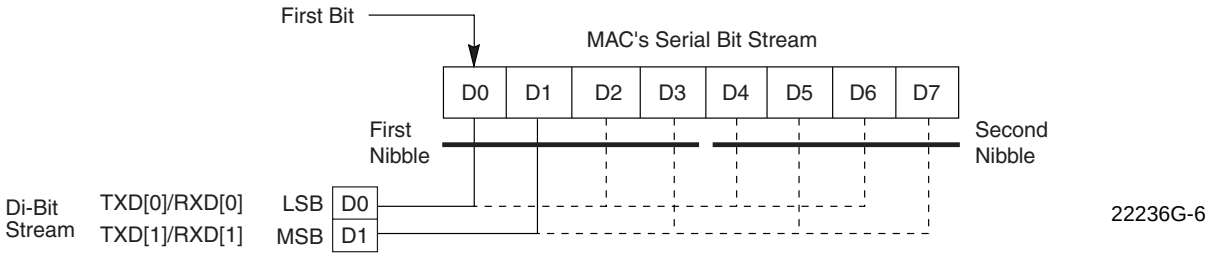


Figure 4. Bit Ordering

100BASE-X Block

The functions performed by the device include encoding of MII 4-bit data (4B/5B), decoding of received code groups (5B/4B), generating carrier sense and collision detect indications, serialization of code groups for transmission, de-serialization of serial data from reception, mapping of transmit, receive, and carrier sense at the RMII interface, and recovery of clock from the incoming data stream. It offers stream cipher scrambling and descrambling capability for 100BASE-TX applications.

In the transmit data path for 100 Mbps, the NetPHY™ 4LP transceiver receives 2-bit wide data across the RMII at 50 million di-bits per second. For 100BASE-TX applications, it encodes and scrambles the data, serializes it, and transmits an MLT-3 data stream to the media via an isolation transformer. For 100BASE-FX applications, it encodes and serializes the data and transmits a Pseudo-ECL (PECL) data stream to the fiber optic transmitter.

The NetPHY™ 4LP transceiver receives an MLT-3 data stream from the network for 100BASE-TX. It then recovers the clock from the data stream, de-serializes the data stream, and descrambles/decodes the data stream (5B/4B) before presenting it at the RMII interface.

For 100BASE-FX operation, the NetPHY™ 4LP receives a PECL data stream from the fiber optic transceiver and decodes that data stream. 100BASE-FX operation is possible only on Port 3.

Within the NetPHY™ 4LP device, this block is replicated for each port. The RMII signals should be taken in context with the port being referred.

The 100BASE-X block consists of the following sub-blocks:

- Transmit Process
- Receive Process
- Internal Loopback Paths
- 4B/5B Encoder and Decoder
- Scrambler/Descrambler
- Link Monitor
- Far End Fault Generation and Detection & Code-Group Generator
- MLT-3 encoder/decoder with Adaptive Equalization
- Serializer/Deserializer and Clock Recovery
- Baseline Restoration

Transmit Process

The transmit process generates code-groups based on the transmit control and data signals on the RMII. This process is also responsible for frame encapsulation into a Physical Layer Stream, generating the collision signal based on whether a carrier is received simultaneously with transmission and generating the Carrier Sense CRS signal at the RMII. The transmit process is implemented in compliance with the transmit state diagram as defined in Clause 24 of the IEEE 802.3u specification.

Receive Process

The receive process passes to the RMII a sequence of data derived from the incoming code-groups. Each code-group is comprised of five code-bits. This process detects channel activity and then aligns the incoming code bits in code-group boundaries for subsequent data decoding. The receive process is responsible for code-group alignment and also generates the Carrier Sense (CRS) signal at the RMII. The receive process is implemented in compliance with the receive state diagram as defined in Clause 24 of the IEEE 802.3u specification. The False Carrier Indication as specified in the standard is also generated by this block, and communicated to the Reconciliation layer through RXD and RX_ER.

Encoder/Decoder

The 100 Mbps process in the NetPHY™ 4LP device uses the 4B/5B encoding scheme as defined in IEEE 802.3, Section 24. This scheme converts between raw data on the RMII and encoded data on the media pins. The encoder converts raw data to the 4B/5B code. It also inserts the stream boundary delimiters (/J/K/ and /T/R/) at the beginning and end of the data stream as appropriate. The decoder converts between encoded data on the media pins and raw data on the RMII. It also detects the stream boundary delimiters to help determine the start and end of packets.

The code-group mapping is defined in Table 1.

Scrambler/Descrambler

The 4B/5B encoded data has repetitive patterns which result in peaks in the RF spectrum large enough to keep the system from meeting the standards set by regulatory agencies such as the FCC. The peaks in the radiated signal are reduced significantly by scrambling the transmitted signal. Scramblers add the output of a random generator to the data signal. The resulting signal has fewer repetitive data patterns.

After reset, the scrambler seed in each port will be set to the PHY address value to help improve the EMI performance of the device.

The scrambled data stream is descrambled, at the receiver, by adding it to the output of another random generator. The receiver's random generator has the same function as the transmitter's random generator.

The scrambler/descrambler configuration is set by the SCRAM_EN pin and the EN_SCRM bit (Register 24, bit 2). The SCRAM_EN pin is latched at the rising edge of the $\overline{\text{RST}}$ signal. The scrambler/descrambler can be enabled if SCRAM_EN latches above 2.0 V. Otherwise, they are all disabled. The EN_SCRM bit sets the scrambler/descrambler configuration for the corresponding port. The bit defaults to 1 at reset.

The scrambler/descrambler can only be enabled when the port is in the 100-Mbps MLT-3 mode. The scrambler is disabled on any port that has a link at 10 Mbps or any port that is forced to 10 Mbps.

Link Monitor

Signal levels are qualified using squelch detect circuits. A signal detect (SD) circuit following the equalizer is asserted high whenever the peak detector detects a post-equalized signal with peak-to-ground voltage level larger than 400 mV, which is about 40% of the normal signal voltage level, and the energy level is sustained longer than 2 ~ 3 ms. It is deasserted approximately 1 ms to 2 ms after the energy level detected in the receiving lines is consistently less than 300 mV peak. The signal is forced to low during a local loopback operation (Register 0, bit 14 Loopback is asserted) and forced to high when a remote Loopback is taking place (Register 24, bit 3 EN_RPBK is set).

In 100BASE-TX mode, when no signal or invalid signals are detected on the receive pair, the link monitor will enter in the "link fail" state where only link pulses will be transmitted. Otherwise, when a valid signal is detected for a minimum period of time, the link monitor will then enter link pass state which transmit and receive functions will be entered.

Table 1. Code-Group Mapping

MII (TXD[3:0])	Name	PCS Code-Group	Interpretation
0 0 0 0	0	1 1 1 1 0	Data 0
0 0 0 1	1	0 1 0 0 1	Data 1
0 0 1 0	2	1 0 1 0 0	Data 2
0 0 1 1	3	1 0 1 0 1	Data 3
0 1 0 0	4	0 1 0 1 0	Data 4
0 1 0 1	5	0 1 0 1 1	Data 5
0 1 10	6	0 1 1 1 0	Data 6
0 1 1 1	7	0 1 1 1 1	Data 7
1 0 0 0	8	1 0 0 1 0	Data 8
1 0 0 1	9	1 0 0 1 1	Data 9
1 0 1 0	A	1 0 1 1 0	Data A
1 0 1 1	B	1 0 1 1 1	Data B
1 1 0 0	C	1 1 0 1 0	Data C
1 1 0 1	D	1 1 0 1 1	Data D
1 1 1 0	E	1 1 1 0 0	Data E
1 1 1 1	F	1 1 1 0 1	Data F
Undefined	I	1 1 1 1 1	IDLE; used as inter-Stream fill code
0 1 0 1	J	1 1 0 0 0	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
0 1 0 1	K	1 0 0 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
Undefined	T	0 1 1 0 1	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
Undefined	R	0 0 1 1 1	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
Undefined	H	0 0 1 0 0	Transmit Error; used to force signaling errors
Undefined	V	0 0 0 0 0	Invalid Code
Undefined	V	0 0 0 0 1	Invalid Code
Undefined	V	0 0 0 1 0	Invalid Code
Undefined	V	0 0 0 1 1	Invalid Code
Undefined	V	0 0 1 0 1	Invalid Code
Undefined	V	0 0 1 1 0	Invalid Code
Undefined	V	0 1 0 0 0	Invalid Code
Undefined	V	0 1 1 0 0	Invalid Code
Undefined	V	1 0 0 0 0	Invalid Code
Undefined	V	1 1 0 0 1	Invalid Code

In 100BASE-FX mode, the external fiber-optic receiver performs the signal energy detection function and communicates this information directly to the NetPHY™ 4LP device through SDI± pins.

In 10BASE-T mode, a link-pulse detection circuit will constantly monitor the RX± pins for the presence of valid link pulses.

10BASE-T Block

The NetPHY™ 4LP transceiver incorporates four fully independent 10BASE-T physical layer functions, including clock recovery (ENDEC), MAUs, and transceiver functions. The NetPHY™ 4LP transceiver receives 10-Mbps data from the MAC, switch, or repeater across the RMII at 5 million di-bits per second. It then Manchester encodes the data before transmission to the network.

The 10BASE-T block consists of the following sub-blocks:

— Transmit Function
— Receive Function
— Interface Status
— Jabber Function
— Reverse Polarity Detect

Refer to Figure 5 for the 10BASE-T transmit and receive data paths.

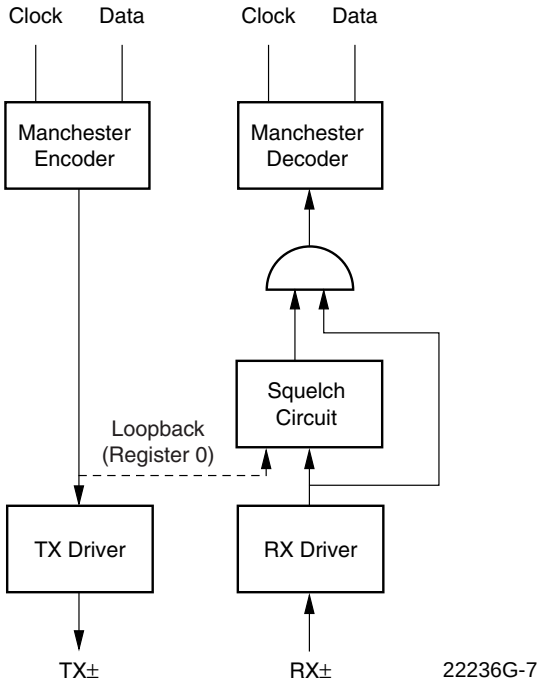


Figure 5. 10BASE-T Transmit/Receive Data Paths

Twisted Pair Transmit Function

Data transmission over the 10BASE-T medium requires use of the integrated 10BASE-T MAU and uses the differential driver circuitry on the TX± pins.

TX± is a differential twisted-pair driver. When properly terminated, TX± meets the transmitter electrical requirements for 10BASE-T transmitters as specified in IEEE 802.3, Section 14.3.1.2. The load is a twisted pair cable that meets IEEE 802.3, Section 14.4.

The TX± signal is filtered on the chip to reduce harmonic content per Section 14.3.2.1 (10BASE-T). Since filtering is performed in silicon, TX± can be connected directly to a standard transformer. External filtering modules are not needed.

Twisted Pair Receive Function

RX± ports are differential twisted-pair receivers. When properly terminated, each RX± port meets the electrical requirements for 10BASE-T receivers as specified in IEEE 802.3, Section 14.3.1.3. Each receiver has internal filtering and does not require external filter modules or common mode chokes.

Signals appearing at the RX± differential input pair are routed to the internal decoder. The receiver function meets the propagation delays and jitter requirements specified by the 10BASE-T Standard. The receiver squelch level drops to half its threshold value after unsquelch to allow reception of minimum amplitude signals and to mitigate carrier fade in the event of worst case signal attenuation and crosstalk noise conditions.

Twisted Pair Interface Status

The NetPHY™ 4LP transceiver will power up in the Link Fail state. The Auto-Negotiation algorithm will apply to allow it to enter the Link Pass state. In the Link Pass state, receive activity which passes the pulse width/amplitude requirements of the RX± inputs cause the PCS Control block to assert Carrier Sense (CRS) signal at the MII interface.

Jabber Function

The Jabber function inhibits the 10BASE-T twisted pair transmit function of the NetPHY™ 4LP transceiver device if the TX± circuits are active for an excessive period (20-150 ms). This prevents one port from disrupting the network due to a *stuck-on* or faulty transmitter condition. If the maximum transmit time is exceeded, the data path through the 10BASE-T transmitter circuitry is disabled (although Link Test pulses will continue to be sent). The PCS Control block also sets the Jabber Detect bit in Register 1. Once the internal transmit data stream from the MENDEC stops, an *unjab* time of 250-750 ms will elapse before this block causes the PCS Control block to re-enable the transmit circuitry.

When jabber is detected, this block allows the PCS Control block to assert or de-assert the CRS pin to indicate the current state of the RX± pair. If there is RX± activity, this block causes the PCS Control block to assert CRS at the RMII. The Jabber function can be disabled by setting Register 24, bit 12.

Reverse Polarity Detect and Correction

Proper 10BASE-T receiver operation requires that the differential input signal be the correct polarity. That is, the RX+ line is connected to the RX+ input pin, and the RX- line is connected to the RX- input pin. Improper setup of the external wiring can cause the polarity to be reversed. The NetPHY™ 4LP receivers have the ability to detect the polarity of the incoming signal and compensate for it. Thus, the proper signal will appear on the MDI regardless of the polarity of the input signals.

The internal polarity detection and correction circuitry is set during the reception of the normal link pulses (NLP) or packets. The receiver detects the polarity of the input

signal on the first NLP. It locks the polarity correction circuitry after the reception of two consecutive packets. The state of the polarity correction circuitry is locked as long as link is established. This function is only available in 10BASE-T mode.

Far-End Fault Indication (FEFI)

Auto-Negotiation provides a remote fault capability for detecting an asymmetric link failure. Since 100BASE-FX systems do not use Auto-Negotiation, an alternative, in-band signaling scheme is used to signal remote fault conditions. This scheme, Far End Fault Indication, relies on the characteristics of the quiescent state, a continuous IDLE stream. The IDLE stream is a continuous stream of logic ones followed by one logic zero, with the pattern repeated at least 3 times.

A Far-End Fault will be signaled under the following three conditions: (1) When no activity is received from the link partner, since this can indicate a broken receive wire, (2) When the clock recovery circuit detects a receive signal error or PLL lock error, (3) When management entity sets the transmit Far-end fault bit (Register 24, bit 7).

The Far-End fault mechanism defaults to enabled in 100BASE-FX mode and disabled in 100BASE-TX and 10BASE-T modes, and may be controlled by software after reset.

MLT-3

This block is responsible for converting the NRZI data stream from the PDX block to the MLT-3 encoded data stream. The effect of MLT-3 is the reduction of energy on the copper media (TX or FX cable) in the critical frequency range of 1 MHz to 100 MHz. The receive section of this block is responsible for equalizing and amplifying the received data stream and link detection. The adaptive equalizer compensates for the amplitude and phase distortion due to the cable.

MLT-3 is a tri-level signal. All transitions are between 0 V and +1 V or 0 V and -1 V. A transition has a logical value of 1 and a lack of a transition has a logical value of 0. The benefit of MLT-3 is that it reduces the maximum frequency over the data line. The bit rate of TX data is 125 Mbps. The maximum frequency (using NRZI) is half of 62.5 MHz. MLT-3 reduces the maximum frequency to 31.25 MHz.

A data signal stream following MLT-3 rules is illustrated in Figure 6. The data stream is 1010101.

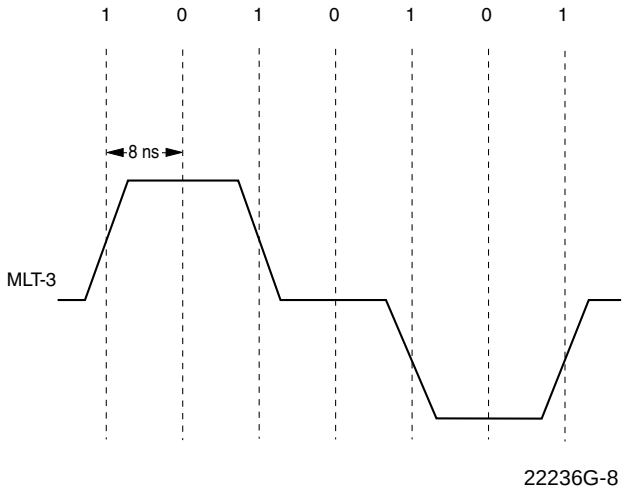


Figure 6. MLT-3 Waveform

The TX± drivers convert the NRZI serial output to MLT-3 format. The RX± receivers convert the received MLT-3 signals to NRZI. The transmit and receive signals will be compliant with IEEE 802.3u, Section 25. The required signals (MLT-3) are described in detail in ANSI X3.263:1995 TP-PMD Revision 2.2 (1995).

The NetPHY™ 4LP device provides on-chip filtering. External filters are not required for either the transmit or receive signals.

The TX± pins can be connected to the media via either a 1:1 transformer or a 1.25:1 transformer. The 1.25:1 ratio provides a 20% transmit power savings over the 1:1 ratio. Refer to Figure 7.

Adaptive Equalizer

The NetPHY™ 4LP device is designed for the maximum of 140 meter UTP-5 cable. A 140-meter UTP-5 cable attenuates the signal by 32 dB at 100 MHz which far exceed the cable plant attenuation (24-26 dB) defined by TP-PMD.

The amplitude and phase distortion from cable causes inter-symbol interference (ISI) which makes clock and data recovery impossible. Adaptive equalization is done by closely matching the characteristics of the twisted-pair cable. This is a variable equalizer which changes equalizer frequency response in accordance with cable length. The cable length is estimated based on comparisons of incoming signal strength against some known cable characteristics. The equalizer tunes itself automatically to the any cable length to compensate for the amplitude and phase distortion incurred from the cable.

Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The media, with transformer and common

mode filtering blocks the DC component of the code and the DC offset of the differential receive input can wander. The shift in the signal levels causes increase in error rates. A DC restoration circuit is needed to compensate for the attenuation of DC components. The NetPHY™ 4LP device implemented a patent-pending DC restoration circuit which, unlike the traditional implementation, does not need the feedback information from the slicer and clock recovery. The baseline wander correction circuit is not required and, therefore, is bypassed when the port is 10BASE-T.

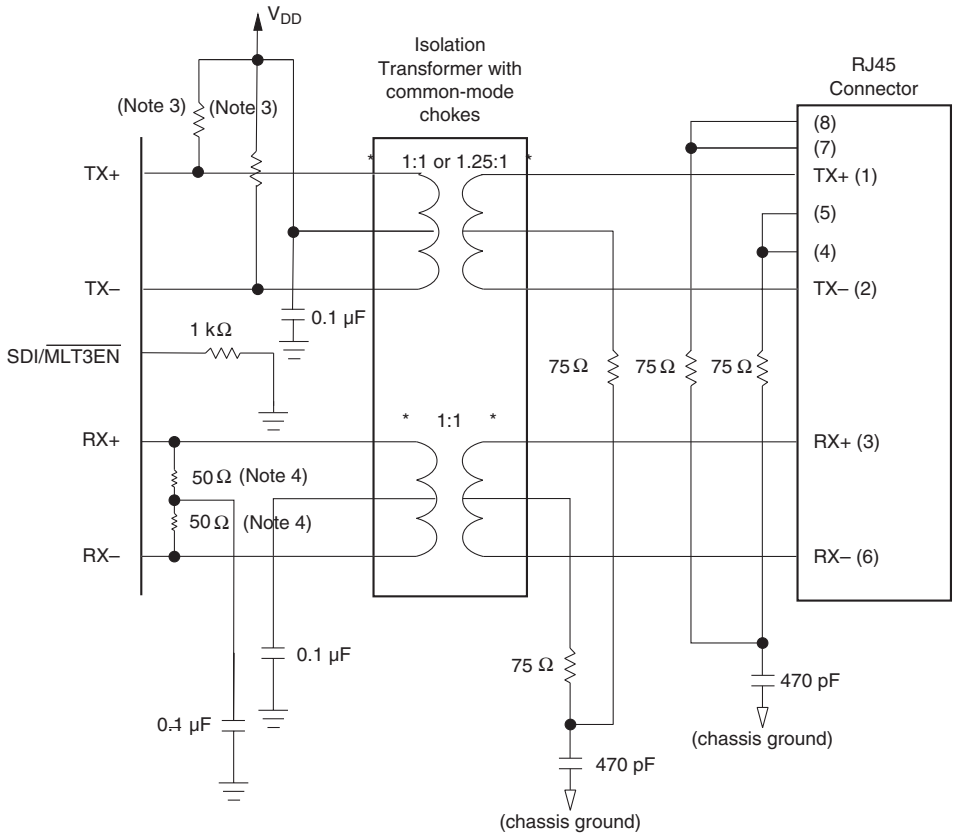
Clock/Data Recovery

The equalized MLT-3 signal is converted into NRZI format. The NetPHY™ 4LP device uses an analog phase locked loop (APLL) to extract clock information of the incoming NRZI data which is used to re-time the data stream and set data boundaries. The receive clocks are locked to the incoming data streams. PPM should be between 50 and 100.

When initial lock is achieved, the APLL switches to lock-to-data stream, extracts a 125-MHz clock. The recovered 125 MHz clock is also used to generate the 25-MHz RX_CLK. The APLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase align (lock) to data in one transition and its data/clock acquisition time after power-on is less than 60 transitions.

The APLL can maintain lock on run-lengths of up to 60 data bits in the absence of signal transitions. When no valid data is present, the APLL switches back to lock with the TX_CLK, providing a continuously running RX_CLK.

The recovered data is converted from NRZI-to-NRZ and then to a 5-bit parallel format. The 5-bit parallel data is not necessarily aligned to 4B/5B code-group's symbol boundary. The data is presented to PCS at receive data register output, gated by the 25-MHz RX_CLK.



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Notes:

2. *The isolation transformers include common-mode chokes.*
3. *Consult magnetics vendors for appropriate termination schemes.*
4. *50 Ω if a 1:1 isolation transformer is used or 78 Ω if a 1.25:1 isolation transformer is used.*
5. *50 (49.9) Ω is normal, but 54.9 Ω can be used for extended cable length operation.*

Figure 7. TX± and RX± Termination for 100BASE-TX and 10BASE-T

Auto-Negotiation and Miscellaneous Functions

Auto-Negotiation

The object of the Auto-Negotiation function is to determine the abilities of the devices sharing a link. After exchanging abilities, the NetPHY™ 4LP device and remote link partner device acknowledge each other and make a choice of which advertised abilities to support. The Auto-Negotiation function facilitates an ordered resolution between exchanged abilities. This exchange allows both devices at either end of the link to take maximum advantage of their respective shared abilities.

The NetPHY™ 4LP device implements the transmit and receive Auto-Negotiation algorithm as defined in IEEE 802.3u, Section 28. The Auto-Negotiation algorithm uses a burst of link pulses called Fast Link Pulses (FLP). The burst of link pulses are spaced between 55 and 140 µs so as to be ignored by the standard 10BASE-T algorithm. The FLP burst conveys information about the abilities of the sending device. The receiver can accept and decode an FLP burst to learn the abilities of the sending device. The link pulses transmitted conform to the standard 10BASE-T template. The NetPHY™ 4LP device can perform auto-negotiation with reverse polarity link pulses. The NetPHY™ 4LP device supports Next Page advertisement.

The NetPHY™ 4LP device uses the Auto-Negotiation algorithm to select the type connection to be established according to the following priority: 100BASE-TX full duplex, 100BASE-T4, 100BASE-TX half-duplex, 10BASE-T full duplex, 10BASE-T half-duplex. The device does not support 100BASE-T4 connections.

The Auto-Negotiation algorithm is initiated when one or the following events occurs: Auto-Negotiation enable bit is set, or reset, or soft reset, or transition to link fail state (when Auto-Negotiation enable bit is set), or Auto-Negotiation restart bit is set. The result of the Auto- Negotiation process can be read from the status register for the port of interest (Diagnostic Register, Register 18).

The NetPHY™ 4LP device supports Parallel Detection for remote legacy devices that do not support the Auto-Negotiation algorithm. In the case that a 100BASE-TX only device is connected to the remote end, the NetPHY™ 4LP device will see scrambled idle symbols and establish a 100BASE-TX only connection. If NLPs are seen, the NetPHY™ 4LP device will establish a 10BASE-T connection.

Loopback Operation

A local loopback and a remote loopback are provided for diagnostic testing. Local loopback can be achieved by writing to Register 0, bit 14 (LPBK). Remote loopback can be achieved by writing to Register 24, bit 3.

The local loopback routes transmitted data at the output of the NRZ-to-NRZI conversion module back to the receiving path's clock and data recovery module for connection to PCS in 5-bit symbol format. This loopback is used to check all the device's connection at the 5-bit symbol bus side and the operation of the analog phase locked loop. In the local loopback mode, the SDI output is forced to high and the TX± outputs are tri-stated.

The remote loopback routes receiving data at the output of the clock and data recovery module to the transmitting path's NRZI-to-MLT-3 conversion module. This loopback is used to check the device's connection on the media side and the operation of its internal adaptive equalizer, digital phase locked loop, and digital wave shape synthesizer. During the remote loopback mode, the SDI output is forced to low.

Power Savings Mechanisms

The NetPHY™ 4LP device has three mechanisms for reducing power: Selectable 1.25:1 transmit transformer ratio, Unplugged, and Power Down.

Selectable Transformer

The TX outputs can drive either a 1:1 transformer or a 1.25:1 transformer. The latter can be used to reduce transmit power further. The TP1_1 pin must be pulled low at reset to select 1.25:1 transformers. The current at the TX± pins for a 1:1 ratio transformer is 40 mA for MLT-3 and 100 mA for 10BASE-T. Using the 1.25:1 ratio reduces the current to 32 mA for MLT-3 and 80 mA for 10BASE-T.

The cost of using the 1.25:1 option is in impedance coupling. The reflected capacitance is increased by the square of the ratio of windings ($1.25^2 = 1.56$). Thus, the reflected capacitance on the media side is roughly 1½ times the capacitance on the board. Extra care in the layout to control capacitance on the board is required.

Unplugged

The Unplugged feature reduces power consumption whenever the PHY is operating. The TX output drivers limit the drive capability if the corresponding receivers do not detect a link partner within 4 seconds. This prevents "wasted" power. If the receiver detects the absence of a link partner, the corresponding transmitter is limited to transmitting normal link pulses. Any energy detected by the receiver enables full transmit capabilities. A typical situation encountered is that most unused ports still consume power. Up to 25% of repeater and switch ports are unconnected to allow room for future expansion. With NetPHY™ 4LP, unconnected ports have their receiver disabled until energy is detected. The power savings is most notable on uncon-

nected ports and ports running at 10 or 100 Mbps with Auto-Negotiation disabled. Typical power becomes 100 mW per port.

Power Down

Most of the NetPHY™ 4LP device can be disabled via the Power Down bit in Register 0, bit 11. Setting this bit on Register 0 of any port will power down the respective port with the exception of the MDIO/MDC management circuitry. Typical power becomes 5 mW or lower per port.

LED Port Configuration

The NetPHY™ 4LP device has several pins that are used for both device configuration and LED drivers. These pins set the configuration of the device on the rising edge of RST and thereafter indicate the state of the respective port. See Table 2.

The polarity of the LED drivers (Active-LOW or Active-HIGH) is set at the rising edge of RST. If the pin is LOW at the rising edge of RST, it becomes an active-HIGH driver. If it is HIGH at the rising edge of RST, it becomes an active-LOW driver.

Proper configuration requires external pull-up or pull-down resistors. If the LED corresponding to a pin is not used, the pin must be terminated via a resistor. The resistor value is not critical and can be in the range of 1 KΩ to 4.7 KΩ. If the corresponding LED is used, the terminating resistor must be placed in parallel with the LED. Figure 8 illustrates the wiring of the LEDs for both configuration settings.

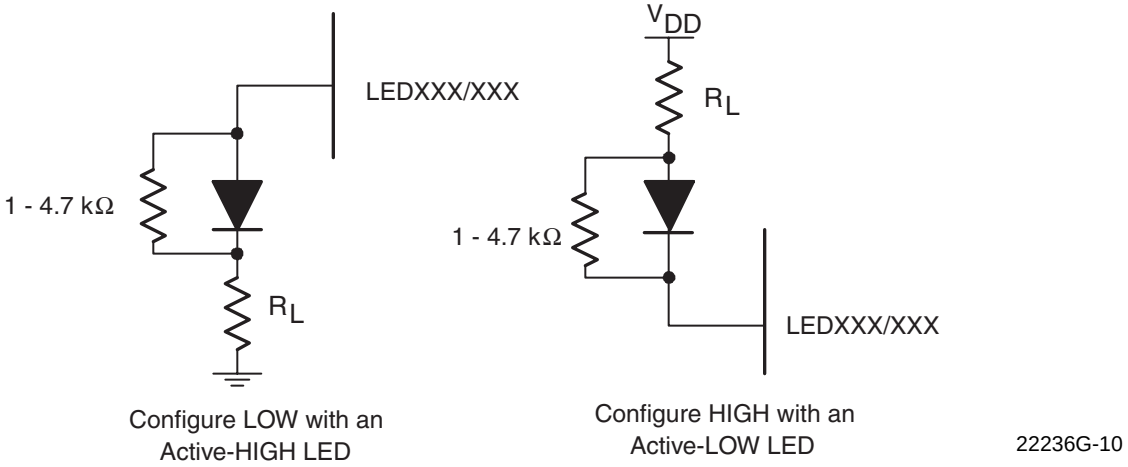
The value of the series resistor (R_L) should be selected to ensure sufficient illumination of the LED. It is dependent on the rating of the LED.

Table 2. LED Display Configuration

	LEDACT_LINK[N]	LEDSPD[N]	LEDDPX[N]
Cable Connected (Link)	LED On	LED Off	LED Off
100Mbps, Half Duplex	LED On	LED On	LED Off
100Mbps, Full Duplex	LED On	LED On	LED On
10Mbps, Half Duplex	LED On	LED Off	LED Off
10Mbps, Full Duplex	LED On	LED Off	LED On
RMII mode: Activity	Blinks on Transmit/Receive Activity	X	X

Notes:

1. *N = PHY port number (0...3)*
2. *X = don't care*



Note: *LEDXXX/XXX = any LED pin.*

Figure 8. LED Port Configuration

PHY Control and Management Block (PCM Block)

Register Administration for 100BASE-X PHY Device

The management interface specified in Clause 22 of the IEEE 802.3u standard provides for a simple two wire, serial interface to connect a management entity and a managed PHY for the purpose of controlling the PHY and gathering status information. The two lines are Management Data Input/Output (MDIO) and Management Data Clock (MDC). A station management entity which is attached to multiple PHY entities must have prior knowledge of the appropriate PHY address for each PHY entity.

Description of the Methodology

The management interface physically transports management information across the RMII. The information is encapsulated in a frame format as specified in Clause 22 of IEEE 802.3u draft standard and is shown in Table 3.

Table 3. Clause 22 Management Frame Format

	PRE	ST	OP	PHYAD	REGADD	TA	DATA	IDLE
READ	1.1	01	10	AAAAA	RRRRR	Z0	D.....D	Z
WRITE	1.1	01	01	AAAAA	RRRRR	10	D.....D	Z

The PHYAD field, which is five bits wide, allows 32 unique PHY addresses. The managed PHY layer device that is connected to a station management entity via the MII interface has to respond to transactions addressed to the PHY's address. A station management entity attached to multiple PHYs, such as in a managed 802.3 Repeater or Ethernet switch, is required to have prior knowledge of the appropriate PHY address.

Setting the PHYAD Bits

The PHYAD of each port is the combination of the setting of the NetPHY™ 4LP device and the port number. The NetPHY™ 4LP device is set by PHYAD[4:2] at the rising edge of $\overline{RST}$. The lower two bits of the PHYAD are set by the individual ports in the PHY. If the PHYAD[4:2] is set to 010, the PHYAD of each port is as follows:

Port 0	01000
Port 1	01001
Port 2	01010
Port 3	01011

Section 22 of the IEEE 802.3 standard states that all PHY devices connected to a mechanical interface will respond to PHYAD “00000” command regardless of the actual address of the PHY. There are applications where it is necessary to avoid setting the PHYAD of a port to “00000.” The NetPHY™ 4LP contains a mechanism that allows the PHYADs to be shifted by 1. The PHYAD_ST pin enables this mechanism. If the pin is LOW at power-up, the PHYADs are incremented by 1. To set the PHYAD pins, use pull-up or pull-down resistors in the range of 1 KΩ to 4.7 KΩ.

If PHYAD is set to 000, the address of each port is as follows:

Port 0	00001
Port 1	00010
Port 2	00011
Port 3	00100

The address shifting carries over the entire address space. If PHYAD[4:2] is set to 111, the PHYAD for each port is as follows:

Port 0	11101
Port 1	11110
Port 2	11111
Port 3	00000

Table 4. PHY Address Setting Frame Structure

	PRE	ST	OP	PHYAD	REGADD	TA	DATA	IDLE
READ	1.1	01	10	00000	RRRRR	Z0	XXXXXXXXXPPAAAAA	Z
WRITE	1.1	01	01	00000	RRRRR	10	XXXXXXXXXPPAAAAA	Z

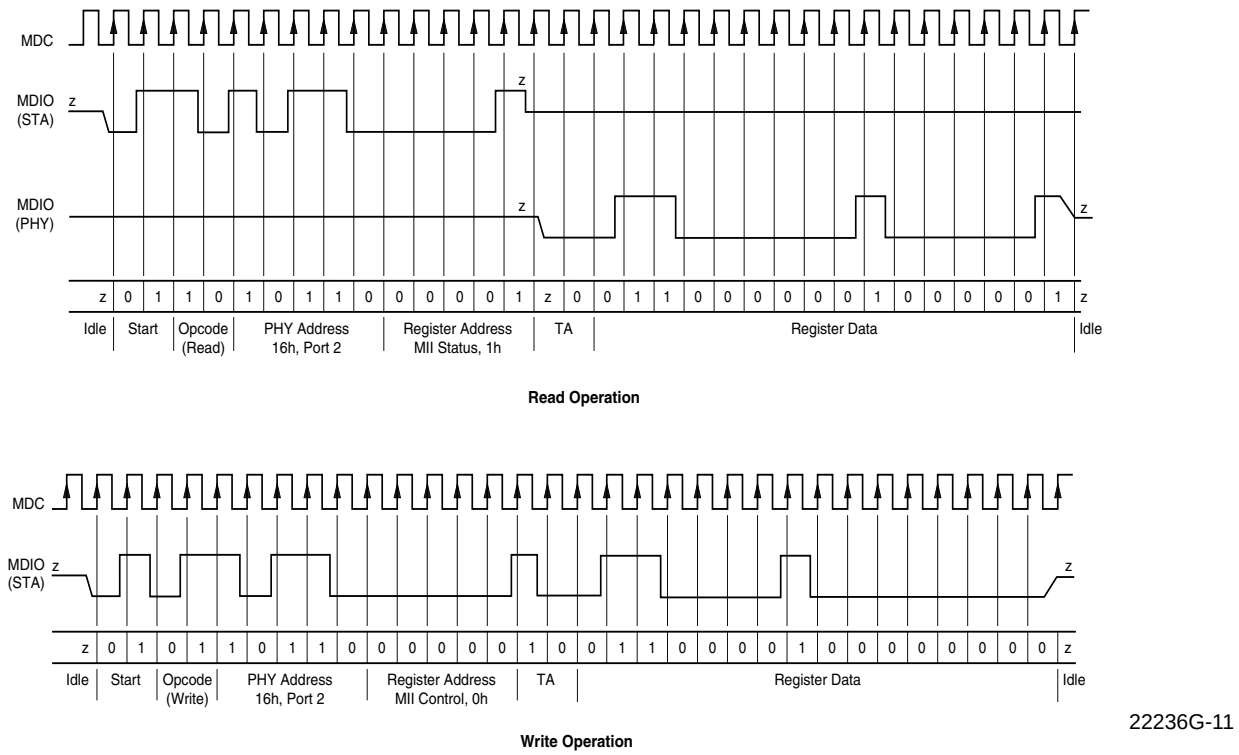


Figure 9. PHY Management Read and Write Operations

Bad Management Frame Handling

The management block of the device can recognize management frames without preambles (preamble suppression). However, if it receives a bad management frame, it will go into a Bad Management Frame state. It will stay in this state and will not respond to any management frame without preambles until a frame with a full 32-bit preamble is received, then it will return to normal operation.

A bad management frame is a frame that does not comply with the IEEE standard specification. It can be one with less than 32-bit preamble, with illegal OP field, etc. However, a frame with more than 32 preamble bits is considered to be a good frame.

Table 5. NetPHY™ 4LP MII Management Register Set

Register Address (in decimal)	Description
0	MII Management Control Register
1	MII Management Status Register
2	PHY Identifier 1 Register
3	PHY Identifier 2 Register
4	Auto-Negotiation Advertisement Register
5	Auto-Negotiation Link Partner Ability Register
6	Auto-Negotiation Expansion Register
7	Next Page Advertisement Register
8-15	Reserved
16	Miscellaneous Features Register
17	Interrupt Control/Status Register
18	Diagnostic Register
19	Test Register
20	Miscellaneous Features 2
21	Receiver Error Counter
22	Reserved
23	Reserved
24	Mode Control Register
25-31	Reserved

The Physical Address of the PHY is set using the pins defined as PHYAD[4:2]. These input signals are strapped externally and sampled as reset is negated. The PHYAD[1:0] will be decoded by the NetPHY™ 4LP device to address its internal four PHY channels.

All registers are available on a per port basis.

Table 6. Legend for Register Tables

Type	Description
RW	Readable and writable
SC	Self Clearing
LL	Latch low until clear
RO	Read Only
RC	Cleared on the read operation
LH	Latch high until clear

MII Management Control Register (Register 0)

Table 7. MII Management Control Register (Register 0)

Reg	Bit	Name	Description	Read/ Write	Default
0	15	Reset	1 = PHY reset. 0 = Normal operation. This bit is self-clearing.	RW/SC	0
0	14	Loopback	1 = Enable loopback mode. This will loopback TXD to RXD, thus it will ignore all the activity on the cable media. 0 = Disable loopback mode. Normal operation.	RW	0
0	13	Speed Select	1 = 100 Mbps. 0 = 10 Mbps.	RW	Set by FORCE100 pin
0	12	Auto-Neg Enable	1 = Enable Auto-Negotiation process (overrides 0.13 and 0.8). 0 = Disable Auto-Negotiation process.	RW	Set by ANEGA pin
0	11	Power Down	1 = Power down. The NetPHY™ 4LP device will shut off all blocks except for MDIO/MDC interface. 0 = Normal operation.	RW	0
0	10	Isolate	1 = Electrically isolate the PHY from MII. However, PHY is still able to respond to MDC/MDIO. 0 = Normal operation.	RW	0
0	9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process. 0 = Normal operation.	RW/SC	0
0	8	Duplex Mode	1 = Full duplex. 0 = Half duplex. Auto-Negotiation enabled: This bit is writable but will be ignored. Auto-Negotiation disabled: This pin is reset read value of DPLX.	RW	Set by DPLX pin
0	7	Collision Test	1 = Enable collision test, which issues the COL signal in response to the assertion of TX_EN signal. Collision test is enabled regardless of the duplex mode. 0 = disable COL test.	RW	0
0	6:0	Reserved	Write as 0, ignore on read.	RW	0

MII Management Status Register (Register 1)

Table 8. MII Management Status Register (Register 1)

Reg	Bit	Name	Description	Read/ Write	Default
1	15	100BASE-T4	1 = 100BASE-T4 able. 0 = Not 100BASE-T4.	RO	0
1	14	100BASE-TX Full Duplex	1 = 100BASE-TX with full duplex. 0 = No 100BASE-TX full duplex ability.	RO	Set by DPLX pin
1	13	100BASE-TX Half Duplex	1 = 100BASE-TX with half duplex. 0 = No 100BASE-TX half-duplex ability.	RO	1
1	12	10BASE-T Full Duplex	1 = 10BASE-T with full duplex. 0 = No 10BASE-T full duplex ability.	RO	Set by DPLX pin
1	11	10BASE-T Half Duplex	1 = 10BASE-T with half duplex. 0 = No 10BASE-T half duplex ability.	RO	1
1	10:7	Reserved	Ignore when read.	RO	0
1	6	MF Preamble Suppression	1 = PHY can accept management (mgmt) frames with or without preamble. 0 = PHY can only accept mgmt frames with preamble.	RO	1
1	5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed. Registers 4, 5, 6 are valid after this bit is set. 0 = Auto-Negotiation process not completed.	RO	0
1	4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault. This bit will remain set until it is cleared by reading register 1 via management interface.	RO/LH	0
1	3	Auto-Negotiation Ability	1 = Able to perform Auto-Negotiation function, its value is determined by ANEGA pin. 0 = Unable to perform Auto-Negotiation function.	RO	Set by ANEGA pin
1	2	Link Status	1 = Link is established, however, if the NetPHY™ 4LP device link fails, this bit will be cleared and remain cleared until register is read via management interface. 0 = Link is down.	RO/LL	0
1	1	Jabber Detect	1 = Jabber condition detect. 0 = No Jabber condition detected.	RO/LH	0
1	0	Extended Capability	1 = Extended register capable. This bit is tied permanently to one.	RO	1

PHY Identifier 1 Register (Register 2)

Table 9. PHY Identifier 1 Register (Register 2)

Reg	Bit	Name	Description	Read/ Write	Default
2	15:0	OUI	Composed of the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022(H)

PHY Identifier 2 Register (Register 3)

Table 10. PHY Identifier 2 Register (Register 3)

Reg	Bit	Name	Description	Read/ Write	Default
3	15:10	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	010101
3	9:4	Model Number	Six bit manufacturer's model number.	RO	010100
3	3:0	Revision Number	Four bit manufacturer's revision number. 0001 stands for Rev. A, etc.	RO	0001

Auto-Negotiation Advertisement Register (Register 4)

Table 11. Auto-Negotiation Advertisement Register (Register 4)

Reg	Bit	Name	Description	Read/ Write	Default
4	15	Next Page	1 = Next Page enabled. 0 = Next Page disabled.	RW	0
4	14	Acknowledge	This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.	RO	0
4	13	Remote Fault	1 = Remote fault supported. 0 = No remote fault.	RW	0
4	12:11	Reserved	Write as 0, ignore when read.	RW	0
4	10	FDFC	Full Duplex Flow Control. 1 = Advertise that the DTE(MAC) has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31 B of 802.3u. 0 = No MAC-based full duplex flow control.	RW	0
4	9	100BASE-T4	The NetPHY™ 4LP device does not support 100BASE-T4 function, i.e., this bit ties to zero.	RO	0
4	8	100BASE-TX Full Duplex	1 = 100BASE-TX with full duplex. 0 = No 100BASE-TX full duplex ability. Default is set by Register 1.14.	RW	Set by DPLX pin
4	7	100BASE-TX Half Duplex	1 = 100BASE-TX with half duplex. 0 = No 100BASE-TX half duplex capability. Default is set by Register 1.13.	RW	1
4	6	10BASE-T Full Duplex	1 = 10 Mbps with full duplex. 0 = No 10Mbps full duplex capability. Default is set by Register 1.12.	RW	Set by DPLX pin
4	5	10BASE-T Half Duplex	1 = 10 Mbps with half duplex. 0 = No 10 Mbps half duplex capability Default is set by Register 1.11.	RW	1
4	4:0	Selector Field	[00001] = IEEE 802.3	RO	00001

Auto-Negotiation Link Partner Ability Register in Base Page Format (Register 5)

Table 12. Auto-Negotiation Link Partner Ability Register in Base Page Format (Register 5)

Reg	Bit	Name	Description	Read/ Write	Default
5	15	Next Page	1 = Next Page Requested by Link Partner. 0 = Next Page Not Requested.	RO	0
5	14	Acknowledge	1 = Link Partner Acknowledgement. 0 = No Link Partner Acknowledgement.	RO	0
5	13	Remote Fault	1 = Link Partner Remote Fault Request. 0 = No Link Partner Remote Fault Request.	RO	0
5	12:11	Reserved	Reserved for Future Technology	RO	
5	10	Flow Control	1 = Link Partner supports Flow Control. 0 = Link Partner does not support Flow Control.	RO	0
5	9	100BASE-T4	1 = Remote Partner is 100BASE-T4 Capable. 0 = Remote Partner is not 100BASE-T4 Capable.	RO	0
5	8	100BASE-TX Full Duplex	1 = Link Partner is capable of 100BASE-TX with Full Duplex. 0 = Link Partner is Not Capable of 100BASE-TX with Full Duplex	RO	0
5	7	100BASE-TX Half Duplex	1 = Link Partner is Capable of 100BASE-TX with Half Duplex. 0 = Link Partner is Not Capable of 100BASE-TX with Half Duplex	RO	0
5	6	10BASE-T Full Duplex	1 = Link Partner is capable of 10BASE-T with Full Duplex. 0 = Link Partner is Not Capable of 10BASE-T with Full Duplex	RO	0
5	5	10BASE-T Half Duplex	1 = Link Partner is capable of 10BASE-T with Half Duplex. 0 = Link Partner is Not Capable of 10BASE-T with Half Duplex.	RO	0
5	4:0	Selector Field	Link Partner Selector Field.	RO	0

Auto-Negotiation Link Partner Ability Register in Next Page Format (Register 5)

Table 13. Auto-Negotiation LInk Partner Ability Register in Next Page Format (Register 5)

Reg	Bit	Name	Description	Read/ Write	Default
5	15	Next Page	1 = Next Page Requested by Link Partner. 0 = Next Page Not Requested.	RO	0
5	14	Acknowledge	1 = Link Partner Acknowledgement. 0 = No Link Partner Acknowledgement.	RO	0
5	13	Message Page	1 = Link Partner message Page Request. 0 = No Link partner Message Page Request.	RO	0
5	12	Acknowledge 2	1 = Link Partner can Comply with Next Page Request. 0 = Link Partner cannot Comply with Next Page Request.	RO	0
5	11	Toggle	Link Partner Toggle.	RO	0
5	10:0	Message Field	Link Partner’s Message Code.	RO	0

Auto-Negotiation Expansion Register (Register 6)

Table 14. Auto-Negotiation Expansion Register (Register 6)

Reg	Bit	Name	Description	Read/ Write	Default
6	15:5	Reserved	Ignore when read.	RO	0
6	4	Parallel Detection Fault	1 = Fault detected by parallel detection logic, this fault is due to more than one technology detecting concurrent link up condition. This bit can only be cleared by reading this register via management interface. 0 = No fault detected by parallel detection logic.	RO/LH	0
6	3	Link Partner Next Page Able	1 = Link partner support next page function. 0 = Link partner does not support next page function.	RO	0
6	2	Next Page Able	Next page is supported, i.e., this bit is permanently ties to 1.	RO	1
6	1	Page Received	It is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register.	RO/LH	0
6	0	Link Partner Auto-Negotiation Able	1 = Link partner is Auto-Negotiation able. 0 = Link partner is not Auto-Negotiation able	RO	0

Auto-Negotiation Next Page Advertisement Register (Register 7)

Table 15. Auto-Negotiation Next page Advertisement Register (Register 7)

Reg	Bit	Name	Description	Read/ Write	Default
7	15	NP	Next page indication: 1 = Another Next Page desired. 0 = No other Next Page Transfer desired	RW	0
7	14	Reserved	Ignore when read.	RO	0
7	13	MP	Message page: 1 = Message page 0 = Un-formatted page.	RW	1
7	12	ACK2	Acknowledge 2 1 = Will comply with message. 0 = Cannot comply with message.	RW	0
7	11	TOG_TX	Toggle: 1 = Previous value of transmitted link code word equals to 0 0 = Previous value of transmitted link code word equals to 1	RW	0
7	10:0	CODE	Message/Un-formatted Code Field.	RW	001

Reserved Registers (Registers 8-15, 22-23, 25-31)

The NetPHY™ 4LP device contains reserved registers at addresses 8-15, 22-23, 25-31. These registers should be ignored when read and should not be written at any time.

Miscellaneous Features Register (Register 16)

Table 16. Miscellaneous Features Register (Register 16)

Reg	Bit	Name	Description	Read/ Write	Default
16	15	Reserved	Write as 0; 1 = factory use only.	RW	0
16	14	INTR_LEVL	1 = INT is forced to 1 to signal an interrupt. 0 = INT is forced to 0 to signal an interrupt.	RW	0
16	13	TXJAM	1 = Force CIM to send jam pattern. 0 = Normal operation mode.	RO	0
16	12:4	Reserved	Write as 0, ignore when read.	RW	00000
16	3:0	Reserved	Ignore when read.	RO	0

Interrupt Control/Status Register (Register 17)

Table 17. Interrupt Control/Status Register (Register 17)

Reg	Bit	Name	Description	Read/ Write	Default
17	15	Jabber_IE	Jabber Interrupt Enable.	RW	0
17	14	Rx_Er_IE	Receive Error Interrupt Enable.	RW	0
17	13	Page_Rx_IE	Page Received Interrupt Enable.	RW	0
17	12	PD_Fault_IE	Parallel Detection Fault Interrupt Enable.	RW	0
17	11	LP_Ack_IE	Link Partner Acknowledge Interrupt Enable.	RW	0
17	10	Link_Not_OK_ IE	Link Status Not OK Interrupt Enable.	RW	0
17	9	R_Fault_IE	Remote Fault Interrupt Enable.	RW	0
17	8	ANeg_Comp_IE	Auto-Negotiation Complete Interrupt Enable.	RW	0
17	7	Jabber_Int	This bit is set when a jabber event is detected.	RC	0
17	6	Rx_Er_Int	This bit is set when RX_ER transitions high.	RC	0
17	5	Page_Rx_Int	This bit is set when a new page is received from link partner during Auto-Negotiation.	RC	0
17	4	PD_Fault_Int	This bit is set when parallel detect fault is detected.	RC	0
17	3	LP_Ack_Int	This bit is set when the FLP with acknowledge bit set is received.	RC	0
17	2	Link_Not_OK Int	This bit is set when link status switches from OK status to Non-OK status (Fail or Ready).	RC	0
17	1	R_Fault_Int	This bit is set when remote fault is detected.	RC	0
17	0	A_Neg_Comp Int	This bit is set when Auto-Negotiation is complete.	RC	0

Diagnostic Register (Register 18)

Table 18. Diagnostic Register (Register 18)

Reg	Bit	Name	Description	Read/ Write	Default
18	15:12	Reserved	Ignore when read.	RO	0
18	11	DPLX	This bit indicates the result of the Auto-Negotiation for duplex arbitration. 1 = Full Duplex. 0 = Half Duplex.	RO	0
18	10	Speed	This bit indicates the result of the Auto-Negotiation for data speed arbitration. 1 = 100 Mbps. 0 = 10 Mbps.	RO	0
18	9	RX_PASS	In 10BASE-T mode, a 1 indicates that Manchester data has been detected. In 100BASE-TX mode, a 1 indicates a valid signal has been received but not necessarily locked onto.	RO	0
18	8	RX_LOCK	1 = Received RLL has locked onto the received signal for selected data-rate (10BASE-T or 100BASE-TX) 0 = Receive PLL has not locked onto received signal. This bit remains set until read.	RO/RC	0
18	7:0	Reserved	Ignore when read.	RO	0x22

Test Register (Register 19)

Table 19. Test Register (Register 19)

Reg	Bit	Name	Description	Read/ Write	Default
19	15:12	Reserved	Ignore when read, write as Default (0x1000).	RW	0x1000
19	11:8	Reserved	Ignore when read, write as Default (0x0010).	RW	0x0010
19	7	Reserved	Ignore when read, write as 0.	RW	0
19	6	1.25:1	Selects transformer ratio. 1 = 1.25:1 0 = 1:1 The default value is controlled by the TP1_1 pin.	RW	0
19	5	10/100 Mbps Transmit Compliance Test	This bit controls internal logic, including power-saving circuitry. For 10 and 100 Mbps transmit compliance testing ONLY, this bit must be turned off, but should be turned on for normal operation. The default is 1 (on). 1 = Normal operation. 0 = Compliance test mode.	RW	1
19	4:0	Reserved	Ignore when read, write as 0.	RW	0

Miscellaneous Features 2 Register (Register 20)

Table 20. Miscellaneous Features 2 Register (Register 20)

Reg	Bit	Name	Description	Read/ Write	Default
20	15:12	Reserved	Ignore when read, write as Default (0x0110).	RW	0x0110
20	11:8	Reserved	Ignore when read, write as Default (0x1001).	RW	0x1001
20	7:4	Cable length indicator	These bits are the cable length indicators. Increment from 0000 to 1111, or approximately every 10 meters. The equivalent is 0 to 32dB with an increment of 2dB @ 100Mhz. The value is read back from the equalizer, and the measured value is not absolute.	RO	0
20	3:0	Reserved	Ignore when read.	RO	0x0010

Receive Error Counter (Register 21)

Table 21. Receive Error Counter (Register 21)

Reg	Bit	Name	Description	Read/ Write	Default
21	15:0	RX_ER Counter	Count of Receive Error Events.	RW	0000 (hex)

Mode Control Register (Register 24)

Table 22. Mode Control Register (Register 24)

Reg	Bit	Name	Description	Read/ Write	Default
24	15	SDCM_SEL	Select Common Mode Voltage Setting for FX Signal Detect (SDI) input signal. 1 = Select Internal Common Mode Setting. 0 = Select External Common Voltage Setting.	RW	0
24	14	Force 10BASE-T Link Up	1 = Force link up at 10 Mbps without checking NLP. Auto-Negotiation must be disabled and the data rate must be 10 Mbps. 0 = Normal Operation.	RW	0
24	13	Force 100BASE-TX Link Up	1 = Force link up at 100 Mbps. Auto-Negotiation must be disabled and the data rate must be 100 Mbps. 0 = Normal Operation.	RW	0
24	12	Jabber Disable	1 = Disable Jabber function in PHY. 0 = Enable Jabber function in PHY.	RW	0
24	11	Reserved	Write as 0, ignore when read.	RW	0
24	10	Activity LED Configuration	1 = Activity only responds to receive operation. 0 = Activity responds to Receive and transmit. In repeater mode, this bit will be ignored.	RW	1
24	9	Reserved	Write as 0, ignore when read.	RW	0
24	8	FEFI_Disable	Set this bit will disable FEFI generation and detection function. The default value of this bit is 0 when the chip is working in FX mode. Otherwise the default value is 1.	RW	Set by FX_DIS and ANEGA pins
24	7	Force FEFI Transmit	This bit is set to force the transmit FEFI pattern.	RW	0
24	6	RX_ER_CNT Full	This bit is set to one to indicate the Receive Error Counter is full.	RO/RC	0
24	5	Disable RX_ER counter	1 = disable Receive Error Counter.	RW	0
24	4	DIS_WDT	1 = Disable the watchdog timer in the decipher.	RW	0
24	3	EN_RPBK	1 = Enable remote loopback, 0 = Disable remote loopback.	RW	0
24	2	EN_SCRM	0 = Disable data scrambling. 1 = Enable data scrambling. When FX_DIS pin is asserted low or FX_SEL bit (Register 24.0) is set to logic high, this bit will be overwritten as “1” automatically. The default of this bit is set by power on read value of FX_DIS.	RW	Set by SCRAM_EN pin
24	1	Reserved	Write as 0, ignore when read.	RO	0
24	0	FX_SEL	Set this bit to logic 1 to select 100BASE-FX mode, set to logic 0 to select 100BASE-TX.	RW	Set by FX_DIS pin

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . .-55°C to +150°C

Ambient Temperature Under Bias . . .-55°C to +150°C

Supply Voltage (V_{DD}) . . . . . -0.5 V to +5.5 V

Voltage Applied to any input pin. . . . . -0.5 V to V_{DD}

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (C):

Operating Temperature (TA) . . . . . 0°C to +70°C

Supply Voltage (all V_{DD}) . . . . . +3.3 V ±5%

Supply Voltage (5-V tolerant pins) . . . . . +5.0 V ±5%

Industrial (I):

Operating Temperature (TA) . . . . . -40°C to +85°C

Supply Voltage (all V_{DD}) . . . . . +3.3 V ±5%

Supply Voltage (5-V tolerant pins) . . . . . +5.0 V ±5%

Operating ranges define those limits between which functionality of the device is guaranteed.

DC CHARACTERISTICS

Note: Parametric Values are the same for Commercial and Industrial devices.

Symbol	Parameter Description	Test Conditions	Minimum	Maximum	Units
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -4 mA	2.4		V
V_{OLL}	Output LOW Voltage (LED)	I_{OL} (LED) = 10 mA		0.4	V
V_{OHL}	Output HIGH Voltage (LED)	I_{OL} (LED) = -10 mA	V_{DD} – 0.4		V
V_{CMP}	Input Common-Mode Voltage PECL (Note 1)		V_{DD} – 1.5	V_{DD} – 0.7	V
V_{IDIFFP}	Differential Input Voltage PECL (Note 1)	V_{DD} = Maximum	400	1,100	mV
V_{OHP}	Output HIGH Voltage PECL (Note 4)	PECL Load	V_{DD} – 1.025	V_{DD} – 0.60	V
V_{OLP}	Output LOW Voltage PECL (Note 4)	PECL Load	V_{DD} – 1.81	V_{DD} – 1.62	V
V_{SDA}	Signal Detect Assertion Threshold Peak-to-Peak (Note 2)	MLT-3/10BASE-T Test Load	-	1000	mV
V_{SDD}	Signal Detect Deassertion Threshold Peak-to-Peak (Note 3)	MLT-3/10BASE-T Test Load	200	-	mV
I_{IL}	Input LOW Current (Note 5)	V_{DD} = Maximum V_{IN} = 0.0 V		-40	µA
I_{IH}	Input HIGH Current (Note 5)	V_{IN} = V_{DD}		40	µA
V_{TXOUT}	Differential Output Voltage (Note 6)	MLT-3/10BASE-T Test Load	950	1050	mV
V_{TXOS}	Differential Output Overshoot (Note 6)	MLT-3/10BASE-T Test Load	-	0.05 * V_{TXOUT}	V
V_{TXR}	Differential Output Voltage Ratio (Note 6 & Note 7)	MLT-3/10BASE-T Test Load	0.98	1.02	-

Symbol	Parameter Description	Test Conditions	Minimum	Maximum	Units
V_{TSQ}	RX± 10BASE-T Squelch Threshold	Sinusoid 5 MHz<f<10 MHz	300	585	mV
V_{THS}	RX± Post-Squelch Differential Threshold 10BASE-T (Note 8)	Sinusoid 5 MHz<f<10 MHz	150	293	mV
V_{RXDTH}	10BASE-T RX± Differential Switching Threshold (Note 8)	Sinusoid 5 MHz<f<10 MHz	-60	60	mV
V_{TX10NE}	10BASE-T Near-End Peak Differential Voltage (Note 9)	MLT-3/10BASE-T Test Load	2.2	2.8	V
I_{OZ}	Output Leakage Current (Note 10)	$0.4\ V < V_{OUT} < V_{DD}$	-30	100	µA

Power Supply Current Consumption

Symbol	Parameter Description	Test Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current for 10BASE-T (Note 11)	V_{DD} = maximum	-	260 (Note 13)	480 (Note 11,12)	mA
I_{DD}	Power Supply Current for 100BASE-TX/FX (Note 11)	V_{DD} = maximum	-	300	380 (Note 11)	mA

Notes:

1. *Applies to FXR+, FXR-, SDI+, and SDI- inputs only. Valid only when Port 3 is in PECL mode. V_{DD} is that of the fiber transceiver.*
2. *Applies to RX± inputs when the corresponding port is in MLT-3 mode only. The RX± input is guaranteed to assert internal signal detect for any valid peak-to-peak input signal greater than V_{SDA} MAX. Tested within limits of V_{SDD} and V_{SDA}.*
3. *Applies to RX± inputs when the corresponding port is in MLT-3 mode only. The RX± input is guaranteed to de-assert internal signal for any peak to peak signal less than V_{SDD} MIN. Tested within limits of V_{SDD} and V_{SDA}.*
4. *Applies to FXT+ and FXT- outputs only. Valid only when Port 3 is in PECL mode. V_{DD} is that of the fiber transceiver.*
5. *Applies to digital inputs and all bidirectional pins. RX± limits up to 1.0 mA max for I_{IL} and -1.0 mA min for I_{IH}. Pull-up/pull-down resistors effect this value.*
6. *Applies to TX± differential outputs only. Valid only when the port is in the MLT-3 mode.*
7. *V_{TXR} is the ratio of the magnitude of TX± in the positive direction to the magnitude of TX± in the negative direction.*
8. *Parameter not tested.*
9. *Only valid for TX output when the port is in the 10BASE-T mode.*
10. *I_{OZ} applies to all high-impedance output pins. Pull-up/pull-down resistors effect this value.*
11. *Tested with all TX± output pins driving the rated load.*
12. *Assumes 80% Utilization with all ports at 10 Mbps, using 1:1 transformers.*
13. *Typical is 30% network utilization.*
14. *Assumes outputs are loaded, and all LEDs are used.*

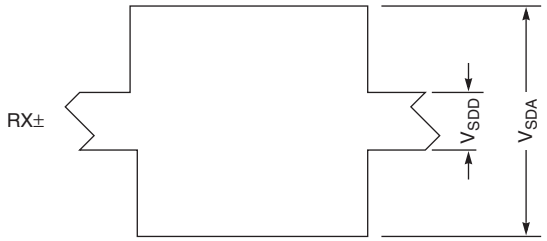
SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING WAVEFORMS



22236G-12

Figure 10. MLT-3 Receive Input

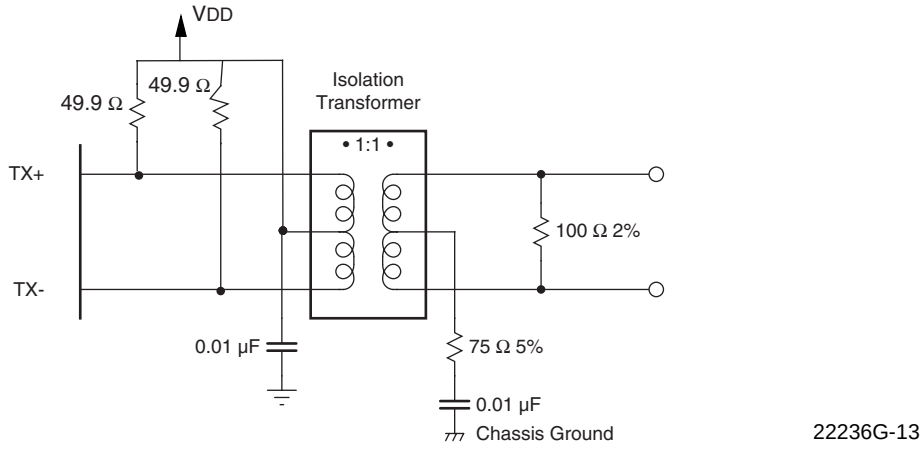


Figure 11. MLT-3 and 10BASE-T Test Load with 1:1 Transformer Ratio

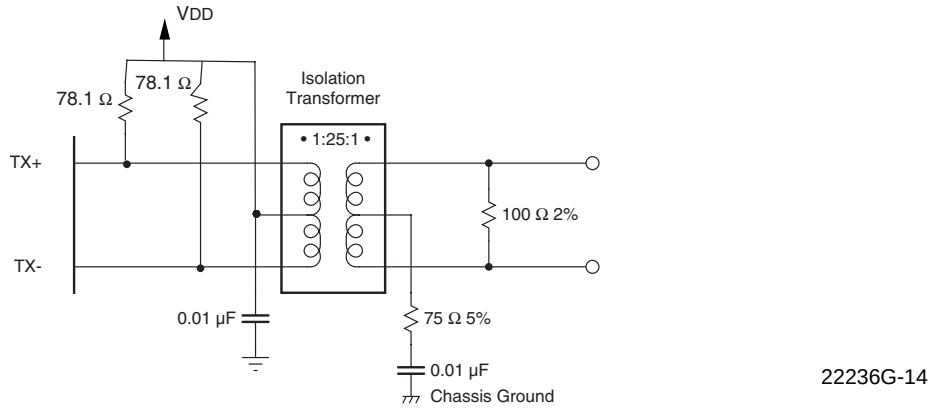


Figure 12. MLT-3 and 10BASE-T Test Load with 1.25:1 Transformer Ratio

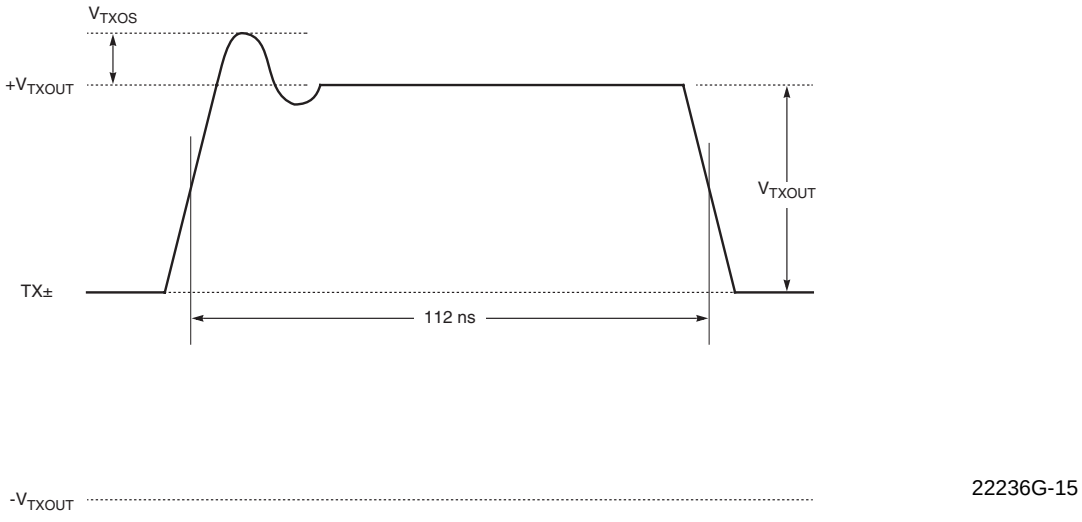
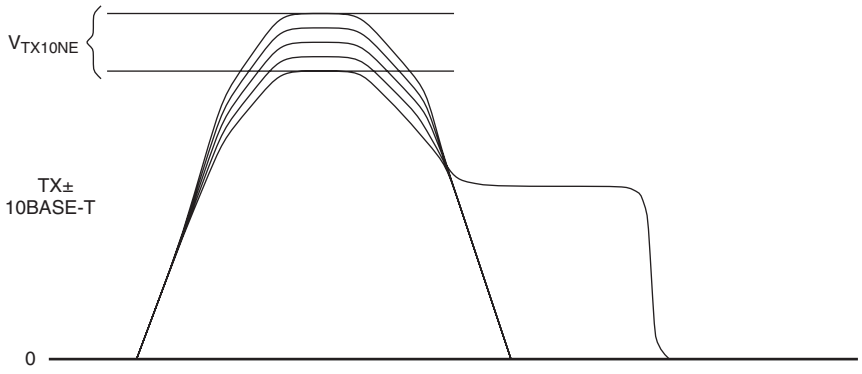


Figure 13. Near-End 100BASE-TX Waveform



22236G-16

Figure 14. Near-End 10BASE-T Waveform

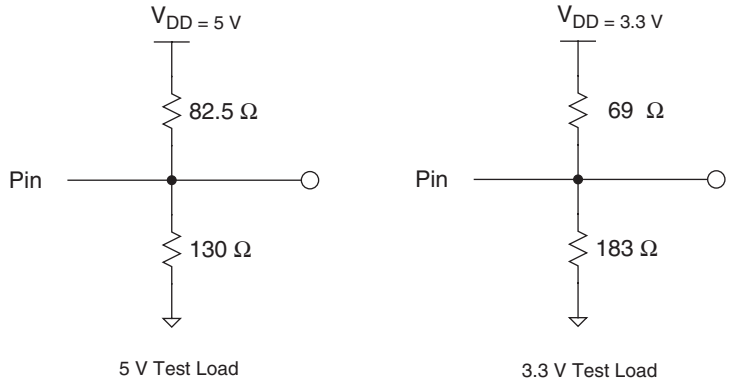


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Figure 15. Recommended PECL Test Loads

SWITCHING CHARACTERISTICS

System Clock Signal

Symbol	Parameter Description	Min.	Max.	Unit
t_{CLK}	REFCLK Period	19.999	20.001	ns
t_{CLKH}	REFCLK Width HIGH	9	11	ns
t_{CLKL}	REFCLK Width LOW	9	11	ns
t_{CLR}	REFCLK Rise Time	-	5	ns
t_{CLF}	REFCLK Fall Time	-	5	ns

Notes:

1. Parametric values are the same for Commercial and Industrial devices.

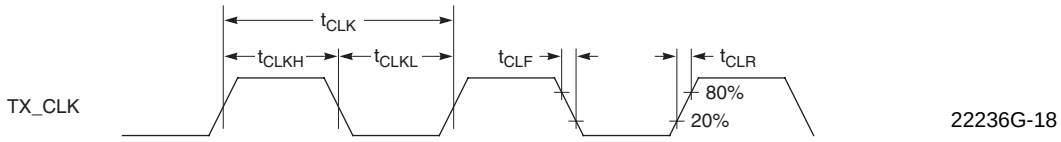


Figure 16. Clock Signal

MLT-3 Signals

Symbol	Parameter Description	Min.	Max.	Unit
t_{TXR}	Rise Time of MLT-3 Signal	3.0	5.0	ns
t_{TXF}	Fall Time of MLT-3 Signal	3.0	5.0	ns
t_{TXRFS}	Rise Time and Fall Time Symmetry of MLT-3 Signal	-	5	%
t_{TXDCD}	Duty Cycle Distortion Peak to Peak	-	0.5	ns
t_{TXJ}	Transmit Jitter Using Scrambled Idle Signals	-	1.4	ns

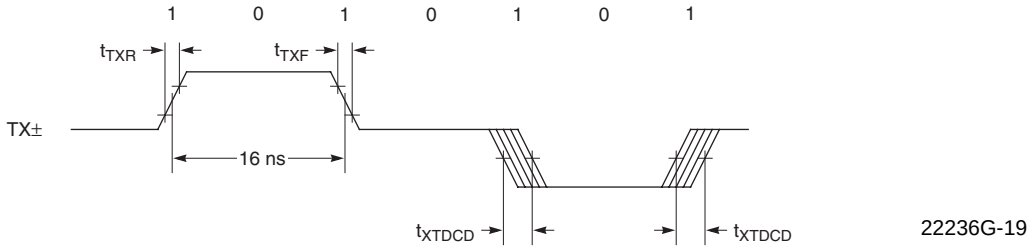


Figure 17. MLT-3 Test Waveform

MII Management Signals

Symbol	Parameter Description	Min.	Max.	Unit
t_{MDPER}	MDC Period	40		ns
t_{MDWH}	MDC Pulse Width HIGH	16		ns
t_{MDWL}	MDC Pulse Width LOW	16		ns
t_{MDPD}	MDIO Delay From Rising Edge of MDC	-	20	ns
t_{MDS}	MDIO Setup Time to Rising Edge of MDC	4		ns
t_{MDH}	MDIO Hold Time From Rising Edge of MDC		3	ns

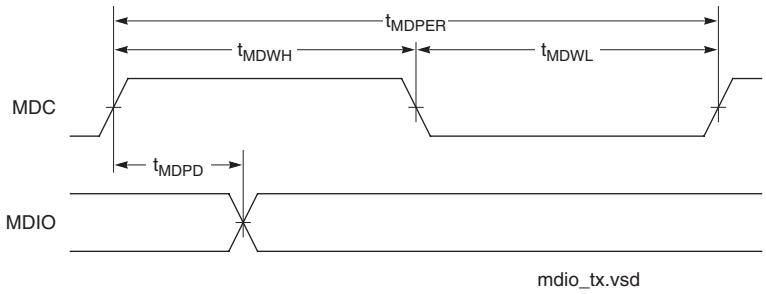


Figure 18. Management Bus Transmit Timing

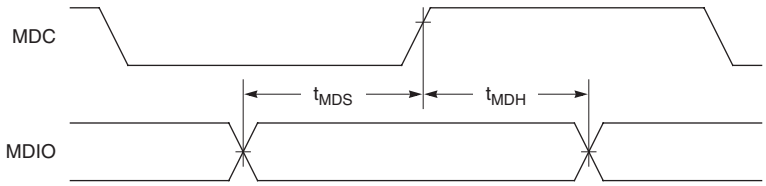


Figure 19. Management Bus Receive Timing

Independent RMII Mode Signals

100 Mbps RMII Transmit

Symbol	Parameter Description	Min.	Max.	Unit
t_{RS100}	TX_EN[X], TXD[X]_[1:0] Setup Time to REFCLK Rising Edge	4	-	ns
t_{RH100}	TX_EN[X], TXD[X]_[1:0] Hold time From REFCLK Rising Edge	2	-	ns
t_{RTJ100}	Transmit Latency TX_EN[X] Sampled by REFCLK to First Bit of /J/	60	100	ns
$t_{TIDLE100}$	Required De-assertion Time Between Packets	120	-	ns

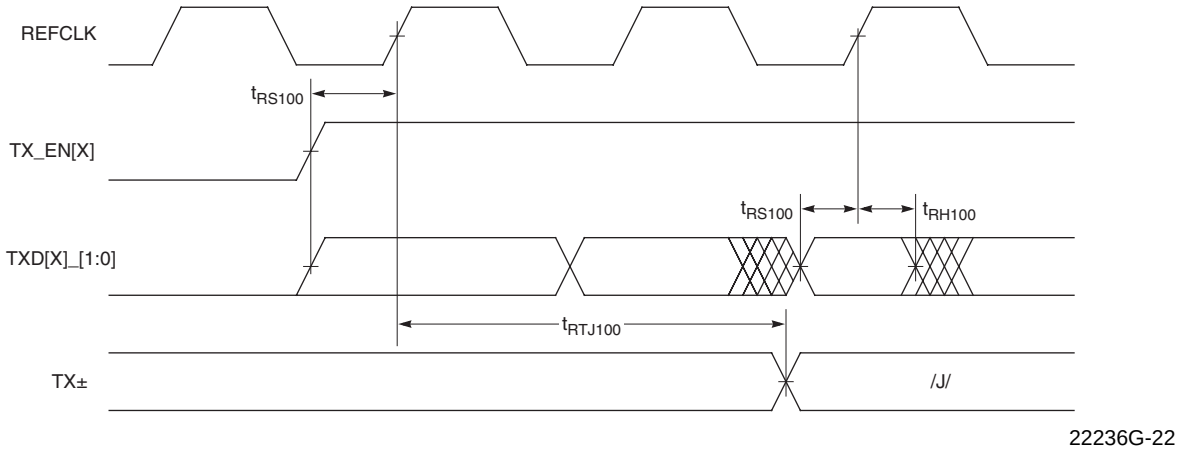


Figure 20. RMII 100 Mbps Transmit Start of Packet

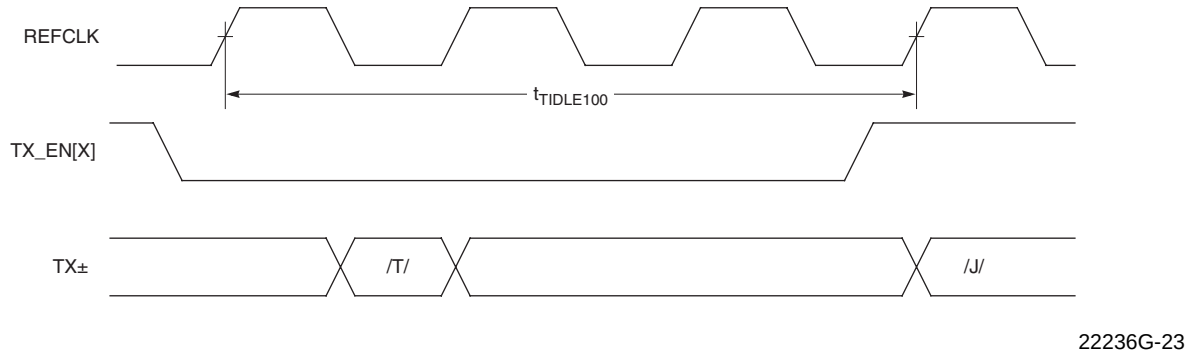


Figure 21. RMII 100 Mbps Transmit End of Packet Timing

100 Mbps RMII Receive

Symbol	Parameter Description	Min.	Max.	Unit
t_{RJC100}	CRS_DV[X] HIGH After First Bit of /J/	80	150	ns
t_{RCR100}	RXD[X]_[1:0], CRS_DV[X] Delay After the Rising Edge of REFCLK	5	13	ns
t_{RTC100}	First Bit of /T/ to CRS_DV[X] LOW	120	190	ns

Note: *CRS_DV[X] is asynchronous at the beginning of receive (1st rising edge of REFCLK), but is synchronous at the end of receive.*

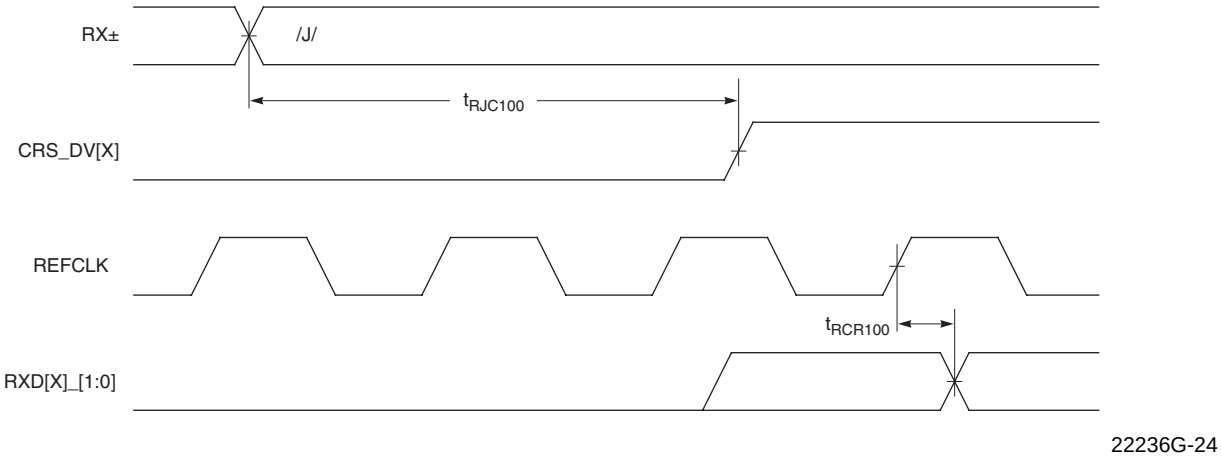


Figure 22. 100 Mbps RMII Receive Start of Packet Timing

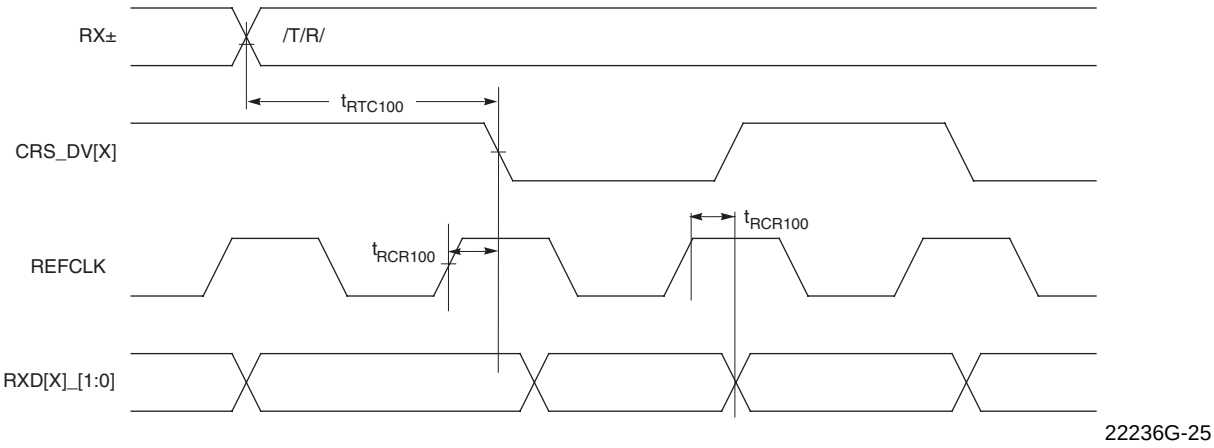


Figure 23. 100 Mbps RMII Receive End of Packet Timing

10 Mbps RMII Transmit

Symbol	Parameter Description	Min.	Max.	Unit
t_{RS10}	TX_EN[X], TXD[X]_[1:0] Setup Time to REFCLK Rising Edge	4	-	ns
t_{RH10}	TX_EN[X], TXD[X]_[1:0] Hold time From REFCLK Rising Edge	2	-	ns
t_{RTP10}	Transmit Latency TX_EN[X] Sampled by REFCLK to Start of Packet	240	360	ns
$t_{TIDLE10}$	Required De-assertion Time Between Packets	300	-	ns

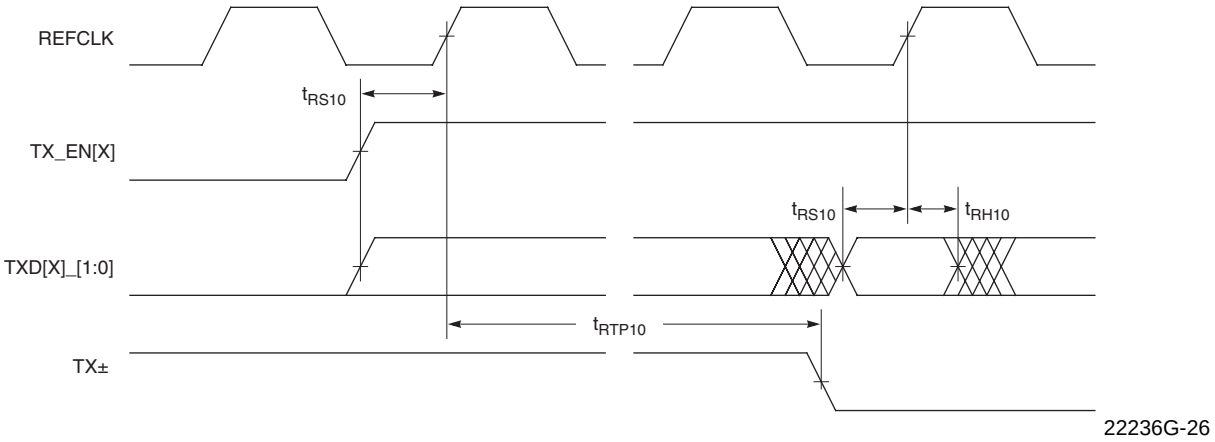


Figure 24. RMII 10 Mbps Transmit Start of Packet

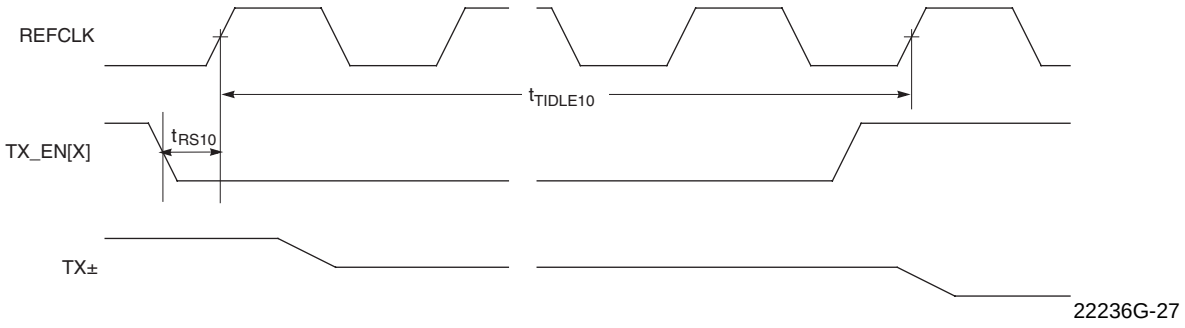


Figure 25. RMII 10 Mbps Transmit End of Packet Timing

10 Mbps RMII Receive

Symbol	Parameter Description	Min.	Max.	Unit
t_{RSPC10}	CRS_DV[X] HIGH After Start of Packet	200	350	ns
t_{RCR10}	RXD[X]_[1:0], CRS_DV[x] Delay After the Rising Edge of REFCLK	5	13	ns
t_{REPC10}	End of Packet to CRS_DV[X] LOW	130	190	ns

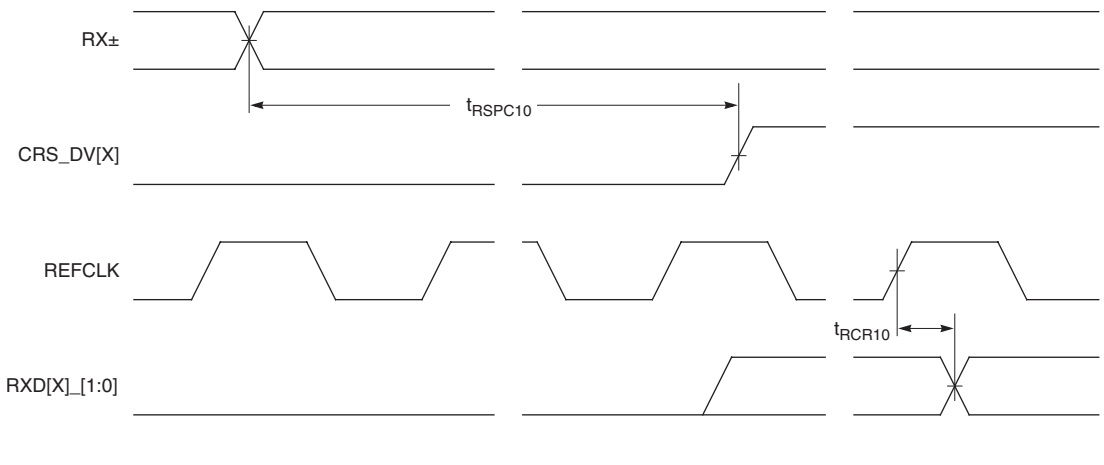


Figure 26. 10 Mbps RMII Receive Start of Packet Timing

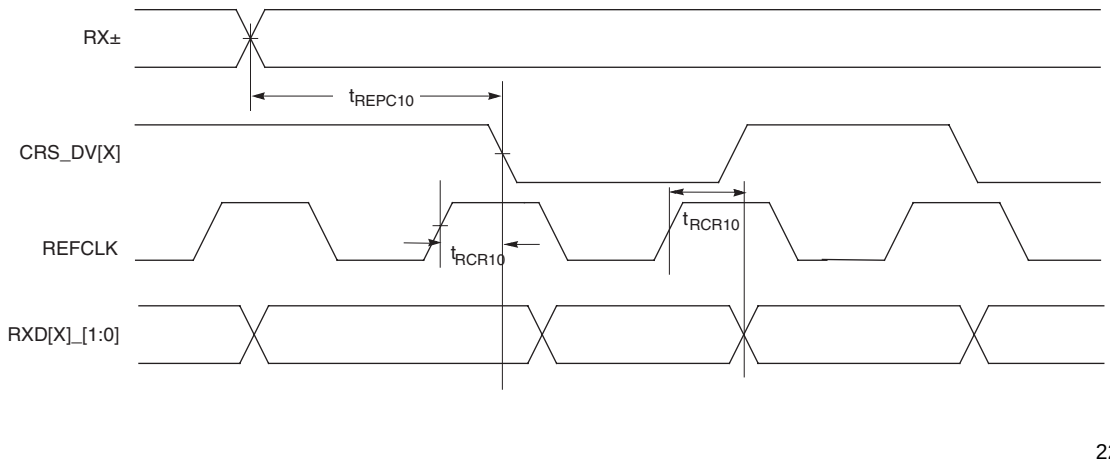
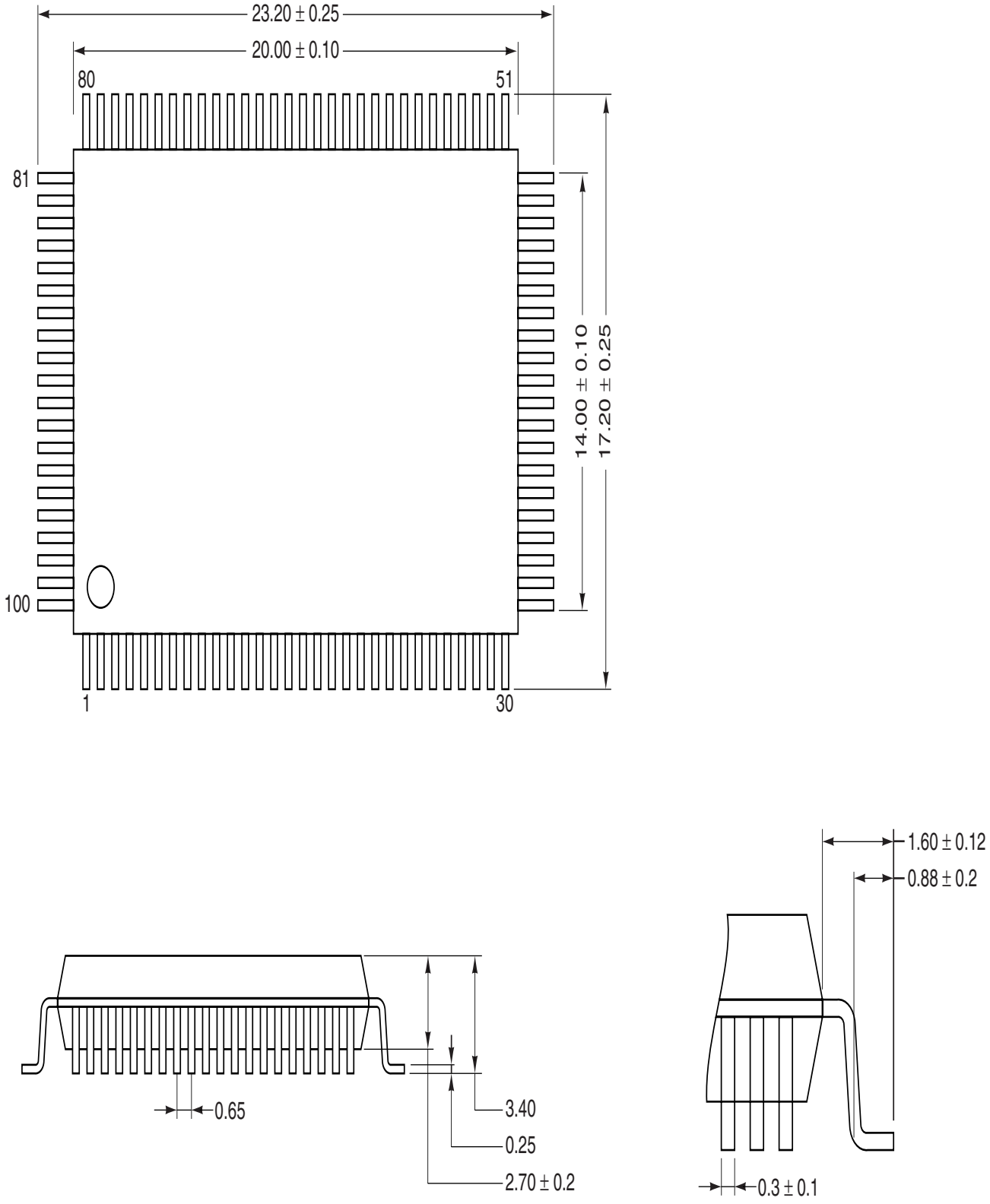


Figure 27. 10 Mbps RMII Receive End of Packet Timing

PHYSICAL DIMENSIONS*

PQR100 (measured in millimeters)



**For reference only. BSC is an ANSI standard for Basic Space Centering.*

ERRATA

NetPHY™ 4LP Revision B.4 is the current production revision silicon with errata – please refer to the descriptions below.

Revision B.4 Errata Summary

The NetPHY™ 4LP device has a total of 5 errata, all of which are minor and should not cause concern. All information below should be used in conjunction with the NetPHY™ 4LP Final Datasheet PID 22236, available on the AMD web site (www.amd.com).

Errata for NetPHY™ 4LP B.4

The SYMPTOM section gives an external description of the problem. The IMPLICATION section explains how the device behaves and its impact on the system. The WORKAROUND section describes a workaround for the problem. The STATUS section indicates when and how the problem will be fixed.

B4.1) 10BASE-T signal acceptance compliance test suite - test #1411.11.03

SYMPTOM: CRS response to Signal 7a, 7b, 8a, 8b and 10 is unreliable unless the signal is preceded by a preamble.

IMPLICATION: These compliance tests reflect boundary conditions unlikely to happen in normal operation. Some boundary conditions are meant to test the receiver's robustness and if it properly receives valid data. We have successfully received 10Mbps data for all cable lengths, and we believe that the chance of failure in the field is extremely low.

WORKAROUND: There is no external work around.

STATUS: This errata will not be fixed.

B4.2) 10BASE-T Local Loopback

SYMPTOM: 10BASE-T Local loopback does not work.

IMPLICATION: This is a minor issue which does not affect normal operation.

WORKAROUND: Loopback testing must be performed external to the device.

STATUS: This errata will not be fixed.

B4.3) 10Mb not interrupted by 100Mb data reception

SYMPTOM: If the PHY is in 10BASE-T and for an unknown reason, 100Mbps data is received, the PHY should drop 10Mb link and establish 100Mb link.

IMPLICATION: This is a minor issue which should not affect normal operation. This is UNH test 25.28c, where it is stated that the standard does not allow for this behavior and that no harm to the network is anticipated. Additionally, it is not uncommon to find this issue with many PHYs today.

WORKAROUND: There is no external workaround.

STATUS: This errata will not be fixed.

B4.4) Delayed idle following abnormal packet transmission

SYMPTOM: If a packet does not end in a /T/R/, the RX_ER signal does not go true immediately after, and is delayed 1 to 2 clock cycles. The receiver will then enter the idle state.

IMPLICATION: This is a minor issue. If the packet does not terminate properly, RX_ER is delayed 1-2 clock cycles. The issue is believed to be minor since the likelihood of encountering improperly terminated data packets is small. However, it will affect the recording of errors by the system. (UNH 1.24)

WORKAROUND: There is no external workaround.

STATUS: This errata will not be fixed.

B4.5) Full Duplex operation with Auto-Negotiation Disabled

SYMPTOM: If Auto-Negotiation is disabled, the device cannot be pin-strapped to full-duplex. LEDDPX[2]/DPLX (Pin 41) should set the duplex at reset if LEDACT_LINK/ANEGA (Pin 39) is LOW at reset. Instead, all 4 ports are half-duplex regardless of the setting of Pin 41.

IMPLICATION: This is a minor issue which should not affect normal operation. Auto-Negotiation operation is usually set by default in systems today so that both link partners can operate at the highest setting (speed and duplex). Very rarely do systems rely on Parallel Detect to set the speed of the link. Note that RMII operation is by definition, full-duplex.

WORKAROUND: Full-duplex operation must be set through management pins, Register 0, bit 8.

STATUS: This errata will not be fixed.

REVISION SUMMARY

Revision C to D

1. Register 18, added bits 8 and 9 for user checking.
2. Register 19, added bit 6, Transformer ratio selection via software.
3. Register 20, added bits 7:4, Cable length indicators.
4. Register 24, added bit 5, RX_ER counter disable.
5. DC Characteristics: added V_{OLL}, new I_{IH}, I_{IL} and I_{OZ} maximum values
6. MII Management signals: MDC period changed to 40ns (min), MDC pulse high/low changed to 16ns (min)
7. MII Management signals: MDIO delay changed to 20ns (max), MDIO setup time changed to 4ns (min), MDIO hold time changed to 3ns (max)

Revision D to E

1. Specified using resistors in the range of 1 KΩ to 4.7 KΩ for setting the PHYAD pins. Figure 8 reflects the correct resistors.
2. Added bit 10, Flow Control Support, to Register 5.

Revision E to F

1. Added industrial temperature support and new OPN(KI).
2. Minor edits.

Revision F to G

1. Removed CIM_DIS references.
2. Added pull-up resistor requirements for LEDACT_LINK[0] and LEDDPX[2]/DPLX.
3. Changed pull-up resistor values for LEDs to 1–4.7 KΩ.
4. Maximum input voltage is 5.5 V; operating voltage for 5-V-tolerant pins is 5.0 V.
5. Minor edits.

Revision G to H

1. Final version
2. Corrected pull-up resistor value for LEDACT_LINK[2] to 1k–4.7KΩ.
3. Updated package drawing - some tolerances modified.

Revision H to I

1. Edited Temperature Range information under Ordering Information on page 5.

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