**CY24204**

# MediaClock™ DTV, STB Clock Generator

## Features

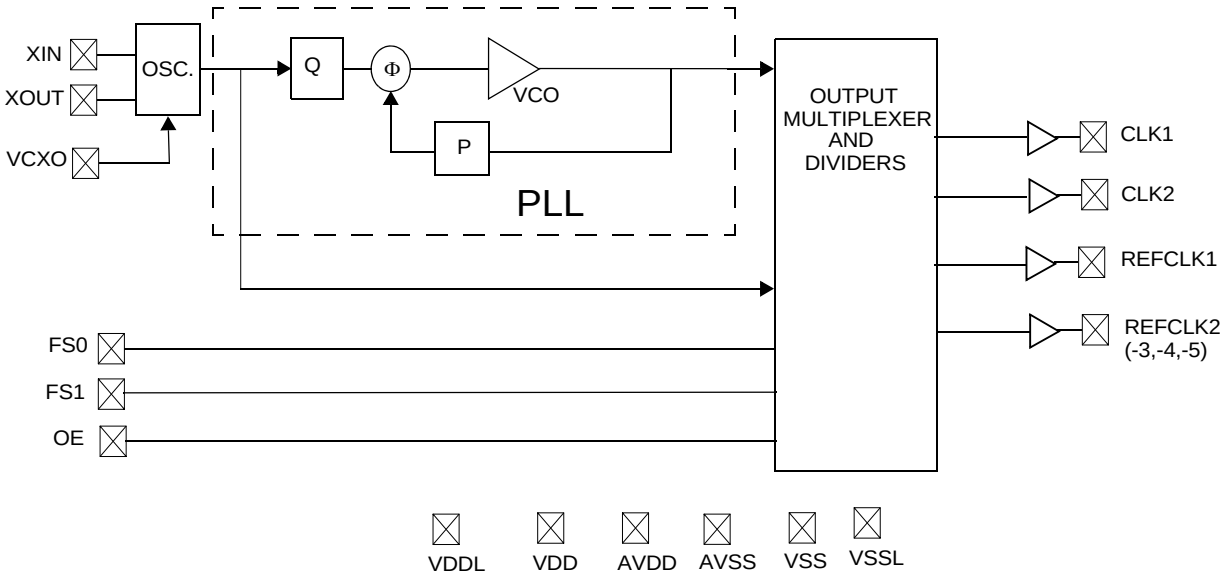
- Integrated phase-locked loop (PLL)
- Low jitter, high-accuracy outputs
- VCXO with Analog Adjust
- 3.3V operation

## Benefits

- Internal PLL with up to 400-MHz internal operation
- Meets critical timing requirements in complex system designs
- Large ±150-ppm range, better linearity
- Enables application compatibility

| Part Number | Outputs | Input Frequency | Output Frequency Range |
|---|---|---|---|
| CY24204-3 | 4 | 27-MHz Crystal Input | Two copies of 27-MHz reference clock output, two copies of 27/27.027/74.250/74.17582418 MHz (frequency selectable) |
| CY24204-4 | 4 | 27-MHz Crystal Input | Two copies of 27-MHz reference clock output, two copies of 27/27.027/74.250/74.17582418 MHz (frequency selectable, Increased VCXO pull range) |
| CY24204-5 | 4 | 27-MHz Crystal Input | Two copies of 27-MHz reference clock output, two copies of 27/27.027/74.250/74.17582418 MHz (frequency selectable, Increased output drive strength) |

## Logic Block Diagram



## Pin Configuration

**Figure 1. CY24204-3,4,5 16-Pin TSSOP**

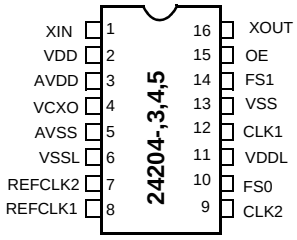



**Table 1. Pin Definition**

| Name | Pin Number | Description |
|---|---|---|
| XIN | 1 | Reference Crystal Input. |
| $V_{DD}$ | 2 | Voltage Supply. |
| $AV_{DD}$ | 3 | Analog Voltage Supply. |
| VCXO | 4 | Input Analog Control for VCXO. |
| $AV_{SS}$ | 5 | Analog Ground. |
| $V_{SSL}$ | 6 | CLK Ground. |
| REFCLK2 | 7 | Reference Clock Output. |
| REFCLK1 | 8 | Reference Clock Output. |
| CLK1 | 9 | 27/27.027/74.250/74.17582418-MHz Clock Output (Frequency Selectable). |
| FS0 | 10 | Frequency Select 0, Weak Internal Pull up. |
| $V_{DDL}$ | 11 | CLK Voltage Supply. |
| CLK2 | 12 | 27/27.027/74.250/74.17582418-MHz Clock Output (Frequency Selectable). |
| $V_{SS}$ | 13 | Ground. |
| FS1 | 14 | Frequency Select 1, Weak Internal Pull up. |
| OE | 15 | Output Enable, Weak Internal Pull up. |
| XOUT | 16 | Reference Crystal Output. |

## Frequency Select Options

| OE | FS1 | FS0 | CLK1/CLK2[1] | REFCLK 1/2 | Unit |
|---|---|---|---|---|---|
| 0 | 0 | 0 | off | 27 | MHz |
| 0 | 0 | 1 | off | 27 | MHz |
| 0 | 1 | 0 | off | 27 | MHz |
| 0 | 1 | 1 | off | 27 | MHz |
| 1 | 0 | 0 | 27 | 27 | MHz |
| 1 | 0 | 1 | 27.027 | 27 | MHz |
| 1 | 1 | 0 | 74.250 | 27 | MHz |
| 1 | 1 | 1 | 74.17582418 | 27 | MHz |

**Note**
1. “off” = output is driven HIGH.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Supply Voltage ($V_{DD}$, $AV_{DDL}$, $V_{DDL}$) .....–0.5 to +7.0V

DC Input Voltage .....–0.5V to $V_{DD}$ + 0.5

Storage Temperature (Non-Condensing).... –55°C to +125°C

Junction Temperature ..... –40°C to +125°C

Data Retention at Tj=125°C .....> 10 years

Package Power Dissipation..... 350 mW

ESD (Human Body Model) MIL-STD-883..... 2000V

## Pullable Crystal Specifications

| Parameter | Description | Comments | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{NOM}$ | Nominal crystal frequency | Parallel resonance, fundamental mode, AT cut | – | 27.0 | – | MHz |
| $C_{LNOM}$ | Nominal load capacitance | | – | 14 | – | pF |
| $R_1$ | Equivalent series resistance (ESR) | Fundamental mode | – | | 25 | Ω |
| $R_3/R_1$ | Ratio of third overtone mode ESR to fundamental mode ESR | Ratio used because typical $R_1$ values are much less than the maximum spec | 3 | – | – | |
| DL | Crystal drive level | No external series resistor assumed | – | 0.5 | 2 | mW |
| $F_{3SEPHI}$ | Third overtone separation from 3*$F_{NOM}$ | High side | 300 | – | – | ppm |
| $F_{3SEPLO}$ | Third overtone separation from 3*$F_{NOM}$ | Low side | – | – | –150 | ppm |
| $C_0$ | Crystal shunt capacitance | | – | – | 7 | pF |
| $C_0/C_1$ | Ratio of shunt to motional capacitance | | 180 | – | 250 | |
| $C_1$ | Crystal motional capacitance | | 14.4 | 18 | 21.6 | fF |

## Recommended Operating Conditions

| Parameter | Description | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}/AV_{DDL}/V_{DDL}$ | Operating Voltage | 3.135 | 3.3 | 3.465 | V |
| $T_A$ | Ambient Temperature | 0 | – | 70 | °C |
| $C_{LOAD}$ | Max. Load Capacitance | – | – | 15 | pF |
| $t_{PU}$ | Power up time for all $V_{DD}$s to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | – | 500 | ms |

## DC Electrical Specifications

| Parameter[1] | Name | Description | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OH1}$ | Output High Current for -3,-4, | $V_{OH} = V_{DD} – 0.5$, $V_{DD}/V_{DDL}$ = 3.3V | 12 | 24 | – | mA |
| $I_{OL1}$ | Output Low Current for -3,-4 | $V_{OL}$ = 0.5, $V_{DD}/V_{DDL}$ = 3.3V | 12 | 24 | – | mA |
| $I_{OH2}$ | Output High Current for -5 | $V_{OH} = V_{DD} – 0.5$, $V_{DD}/V_{DDL}$ = 3.3V | 18 | 26 | – | mA |
| $I_{OL2}$ | Output Low Current for -5 | $V_{OL}$ = 0.5, $V_{DD}/V_{DDL}$ = 3.3V | 18 | 26 | – | mA |
| $V_{IH}$ | Input High Voltage | CMOS levels, 70% of $V_{DD}$ | 0.7 | – | – | $V_{DD}$ |
| $V_{IL}$ | Input Low Voltage | CMOS levels, 30% of $V_{DD}$ | – | – | 0.3 | $V_{DD}$ |
| $I_{VDD}$ | Supply Current | $AV_{DD}/V_{DD}$ Current | – | – | 25 | mA |
| $I_{VDDL}$ | Supply Current | $V_{DDL}$ Current ($V_{DDL}$ = 3.47V) | – | – | 20 | mA |
| $C_{IN}$ | Input Capacitance | | – | – | 7 | pF |

**Note**
1. Not 100% tested.

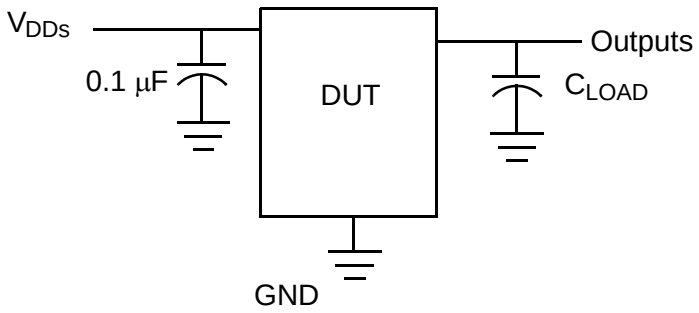
## DC Electrical Specifications (continued)

| Parameter[1] | Name | Description | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{\Delta XO}$ | $V_{CXO}$ pullability range | Nominal pullability for -3,-5 | ±150 | – | – | ppm |
| $f_{\Delta XO}$ | $V_{CXO}$ pullability range | Extended pullability for -4 | – | ±200 | – | ppm |
| $V_{VCXO}$ | $V_{CXO}$ input range | | 0 | – | $V_{DD}$ | V |
| $R_{UP}$ | Pull up resistor on inputs | $V_{DD}$ = 3.14 to 3.47V, measured at $V_{IN}$ = 0V | – | 100 | 150 | kΩ |

## AC Electrical Specifications

| Parameter[1] | Name | Description | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| DC | Output Duty Cycle | Duty Cycle is defined in Figure 3; t1/t2, 50% of $V_{DD}$ | 45 | 50 | 55 | % |
| $ER_1$ | Rising Edge Rate for -3,-4 | Output Clock Edge Rate, Measured from 20% to 80% of $V_{DD}$, $C_{LOAD}$ = 15 pF See Figure 4. | 0.8 | 1.4 | – | V/ns |
| $EF_1$ | Falling Edge Rate for -3,-4 | Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD}$, $C_{LOAD}$ = 15 pF See Figure 4. | 0.8 | 1.4 | – | V/ns |
| $ER_2$ | Rising Edge Rate for -5 | Output Clock Edge Rate, Measured from 20% to 80% of $V_{DD}$, $C_{LOAD}$ = 15 pF See Figure 4. | 1.0 | 1.8 | – | V/ns |
| $EF_2$ | Falling Edge Rate for -5 | Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD}$, $C_{LOAD}$ = 15 pF See Figure 4. | 1.0 | 1.8 | – | V/ns |
| $t_9$ | Clock Jitter | CLK1, CLK2 Peak-Peak period jitter | – | 120 | – | ps |
| $t_{10}$ | PLL Lock Time | | – | – | 3 | ms |

**Figure 2. Test and Measurement Setup**




## Voltage and Timing Definitions

**Figure 3. Duty Cycle Definition**

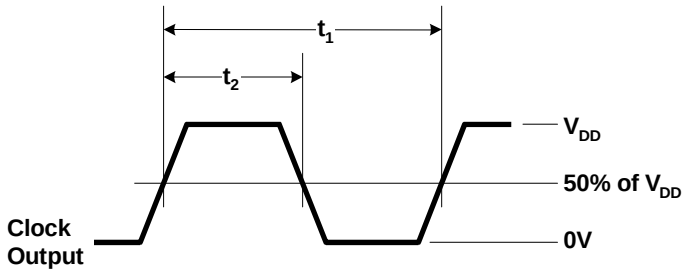
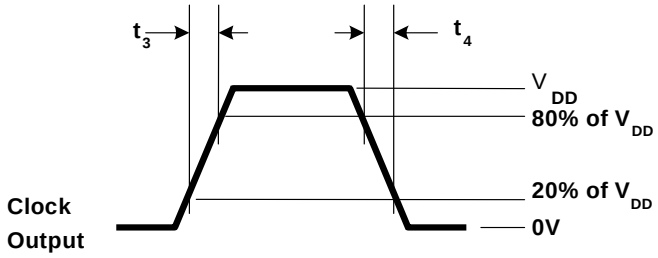


Figure 4. ER = (0.6 x $V_{DD}$) /t3, EF = (0.6 x $V_{DD}$) /t4



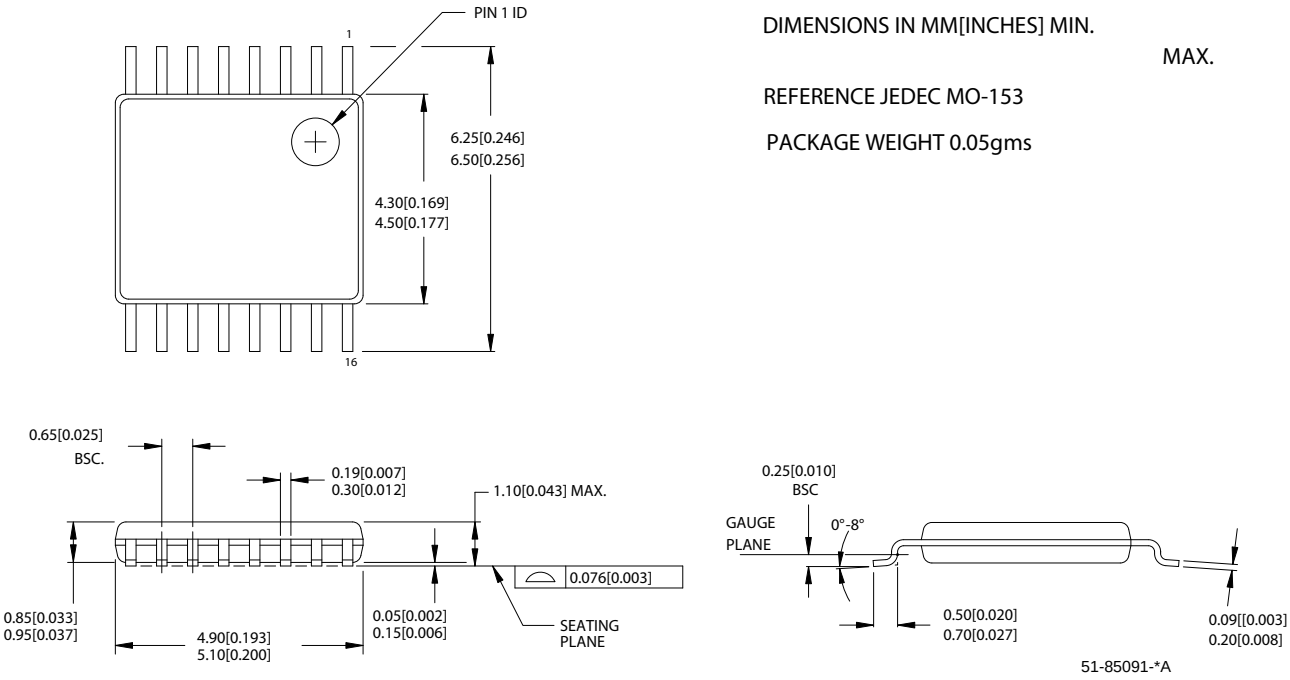

## Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range | Operating Voltage |
|---|---|---|---|---|
| **Pb-Free** | | | | |
| CY24204ZXC-3[2] | ZZ16 | 16-Pin TSSOP | Commercial | 3.3V |
| CY24204ZXC-3T[2] | ZZ16 | 16-Pin TSSOP-Tape and Reel | Commercial | 3.3V |
| CY24204ZXC-4[2] | ZZ16 | 16-Pin TSSOP | Commercial | 3.3V |
| CY24204ZXC-4T[2] | ZZ16 | 16-Pin TSSOP-Tape and Reel | Commercial | 3.3V |
| CY24204ZXC-5[2] | ZZ16 | 16-Pin TSSOP | Commercial | 3.3V |
| CY24204ZXC-5T[2] | ZZ16 | 16-Pin TSSOP-Tape and Reel | Commercial | 3.3V |
| CY24204KZXC-3 | ZZ16 | 16-Pin TSSOP | Commercial | 3.3V |
| CY24204KZXC-3T | ZZ16 | 16-Pin TSSOP-Tape and Reel | Commercial | 3.3V |

**Note**
2. Not recommended for new designs.

## Package Drawing

**Figure 5. 16-Lead TSSOP 4.40mm Body 16.173**



## Document History Page

| Document Title: CY24204 MediaClock™ DTV, STB Clock Generator<br>Document Number: 38-07450 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 123842 | 04/10/03 | CKN | New Data Sheet |
| *A | 128775 | 09/0803 | IJA | Added -4 and -5 parts |
| *B | 214080 | See ECN | RGL | Added -6 part |
| *C | 310573 | See ECN | RGL | Removed -1,-2 and -6 parts<br>Added Lead-free devices for -3, -4, and -5 parts |
| *D | 2440886 | See ECN | KVM/AESA | Updated template. Added Note “Not recommended for new designs.”<br>Added part number CY24204KZXC-3, and CY24204KZXC-3T in ordering information table.<br>Removed non-Pb-free part numbers (those beginning CY24204ZC).<br>Replaced “Lead-free” with “Pb-Free”. |

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