CY2DP1510

1:10 LVPECL Fanout Buffer with Selectable Clock Input

Features

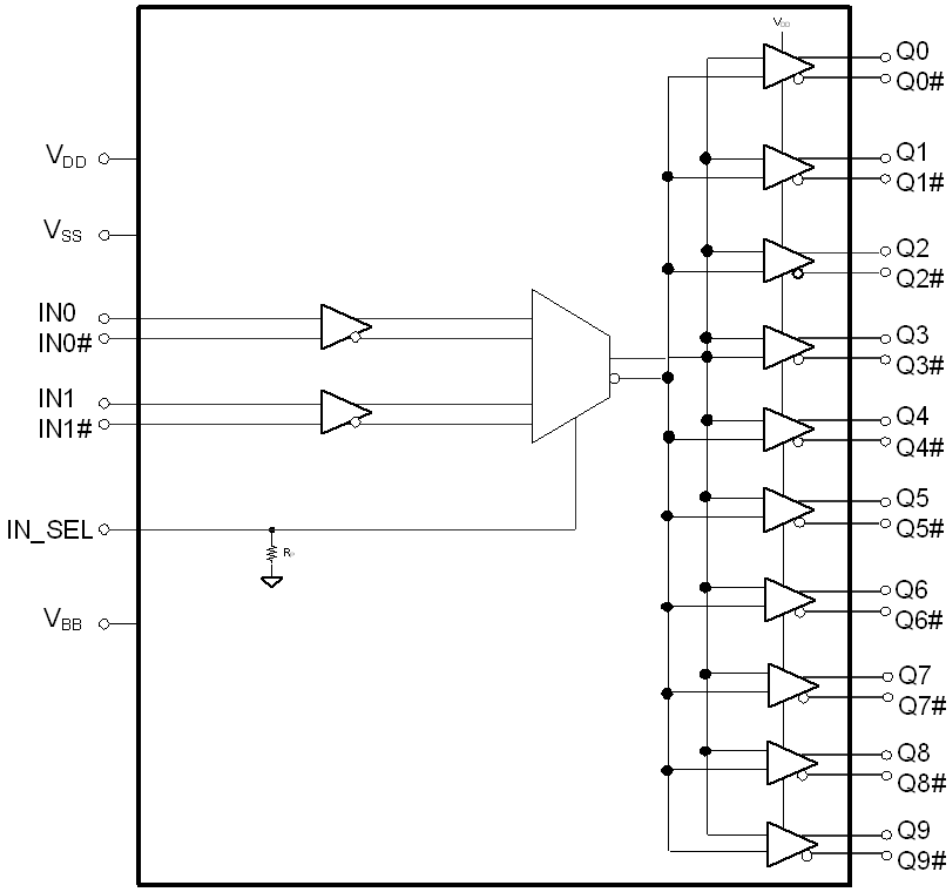
- Select one of two differential (LVPECL, LVDS, HCSL, or CML) input pairs to distribute to 10 LVPECL output pairs
- Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on INx# input
- 40-ps maximum output-to-output skew
- 600-ps maximum propagation delay
- 0.11-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 1.5-GHz operation
- 32-pin thin quad flat pack (TQFP) package
- 2.5-V or 3.3-V operating voltage [1]
- Commercial and industrial operating temperature range

Functional Description

The CY2DP1510 is an ultra-low noise, low skew, low-propagation delay 1:10 LVPECL fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2DP1510 can select between two separate differential (LVPECL, LVDS, HCSL, or CML) input clock pairs using the IN_SEL pin. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 1.5 GHz.

For a complete list of related documentation, click here.

Logic Block Diagram

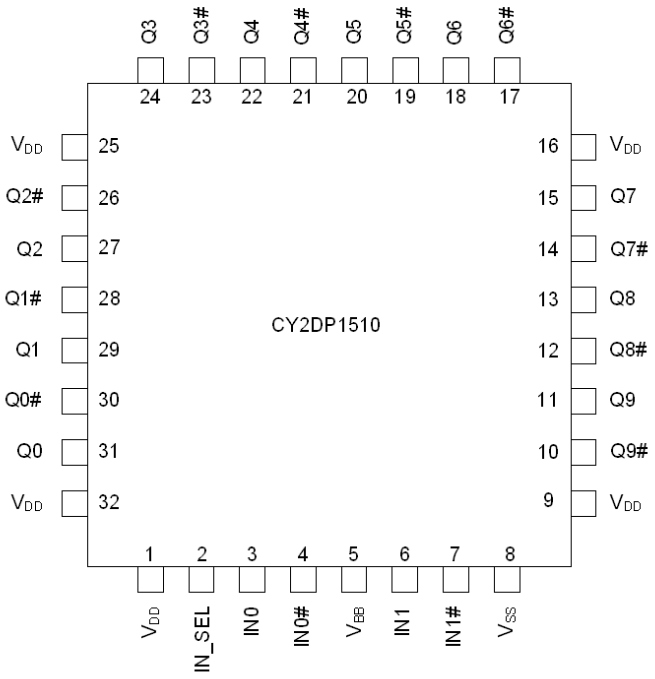


Note
1. Input AC-coupling capacitors are required for voltage-translation applications.

Contents

Pin Configuration

Figure 1. 32-pin TQFP (7 × 7 × 1.0 mm) pinout



Pin Definitions

Pin No.	Pin Name	Pin Type	Description
1, 9, 16, 25, 32	V_{DD}	Power	Power supply
2	IN_SEL	Input	Input clock select pin. Low-voltage complementary metal oxide semiconductor (LVCMOS)/low-voltage transistor-transistor-logic (LVTTL). When IN_SEL = Low, the IN0/IN0# differential input pair is active When IN_SEL = High, the IN1/IN1# differential input pair is active
3	IN0	Input	Differential (LVPECL, LVDS, HCSL, or CML) input clock. Active when IN_SEL = Low
4	IN0#	Input	Differential (LVPECL, LVDS, HCSL, or CML) complementary input clock. Active when IN_SEL = Low
5	V_{BB}	Output	LVPECL reference voltage output
6	IN1	Input	Differential (LVPECL, LVDS, HCSL, or CML) input clock. Active when IN_SEL = High
7	IN1#	Input	Differential (LVPECL, LVDS, HCSL, or CML) complementary input clock. Active when IN_SEL = High
8	V_{SS}	Power	Ground
10, 12, 14, 17, 19, 21, 23, 26, 28, 30	Q(0:9)#	Output	LVPECL complementary output clocks
11, 13, 15, 18, 20, 22, 24, 27, 29, 31	Q(0:9)	Output	LVPECL output clocks
–	EPAD	–	Exposed paddle. Connect to ground plane for package heat dissipation. No electrical connection.

Absolute Maximum Ratings

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	Nonfunctional	–0.5	4.6	V
V_{IN}[2]	Input voltage, relative to V_{SS}	Nonfunctional	–0.5	Lesser of 4.0 or V_{DD} + 0.4	V
V_{OUT}[2]	DC output or I/O voltage, relative to V_{SS}	Nonfunctional	–0.5	Lesser of 4.0 or V_{DD} + 0.4	V
T_S	Storage temperature	Nonfunctional	–55	150	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection (Human body model)	JEDEC STD 22-A114-B	2000	–	V
L_U	Latch up		Meets or exceeds JEDEC Spec JESD78B IC latch up test		
UL–94	Flammability rating	At 1/8 in	V – 0		
MSL	Moisture sensitivity level		3		

Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.5-V supply	2.375	2.625	V
		3.3-V supply	3.135	3.465	V
T_A	Ambient operating temperature	Commercial	0	70	°C
		Industrial	–40	85	°C
t_{PU}	Power ramp time	Power-up time for V_{DD} to reach minimum specified voltage (power ramp must be monotonic).	0.05	500	ms

Note
2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is not required.

DC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Max	Unit
I_{DD}	Operating supply current	All LVPECL outputs floating (internal I_{DD})	–	120	mA
V_{IH1}	Input high voltage, differential input clocks IN0 and IN0#, IN1 and IN1#		–	V_{DD} + 0.3	V
V_{IL1}	Input low voltage, differential input clocks IN0 and IN0#, IN1 and IN1#		–0.3	–	V
V_{IH2}	Input high voltage, IN_SEL	V_{DD} = 3.3 V	2.0	V_{DD} + 0.3	V
V_{IL2}	Input low voltage, IN_SEL	V_{DD} = 3.3 V	–0.3	0.8	V
V_{IH3}	Input high voltage, IN_SEL	V_{DD} = 2.5 V	1.7	V_{DD} + 0.3	V
V_{IL3}	Input low voltage, IN_SEL	V_{DD} = 2.5 V	–0.3	0.7	V
V_{ID} [3]	Input differential amplitude	See Figure 2 on page 8	0.4	1.0	V
V_{ICM}	Input common mode voltage	See Figure 2 on page 8	0.2	V_{DD} – 0.2	V
I_{IH}	Input high current, All inputs	Input = V_{DD} [4]	–	150	µA
I_{IL}	Input low current, All inputs	Input = V_{SS} [4]	–150	–	µA
V_{OH}	LVPECL output high voltage	Terminated with 50 Ω to V_{DD} – 2.0 [5]	V_{DD} – 1.20	V_{DD} – 0.70	V
V_{OL}	LVPECL output low voltage	Terminated with 50 Ω to V_{DD} – 2.0 [5]	V_{DD} – 2.0	V_{DD} – 1.63	V
V_{BB}	Output reference voltage	0 to 150 µA output current	V_{DD} – 1.40	V_{DD} – 1.16	V
R_P	Internal pull-down resistance	IN_SEL pin	60	165	kΩ
C_{IN}	Input capacitance	Measured at 10 MHz; per pin	–	3	pF

Thermal Resistance

Parameter [6]	Description	Test Conditions	32-pin TQFP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	45	°C/W
θ_{JC}	Thermal resistance (junction to case)		14	°C/W

Notes
3. V_{ID} minimum of 400 mV is required to meet all output AC electrical specifications. The device is functional with V_{ID} minimum of greater than 200 mV.
4. Positive current flows into the input pin, negative current flows out of the input pin.
5. Refer to Figure 3 on page 8.
6. These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{IN}	Input frequency	Differential Input	DC	–	1.5	GHz
		Single ended input [7]	DC	–	250	MHz
F_{OUT}	Output frequency	F_{OUT} = F_{IN}, Differential Input	DC	–	1.5	GHz
		F_{OUT} = F_{IN}, Single ended input [7]	DC		250	MHz
V_{PP}	LVPECL differential output voltage peak to peak, single ended. Terminated with 50 Ω to V_{DD} – 2.0 [8]	Fout = DC to 150 MHz	600	–	–	mV
		Fout ≥150 MHz to 1.5 GHz	400	–	–	mV
t_{PD} [9]	Propagation delay differential input pair to differential output pair	Input rise/fall time < 1.5 ns (20% to 80%)	–	–	600	ps
t_{ODC} [10]	Output duty cycle	50% duty cycle at input, Frequency range up to 1 GHz, Differential input	48	–	52	%
		50% duty cycle at input, Frequency range up to 250 MHz, Single ended input [7]	45	–	55	%
t_{SK1} [11]	Output-to-output skew	Any output to any output, with same load conditions at DUT	–	–	40	ps
t_{SK1D} [11]	Device-to-device output skew	Any output to any output between two or more devices. Devices must have the same input and have the same output load.	–	–	150	ps
PN_{ADD}	Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV or Input Swing = 3.0 V [7]	Offset = 1 kHz	–	–	–120	dBc/Hz
		Offset = 10 kHz	–	–	–130	dBc/Hz
		Offset = 100 kHz	–	–	–140	dBc/Hz
		Offset = 1 MHz	–	–	–150	dBc/Hz
		Offset = 10 MHz	–	–	–154	dBc/Hz
		Offset = 20 MHz	–	–	–155	dBc/Hz

Notes
7. Refer to Application Information on page 10.
8. Refer to Figure 3 on page 8.
9. Refer to Figure 4 on page 8.
10. Refer to Figure 5 on page 8.
11. Refer to Figure 6 on page 9.

AC Electrical Specifications (continued)

(V_{DD} = 3.3 V ± 5% or 2.5 V ± 5%; T_A = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

Parameter	Description	Condition	Min	Typ	Max	Unit
t_{JIT} [12]	Additive RMS phase jitter (Random)	156.25 MHz, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV	–	0.043	0.11	ps
		156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V [13]	–	0.05	0.11	ps
t_R, t_F [14]	Output rise/fall time	50% duty cycle at input, 20% to 80% of full swing (V_{OL} to V_{OH}), Input rise/fall time < 1.5 ns (20% to 80%)	–	–	300	ps

Notes
12. Refer to Figure 7 on page 9.
13. Refer to Application Information on page 10.
14. Refer to Figure 8 on page 9.

Switching Waveforms

Figure 2. Input Differential and Common Mode Voltages

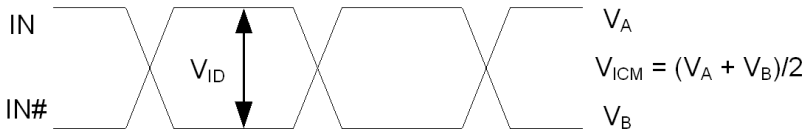


Figure 3. Output Differential Voltage

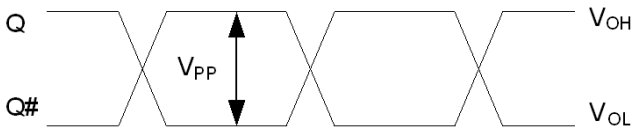


Figure 4. Input to Any Output Pair Propagation Delay

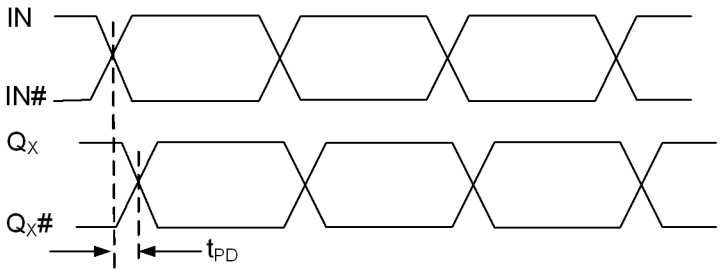
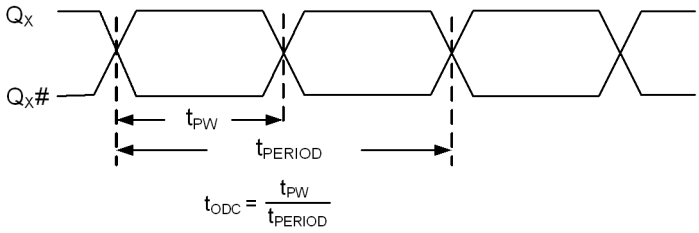


Figure 5. Output Duty Cycle



Switching Waveforms (continued)

Figure 6. Output-to-Output and Device-to-Device Skew

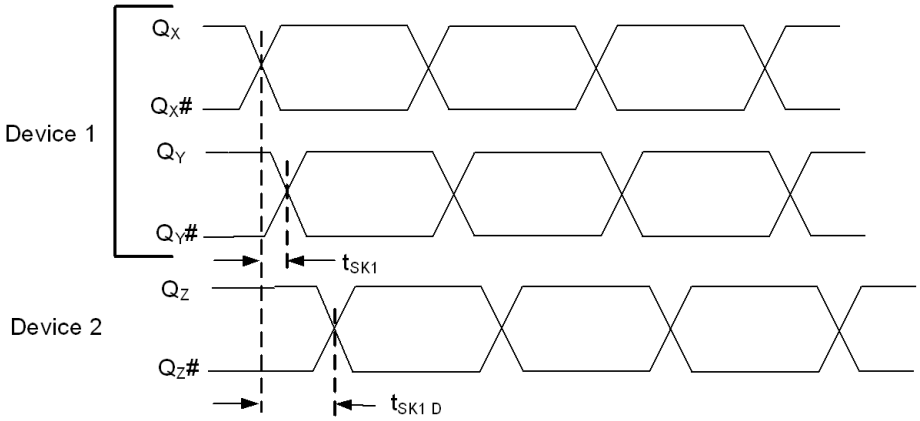


Figure 7. RMS Phase Jitter

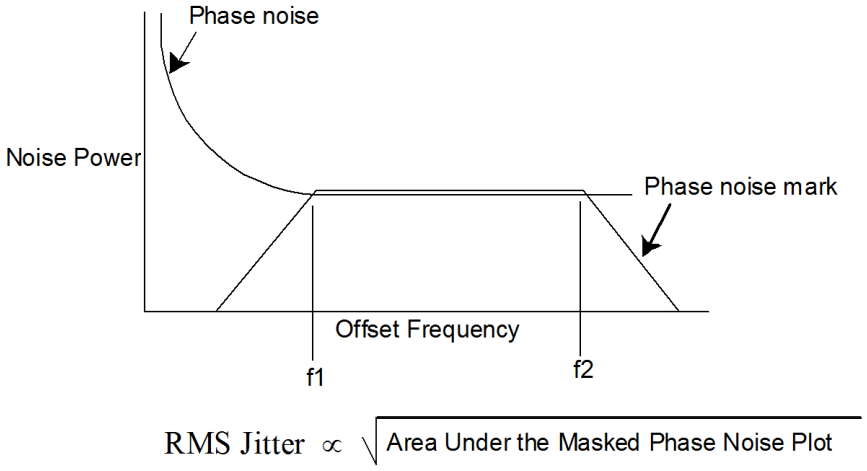
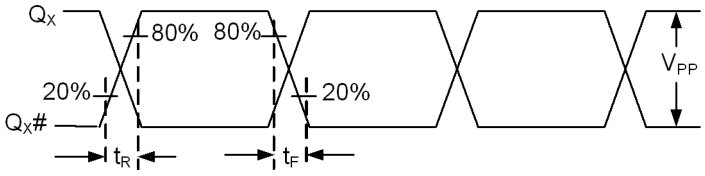


Figure 8. Output Rise/Fall Time



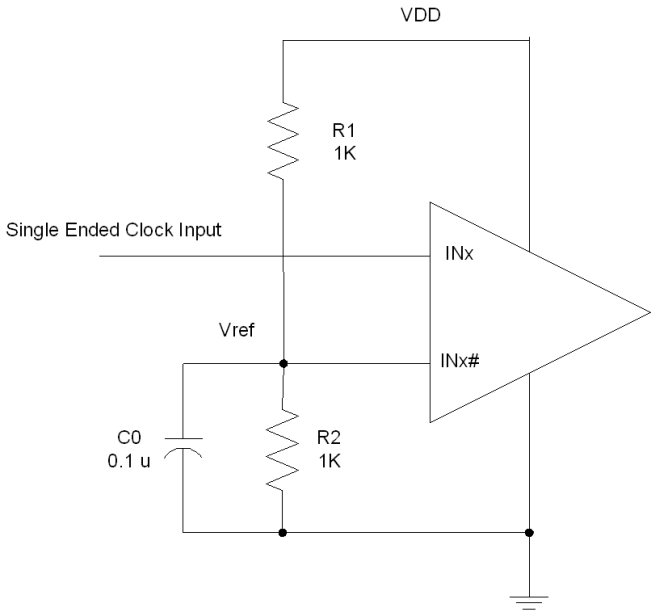
Application Information

CY2DP1510 can be used with a single ended CMOS input by biasing the Complementary Input Clock (INx#). “True” input pins (INx) of differential input pair can be fed with a single ended CMOS input signal. The “complementary” input pin (INx#) of the same differential input pair can be biased with Vref.

Figure 9 shows the schematic which can be used to give single ended CMOS input to the CY2DP1510.

The reference voltage Vref = VDD/2 is generated by the bias resistors R1, R2 and capacitor C0. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the Vref in the center of the input voltage swing. For example, if the input clock swing is 2.5 V and VDD = 3.3 V, Vref should be 1.25 V and R2/R1 = 0.609.

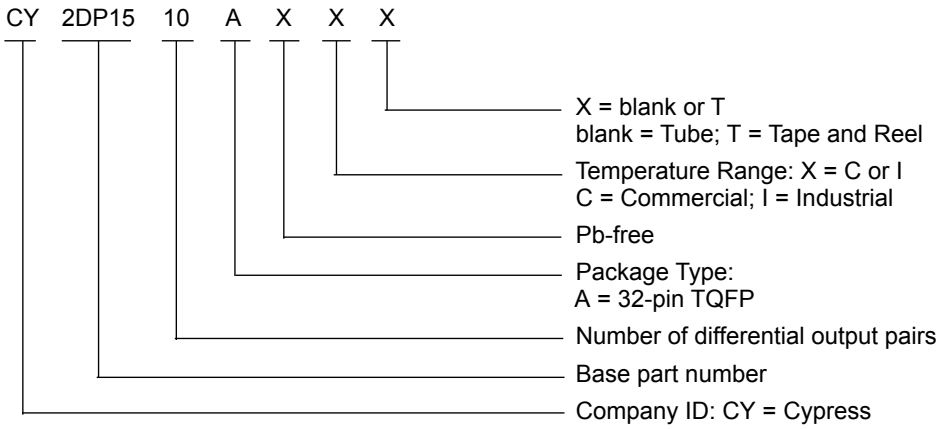
Figure 9. Single ended CMOS input given to the CY2DP1510



Ordering Information

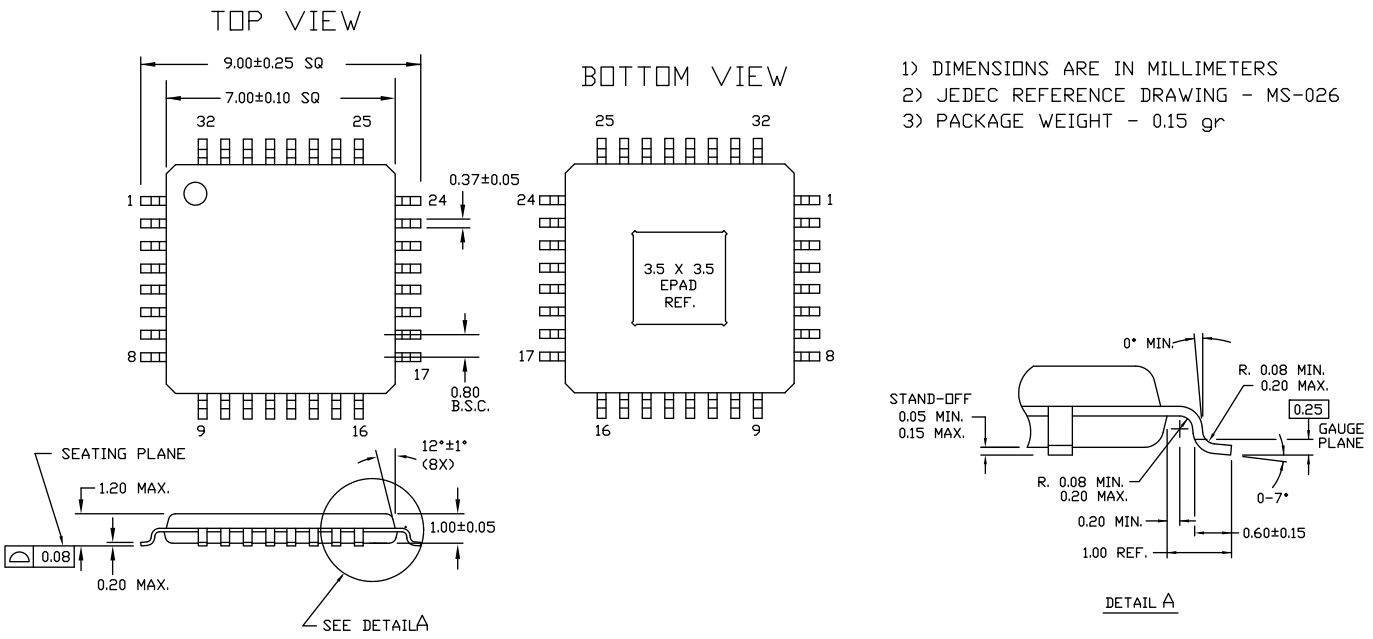
Part Number	Type	Production Flow
Pb-free		
CY2DP1510AXC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY2DP1510AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to 70 °C
CY2DP1510AXI	32-pin TQFP	Industrial, –40 °C to 85 °C
CY2DP1510AXIT	32-pin TQFP – Tape and Reel	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Package Diagram

Figure 10. 32-pin TQFP (7 × 7 × 1.0 mm) AE32A (3.5 × 3.5 E-Pad) Package Outline, 001-54497



Acronyms

Acronym	Description
CML	Current Mode Logic
ESD	Electrostatic Discharge
HBM	Human Body Model
HCSL	High-Speed Current Steering Logic
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LVDS	Low-Voltage Differential Signal
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
LVTTL	Low-Voltage Transistor-Transistor Logic
RMS	Root Mean Square
TQFP	Thin Quad Flat Pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dBc	decibels relative to the carrier
GHz	gigahertz
Hz	hertz
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY2DP1510, 1:10 LVPECL Fanout Buffer with Selectable Clock Input Document Number: 001-55566				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2782891	CXQ	10/09/09	New data sheet.
*A	2838916	CXQ	01/05/2010	Changed status from “ADVANCE” to “PRELIMINARY”. Updated Features (changed from 0.34 ps to 0.25 ps maximum additive jitter). Updated Operating Conditions (added t_{PU} parameter). Updated DC Electrical Specifications (changed minimum value of V_{OH} parameter from V_{DD} – 1.15 V to V_{DD} – 1.20 V; changed maximum value of V_{OH} parameter from V_{DD} – 0.75 V to V_{DD} – 0.70 V, removed V_{OD} parameter, changed maximum value of V_{BB} parameter from V_{DD} – 1.38 V to V_{DD} – 1.40 V, Added R_P parameter and its details (minimum value = 60 kΩ, maximum value = 140 kΩ), added a measurement definition for C_{IN} parameter). Updated AC Electrical Specifications (Added V_{PP} parameter and its details (minimum value = 600 mV for F_{out} = DC to 150 MHz and minimum value = 400 mV for F_{out} = 150 MHz to 1.5 GHz), changed letter case and some names of all the timing parameters to be consistent with EROS, lowered all additive phase noise mask parameters by 3 dB, changed maximum value of t_{JIT} parameter from 0.34 ps to 0.25 ps, added condition to t_R and t_F parameters that input rise/fall time must be less than 1.5 ns (20% to 80%)). Changed letter case and some names of all the timing parameters in Figure 3, Figure 4, Figure 5, Figure 6 and Figure 8, to be consistent with EROS.
*B	2885033	CXQ	02/26/2010	Updated Package Diagram (32-pin TQFP).
*C	3011766	CXQ	08/23/2010	Updated Features (changed from 0.25 ps to 0.11 ps maximum additive jitter). Updated Functional Description (removed reference to data distribution). Updated Logic Block Diagram (changed R_P for differential inputs from 100 kΩ to 150 kΩ). Updated Pin Definitions (added description of EPAD). Updated DC Electrical Specifications (added maximum value of V_{ID} parameter (1.0 V), added note 4 to describe I_{IH} and I_{IL} parameters, changed maximum value of V_{BB} parameter from V_{DD} – 1.26 V to V_{DD} – 1.16 V, changed maximum value of R_P parameter from 140 kΩ to 210 kΩ, changed minimum value of R_P parameter from 60 kΩ to 90 kΩ). Updated AC Electrical Specifications (changed maximum value of t_{PD} parameter from 480 ps to 600 ps, added “Frequency range up to 1 GHz” condition to t_{ODC} parameter, changed phase noise parameters for 1 k / 10 k / 100 k / 1 M / 10 M / 20 MHz offset to –120 / –130 / –135 / –150 / –150 / –150 dBc/Hz, respectively, changed maximum value of t_{JIT} parameter from 0.25 ps to 0.11 ps). Updated Package Diagram (To 001-54497 to reflect use of EPAD package). Added Ordering Code Definitions. Added Acronyms and Units of Measure.
*D	3017258	CXQ	08/27/2010	Updated Figure 8 (Corrected Output Rise/Fall time diagram).
*E	3100234	CXQ	11/18/2010	Updated Absolute Maximum Ratings (changed maximum value of V_{IN} and V_{OUT} parameters from 4.0 V to “lesser of 4.0 or V_{DD} + 0.4”, removed minimum value of L_U parameter (200 mA), replaced minimum value and maximum value of L_U parameter with “Meets or exceeds JEDEC Spec JESD78B IC Latch up Test”. Updated DC Electrical Specifications (removed R_P parameter for differential input clock pins IN_X and IN_X#, changed C_{IN} parameter condition to “Measured at 10 MHz”). Updated AC Electrical Specifications (changed PN_{ADD} parameters for 100 kHz, 10 MHz, and 20 MHz offsets).

Document History Page (continued)

Document Title: CY2DP1510, 1:10 LVPECL Fanout Buffer with Selectable Clock Input Document Number: 001-55566				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*F	3135201	CXQ	01/12/2011	Changed status from "PRELIMINARY" to "FINAL". Updated Logic Block Diagram (Removed pull-up/pull-down resistors from IN_x/IN_x# pins).
*G	3090938	CXQ	02/25/2011	Post to external web.
*H	3208609	CXQ	03/29/2011	Updated Logic Block Diagram (changed maximum value of R_P parameter from 140 kΩ to 165 kΩ). Updated DC Electrical Specifications (changed maximum value of R_P parameter from 140 kΩ to 165 kΩ).
*I	3273648	CXQ	06/03/2011	Updated Features (changed supported differential input clock types to include LVDS and CML). Updated Functional Description (changed supported differential input clock types to include LVDS and CML). Updated Pin Definitions (changed supported differential input clock types to include LVDS and CML).
*J	3280992	CXQ	06/12/2011	No technical updates.
*K	3395868	PURU	10/05/11	Updated Features (changed supported differential input clock types to include HCSL). Updated Pin Configuration (changed supported differential input clock types to include HCSL). Updated DC Electrical Specifications (changed minimum value of V_{ICM} parameter).
*L	3443943	BASH	11/21/2011	Updated AC Electrical Specifications (Added typical value of t_{JIT} parameter). Updated in new template.
*M	3775718	PURU	10/12/2012	Updated Features (Added "Translates any single-ended input signal to 3.3 V LVPECL levels with resistor bias on INx# input"). Updated AC Electrical Specifications: Added Note 7 and Note 13. Added F_{IN} parameter values for "Single Ended Input" condition (Minimum value = DC, Maximum value = 250 MHz). Added F_{OUT} parameter values for "Single Ended Input" condition (Minimum value = DC, Maximum value = 250 MHz). Added t_{ODC} parameter values for "Single Ended Input" condition (Mininmum value = 45%, Maximum value = 55%). Updated Description of PN_{ADD} parameter (Replaced "Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV" with "Additive RMS phase noise, 156.25-MHz input, Rise/fall time < 150 ps (20% to 80%), V_{ID} > 400 mV or Input Swing = 3.0 V[7]"). Added t_{JIT} parameter values for the Condition "156.25 MHz Sinewave, 12 kHz to 20 MHz offset, input rise/fall time < 150 ps (20% to 80%), Input Swing = 3.0 V [13]" (Typical value = 0.05 ps and Maximum value = 0.11 ps). Added Application Information.
*N	3945010	CINM	03/26/2013	No technical updates. Completing Sunset Review.
*O	4587303	CINM	12/04/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Package Diagram: spec 001-54497 – Changed revision from *A to *B.
*P	5264122	TAVA	05/09/2016	Updated to new template. Completing Sunset Review.
*Q	5275805	PSR	05/18/2016	Added Thermal Resistance.

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