

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 1 μ A
 - Maximum standby current: 4 μ A
- Ultra low active power
 - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with \overline{CE} , and \overline{OE} features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-Pin thin small outline package (TSOP) II package

Functional Description

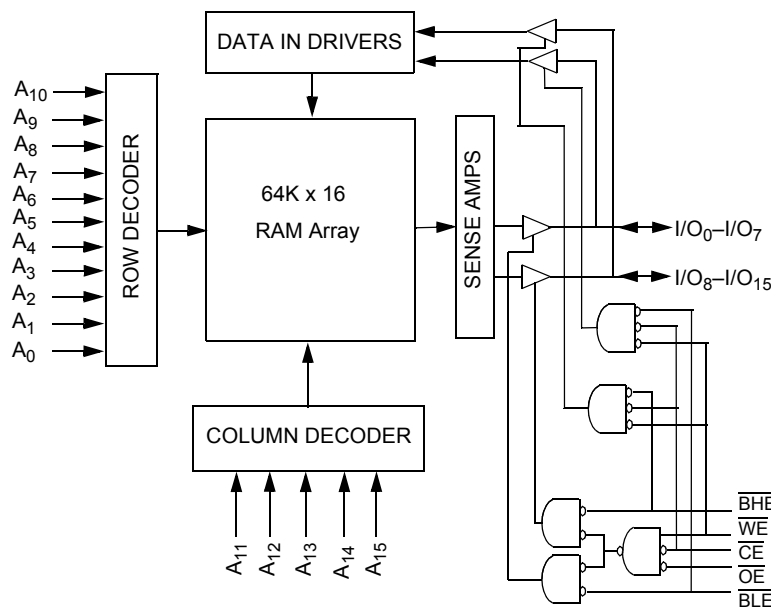
The CY62126ESL is a high performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable

applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99 percent when deselected (\overline{CE} HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₅). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₅).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

Logic Block Diagram



Contents

Pin Configuration	3	Ordering Information	12
Product Portfolio	3	Ordering Code Definitions	12
Maximum Ratings	4	Package Diagram	13
Operating Range	4	Acronyms	14
Electrical Characteristics	4	Document Conventions	14
Capacitance	5	Units of Measure	14
Thermal Resistance	5	Document History Page	15
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	16
Data Retention Characteristics	6	Worldwide Sales and Design Support	16
Data Retention Waveform	6	Products	16
Switching Characteristics	7	PSoC [®] Solutions	16
Switching Waveforms	8	Cypress Developer Community	16
Truth Table	11	Technical Support	16

Pin Configuration

44-pin TSOP II pinout (Top View)^[1]

A ₄	1	44	A ₅
A ₃	2	43	A ₆
A ₂	3	42	A ₇
A ₁	4	41	OE
A ₀	5	40	BHE
CE	6	39	BLE
I/O ₀	7	38	I/O ₁₅
I/O ₁	8	37	I/O ₁₄
I/O ₂	9	36	I/O ₁₃
I/O ₃	10	35	I/O ₁₂
V _{CC}	11	34	V _{SS}
V _{SS}	12	33	V _{CC}
I/O ₄	13	32	I/O ₁₁
I/O ₅	14	31	I/O ₁₀
I/O ₆	15	30	I/O ₉
I/O ₇	16	29	I/O ₈
WE	17	28	NC
A ₁₅	18	27	A ₈
A ₁₄	19	26	A ₉
A ₁₃	20	25	A ₁₀
A ₁₂	21	24	A ₁₁
NC	22	23	NC

Product Portfolio

Product	Range	V _{CC} Range (V) ^[2]	Speed (ns)	Current Consumption					
				Operating I _{CC} (mA)				Standby, I _{SB2} (μA)	
				f = 1 MHz		f = f _{max}			
				Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max
CY62126ESL	Automotive-A	2.2 V–3.6 V and 4.5 V–5.5 V	45	1.3	2	11	16	1	4

Notes

1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V_{CC} in the range of 3.6 V to 4.5 V.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	55 °C to +125 °C
Supply voltage to ground potential [4, 5]	-0.5 V to 6.0 V
DC voltage applied to outputs in High Z state [4, 5]	-0.5 V to 6.0 V
DC input voltage [4, 5]	-0.5 V to 6.0 V

Output current into outputs (low)	20 mA
Static discharge voltage (MIL-STD-883, method 3015)	> 2001 V
Latch-up current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} [6]
CY62126ESL	Automotive-A	-40 °C to +85 °C	2.2 V–3.6 V, and 4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit	
			Min	Typ [7]	Max		
V _{OH}	Output high voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OH} = -0.1 mA	2.0	-	-	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OH} = -1.0 mA	2.4	-	-	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OH} = -1.0 mA	2.4	-	-	
V _{OL}	Output low voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OL} = 0.1 mA	-	-	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OL} = 2.1 mA	-	-	0.4	
		4.5 ≤ V _{CC} ≤ 5.5	I _{OL} = 2.1 mA	-	-	0.4	
V _{IH}	Input high voltage	2.2 ≤ V _{CC} ≤ 2.7		1.8	-	V _{CC} + 0.3	V
		2.7 ≤ V _{CC} ≤ 3.6		2.2	-	V _{CC} + 0.3	
		4.5 ≤ V _{CC} ≤ 5.5		2.2	-	V _{CC} + 0.5	
V _{IL}	Input low voltage	2.2 ≤ V _{CC} ≤ 2.7		-0.3	-	0.6	V
		2.7 ≤ V _{CC} ≤ 3.6		-0.3	-	0.8	
		4.5 ≤ V _{CC} ≤ 5.5		-0.5	-	0.8	
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}		-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , Output disabled		-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{max} = 1/t _{RC}	V _{CC} = V _{CCmax} , I _{OUT} = 0 mA, CMOS levels	-	11	16	mA
		f = 1 MHz		-	1.3	2.0	
I _{SB1}	Automatic CE power-down current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, f = f _{max} (address and data only), f = 0 (\overline{OE} and \overline{WE}), V _{CC} = V _{CC(max)}		-	1	4	μA
I _{SB2} [8]	Automatic CE power-down current — CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, f = 0, V _{CC} = V _{CC(max)}		-	1	4	μA

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- Chip enable (CE) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

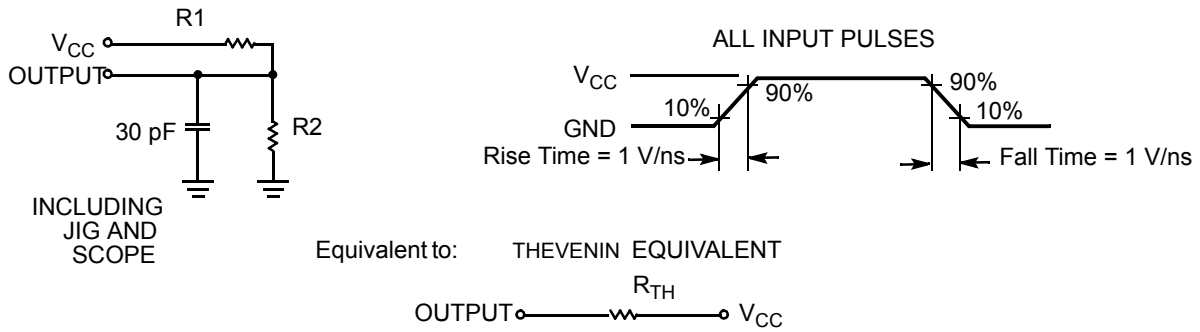
Parameter ^[9]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[9]	Description	Test Conditions	TSOP II	Unit
θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	28.2	°C/W
θ _{JC}	Thermal resistance (junction to case)		3.4	°C/W

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	5.0 V	Unit
R ₁	16600	1103	1800	Ω
R ₂	15400	1554	990	Ω
R _{TH}	8000	645	639	Ω
V _{TH}	1.2	1.75	1.77	V

Note

9. Tested initially and after any design or process changes that may affect these parameters.

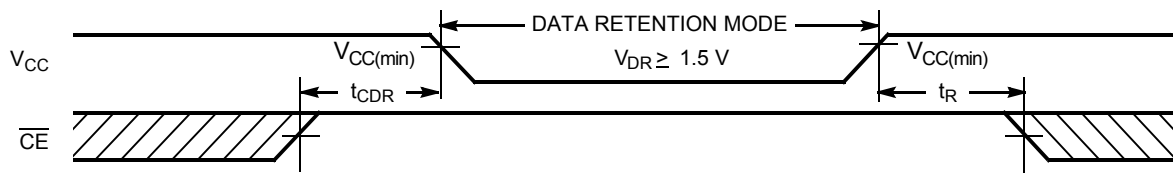
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
$I_{CCDR}^{[11]}$	Data retention current	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	3	μA
$t_{CDR}^{[12]}$	Chip deselect to data retention time		0	–	–	ns
$t_R^{[13]}$	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 2. Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ }^\circ\text{C}$.
11. Chip enable (\overline{CE}) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[15]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[15, 16]	–	18	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[15]	10	–	ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[15, 16]	–	18	ns
t_{PU}	\overline{CE} LOW to power up	0	–	ns
t_{PD}	\overline{CE} HIGH to power up	–	45	ns
t_{DBE}	$\overline{BHE} / \overline{BLE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BHE} / \overline{BLE}$ LOW to Low Z ^[15]	5	–	ns
t_{HZBE}	$\overline{BHE} / \overline{BLE}$ HIGH to High Z ^[15, 16]	–	18	ns
Write Cycle ^[17, 18]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE} LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address Hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	ns
t_{BW}	$\overline{BHE} / \overline{BLE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[15, 16]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[15]	10	–	ns

Notes

14. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the [Figure 1 on page 5](#).
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the output enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
18. The minimum write pulse width for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [19, 20]

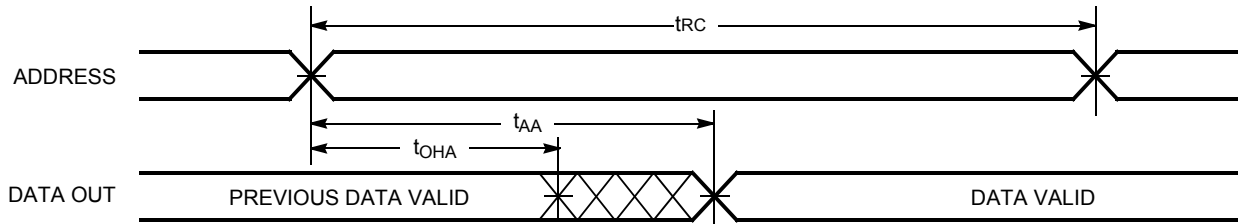
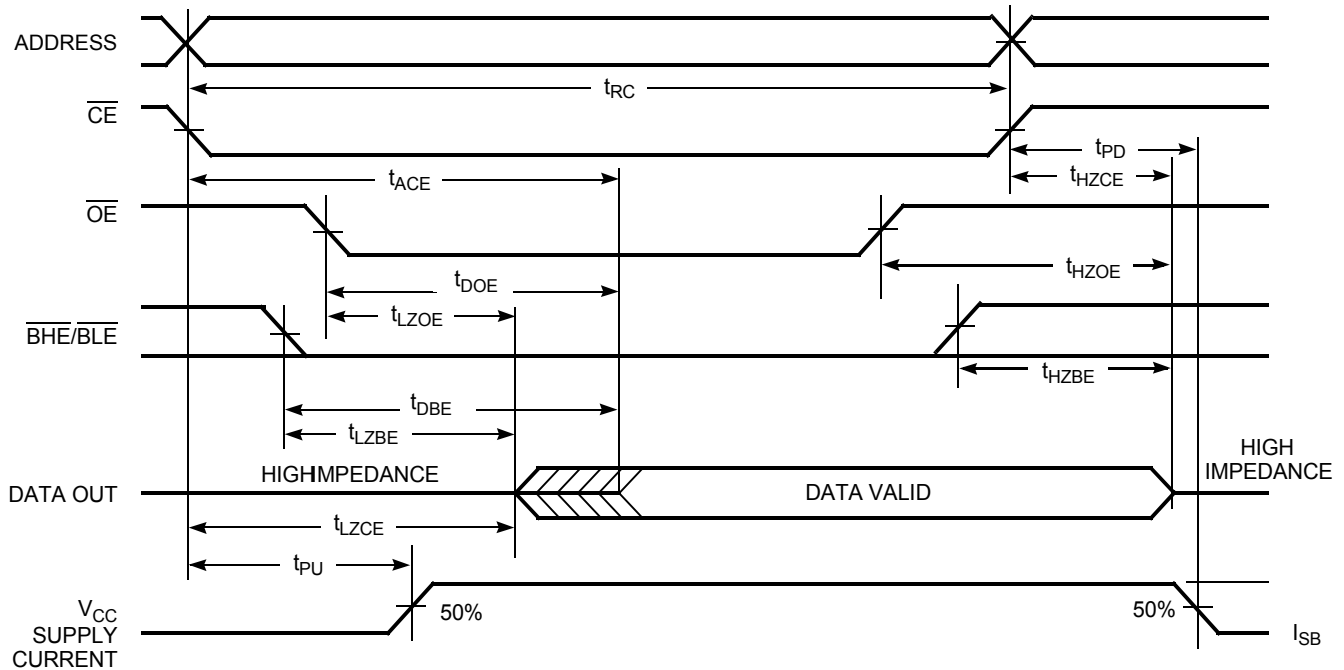


Figure 4. Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) [20, 21]



Notes

- 19. Device is continuously selected. $\overline{\text{OE}}, \overline{\text{CE}} = V_{\text{IL}}$.
- 20. $\overline{\text{WE}}$ is high for read cycles.
- 21. Address valid before or similar to $\overline{\text{CE}}$ transition low.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} HIGH During Write) [22, 23]

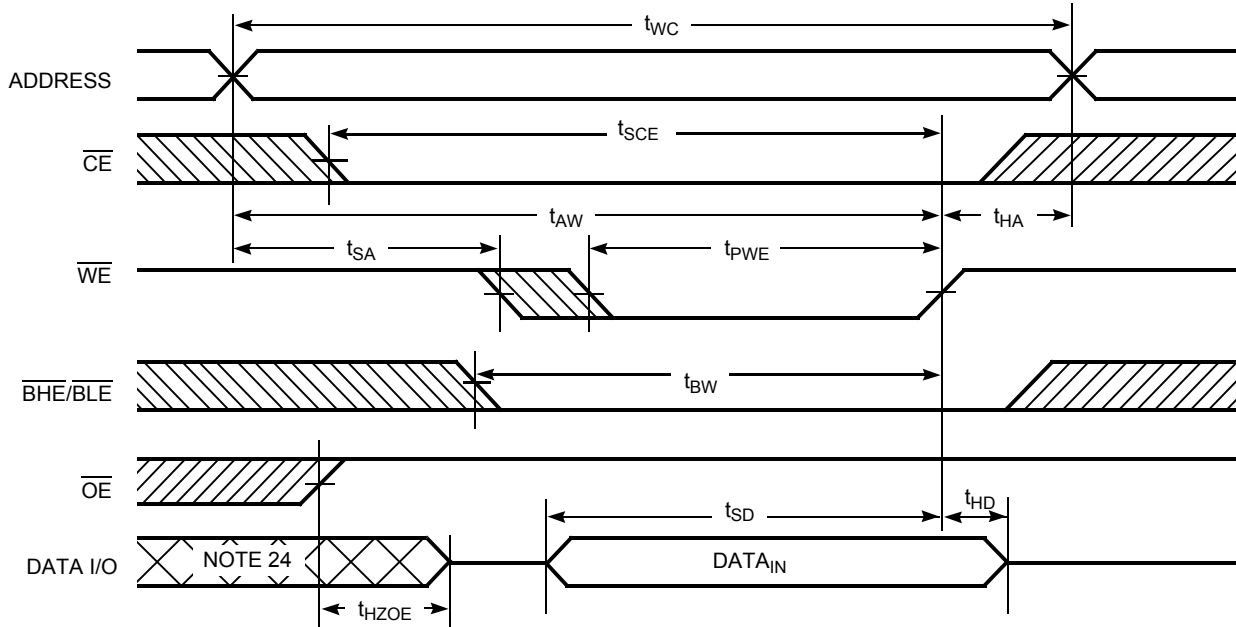
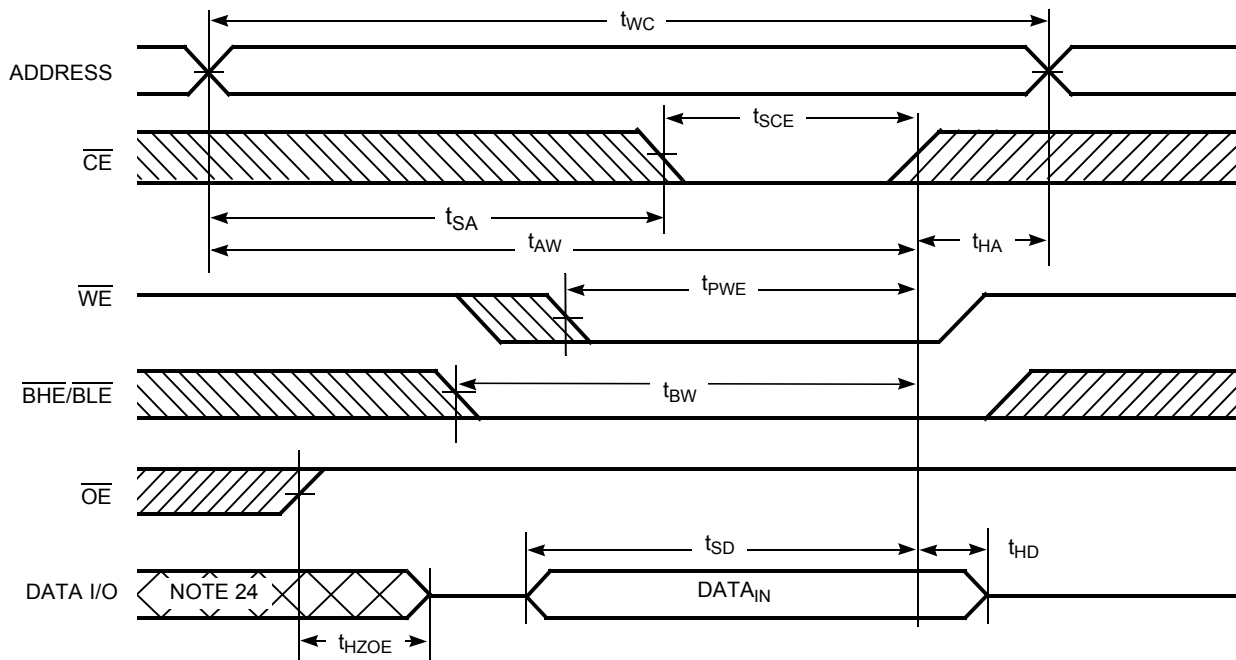


Figure 6. Write Cycle No. 2 (\overline{CE} Controlled) [22, 23]



Notes

- 22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 23. If \overline{CE} goes high simultaneously with \overline{WE} high, the output remains in high impedance state.
- 24. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [25, 26]

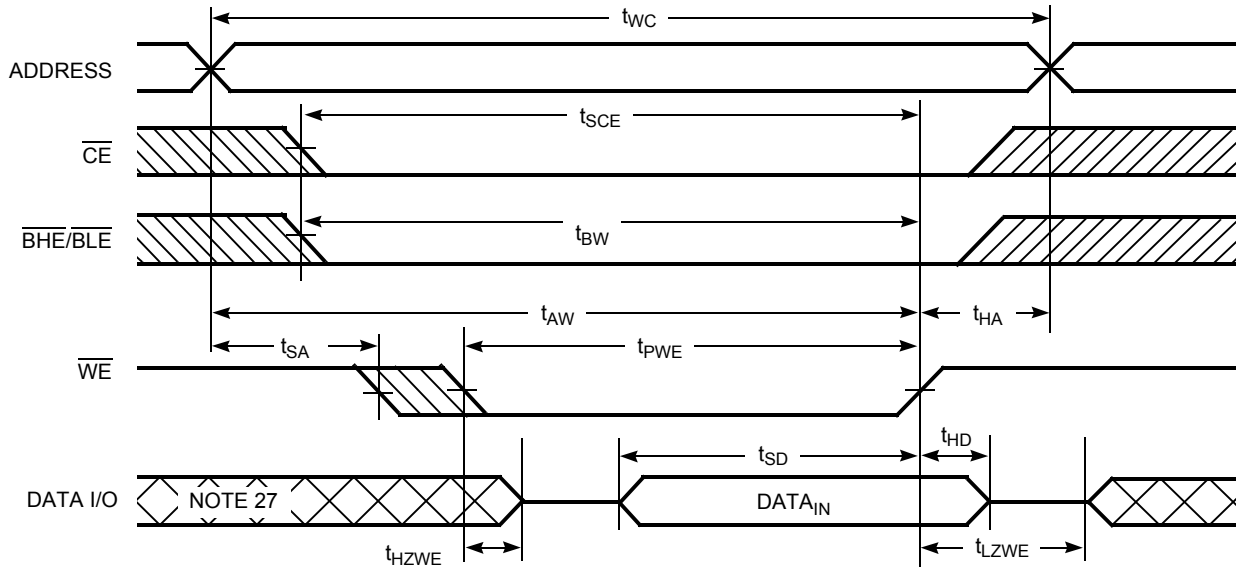
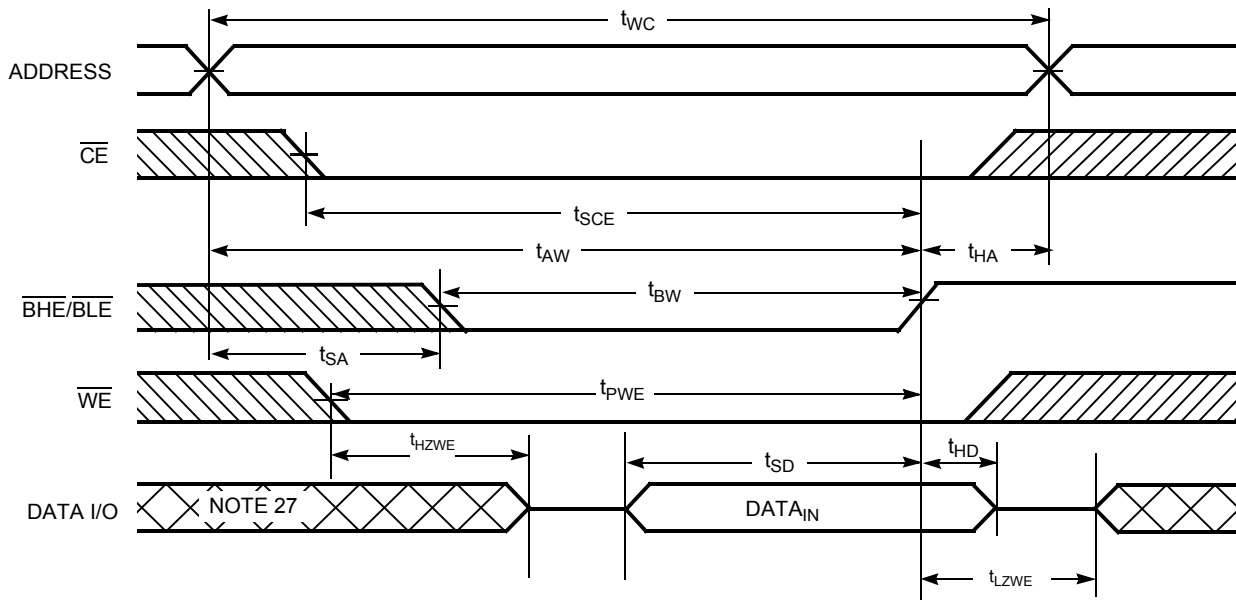


Figure 8. Write Cycle No. 4 ($\overline{BHE/BLE}$ Controlled, \overline{OE} LOW) [25]



Notes

- 25. If \overline{CE} goes high simultaneously with \overline{WE} high, the output remains in high impedance state.
- 26. The minimum write pulse width for Write Cycle No. 3 (\overline{WE} controlled, \overline{OE} LOW) should be sum of t_{HZWE} and t_{SD} .
- 27. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

\overline{CE} [28]	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect or power-down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

Note

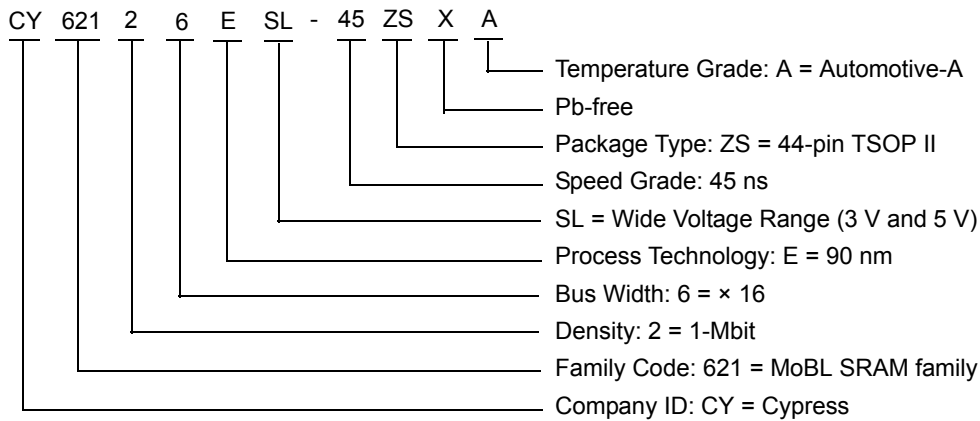
28. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62126ESL-45ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A

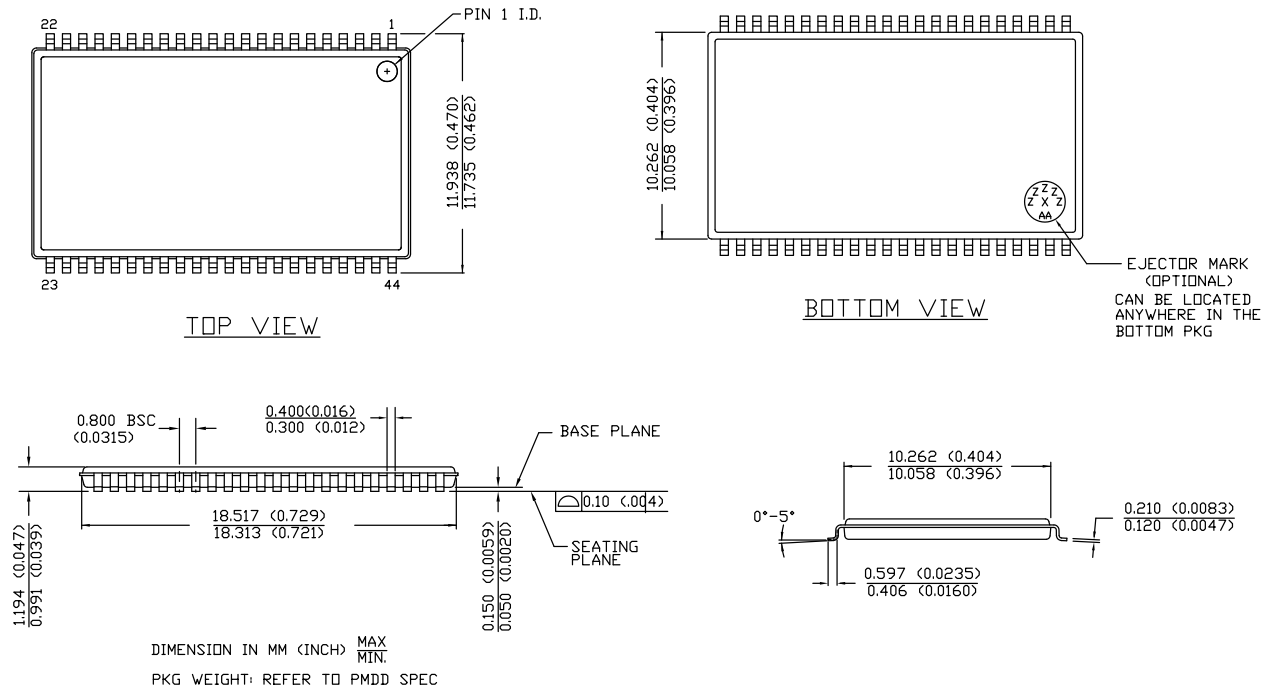
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 9. 44-pin TSOP II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	Byte High Enable
$\overline{\text{BLE}}$	Byte Low Enable
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mV	millivolt
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62126ESL MoBL [®] Automotive, 1-Mbit (64 K × 16) Static RAM				
Document Number: 001-66522				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	3144223	01/17/2011	RAME	New data sheet for Automotive parts.
*A	4297746	03/06/2014	MEMJ	<p>Updated Functional Description: Removed reference to the Application Note AN1064.</p> <p>Updated Product Portfolio: No technical updates. Changed format only.</p> <p>Updated Switching Characteristics: Added Note 18 and referred the same note in "Write Cycle".</p> <p>Updated Switching Waveforms: Added Note 26 and referred the same note in Figure 7.</p> <p>Updated Package Diagram: spec 51-85087 – Changed revision from *C to *E.</p> <p>Updated to new template.</p> <p>Completing Sunset Review.</p>
*B	4582964	11/29/2014	VINI	<p>Updated Maximum Ratings: Referred Notes 4, 5 in "Supply voltage to ground potential".</p>

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

psoc.cypress.com/solutions
[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

Technical Support

cypress.com/go/support

© Cypress Semiconductor Corporation, 2011-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [SRAM](#) category:

Click to view products by [Cypress](#) manufacturer:

Other Similar products are found below :

[CY6116A-35DMB](#) [CY7C1049GN-10VXI](#) [CY7C128A-45DMB](#) [GS8161Z36DD-200I](#) [GS88237CB-200I](#) [RMLV0408EGSB-4S2#AA0](#)
[IDT70V5388S166BG](#) [IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#)
[CY7C1353S-100AXC](#) [AS6C8016-55BIN](#) [AS7C164A-15PCN](#) [515712X](#) [IDT71V67603S133BG](#) [IS62WV51216EBLL-45BLI](#)
[IS63WV1288DBLL-10HLI](#) [IS66WVE2M16ECLL-70BLI](#) [70V639S10BCG](#) [IS66WVE4M16EALL-70BLI](#) [IS62WV6416DBLL-45BLI](#)
[IS61WV102416DBLL-10TLI](#) [CY7C1381KV33-100AXC](#) [CY7C1381KVE33-133AXI](#) [8602501XA](#) [5962-3829425MUA](#) [5962-3829430MUA](#)
[5962-8855206YA](#) [5962-8866201YA](#) [5962-8866204TA](#) [5962-8866206MA](#) [5962-8866208UA](#) [5962-8872502XA](#) [5962-9062007MXA](#) [5962-](#)
[9161705MXA](#) [70V3579S6BFI](#) [GS882Z18CD-150I](#) [M38510/28902BVA](#) [8413202RA](#) [5962-9161708MYA](#) [5962-8971203XA](#) [5962-](#)
[8971202ZA](#) [5962-8872501LA](#) [5962-8866208YA](#) [5962-8866205YA](#) [5962-8866205UA](#) [5962-8866203YA](#) [5962-8855202YA](#)